Linearity Testing for G.hn PLC Line Drivers (Part 2 of 2)

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Abstract: Emerging in home wideband Power Line Communications (PLC) networks are pushing the transmit frequencies through 50MHz today and possibly through 100MHz carriers into the future. The line driver must not only deliver the desired signal onto a difficult load, but must also not introduce a non-linear load during its shutdown for this TDMA system. Since these systems act like a party line on the in home power lines, where a single transmitter is enabled while all other PLC ports show a disabled line driver in parallel with the receivers, those disabled ports must be able to receive the signal without introducing excessive nonlinearity into the broadband load. Test methodology and data on a 3rd generation wideband differential driver will be developed in 2 parts.

Part 1 described the signal source generation and measurements for a 50MHz PLC signal at full line power of 15dBm with 14.6dB PAR using the ISL15100 driving a 34.6Ω load where <-50dBc MTPR was measured up through the power cutback frequency of 30Mhz.

Part 2 will add a 2nd driver to the load network showing a measurement setup for introducing this active load while tapping off the transmit signal for MTPR degradation measurement. Lab measurements with a disabled drivers added to the measurement load will show negligible change to transmit MTPR performance relative to earlier devices.

PLC system requirements for disabled drivers

In a minimal 2-transceiver system, each port must both send and receive signal as shown in figure 10 for this TDMA system.

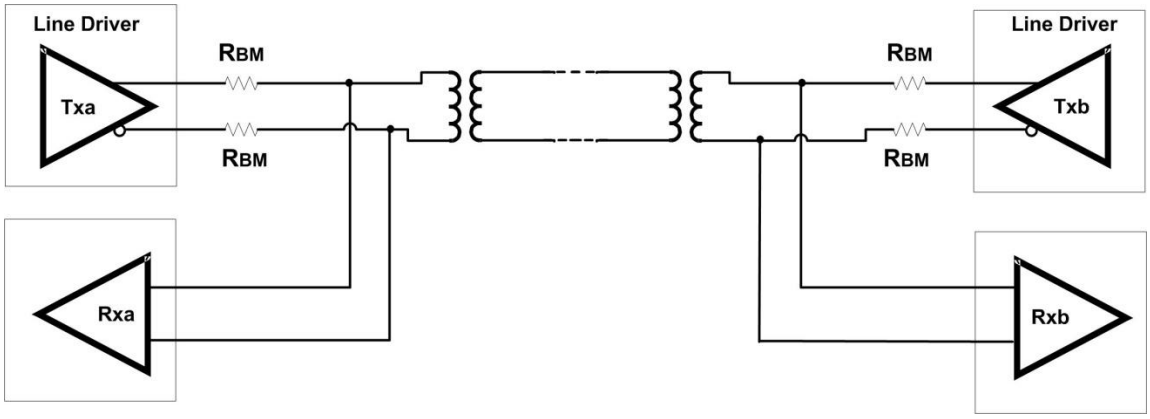

Figure 10. Simplified PLC send & receiver pair

Consider the line driver to the left as a transmitter while the Rxb is receiving with Txb disabled. Full power using a +12V supply produced approximately 6.2Vp differential at the output side of the Rbm resistors for a nominal line impedance of 100Ω.That will get stepped up by the transformer (1:1.7

assumed here) and then down again going to Rxb port. For worst case, develop the maximum 7.9V peak swing at the receiver resistors and measure the MTPR with the disabled driver either inserted into the test board or removed. This 7.9Vp should be slightly higher than physical systems but will be used t as worst case. There will be some degradation in the MTPR performance for these highest swings into the disabled port but far less than earlier line drivers with the simple power shutdown disable feature. Newer devices like the ISL15100 include active circuitry during the shutdown mode to bootstrap out the output transistor network when disabled from whatever signal is being sensed at the output pins.

Evaluation board circuit for differential PLC line drivers

For lab characterization, the circuit of figure 11 is used where instead of a single +12V supply, split +/-6V supplies are used. This eliminates some of the DC level shifting inconvenience in a lab environment.

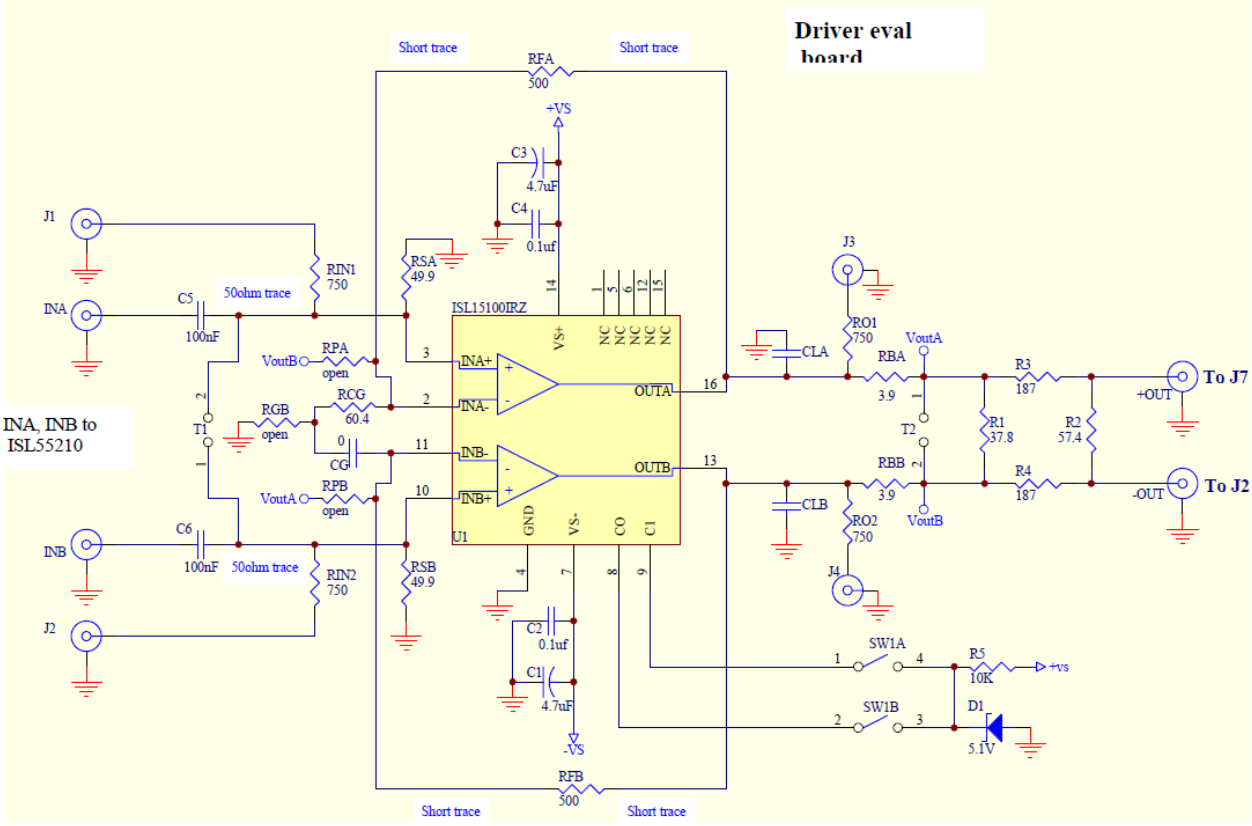

Figure 11. Differential line driver AC characterization circuit.

There are numerous optional elements in the EVAL circuit that are there, but not populated, for this test. The test input signal arrives at INA&INB from the postamplifier of fig. 3. That 2MHz minimum carrier is AC coupled to the 49.9Ω terminations (RSA & RSB). Probe points at this input signal are added through J1 and J2. The Cg capacitor is a short for this test but can be inserted to limit any DC output current that might be generated due to an output differential offset voltage. The RFA,RFB and RCG resistors are set to get the gain of 25dB intended in this example. The CLA and CLB capacitors are not populated but intended to provide a means of testing stability with small parasitic layout capacitance in

the design. It is always best to reduce if possible any source of parasitic C directly on the output pins of these high speed drivers.

The target differential output swing is measured at J4 – J3 and should be ≈7.9Vp for full line power using the intended 1:1.7 turns ratio to a 100Ω line. Figure 12 shows a typical time waveform probing at J4&J3. Recall the differential swing is double this Vp number as the two outputs reverse polarity.

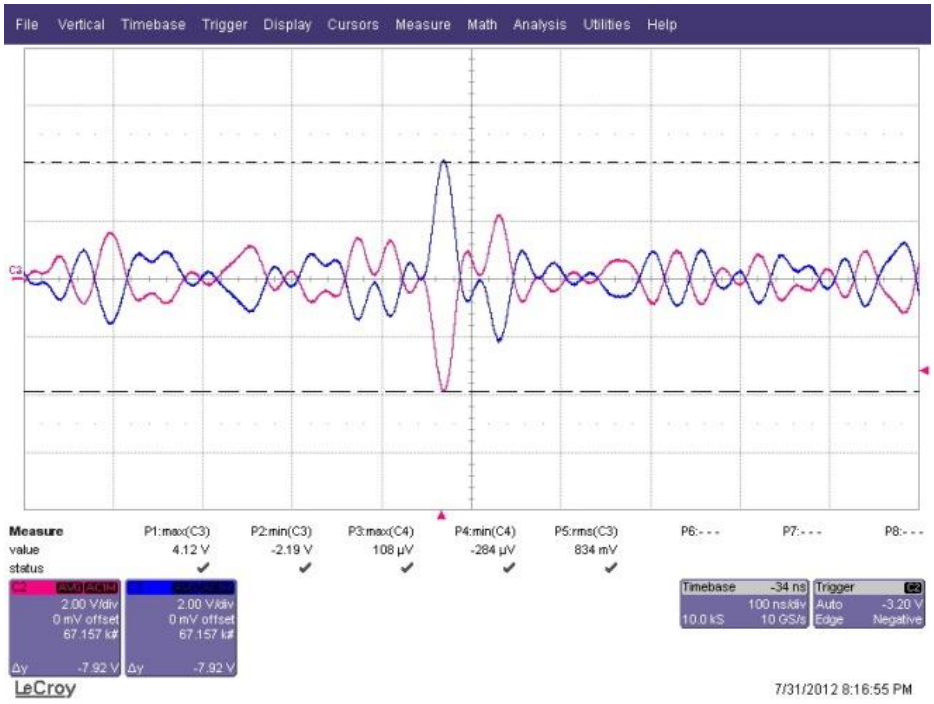

Figure 12. Differential swing across amplifier output pins.

The 7.9Vp swing at the output pins is reduced to 6.5Vp at the T2 test point of Figure 11 by the resistive loss through the Rb resistors (3.9Ω each) to an assumed 34.9Ω load. Since this is a general purpose test circuit, the resistor elements in the pi structure can be modified to implement different input and source impedances assuming different measurement impedances after this board. Here, R1->R4 are set to show a differential load of 34.9Ω and present 25Ω source on each output leg. This then feeds a transformer board to get back to single ended in a 50Ω measurement system. This is used for all of the amplifier frequency response and distortion measurements. Elements R2, R3, & R4 are intended to present a 400Ω differential input impedance converted to 50Ω differential output impedance where that 400Ω input assumes a matched 50Ω load going off board (ref. 6). This allows 50Ω cabling to be inserted without reflection or VSWR issues modifying the measurements. This network does insert ≈-24.6dB insertion loss. Since the full scale input for the DAQ board (ref. 3) is 200mVpp, this test will still require a bit more added attenuation as shown in the test block diagram of figure 1.

Adding a disabled line driver into the load circuit

One approach to inserting a disabled line driver would be to emulate the actual 100Ω line impedance at the outputs of the 2 Rba and Rbb resistors of fig. 11 using another 2- transformer board with the intended disabled line driver between those two transformers. Figure 11 could have been modified to a custom board with a disabled line driver attached at T2, but this approach allows separate “DUT” loads to be tested without customizing the general characterization board of fig. 11. To ensure that enough swing can be produced at the disabled output pins, a 1:2 stepup transformer was used into that DUT board. To get an input impedance of 100ohms there, the interstage network should be developing a 400Ω differential impedance. This is built up in 3 pieces as shown in the DUT board schematic of fig. 13. First, 2 -5kΩ resistors ensure this inner network sits near ground to eliminate in common mode issues back into the disabled amplifier. Next, the disabled driver amplifier will present the sum of its Rf and Rg resistors as a passive differential load. Here, the 25dB gain with Rf = 500Ω will add a 1.07kΩ resistive path along with a possibly non-linear load at the amplifier output pins. To now hit a 402ohm total impedance, the differential to single ended sense path needs to present a 688Ω differential impedance. This is a solution (ref. 6) for each ½ circuit to present 344Ω input (assuming a final termination reflected back through the 1:1 transformer of 25Ω on each ½ circuit) while providing a 25Ω source at each leg going into the 1:1 transformer. The values shown will approximately do this giving a very low distortion passive differential to signal ended conversion to pass on to a single ended 50Ω input DAQ board.

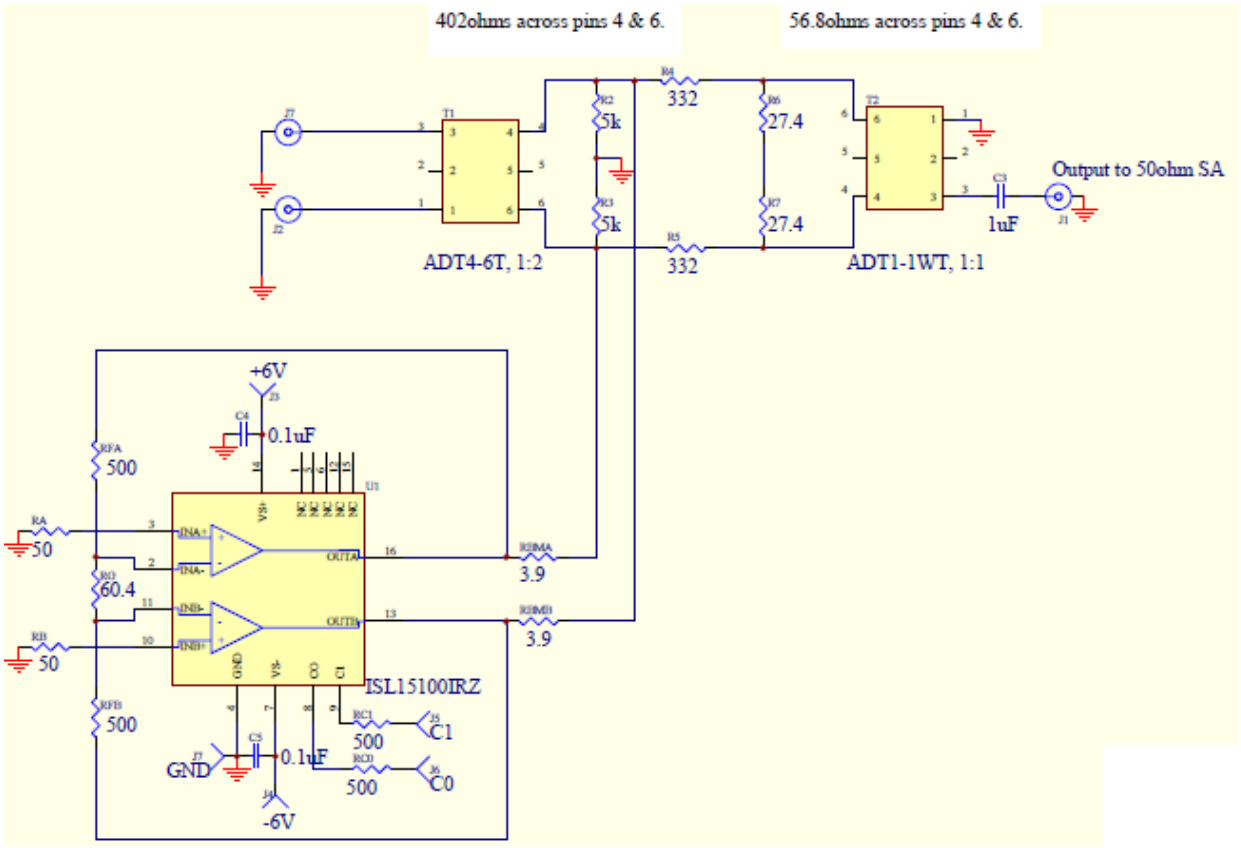

Figure 13. Disabled differential line driver DUT load board.

Going back to the input side of fig. 13, this 402Ω total differential impedance between the transformers becomes a midband 100ohm impedance looking into the 1:2 step up. Removing the passive load of fig. 11 (R1 to R4) and inserting a 1:1.7 tranformer will get the active driver board to where it is emulating the line driver condition. It will now see the 100Ω input impedance at the load DUT board input referred as the intended line driver load of 34.7Ω at the 3.9Ω output resistors.

Setting this circuit up in a free Spice simulator (ref.7) gives the circuit of figure 14 where only the passive load presented by the disabled line drivers feedback network is shown as R8.

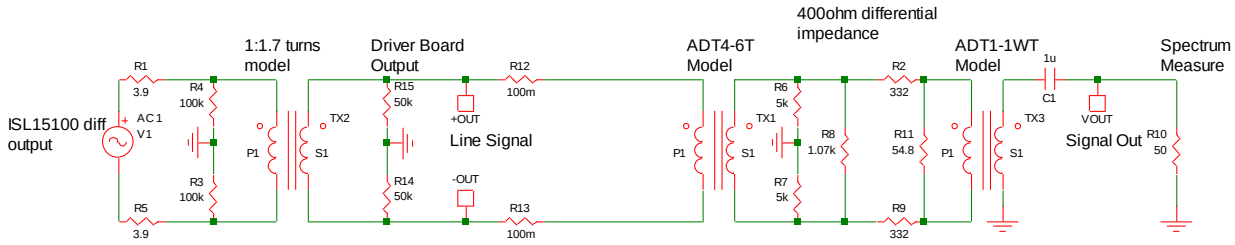

Figure 14. Simulation circuit for this load DUT

Simulating this separately from any flatness issues coming out of the line driver (V1 is ideal) gives the response from the line driver output pins to the signal developed across the disabled line driver at R8 (ref. 8). This is showing 8.8dB midband gain and good flatness through the 2MHz to 50Mhz signal span. This approach actually provides some gain if needed from the active line driver output. This was used to allow extreme signal swings to be developed testing the limits of emerging line drivers.

Figure 15. Simulated response to disable driver output pins.

MTPR degradation adding a disabled line driver to PLC test waveform.

Now with everything configured to generate a typical PLC waveform at the output pins of a disabled line driver as in fig. 13, a MTPR sweep will be first performed with the amplifier removed from the circuit of

fig. 13, (but the feedback and gain resistors are still present). The output power of the active driver is reduced (to account for the gain in the board DUT) until a 7.9Vp signal is being produced at the 3.9Ω resistors going back into the dual op amp outputs in fig. 13. This does change the active driver swing from the passive test of Part 1, but the baseline MTPR will be re-measured here and then the disabled amplifier re-inserted and the test repeated to isolate on any nonlinear loading effects introduced by the driver. Since many of these drivers are pin compatible, this allows a way to insert (QFN socket) different drivers and take comparative data quickly. The 3 curves of fig. 16 show the baseline MTPR with the driver removed, the MTPR with a disabled ISL15100 inserted, and then a comparison to a legacy PLC driver inserted as a last step. This earlier device provided some off state linearization, but clearly is not nearly as effective as the most recent device.

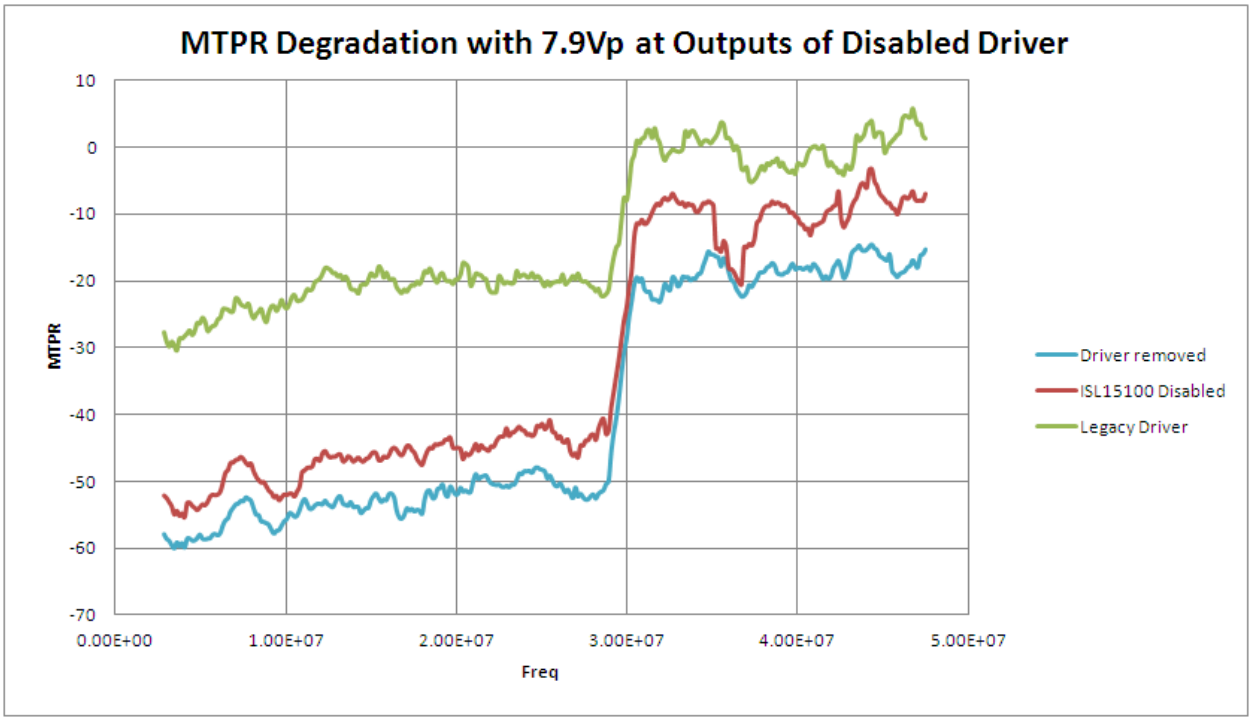

Figure 14. MTPR measurements with disabled drivers added to passive load

This 7.9Vp test signal into the disable driver is an extreme condition. Most system implementations will show a lower received signal power where the MTPR degradation will be less than shown in fig. 14.

Summary and Conclusions

For Power Line Communication (PLC) (ref. 9) systems to achieve multiport deployment within residential wiring they will need to consider the parasitic loading of the ports in receive mode. This is both a passive impedance issue and a non-linear output impedance issue. The results here show the available line drivers are improving on off state linearity. The specific test here was at very large swings into the disabled driver output. This would emulate a back to back socket send receive pair on opposite sides of a wall. More typically, the receiver will be seeing much lower swings activating less non-linear turn on issues in the driver. However, very low feedback network resistors and/or receive path impedances can

start to combine in parallel on a multi-port system to drag down the combined line load for the active driver. Also, lower gain configurations should consider the signal that gets back across the summing junctions of the differential drivers and ensure that path remains linear as well.

G.Hn Line driver article references – Part 2 added to Part 1 here.

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1. Contact the authors for the prelim data sheet on this or other DSL/PLC line driver devices

2. “Ultra Low Power Broadband 8 to 14-Bit Data Acquisition Platform”, http://www.intersil.com/en/products/data-converters/high-speed-a-d-converters/ISLA112P50-55210EV1Z.html

3. 12bit, 500MSPS DAQ users guide, http://www.intersil.com/content/dam/Intersil/documents/an17/an1725.pdf

4. Low power, 4GHz, ultra low noise FDA, http://www.intersil.com/content/intersil/en/products/amplifiers-and-buffers/all-amplifiers/amplifiers/ISL55210.html

5. . Contact the authors for this schematic

6. Contact msteffes@intersil.com for a spreadsheet to set this network up.

7. Free Intersil Spice simulator http://intersil.transim.com/iSimPE.aspx,

8. Contact msteffes@intersil.com for this simulation file showing the transformer model detail.

9. PLC can mean either “Power Line Communications” or “Programmable Logic Controller” http://en.wikipedia.org/wiki/List_of_computing_and_IT_abbreviations#P