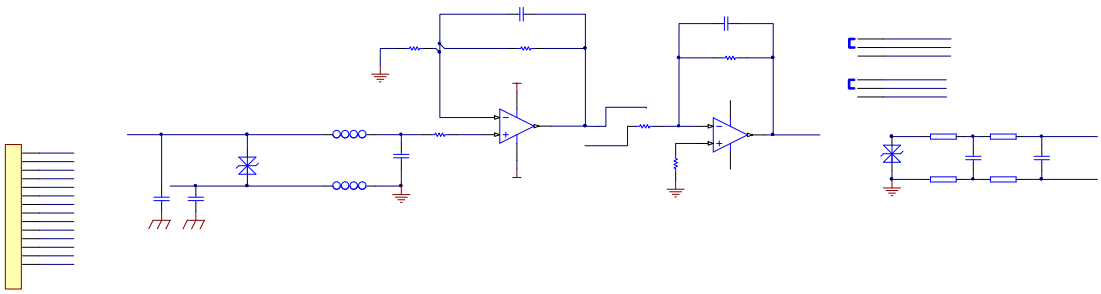
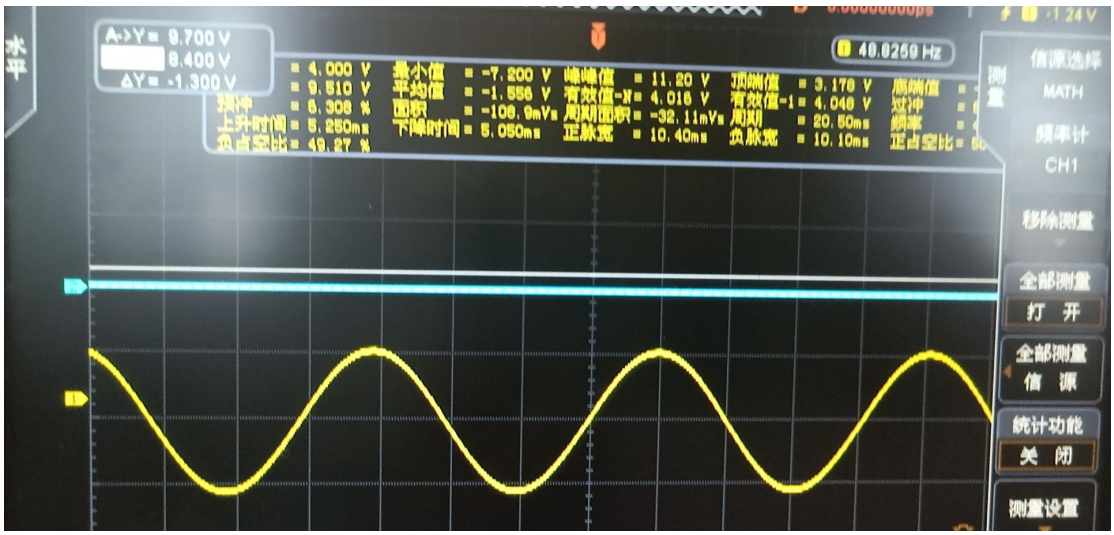


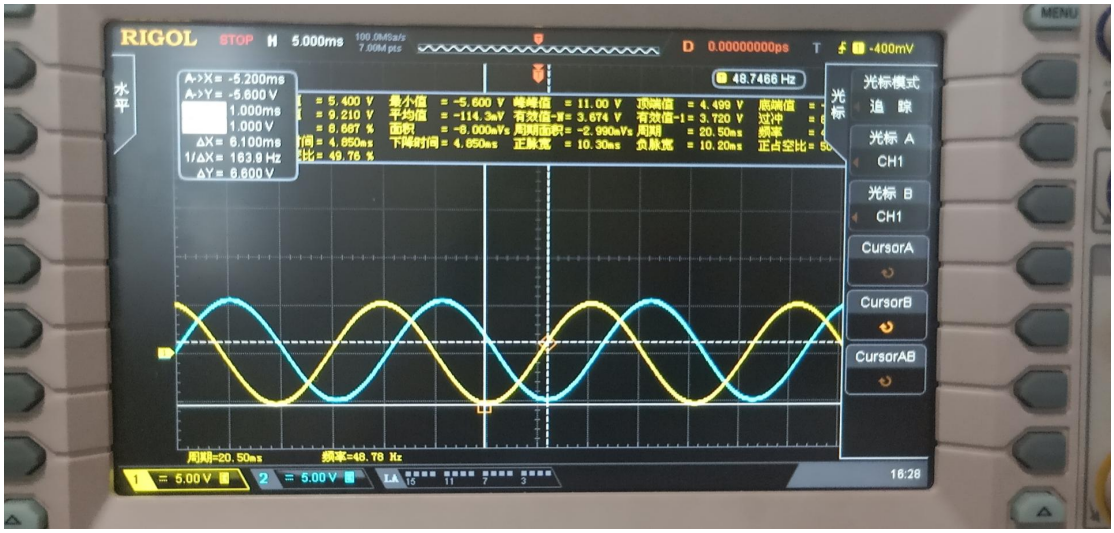
My input is 50HZ　50Mv about sin signal,

When my R40 is 680k, R45 is 20K5, C71 is 0.15uF, the 7th pin output has a DC offset of about 1.5V

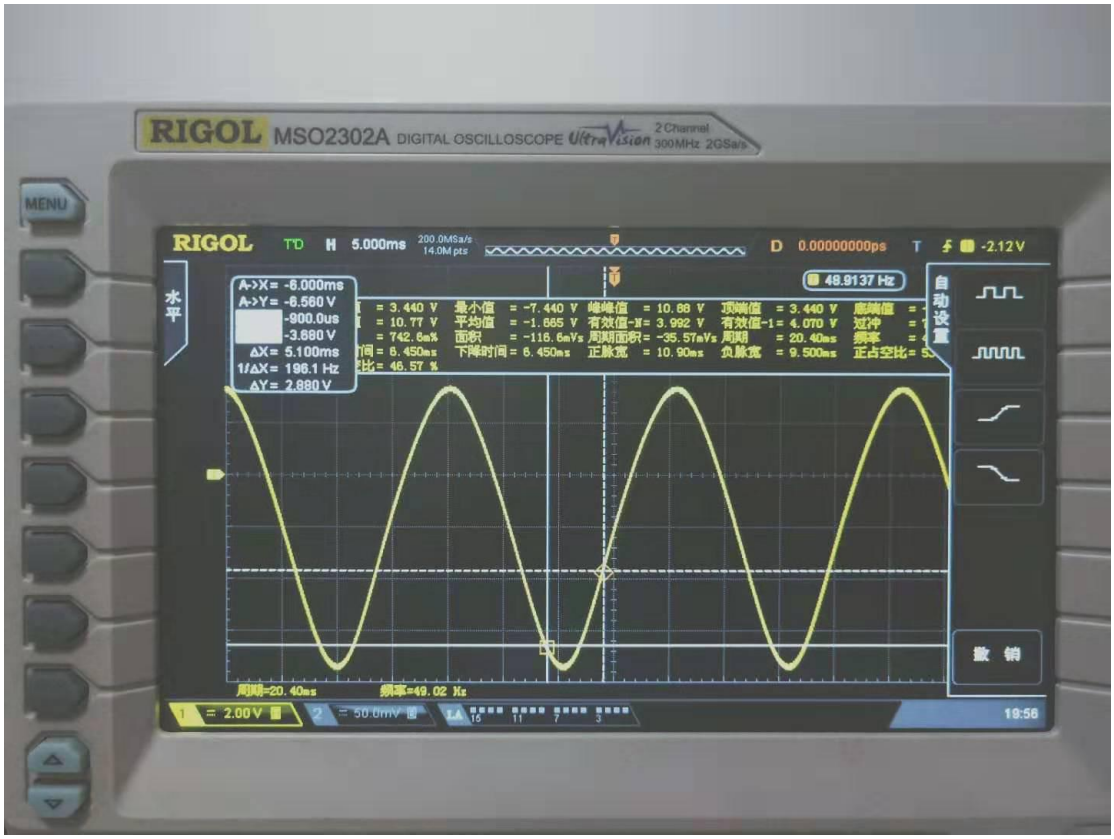
about.Phase offset 5.1ms.I think this offset is abnormal.phase offset is ok



When my R40 is 100k, R45 is 20K5, C71 is 0.15uF, the 7th pin output has a DC offset of about -114.3mV.Phase offset 6.1ms.I think this offset is ok.but phase offset is abnormal



WHY? can i modify R40 from 680K to 100k , if i use 100k, how to get 5.1ms phase offset.According to TIDA-00777 design ,when R40 is 100k,the RF(C71)should be 1uf ,then Keep the gain 1.04 unchanged。the R45 should be 3.08K(in fact,i choose 3.16k)，but after i change R45 and C71,



It becomes a DC bias of about 1.6V.why？Is this TIDA-00777 design wrong?

how should i do if i make R40 is 100k，C71 0.15uf ，but i still get Phase offset 5.1ms？