



OPA234 OPA2234 OPA4234

SBOS055A - MAY 1996 - REVISED JUNE 2004

Low-Power, Precision SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

FEATURES

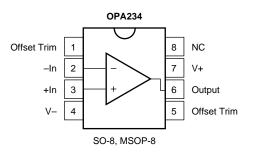
- WIDE SUPPLY RANGE: Single Supply: V_S = +2.7V to +36V Dual Supply: V_S = ±1.35V to ±18V
- SPECIFIED PERFORMANCE: +2.7V, +5V, and ±15V
- LOW QUIESCENT CURRENT: 250µA/amp
- LOW INPUT BIAS CURRENT: 25nA max
- LOW OFFSET VOLTAGE: 100µV max
- HIGH CMRR, PSRR, and A_{OL}
- SINGLE, DUAL, and QUAD VERSIONS

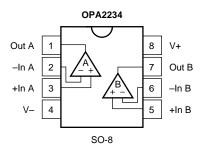
DESCRIPTION

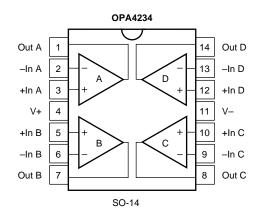
The OPA234 series low-cost op amps are ideal for single-supply, low-voltage, low-power applications. The series provides lower quiescent current than older "1013"-type products and comes in current industrystandard packages and pinouts. The combination of low offset voltage, high common-mode rejection, high power-supply rejection, and a wide supply range provides excellent accuracy and versatility. Single, dual, and quad versions have identical specifications for maximum design flexibility. These general-purpose op amps are ideal for portable and battery-powered applications.

The OPA234 series op amps operate from either single or dual supplies. In single-supply operation, the input common-mode range extends below ground and the output can swing to within 50mV of ground. Excellent phase margin makes the OPA234 series ideal for demanding applications, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

Single version packages are in an SO-8 surface-mount and a space-saving MSOP-8 surface-mount. Dual packages are in an SO-8 surface-mount. Quad packages are in an SO-14 surface-mount. All are specified for -40° C to +85°C operation.









Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ELECTRICAL CHARACTERISTICS: $V_s = +5V$

At T_A = 25°C, V_S = +5V, R_L = 10k Ω connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

			OPA234U, E OPA2234U			OPA234UA, EA OPA2234UA OPA4234UA, U			
PARAMETER		CONDITION	MIN	TYP	MAX	MIN	ТҮР	MAX	UNITS
OFFSET VOLTAGE Input Offset Voltage OPA234E, EA vs Temperature ⁽¹⁾ vs Power Supply vs Time Channel Separation (Dual, Quad)	V _{os} dV _{os} /dT PSRR	V_{CM} = 2.5V Operating Temperature Range V_{S} = +2.7V to +30V, V_{CM} = 1.7V		$\pm 40 \\ \pm 100 \\ \pm 0.5 \\ 3 \\ 0.2 \\ 0.3$	±100 ±150 ±3 10		* * * * *	±250 ±350 * 20	μV μV μV/°C μV/V μV/mo μV/V
INPUT BIAS CURRENT Input Bias Current ⁽²⁾ Input Offset Current	I _B I _{OS}	V _{CM} = 2.5V V _{CM} = 2.5V		-15 ±1	-30 ±5		*	-50 *	nA nA
NOISE Input Voltage Noise Density Current Noise Density	v _n i _n	f = 1kHz		25 80			* *		nV/√Hz fA/√Hz
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection	CMRR	$V_{CM} = -0.1V$ to 4V	-0.1 91	106	(V+) −1	* 86	*	*	V dB
INPUT IMPEDANCE Differential Common-Mode		V _{CM} = 2.5V		10 ⁷ 5 10 ¹⁰ 6			*		Ω pF Ω pF
OPEN-LOOP GAIN Open-Loop Voltage Gain	A _{OL}	$V_{O} = 0.25V \text{ to } 4V$ $R_{L} = 10k\Omega$ $R_{L} = 2k\Omega$	108 86	120 96œ86	*	100	* dB		dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time	GBW SR	$C_{L} = 100pF$ $G = 1, 3V \text{ Step, } C_{L} = 100pF$ $G = 1, 3V \text{ Step, } C_{L} = 100pF$ $(V_{IN}) \text{ (Gain)} = V_{S}$		0.35 0.2 15 25 16			* * * *		MHz V/μs μs μs μs
OUTPUT Voltage Output: Positive Negative Positive Negative Short-Circuit Current Capacitive Load Drive (Stable Operation	I _{SC} Ition) ⁽³⁾	$\begin{array}{l} R_L = 10 k\Omega \text{ to } V_S/2 \\ R_L = 10 k\Omega \text{ to } V_S/2 \\ R_L = 10 k\Omega \text{ to Ground} \\ R_L = 10 k\Omega \text{ to Ground} \\ \end{array}$	(V+) -1 0.25 (V+) -1 0.1	(V+) −0.65 0.05 (V+) −0.65 0.05 ±11 1000		* * * *	* * * * *		V V V mA pF
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	١ _Q	I _O = 0	+2.7	+5 250	+36 300	*	*	*	V V μA
TEMPERATURE RANGE Specified Range Operating Range Storage Thermal Resistance	$ heta_{JA}$		40 40 55		+85 +125 +125	* * *		* * *	°C °C °C
8-Pin DIP SO-8 Surface-Mount MSOP-8 Surface-Mount 14-Pin DIP SO-14 Surface-Mount				100 150 220 80 110			* * * *		°C/W °C/W °C/W °C/W °C/W

* Specifications same as OPA234U, E.

NOTES: (1) Wafer-level tested to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See Small-Signal Overshoot vs Load Capacitance typical curve.



ELECTRICAL CHARACTERISTICS: $V_S = +2.7V$

At T_A = 25°C, V_S = +2.7V, R_L = 10k Ω connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

			OPA234U, E OPA2234U			OPA234UA, EA OPA2234UA OPA4234UA, U			
PARAMETER		CONDITION	MIN	ТҮР	MAX	MIN	ТҮР	MAX	UNITS
OFFSET VOLTAGE Input Offset Voltage OPA234E, EA vs Temperature ⁽¹⁾ vs Power Supply vs Time Channel Separation (Dual, Quad)	V _{OS} dV _{OS} /dT PSRR	V_{CM} = 1.35V Operating Temperature Range V_{S} = +2.7V to +30V, V_{CM} = 1.7V		$\pm 40 \\ \pm 100 \\ \pm 0.5 \\ 3 \\ 0.2 \\ 0.3$	±100 ±150 ±3 10		* * * * *	±250 ±350 * 20	μV μV μV/°C μV/V μV/mo μV/V
INPUT BIAS CURRENT Input Bias Current ⁽²⁾ Input Offset Current	I _B I _{OS}	V _{CM} = 1.35V V _{CM} = 1.35V		-15 ±1	-30 ±5		* *	-50 *	nA n
NOISE Input Voltage Noise Density Current Noise Density	v _n i _n	f = 1kHz		25 80			* *		nV/√Hz fA/√Hz
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection	CMRR	V_{CM} = -0.1V to 1.7V	-0.1 91	106	(V+) –1	* 86	*	*	V dB
INPUT IMPEDANCE Differential Common-Mode		V _{CM} = 1.35V		10 ⁷ 5 10 ¹⁰ 6			*		Ω pF Ω pF
OPEN-LOOP GAIN Open-Loop Voltage Gain	A _{OL}	$V_{O} = 0.25V \text{ to } 1.7V$ $R_{L} = 10k\Omega$ $R_{L} = 2k\Omega$	108 86	125 96		100 86	* *		dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time	GBW SR	$C_{L} = 100pF$ $G = 1, 1V \text{ Step, } C_{L} = 100pF$ $G = 1, 1V \text{ Step, } C_{L} = 100pF$ $(V_{ N}) \text{ (Gain)} = V_{S}$		0.35 0.2 6 16 8			* * * *		MHz V/μs μs μs μs
OUTPUT Voltage Output: Positive Negative Positive Negative Short-Circuit Current Capacitive Load Drive (Stable Operation	I _{SC} ation) ⁽³⁾	$\begin{array}{l} R_L = 10 k\Omega \text{ to } V_S/2 \\ R_L = 10 k\Omega \text{ to } V_S/2 \\ R_L = 10 k\Omega \text{ to Ground} \\ R_L = 10 k\Omega \text{ to Ground} \\ \end{array}$	(V+) -1 0.25 (V+) -1 0.1	(V+) −0.6 0.05 (V+) −0.65 0.05 ±8 1000		* * *	* * * * *		V V V mA pF
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	Ι _Q	I _O = 0	+2.7	+2.7 250	+36 300	*	*	*	V V μA
TEMPERATURE RANGE Specified Range Operating Range Storage Thermal Resistance 8-Pin DIP SO-8 Surface-Mount	$ heta_{JA}$		-40 -40 -55	100 150	+85 +125 +125	* * *	* *	* * *	°C ℃ ℃ W\℃
MSOP-8 Surface-Mount 14-Pin DIP SO-14 Surface-Mount				220 80 110			* * *		°C/W °C/W °C/W

* Specifications same as OPA234U, E.

NOTES: (1) Wafer-level tested to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See Small-Signal Overshoot vs Load Capacitance typical curve.



ELECTRICAL CHARACTERISTICS: $V_s = \pm 15V$

At T_A = 25°C, V_S = ±15V, and R_L = 10k Ω connected to ground, unless otherwise noted.

		OPA234U, E OPA2234U			OPA234UA, EA OPA2234UA OPA4234UA, U			
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	ТҮР	MAX	UNITS
OFFSET VOLTAGE Input Offset Voltage V ₀ OPA4234U Model vs Temperature ⁽¹⁾ dV _{OS} /d vs Power Supply PSR vs Time	C Operating Temperature Range		±70 ±0.5 3 0.2	±250 ±5 10		* ±70 * *	±500 ±250 * 20	μV μV μV/°C μV/V μV/mo
Channel Separation (Dual, Quad)			0.3			*		μV/V
INPUT BIAS CURRENT Input Bias Current ⁽²⁾ Input Offset Current			-12 ±1	-25 ±5		* *	-50 *	nA nA
	f = 1kHz		25 80			* *		nV/√Hz fA/√Hz
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection CMR	$V_{CM} = -15V$ to 14V	(V–) 91	106	(V+) –1	* 86	*	*	V dB
INPUT IMPEDANCE Differential Common-Mode	V _{CM} = 0V		10 ⁷ 5 10 ¹⁰ 6			*		Ω pF Ω pF
OPEN-LOOP GAINOpen-Loop Voltage GainAction	$V_{\rm O} = -14.5V$ to 14V	110	120		100	*		dB
FREQUENCY RESPONSE Gain-Bandwidth Product GBV Slew Rate S Settling Time: 0.1% 0.01% Overload Recovery Time S			0.35 0.2 41 47 22			* * * * *		MHz V/μs μs μs μs
OUTPUT Voltage Output: Positive Negative Short-Circuit Current Capacitive Load Drive (Stable Operation) ⁽³⁾	G = +1	(V+) −1 (V−) +0.5	(V+) −0.7 (V−) +0.15 ±22 1000		* *	* * * *		V V mA pF
	2 I ₀ = 0	±1.35	±15 ±275	±18 ±350	*	*	*	ν ν μΑ
TEMPERATURE RANGE Specified Range Operating Range Storage Thermal Resistance		-40 -40 -55		+85 +125 +125	* * *		* * *	2° 2° 2°
8-Pin DIP SO-8 Surface-Mount MSOP-8 Surface-Mount 14-Pin DIP SO-14 Surface-Mount	A		100 150 220 80 110			* * * *		°C/W °C/W °C/W °C/W °C/W

* Specifications same as OPA234U, E.

NOTES: (1) Wafer-level tested to 95% confidence level. (2) Positive conventional current flows into the input terminals. (3) See Small-Signal Overshoot vs Load Capacitance typical curve.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE MARKING
Single OPA234EA OPA234E OPA234UA OPA234U	MSOP-8 Surface-Mount " SO-8 Surface-Mount	A34 " OPA234UA OPA234U
Dual OPA2234UA OPA2234U	SO-8 Surface-Mount	OPA2234UA OPA2234U
Quad OPA4234UA OPA4234U	SO-8 Surface-Mount	OPA4234UA OPA4234U

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

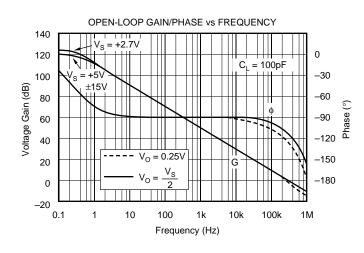
Supply Voltage, V+ to V	
Input Voltage	(V–) –0.7V to (V+) +0.7V
Output Short-Circuit ⁽¹⁾	Continuous
Operating Temperature	40°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

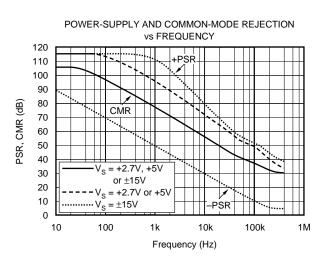
NOTE: (1) Short-circuit to ground, one amplifier per package.

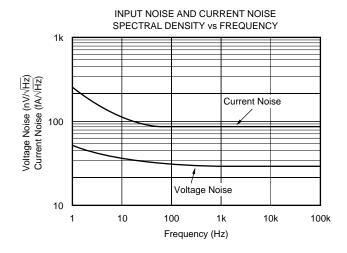


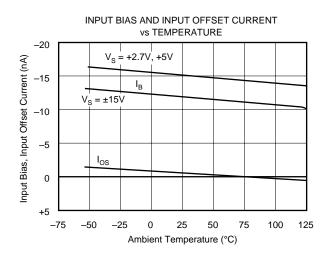
TYPICAL CHARACTERISTIC CURVES

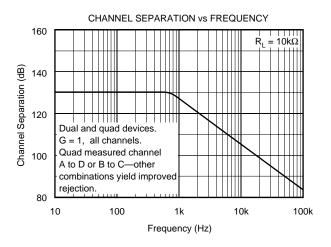
At $T_A = +25^{\circ}C$ and $R_L = 10k\Omega$, unless otherwise noted.

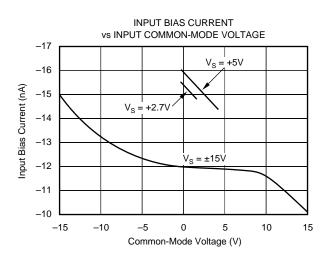










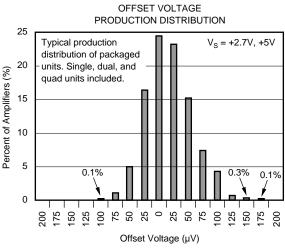


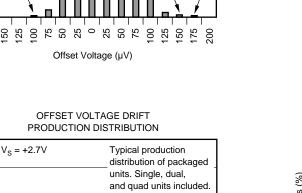


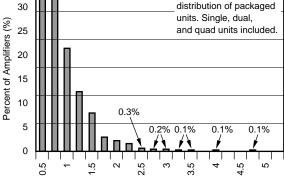
OPA234, OPA2234, OPA4234 SBOS055A

TYPICAL CHARACTERISTIC CURVES (Cont.)

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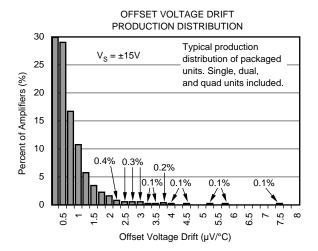


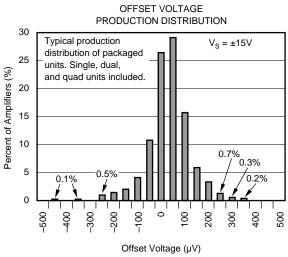




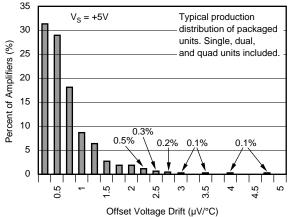
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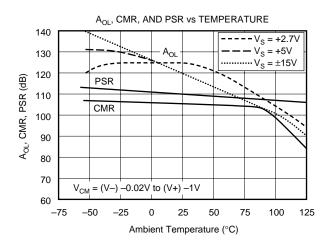
Offset Voltage Drift (µV/°C)





OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

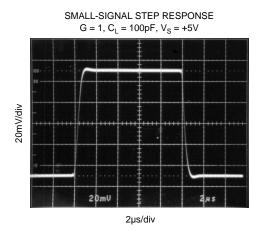


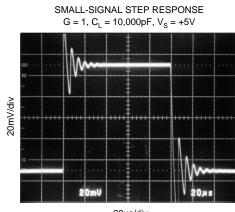


OPA234, OPA2234, OPA4234 SBOS055A

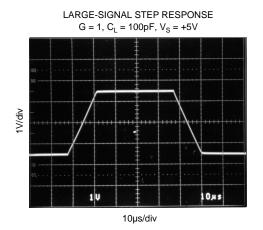
TYPICAL CHARACTERISTIC CURVES (Cont.)

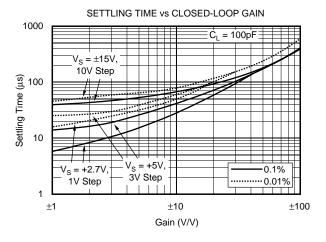
At $T_A = +25^{\circ}C$ and $R_L = 10k\Omega$, unless otherwise noted.

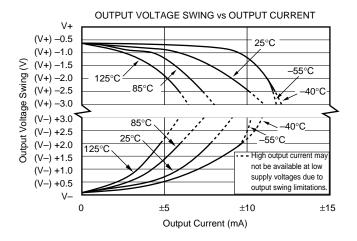




20µs/div





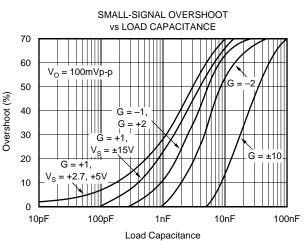


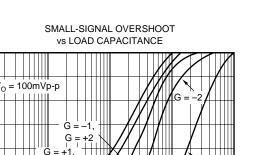
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TEXAS

INSTRUMENTS

www.ti.com

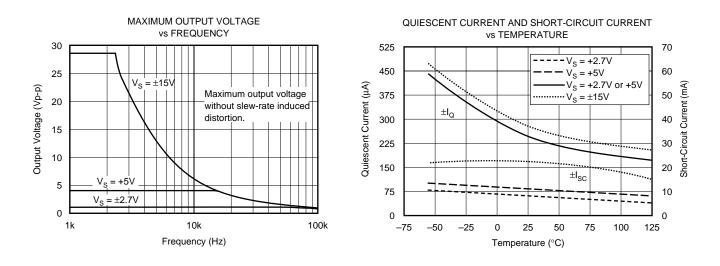




OPA234, OPA2234, OPA4234 SBOS055A

TYPICAL CHARACTERISTIC CURVES (Cont.)

At $T_A = +25^{\circ}C$ and $R_L = 10k\Omega$, unless otherwise noted.



APPLICATIONS INFORMATION

The OPA234 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power-supply pins should be bypassed with 10nF ceramic capacitors.

OPERATING VOLTAGE

The OPA234 series op amps operate from single (+2.7V to +36V) or dual (\pm 1.35V to \pm 18V) supplies with excellent performance. Specifications are production tested with +2.7V, +5V, and \pm 15V supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Characterisitc curves.

OFFSET VOLTAGE TRIM

Offset voltage of the OPA234 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA234 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer, as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

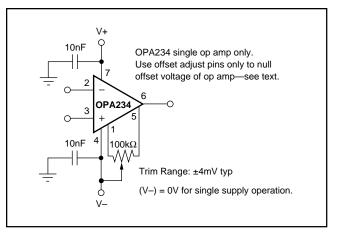


FIGURE 1. OPA234 Offset Voltage Trim Circuit.





25-Jun-2004

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
OPA2234P	OBSOLETE	PDIP	Р	8	
OPA2234PA	OBSOLETE	PDIP	Р	8	
OPA2234U	ACTIVE	SOIC	D	8	100
OPA2234U/2K5	ACTIVE	SOIC	D	8	2500
OPA2234UA	ACTIVE	SOIC	D	8	100
OPA2234UA/2K5	ACTIVE	SOIC	D	8	2500
OPA234E/250	ACTIVE	VSSOP	DGK	8	250
OPA234E/2K5	ACTIVE	VSSOP	DGK	8	2500
OPA234EA/250	ACTIVE	VSSOP	DGK	8	250
OPA234EA/2K5	ACTIVE	VSSOP	DGK	8	2500
OPA234P	OBSOLETE	PDIP	Р	8	
OPA234PA	OBSOLETE	PDIP	Р	8	
OPA234U	ACTIVE	SOIC	D	8	100
OPA234U/2K5	ACTIVE	SOIC	D	8	2500
OPA234UA	ACTIVE	SOIC	D	8	100
OPA234UA/2K5	ACTIVE	SOIC	D	8	2500
OPA4234PA	OBSOLETE	PDIP	Ν	14	
OPA4234U	ACTIVE	SOIC	D	14	58
OPA4234U/2K5	ACTIVE	SOIC	D	14	2500
OPA4234UA	ACTIVE	SOIC	D	14	58
OPA4234UA/2K5	ACTIVE	SOIC	D	14	2500

(1) The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design. **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

MECHANICAL DATA

MPDI001A - JANUARY 1995 - REVISED JUNE 1999



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



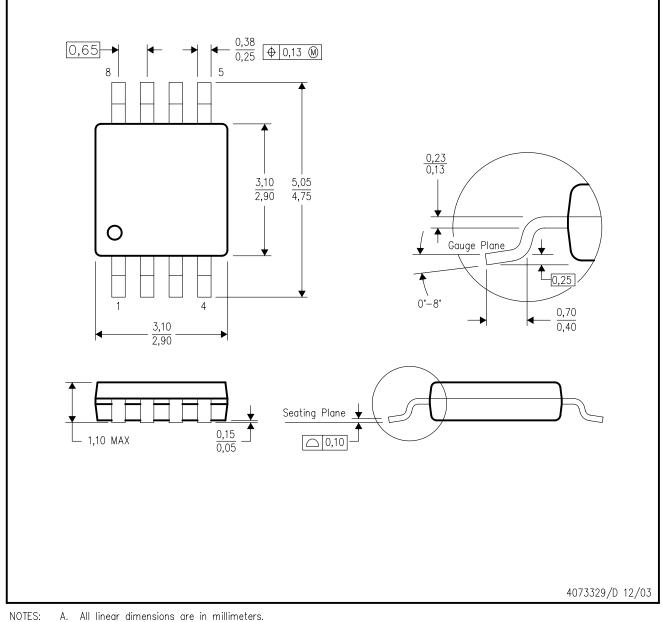
NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-187 variation AA.

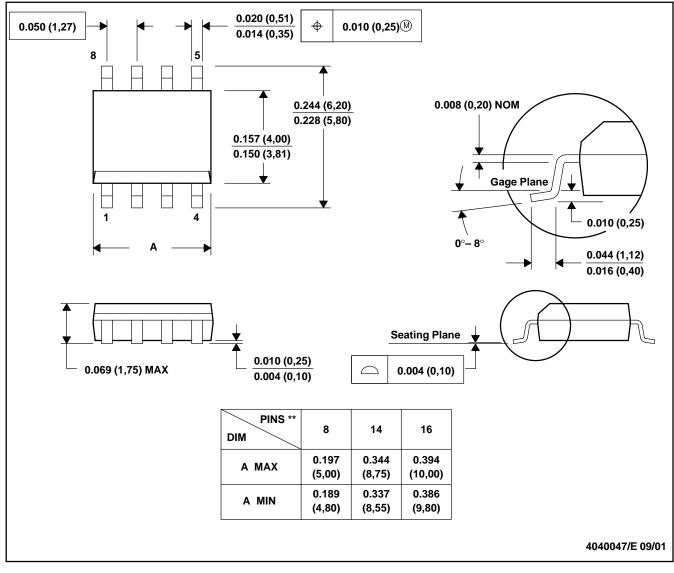


MECHANICAL DATA

MSOI002B - JANUARY 1995 - REVISED SEPTEMBER 2001

PLASTIC SMALL-OUTLINE PACKAGE

D (R-PDSO-G**) 8 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012



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Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
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