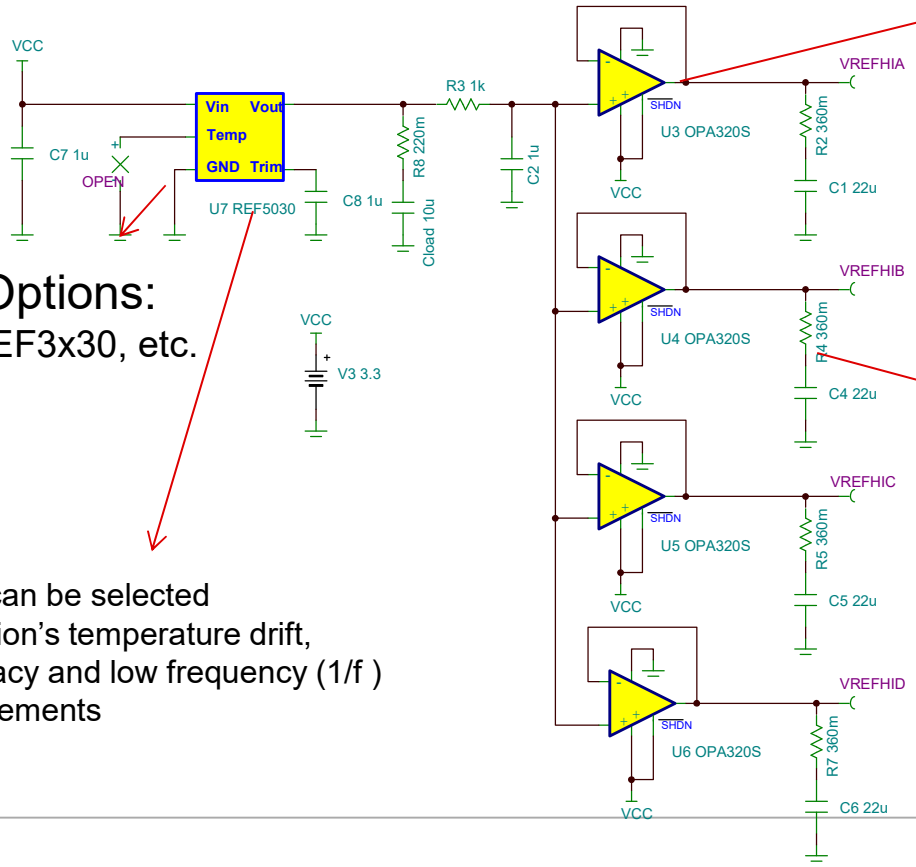
TMS320F283x Reference Drive TINA simulation
4x Reference Inputs
1x REFxx30 + 2x OPA2320 (2x OPA2325)

Rev 1, 3-25-2020

Luis Chioye – Precision Amplifiers Applications

Suggested Reference Drive for TMS320F2838
Sampling Rate ~ 1-MSPS per ADC

OPAx320 or OPAx325



Possible Options:

REF5030, REF3x30, etc.

Reference can be selected per application's temperature drift, initial accuracy and low frequency (1/f) noise requirements

Use 22µF+ ~360mΩ for OPAx320

Use 22µF+ ~500mΩ for OPAx325

Important Datasheet Parameters

TMS320F283x 16-B, 1.1-MSPS, Fully-Differential Input ADC

Assume Max Sampling Rate = 1.0-MSPS
Throughput Period: t_{cycle}=1µs
t_{EOC} = 31.0 ADCCLK Cycles (from Table 5-47 datasheet) Conversion Time:
Assuming ADCCLK @ 50MHz, t_{conv}=620ns (max)
ADC Input Equivalent Circuit: R_{ON} / C_H

For differential operation, the ADC input characteristics are given by Table 5-43 and Figure 5-28.

Table 5-43. Differential Input Model Parameters (16-bit Resolution)

	DESCRIPTION	VALUE
C_p	Parasitic input capacitance	See Table 5-44
R_{on}	Sampling switch resistance	700 Ω
C_h	Sampling capacitor	16.5 pF
R_s	Nominal source impedance	50 Ω

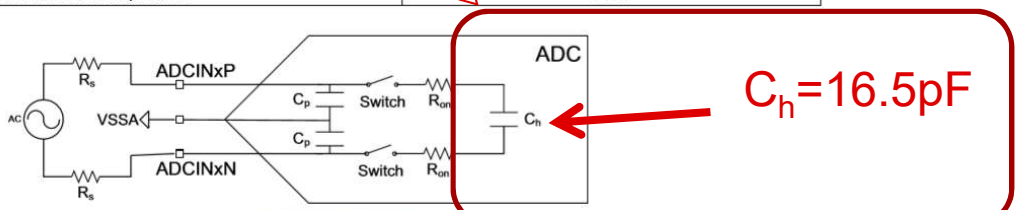


Figure 5-28. Differential Input Model

Table 5-44 lists the parasitic capacitance on each channel. Also, enabling a comparator adds approximately 1.4 pF of capacitance on positive comparator inputs and 2.5 pF of capacitance on negative comparator inputs.

Important Datasheet Parameters

TMS320F283x 16-B, 1.1-MSPS, Fully-Differential Input ADC

VREF = 3V
Fully-Differential Input ADC

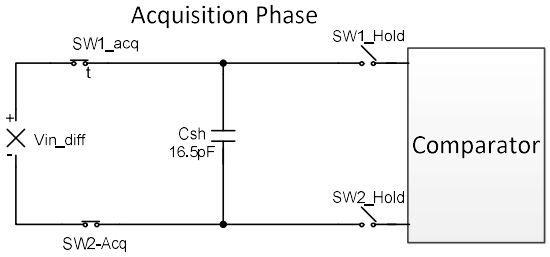
Full-scale Range: ±VREF = ±3V = 6V

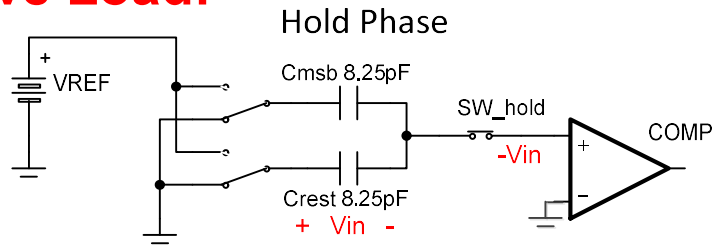
ADC Resolution / Least Significant Bit (LSB):

$$LSB = \frac{\pm VREF}{2^N} = \frac{2 \cdot VREF}{2^{16}} = 91.6uV$$

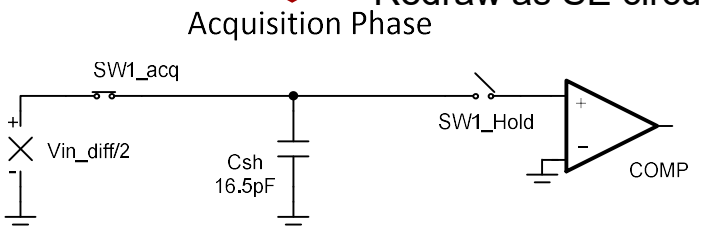
$$\frac{1}{2} LSB = 45.8uV$$

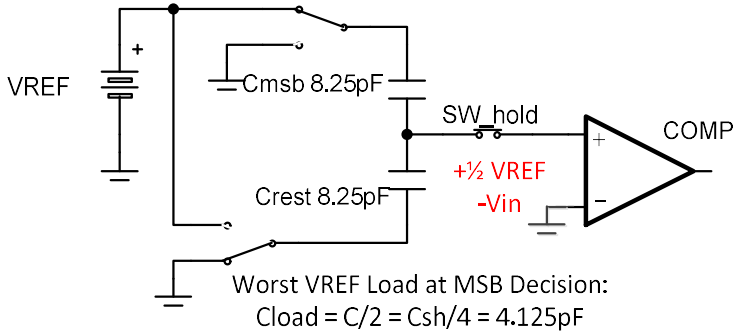
Estimate the worst case REFIN Capacitive Load:

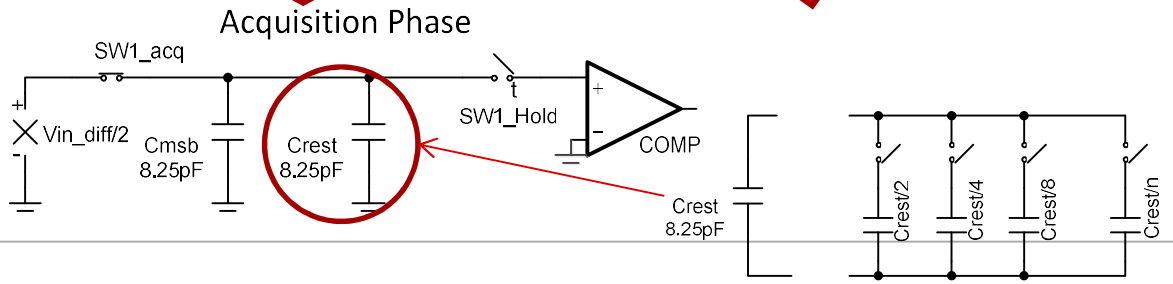




Redraw as SE circuit



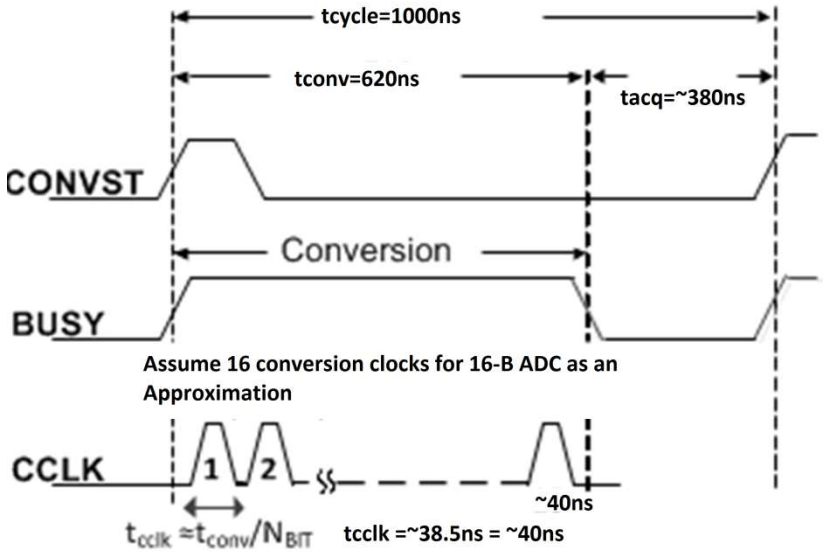




NOTE: REFIN Cmsb not always ¼ Csh; depends on device Architecture!!
This is a first order estimate.

Conversion Period and Conversion Clock Timing

Estimate internal ADC Conversion Clock period



$$Fsample = 1000kHz$$

$$tcycle = \frac{1}{1000kHz} = 1us$$

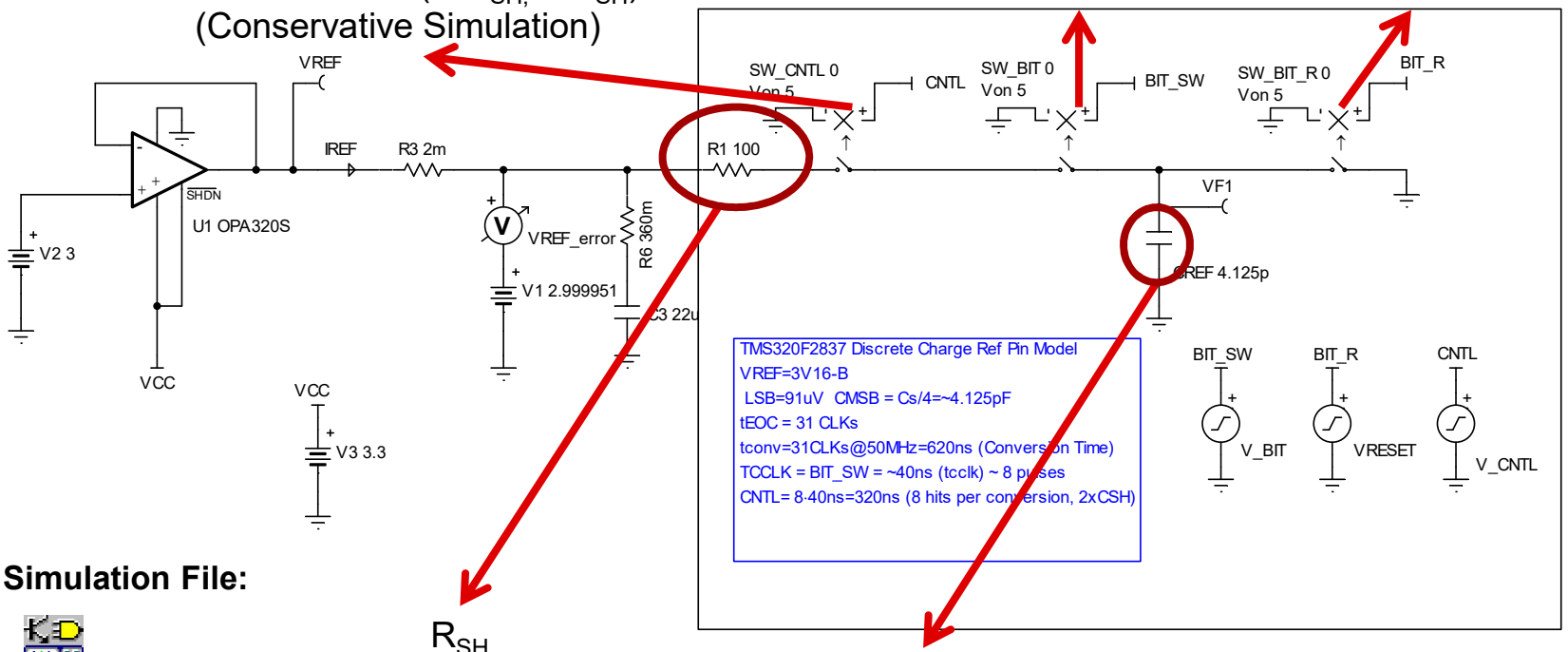
$$t_{conv} = 620ns$$

$$t_{cclk} \approx \frac{t_{conv}}{N_{BIT}} = \frac{620ns}{16} \approx 38.75ns \approx 40ns$$

TINA SPICE Equivalent Model

t_{CNTL} =40ns*8=320ns (mask)
4-8 transients (1*$C_{SH,}$ 2*C_{SH})
(Conservative Simulation)

Conversion Clock (CCLK) Resets
t_{cclk} =~40ns (25MHz) CREF to 0V



TINA Simulation File:

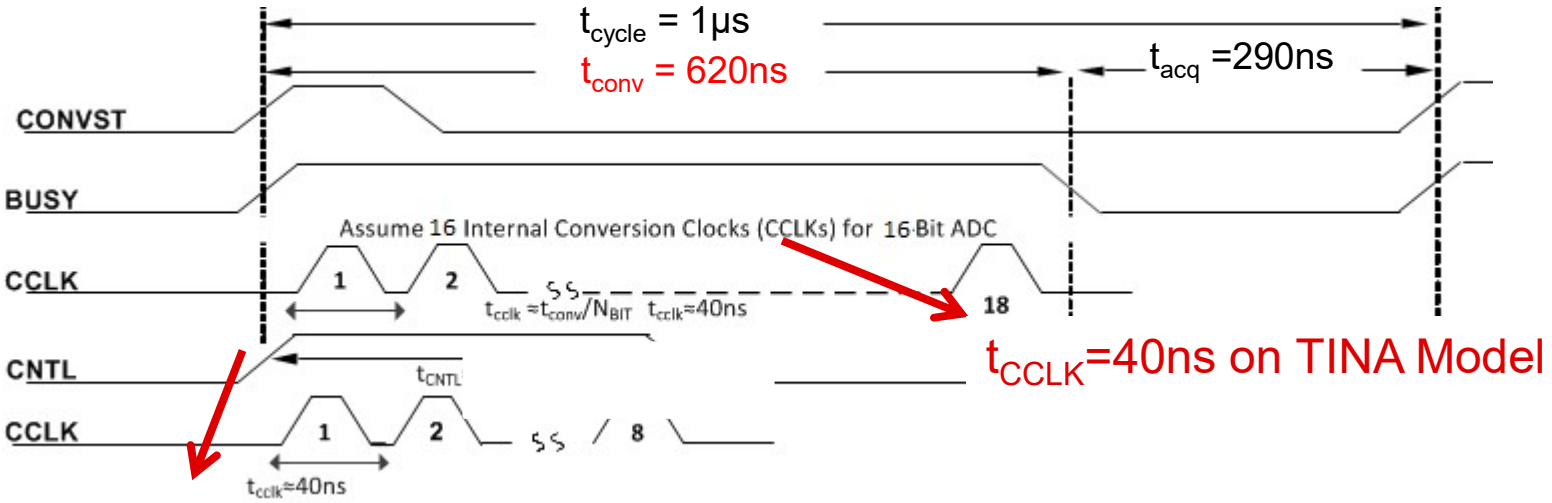
ReferenceDrive_TMS330_opa320_22uF.TSC

R_{SH}

C_{LOAD} = 1/4 C_{SH}= 4.125pF

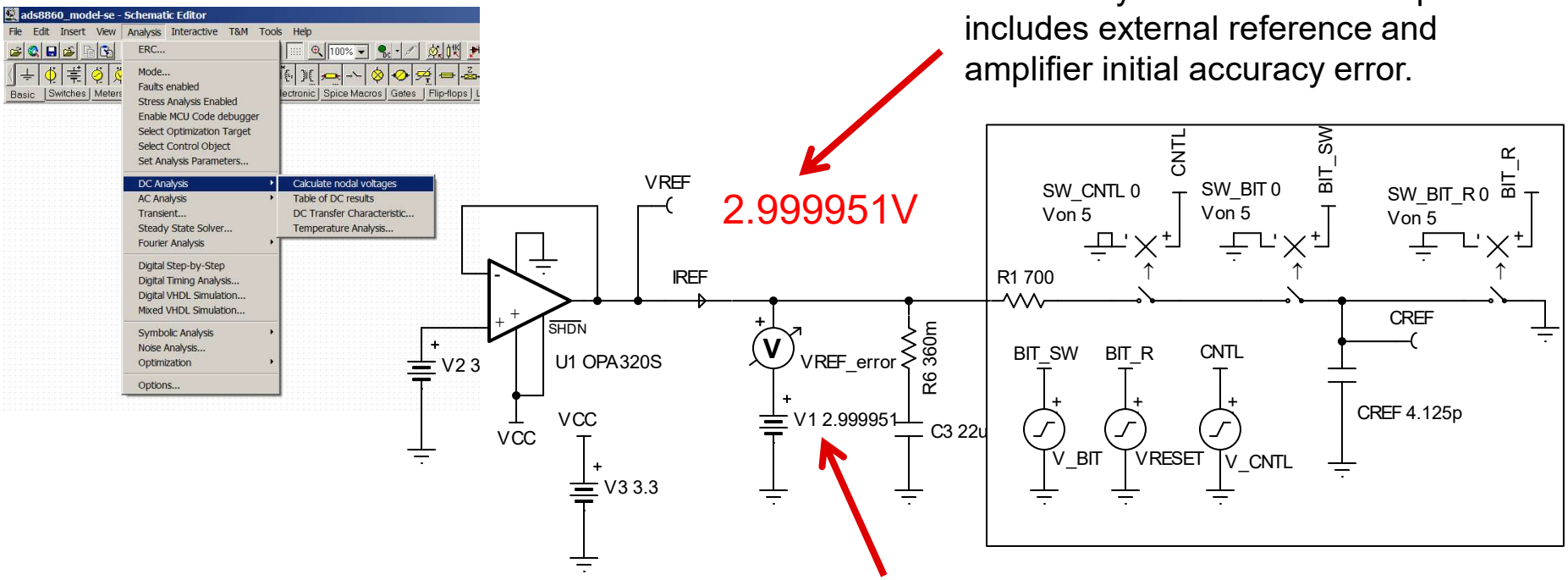
Timing diagram (Approximation)

Assume C_{LMSB_LOAD} switches 8x times During each Conversion:
Total C_{LOAD} = 2 x C_{SH} (Conservative Approximation for Margin)



CNTL: SPICE Model Signal, used to mask CCLK
Allow 8x C_{LOAD} transients (8x CCLKs) per conversion (conservative Estimate)

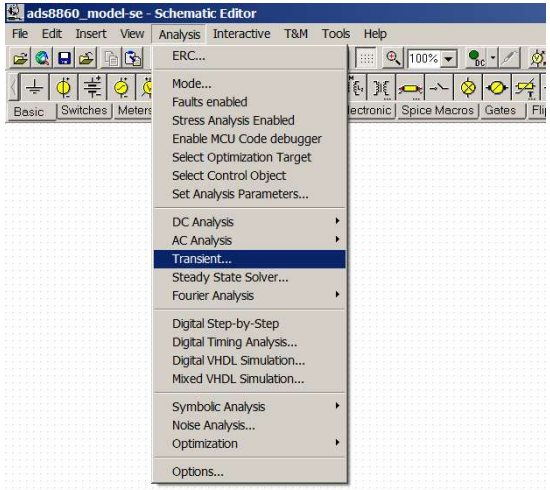
Steady state Simulation Results

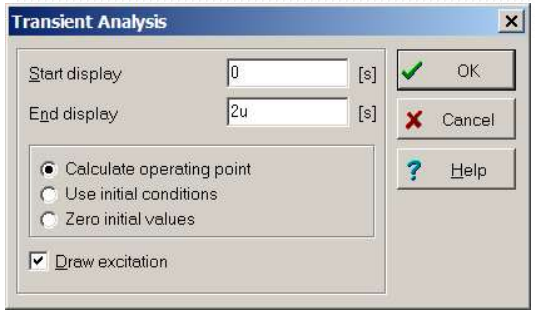


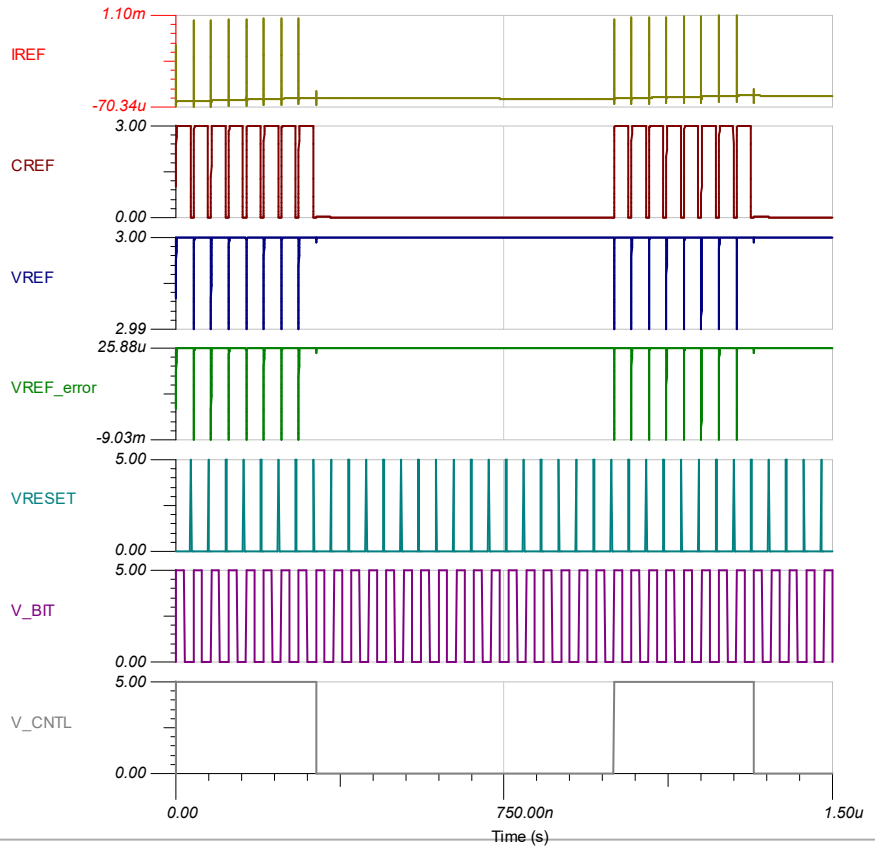
The steady state Reference input to the includes external reference and amplifier initial accuracy error.

Set the Reference input source to match the steady state Reference input.

Example simulation: transient results







Transient Current into REFIN Pin

Voltage on CREF_Load internal capacitor

REFIN Pin voltage

REFIN error Voltage

Switch control signal RESETs C_{REF} voltage

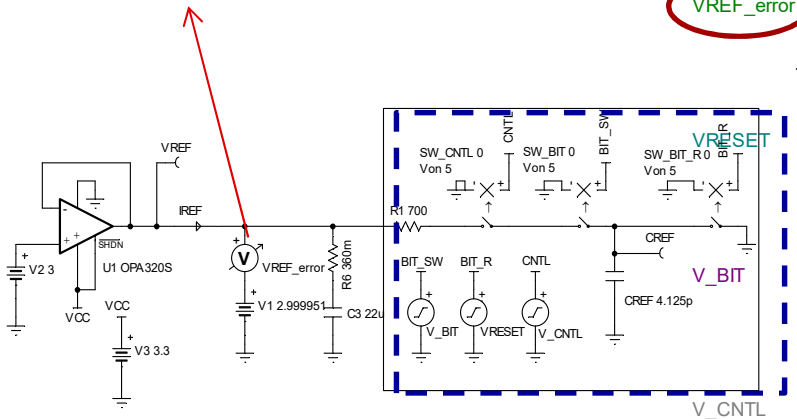
Switch control signal Conv Clock (CCLK)

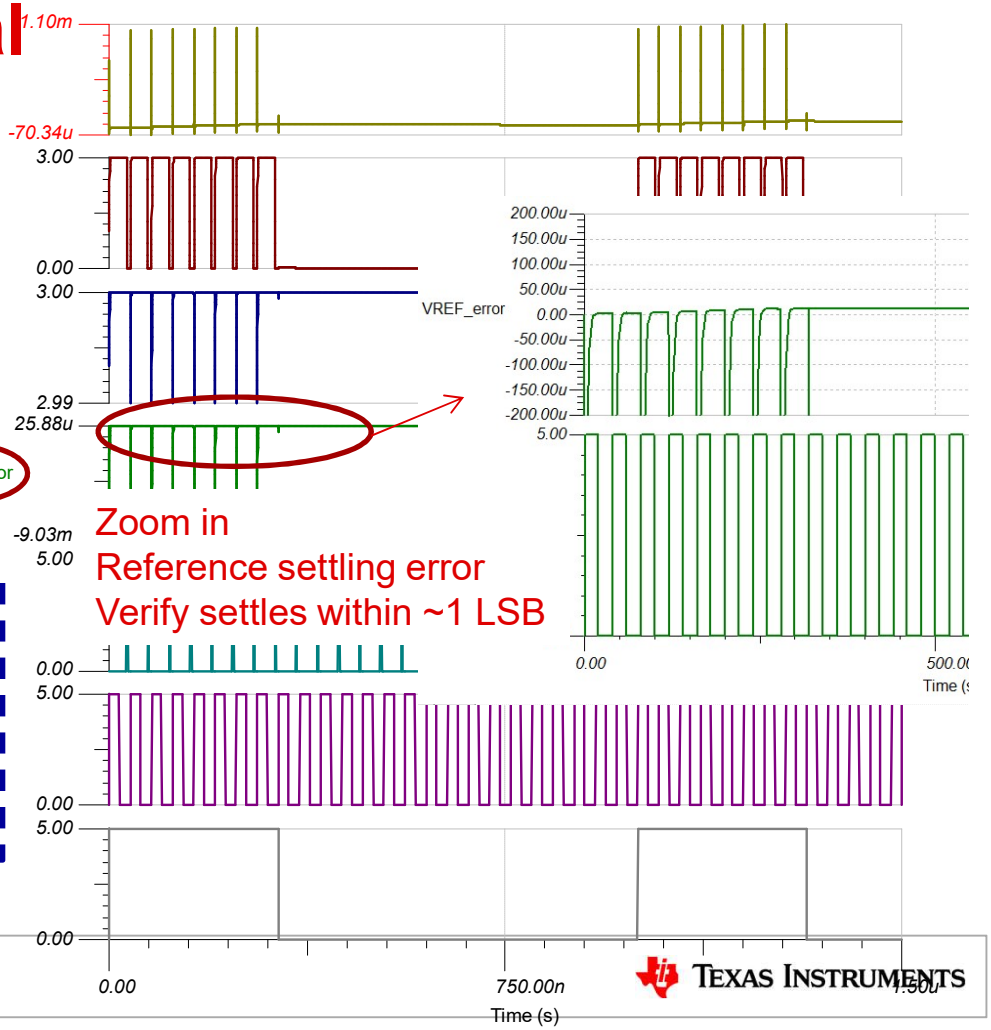
CNTL switch signal (8xC_{REF} Loads per Conv)

Key Result: Error Signal

Must settle within each
Tconv clock cycle
To less than LSB (91µV)

Check Settling



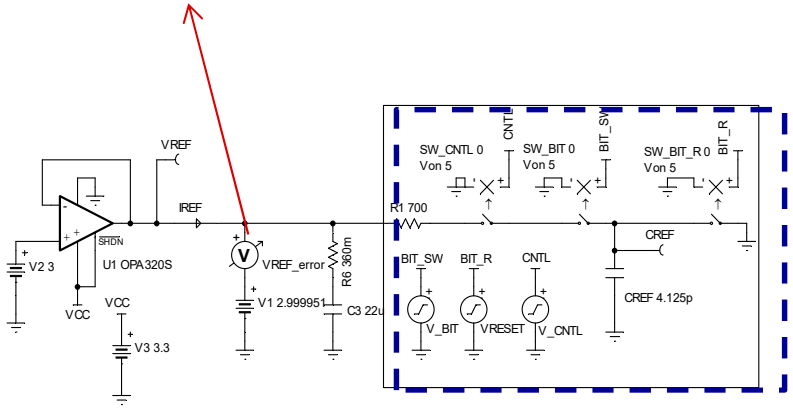


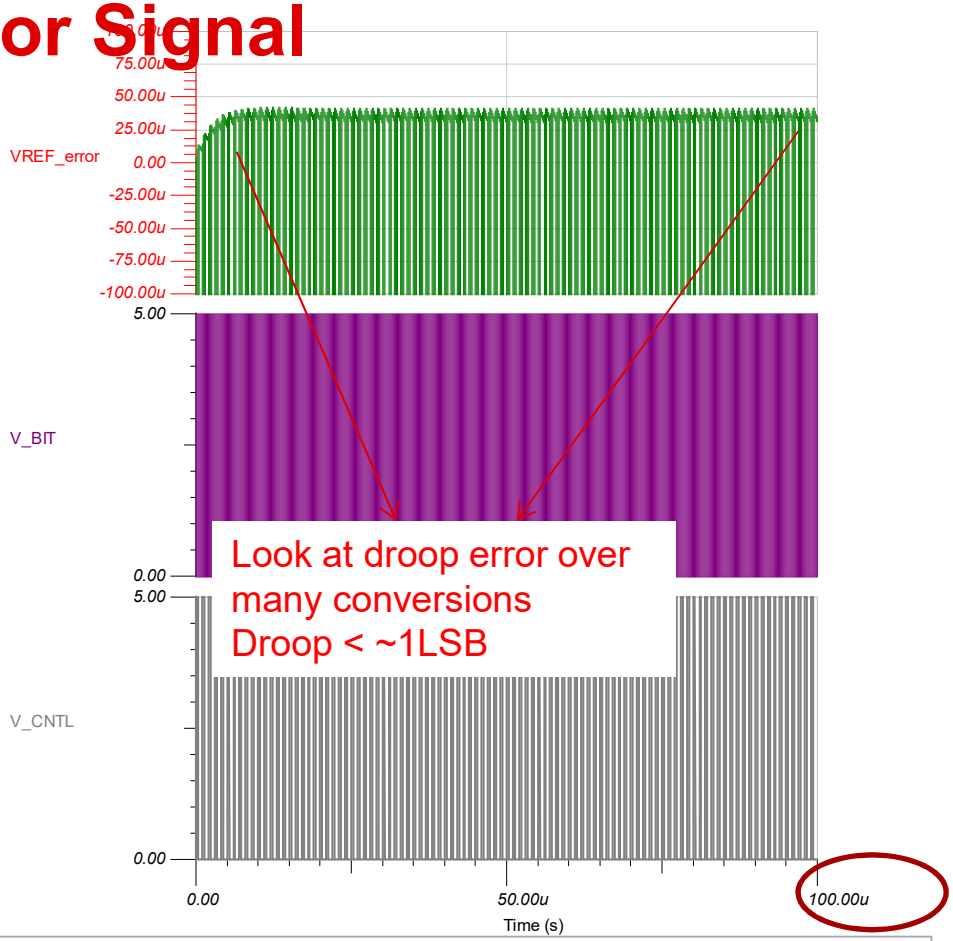
Zoom in
Reference settling error
Verify settles within ~1 LSB

OPA2320 Key Result: Error Signal

Check Settling over many conversions for droop.

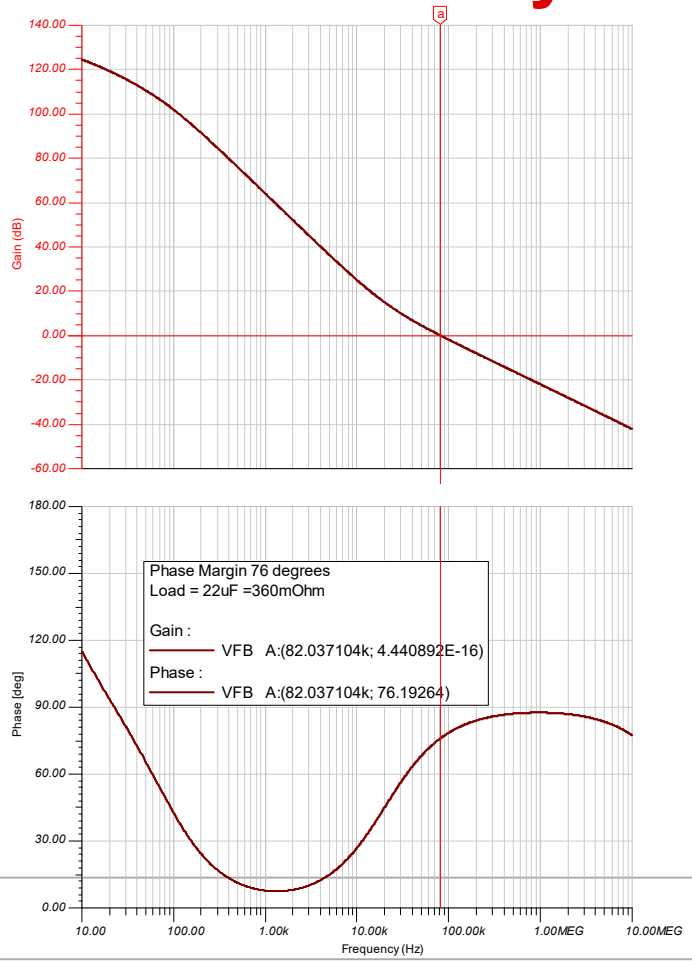
Check Settling



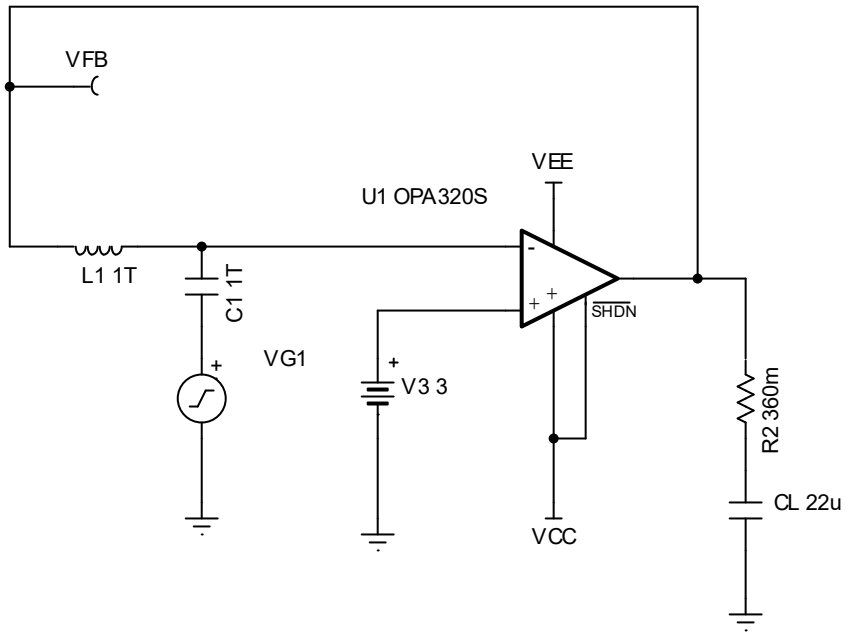


OPA320 Stability Simulation

TINA Simulation:



opa320_ref_stability_22u_360mOhm_3_25_20.TSC



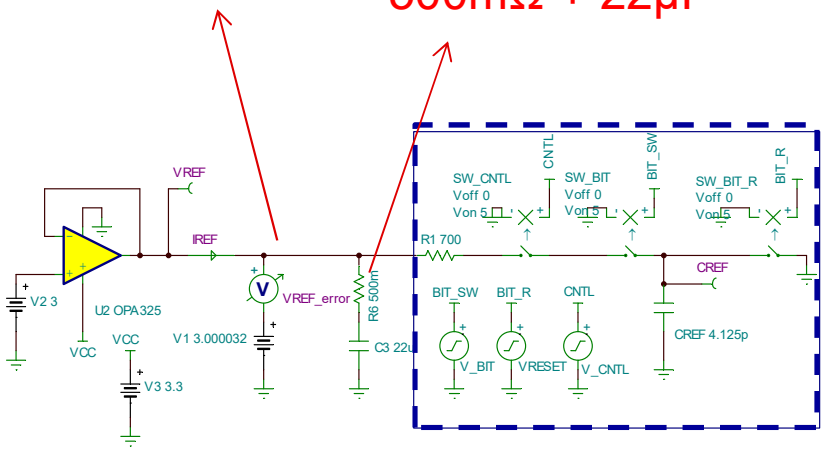
1x REFxx30 + 2x OPA2325 Simulations (Alternative Solution)

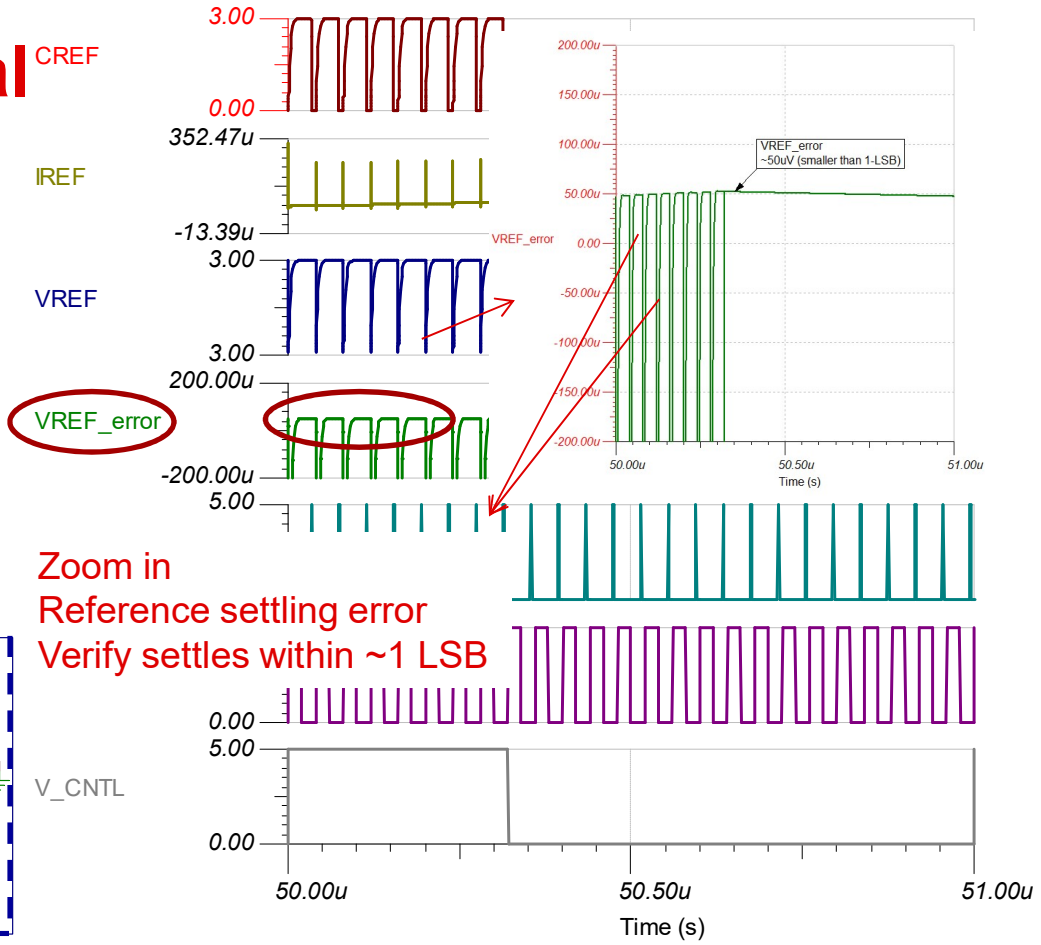
Key Result: Error Signal

Must settle within each
Tconv clock cycle
To less than LSB (91µV)

Check Settling

500mΩ + 22µF

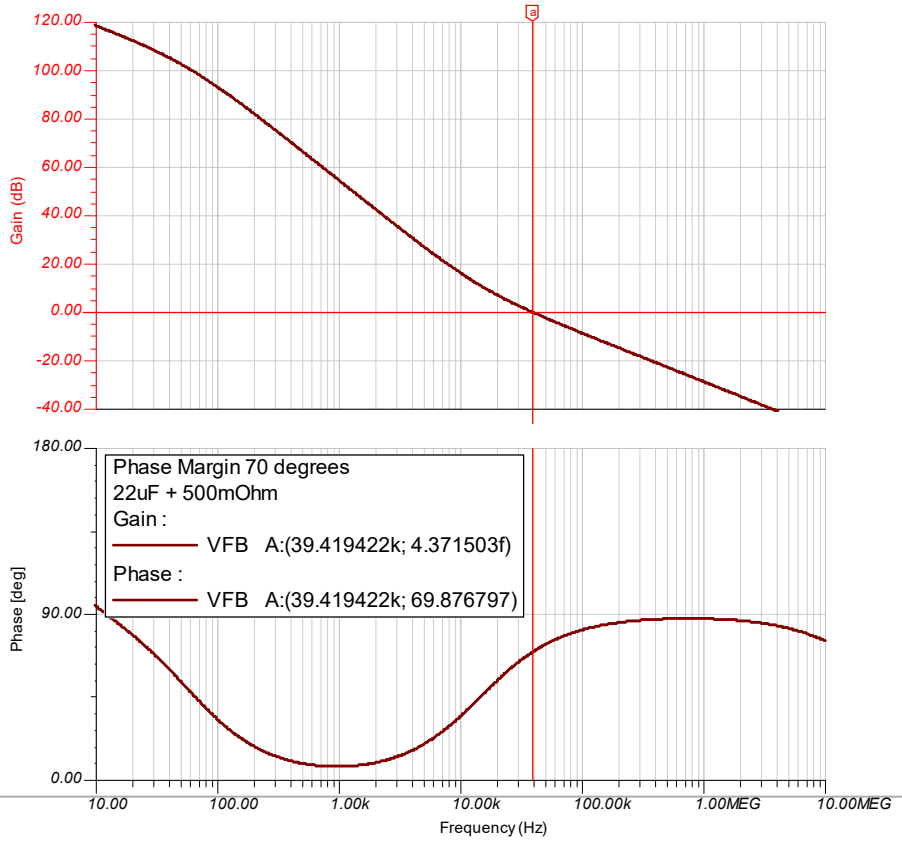


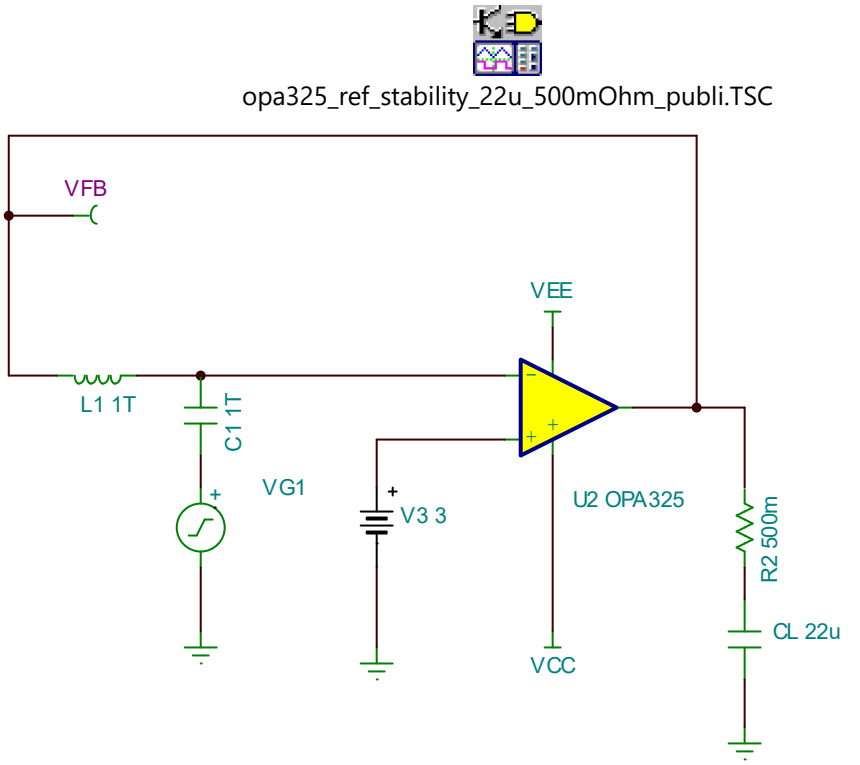


Zoom in
Reference settling error
Verify settles within ~1 LSB

OPA325 Stability Simulation

TINA Simulation:





Thanks for your time!

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