What happens if input(s) go below ground?

Going below ground by more than 500mV (actual voltage varies with temperature) will create new current paths (shorts) in die layout specific parasitic transistors. It is similar to dropping your phone in salt water (shorts out).

There are several symptoms; input current will flow and can be excessive if not limited by external resistance. ICC can increase. Nearby pin current can increase. Some other pins (usually output) may also go below ground. The output could have phase inversion.

All samples of the same die design will usually have the same results. However, depending on this fact is not a good design practice.

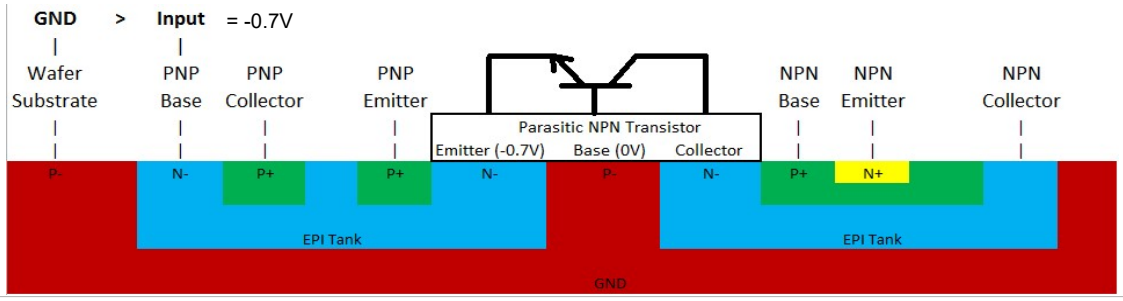
Two die designs from same manufacturer might have different results.

Devices from two different manufacturers might have different results.

The moral is to not let input(s) go below ground but if you do, be prepared for instant or distant future production problems. At a minimum put note in the design for future reference.

How do these parasitic transistors form?

The wafer substrate is connected to the most negative device pin usually GND, VEE, or VCC-. In this example there are two transistors in blue tanks (in some processes, called wells); an op-amp input is -0.7V and connects to a PNP transistor base (on left). This forward biases a PN junction everywhere the left EPI tank touches substrate. So electrons are emitted into the substrate where they become minority carriers. Most of these electrons are drawn to other EPI tanks where they are collected. This action matches the name of the NPN pins seen in center, emitter, base and collector. The parasitic transistor steals current from the transistor on right. Normally these two transistors operate independently

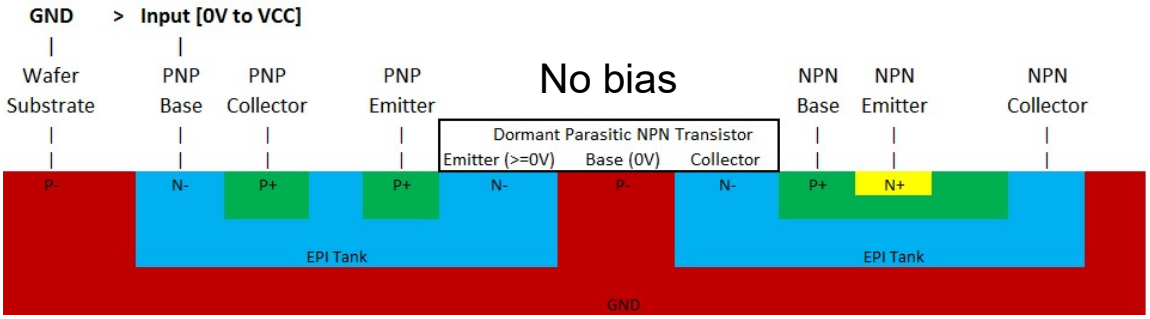


The reason these parasitic transistors normally lie dormant.

In normal operation, all of EPI tanks are 0V or positive. Therefore all the tank to substrate diodes are unbiased or reverse biased. No current flows from tank to tank therefore each tank runs independently as if the parasitic transistor was not there.

Most CMOS op-amp also have these parasitic NPN transistors even though the intentional transistors have drain, back-gate, and source terminals with P and N doped silicon.

Only devices with oxide isolated well/tanks can avoid these parasitic transistors.



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