Parasitics in Precision PCB Layouts

Material created by Ian Williams and Chris Featherstone

Presented by Thomas Kuehl

February 2013

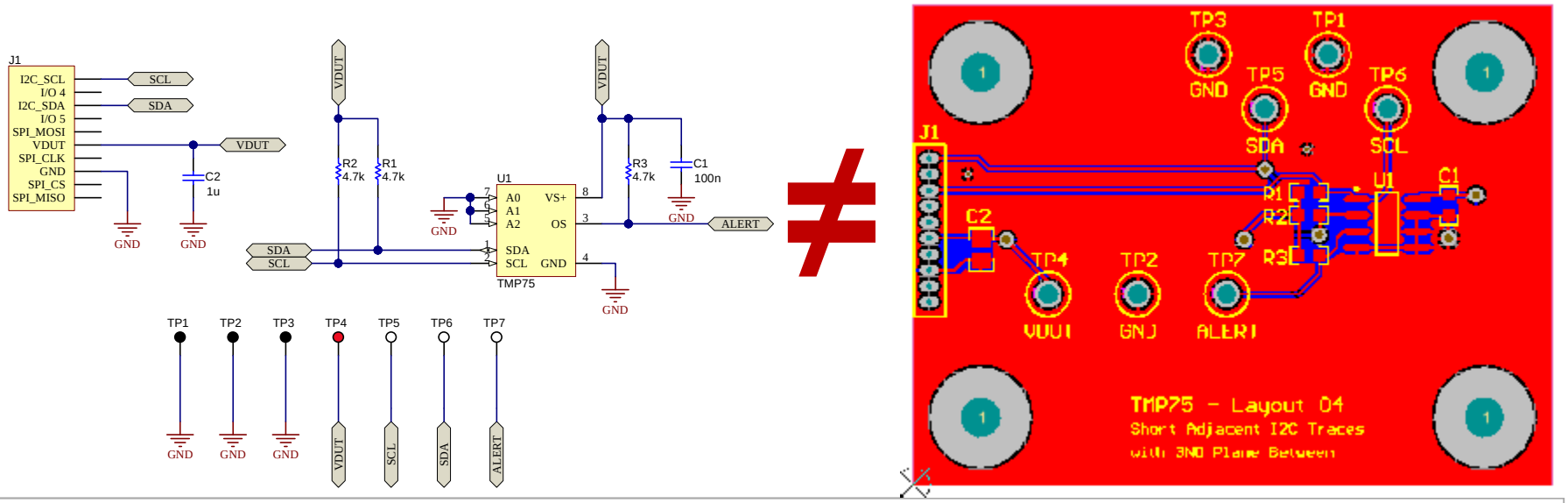
Agenda

- **Background**
  - What are printed circuit board parasitics?
  - Why do they matter?
- **Parasitics Discussion**
  - Parasitic thermocouples
    - Theory of formation and circuit effects
    - Test case: INA333 V_{OS}
  - Solder Flux Contamination
    - What is solder flux?
    - Circuit effects
    - Test case: INA333 bridge sensor
  - Parasitic Capacitance and Inductance
    - Theory of formation and circuit effects
    - Test cases: TMP75 I^2C bus, INA331 & INA333 bridge sensor
- **Summary**

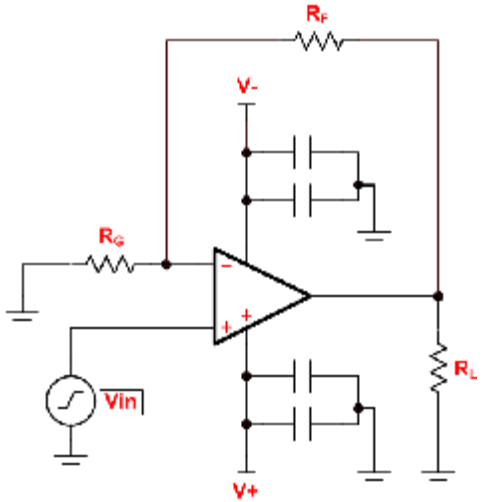
Background

What Are PCB Parasitics?

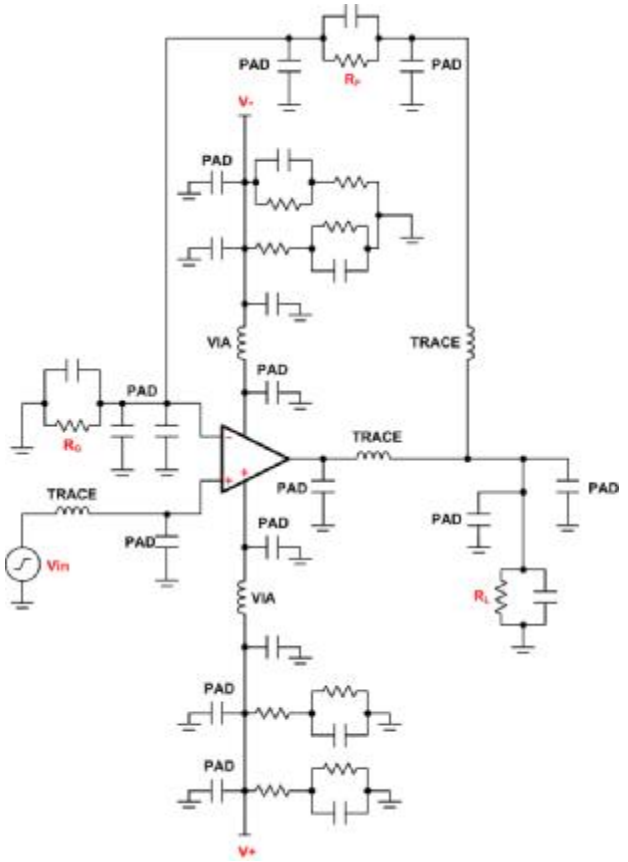
- An ideal printed circuit board has no impact on a circuit's performance
  - Circuit behaves exactly as designed & simulated on the schematic level
- In reality, certain PCB layout techniques, electronic components, and other materials create "extra" circuit elements
- These are known as **parasitics**!
- Examples: capacitors, inductors, resistors, thermocouples



What Do You Mean, “Extra” Circuit Elements?



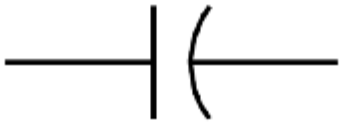
Typical op-amp circuit
(as designed)



Typical op-amp circuit
(including parasitics)

Source: “A Practical Guide to High-Speed Printed-Circuit-Board Layout”

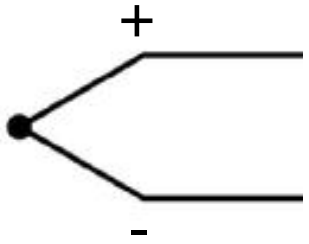
Why Do Parasitics Matter?



- Capacitors
  - Allow unwanted signal and noise coupling between nodes
  - Alter frequency response (create filters)
  - Cause instability issues

- Inductors
  - Allow unwanted signal and noise coupling between nodes
  - Increase return loop inductance

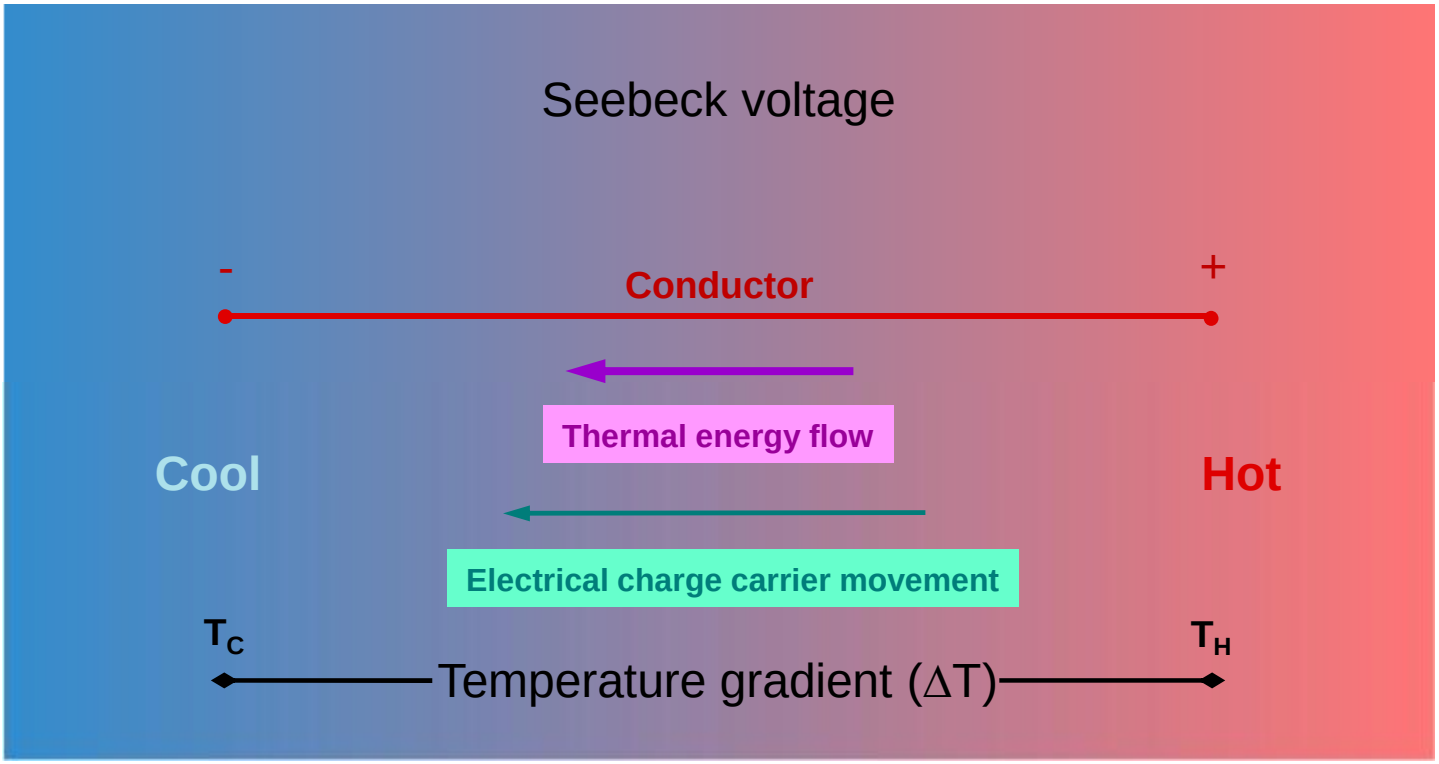
- Resistors
  - Cause gain errors
  - Cause DC voltage errors
  - Create current leakage paths
  - Create mismatches at inputs of amplifiers (degrades CMRR)



- Thermocouples
  - Cause DC voltage errors when exposed to thermal gradients

Thermocouples

Thermocouple Theory



- Any conductor will produce a voltage when there is a temperature gradient (ΔT) across it
  - Known as the **"Seebeck Effect"**

Thermocouple Theory

Thermoelectric Sensitivity

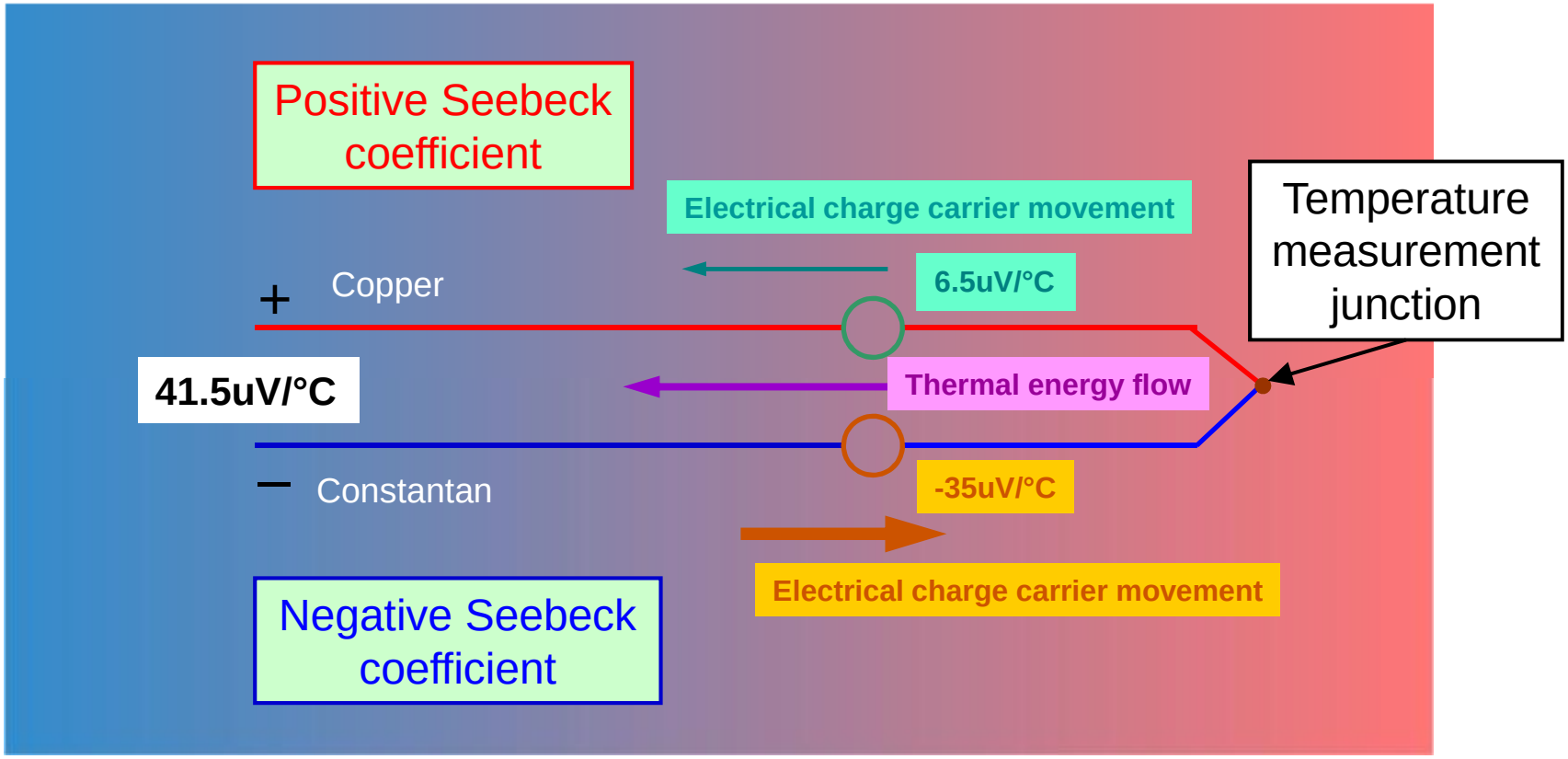
The Seebeck coefficients (thermoelectric sensitivities) of some common materials at 0 °C (32 °F) are listed in the following table.

Material	Seebeck Coeff. *	Material	Seebeck Coeff. *	Material	Seebeck Coeff. *
Aluminum	3.5	Gold	6.5	Rhodium	6.0
Antimony	47	Iron	19	Selenium	900
Bismuth	-72	Lead	4.0	Silicon	440
Cadmium	7.5	Mercury	0.60	Silver	6.5
Carbon	3.0	Nichrome	25	Sodium	-2.0
Constantan	-35	Nickel	-15	Tantalum	4.5
Copper	6.5	Platinum	0	Tellurium	500
Germanium	300	Potassium	-9.0	Tungsten	7.5

*: Units are μV/°C; all data provided at a temperature of 0 °C (32 °F)

Source: www.efunda.com

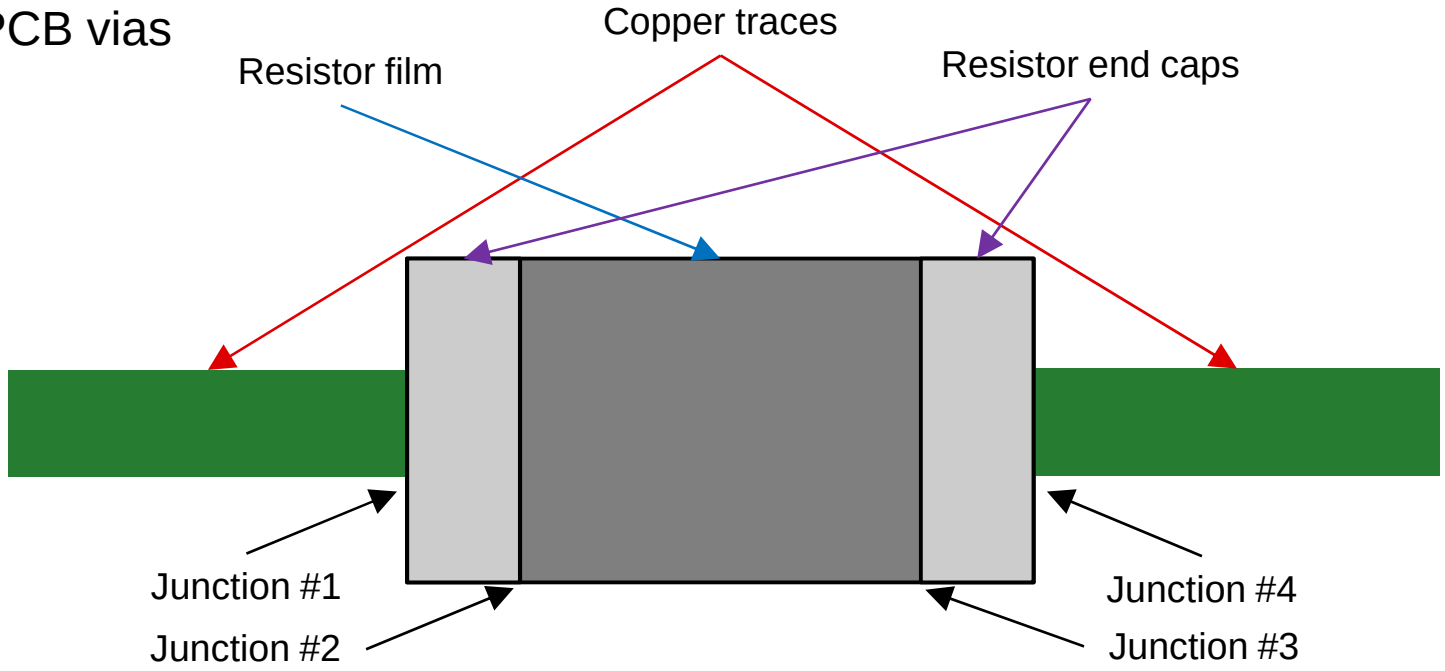
Thermocouple Theory



- Different metals have different **thermal sensitivities**
- Two metals can be joined together to create a practical temperature measurement device with a known thermoelectric behavior

Thermocouples on PCBs

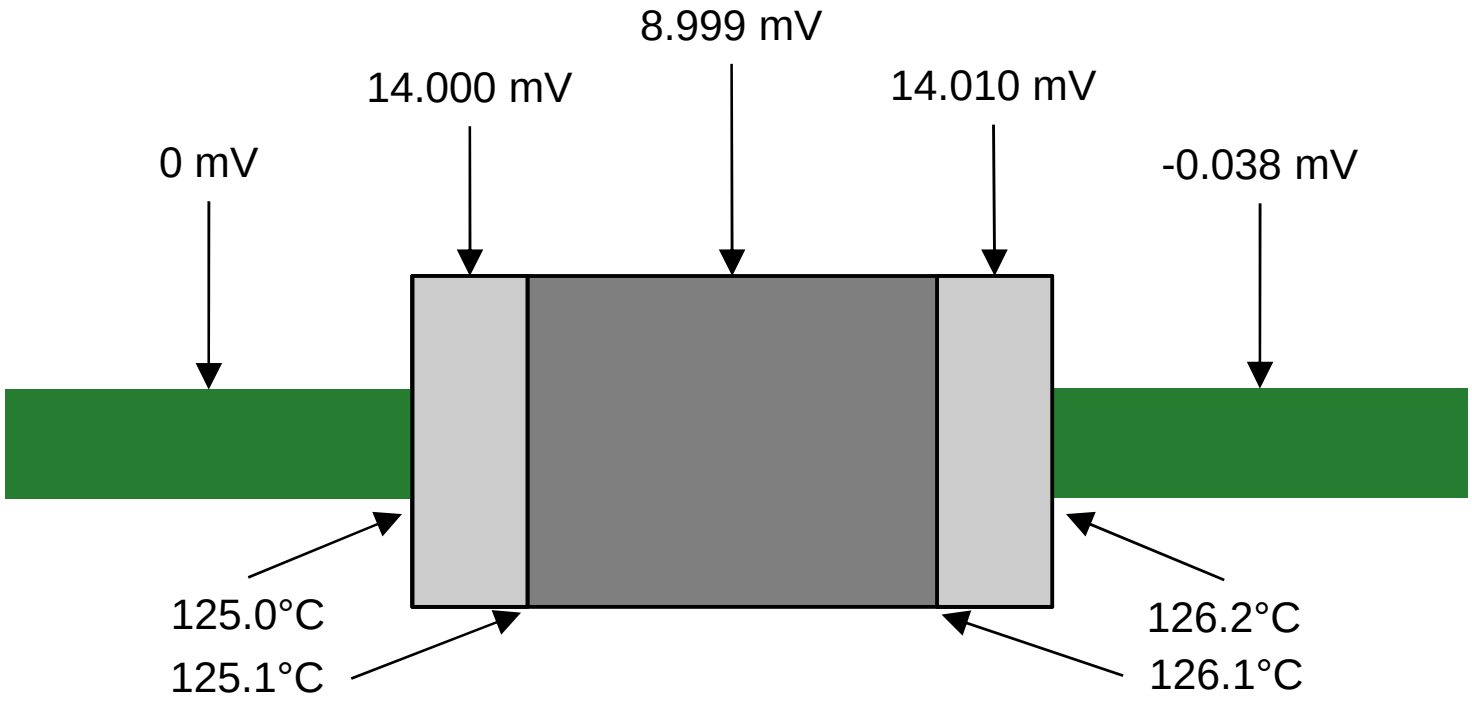
- Junctions of dissimilar conductors are everywhere on a PCB!
  - Components soldered to a copper pad
  - Wires mechanically attached to the PCB
  - Jumpers and connectors
  - Solder joints
  - PCB vias



Source: “Op Amp Precision Design: PCB Layout Techniques”

Thermocouples on PCBs

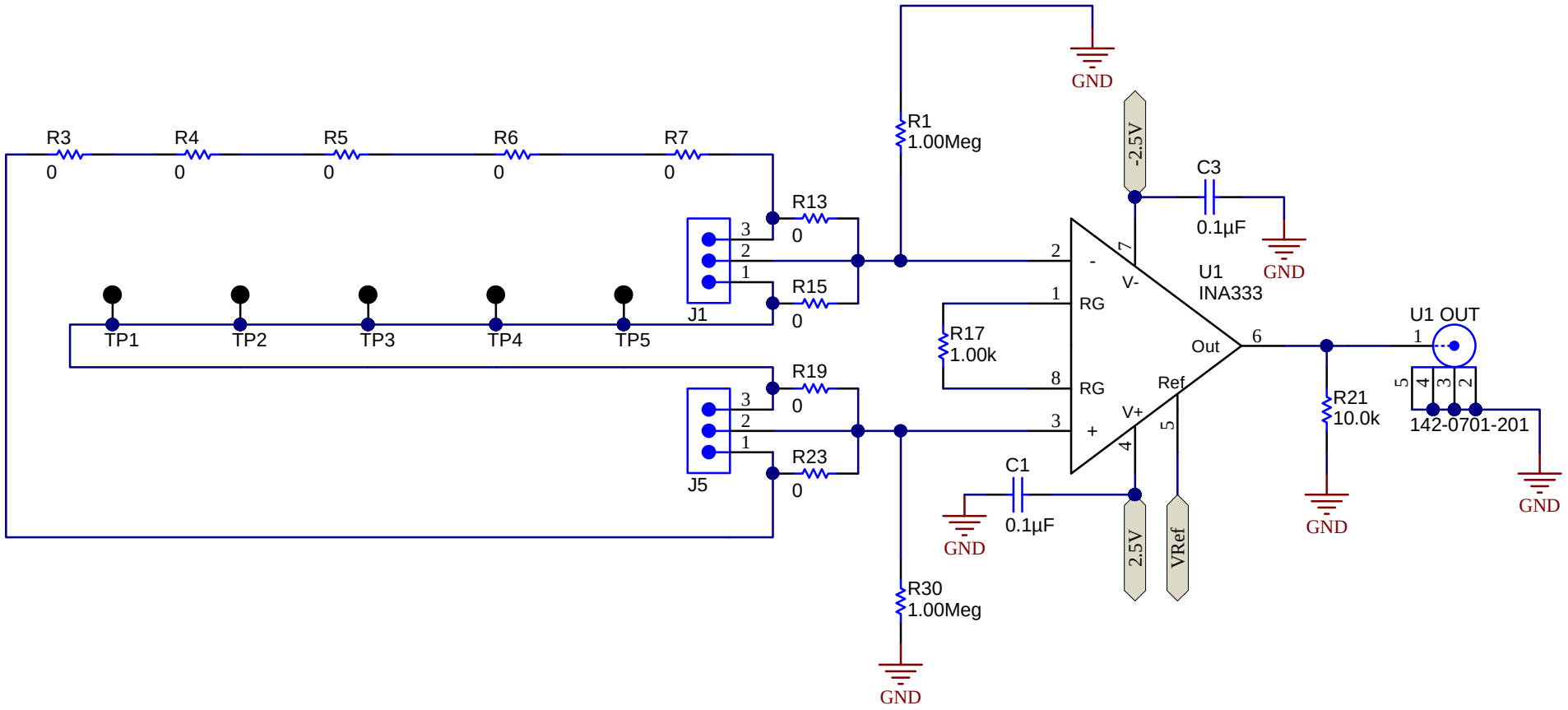
- If temperature gradients are present, these junctions will create a thermoelectric voltage.



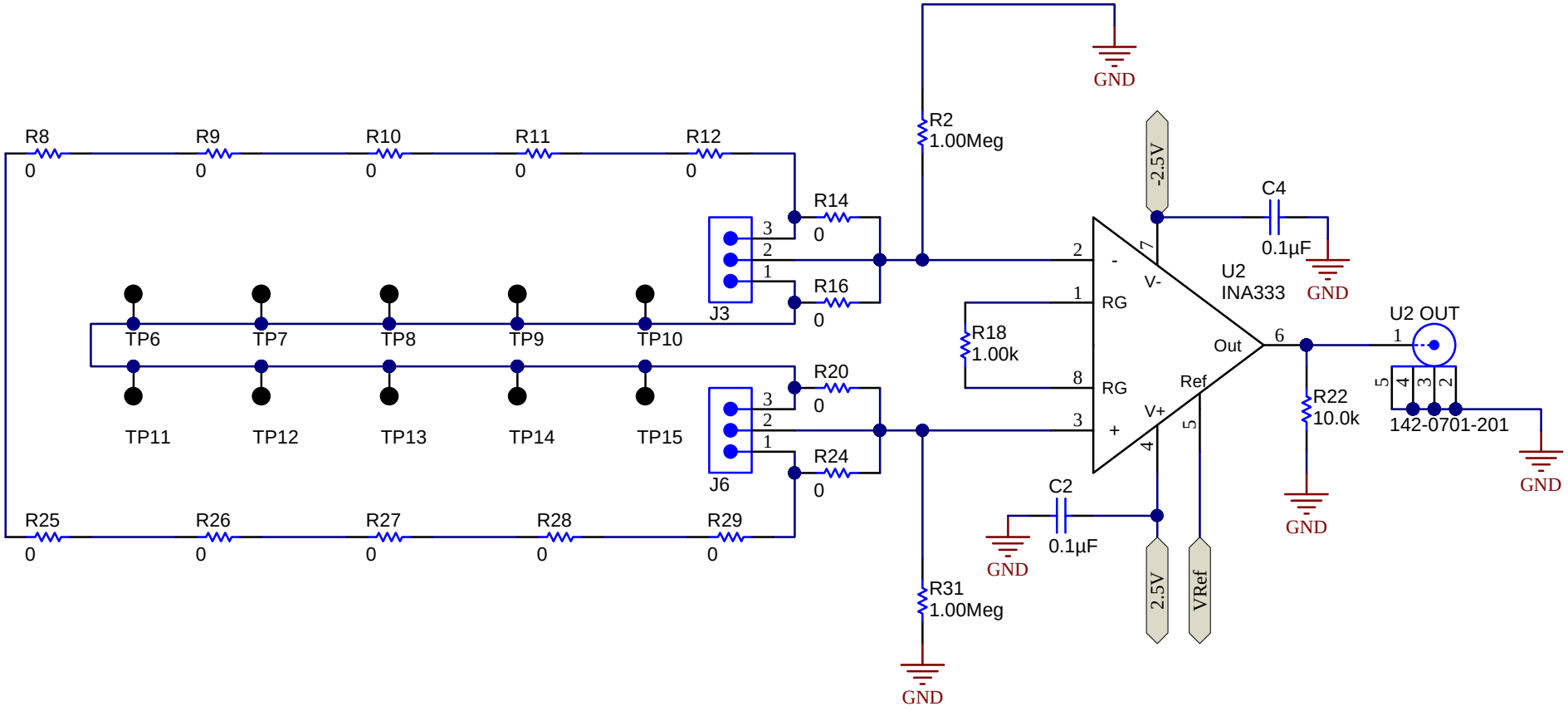
- In this example, a temperature gradient of +1.2°C caused a total of -38 µV to appear across a resistor.

Source: “Op Amp Precision Design: PCB Layout Techniques”

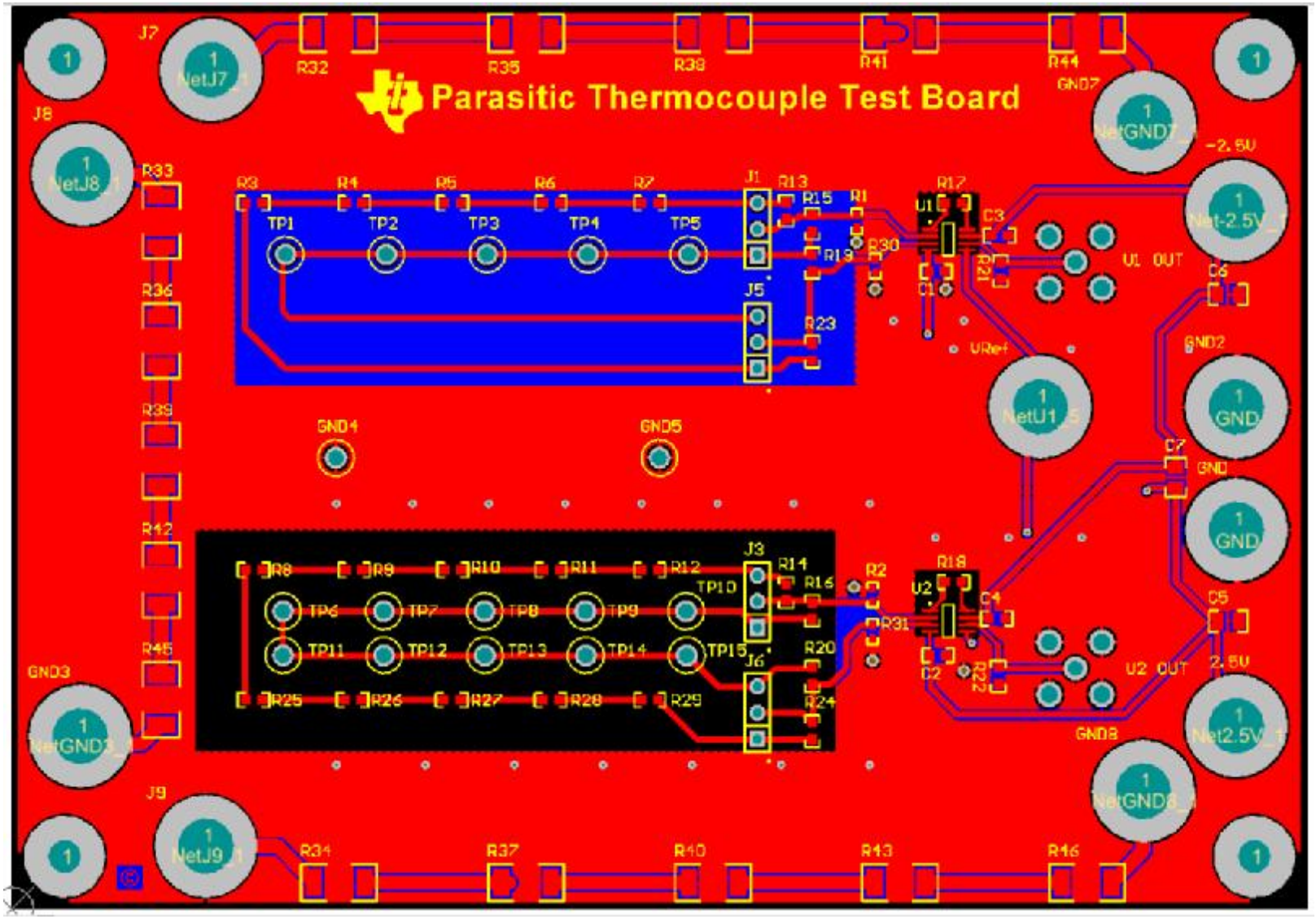
Test Case: INA333 V_{OS} Circuit



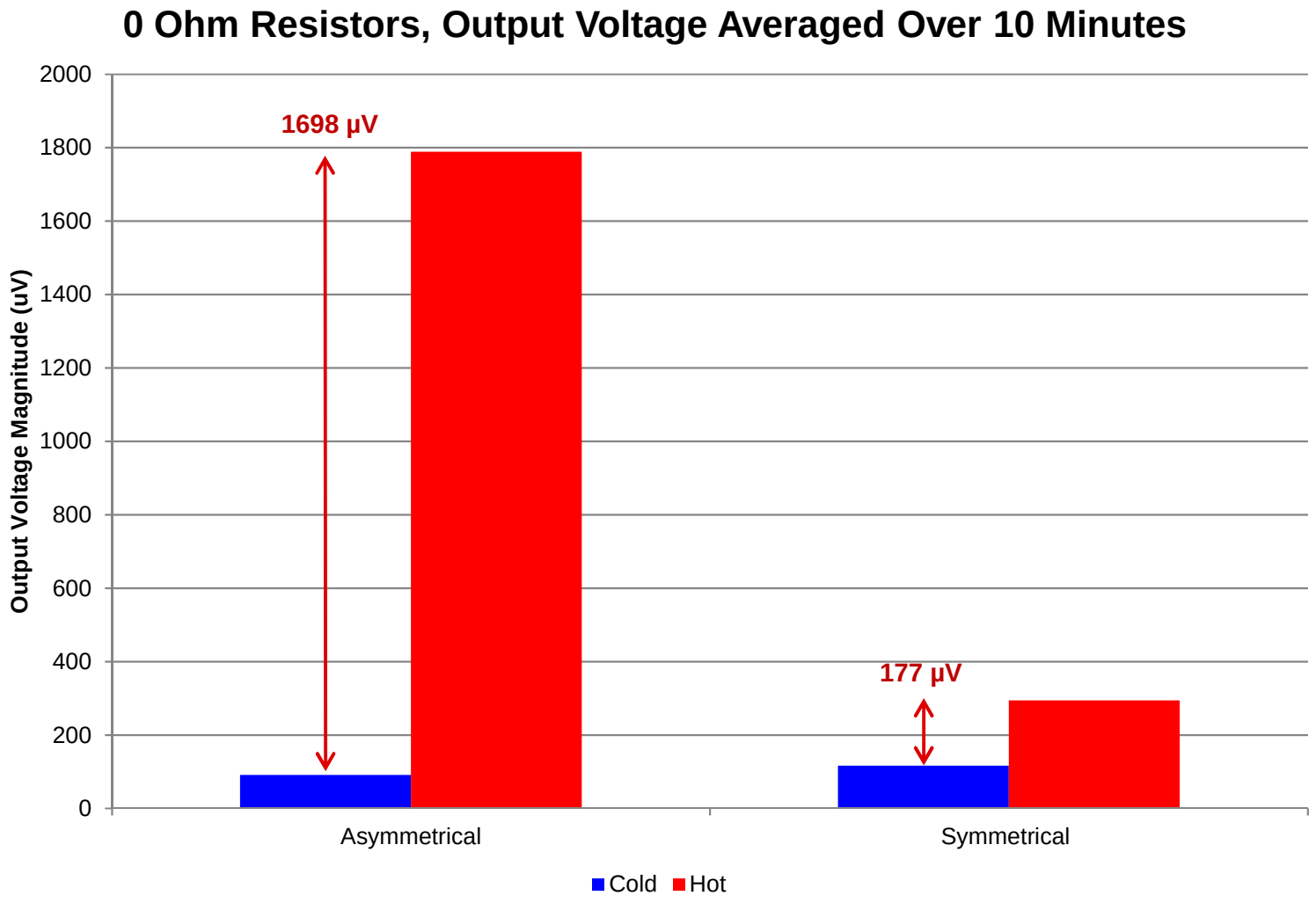
INA333 V_{OS} Circuit (Symmetrical)



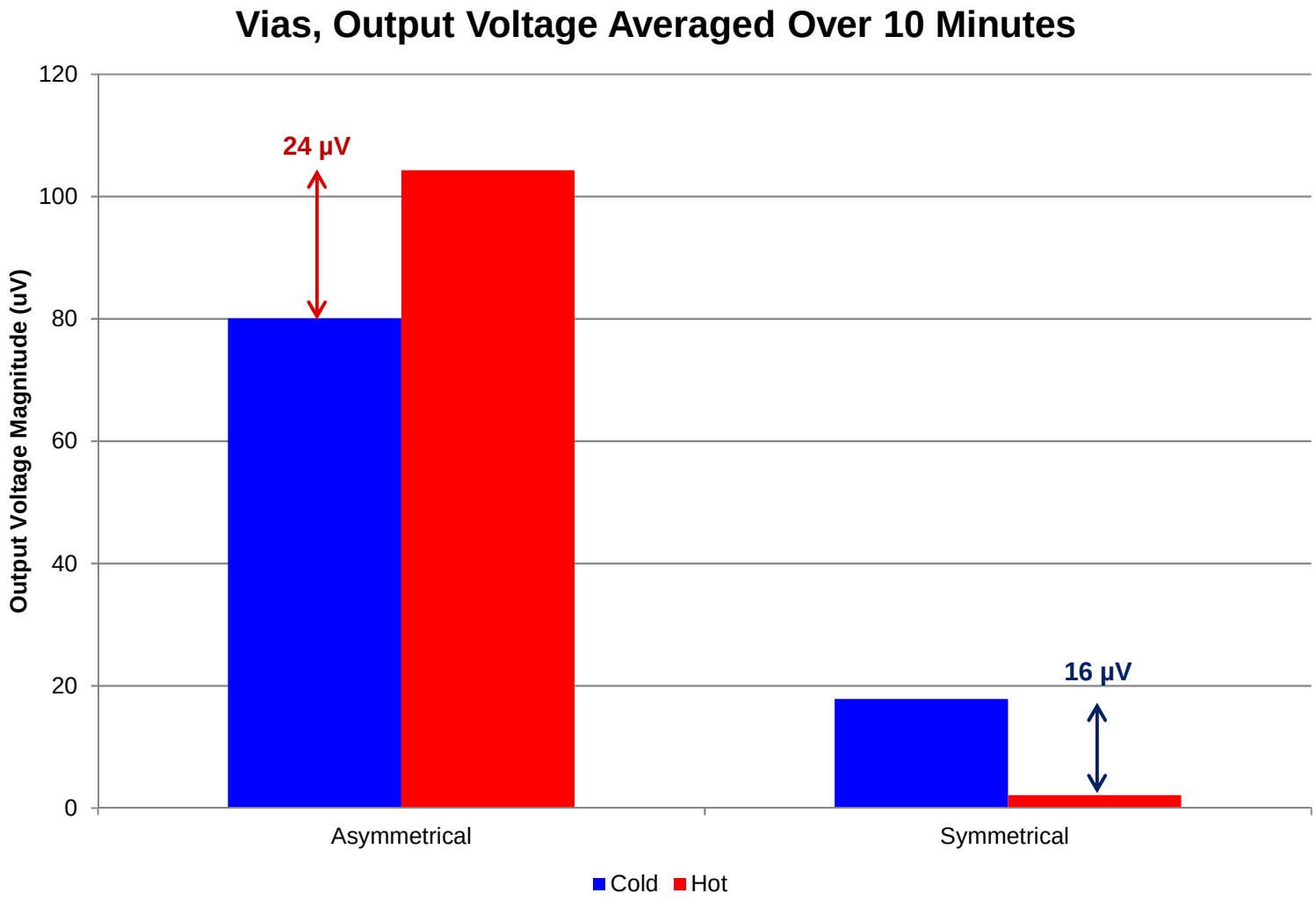
INA333 V_{OS} Circuit Layout



INA333 V_{OS} Results – 0Ω Resistors



INA333 V_{OS} Results – Vias



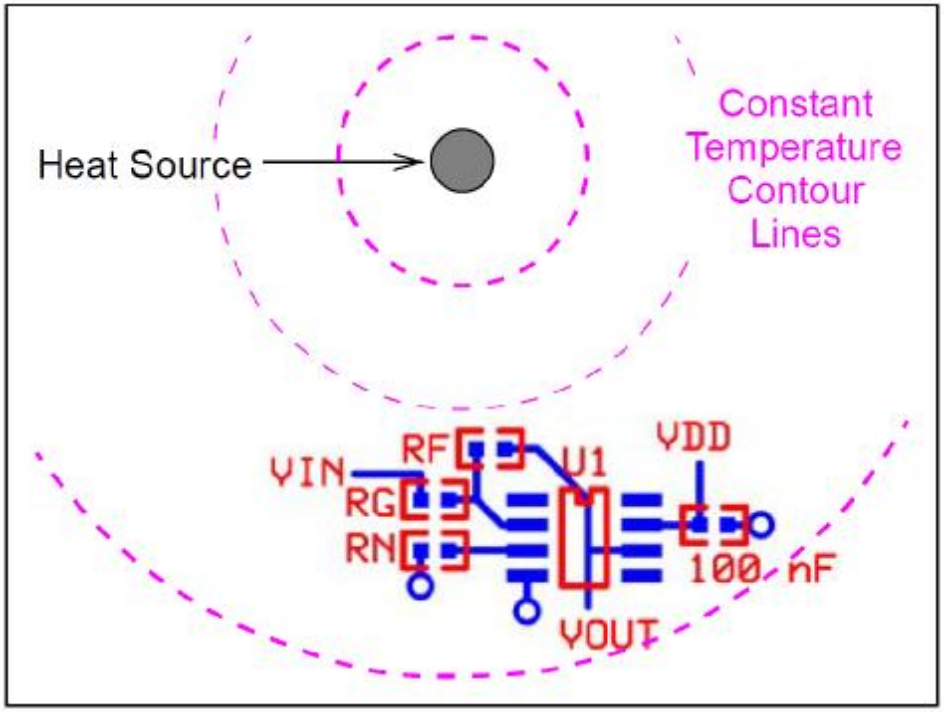
Thermocouples - Conclusions

- Parasitic thermocouples can have a significant impact on V_{OS}!
- As expected, asymmetrical configurations see a much more pronounced increase in offset voltage
- 0Ω resistors key result - V_{OS} (RTI) increased by up to 17µV!
- Vias key result - V_{OS} (RTI) increased by up to 250nV
  - Difference small enough to be solely caused by INA V_{OS} and gain drift
- Additional testing will be done to isolate the thermocouple effect from the V_{OS} and gain error drift of the INA333

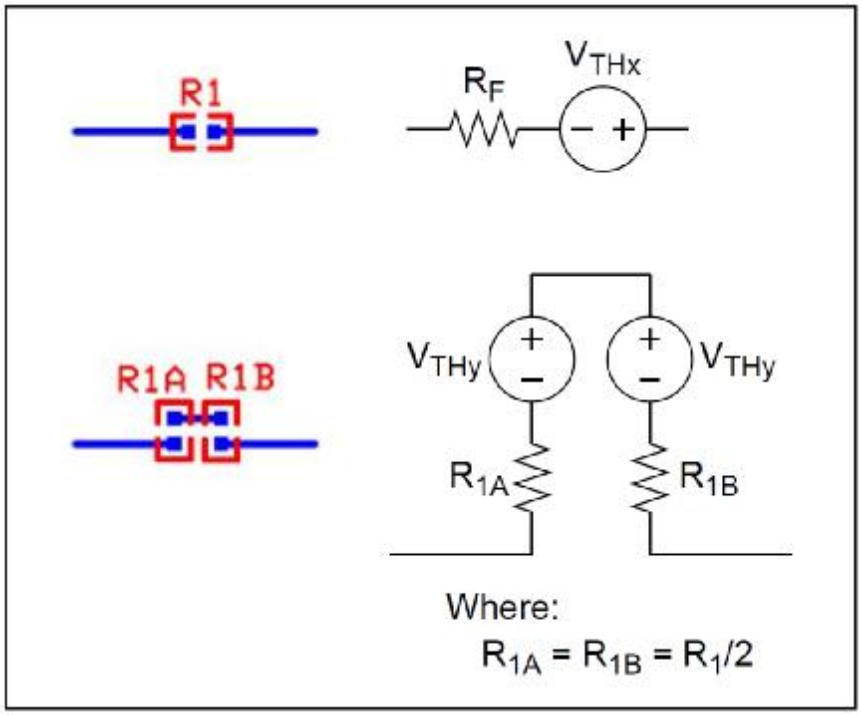
Thermocouples - Recommendations

- Use symmetrical configurations to minimize V_{OS} and CMRR degradation
- Isolate sensitive nodes from thermal gradients by removing copper pours which dissipate heat
- Reduce the board's heat generation or redirect the heat flow away from critical areas through the use of heat sinks or fans
- Place critical components in areas of constant temperature
  - Heat travels radially, so follow thermal contour lines
- Use materials with similar Seebeck coefficients (when possible)
- Replace single resistors with equivalent parallel resistor combinations in order to cancel thermoelectric voltages

Thermocouples - Recommendations



Components aligned with thermal contour lines



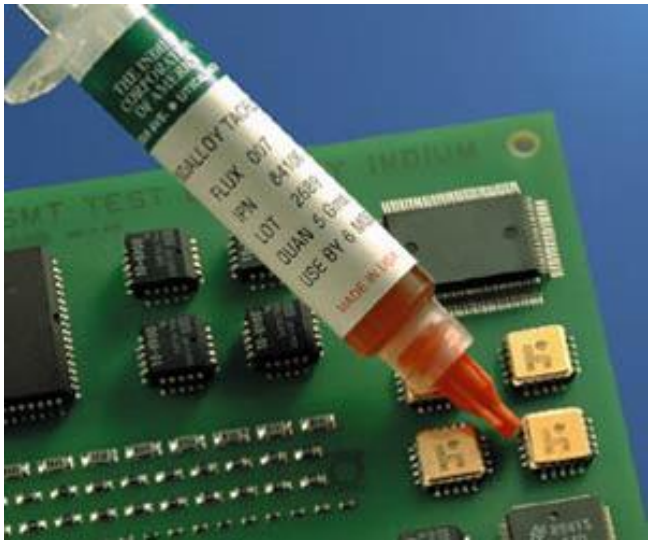
Series resistor substitution

Source: “Op Amp Precision Design: PCB Layout Techniques”

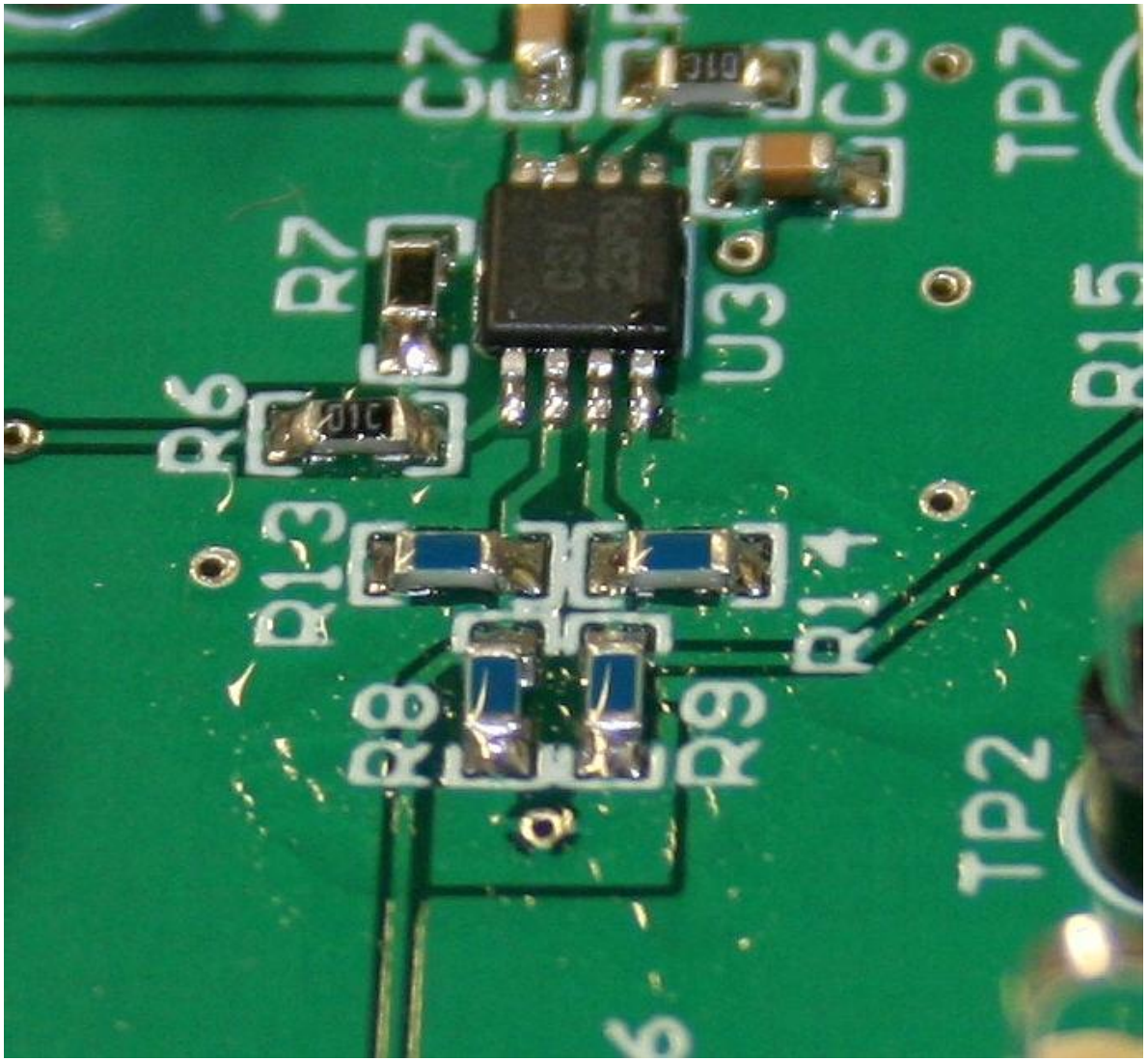
Solder Flux Contamination

What Is Solder Flux?

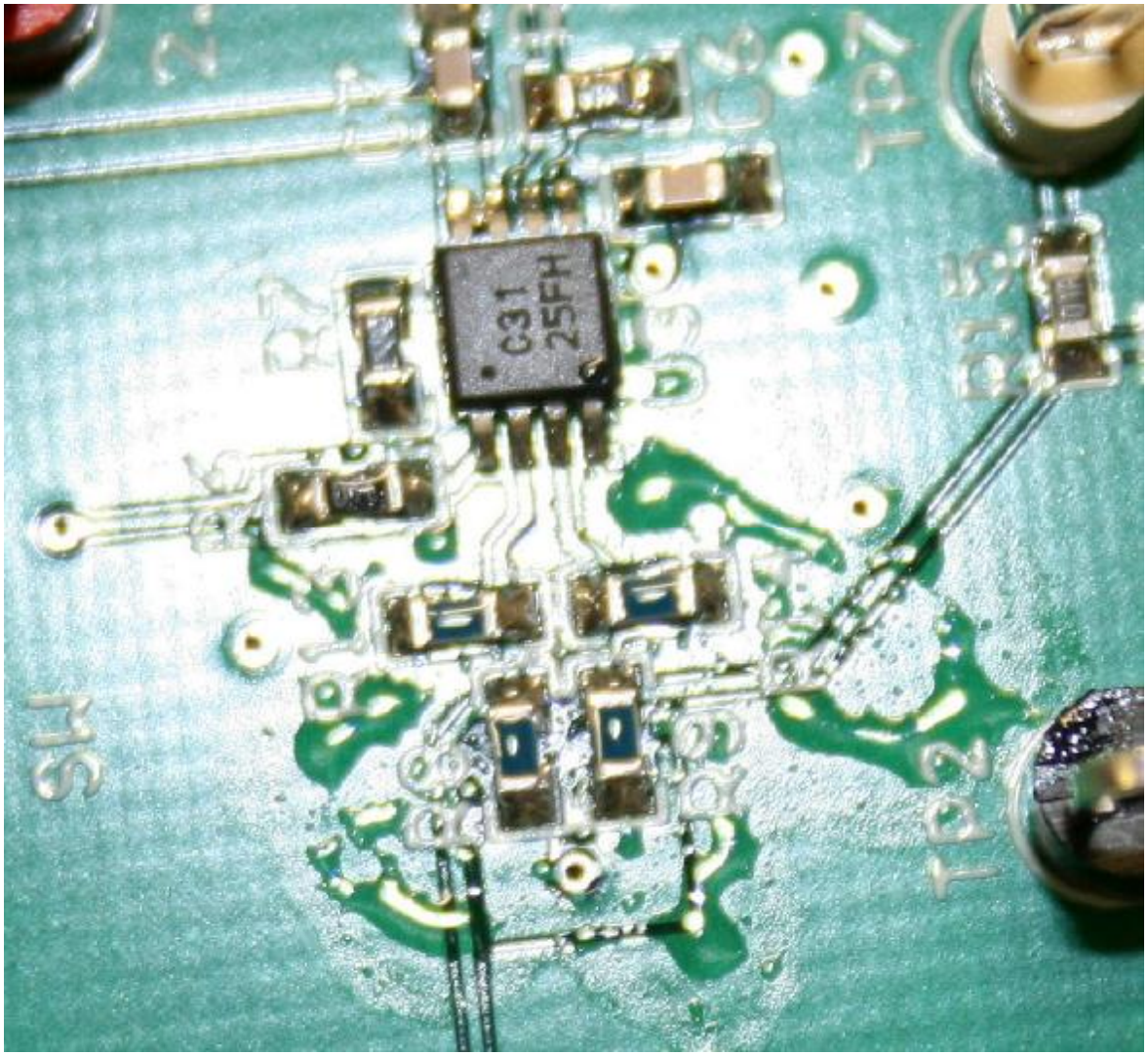
- A chemical agent used to facilitate the soldering of components to a printed circuit board
- Solder flux serves three main purposes:
  - Removes oxidation from surfaces to be soldered
  - Seals out air, preventing further oxidation
  - Improves “wetting” characteristic of the liquid solder
    - Solder flows more easily onto solder pads and device pins
- Many different types of solder flux
  - Resin, organic, inorganic
  - Liquid, solid, paste



What Is Solder Flux?

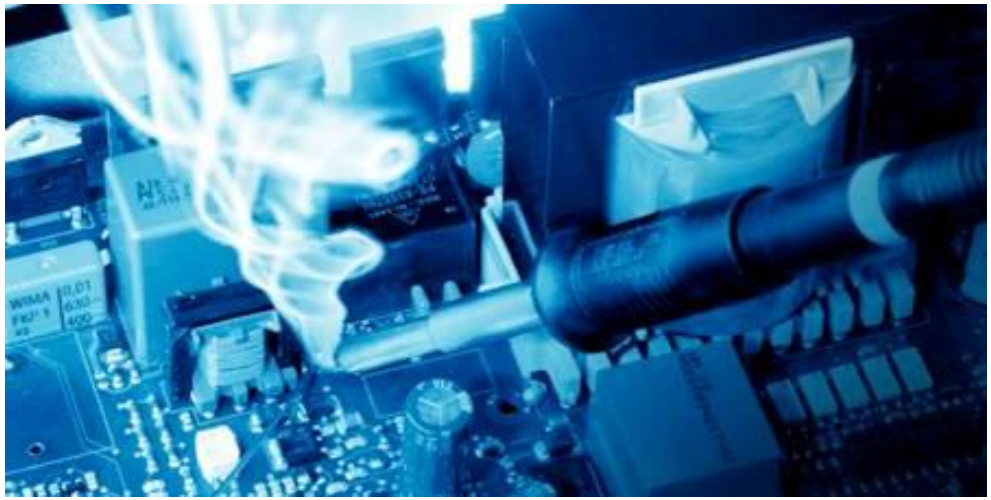


What Is Solder Flux?

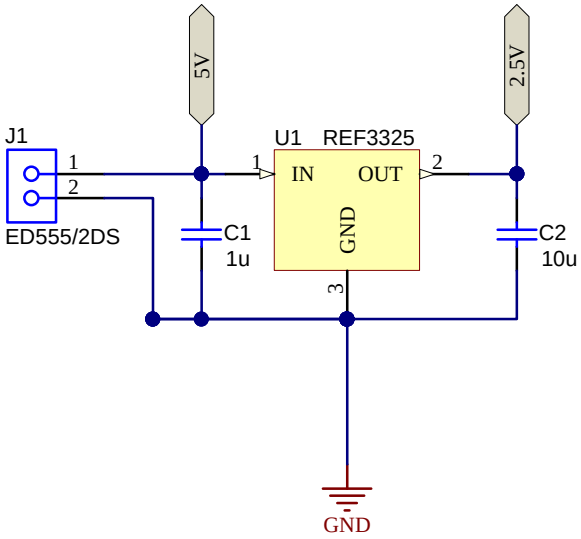


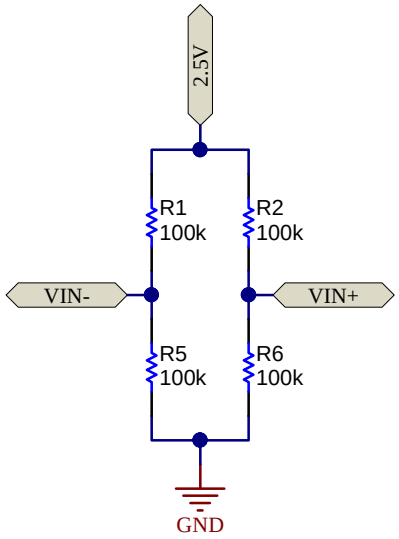
Drawbacks of Solder Flux

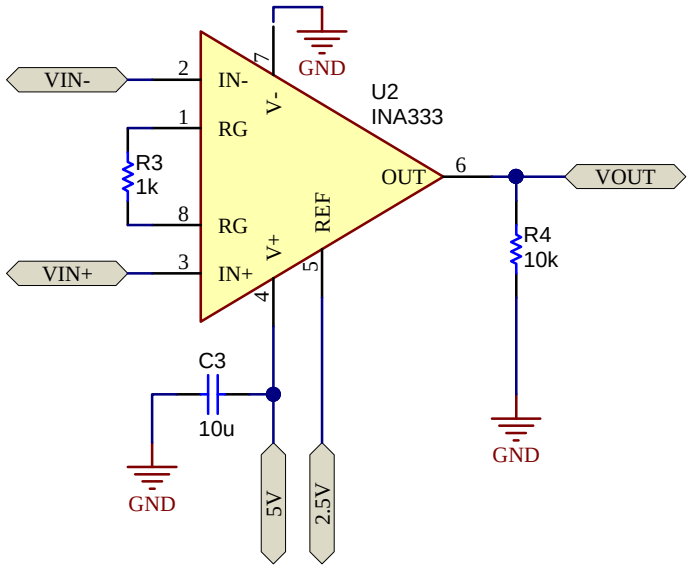
- **Deterioration of surface insulation resistance**
- Contamination of sensitive parts
  - Connector contacts, mechanical switches, MEMS assemblies
- Growth of whiskers between nearby traces
- Fumes liberated during soldering have adverse health effects
- Solvents required for post-soldering cleaning can be expensive and not environmentally friendly



Test Case: INA333 Bridge Sensor Circuit

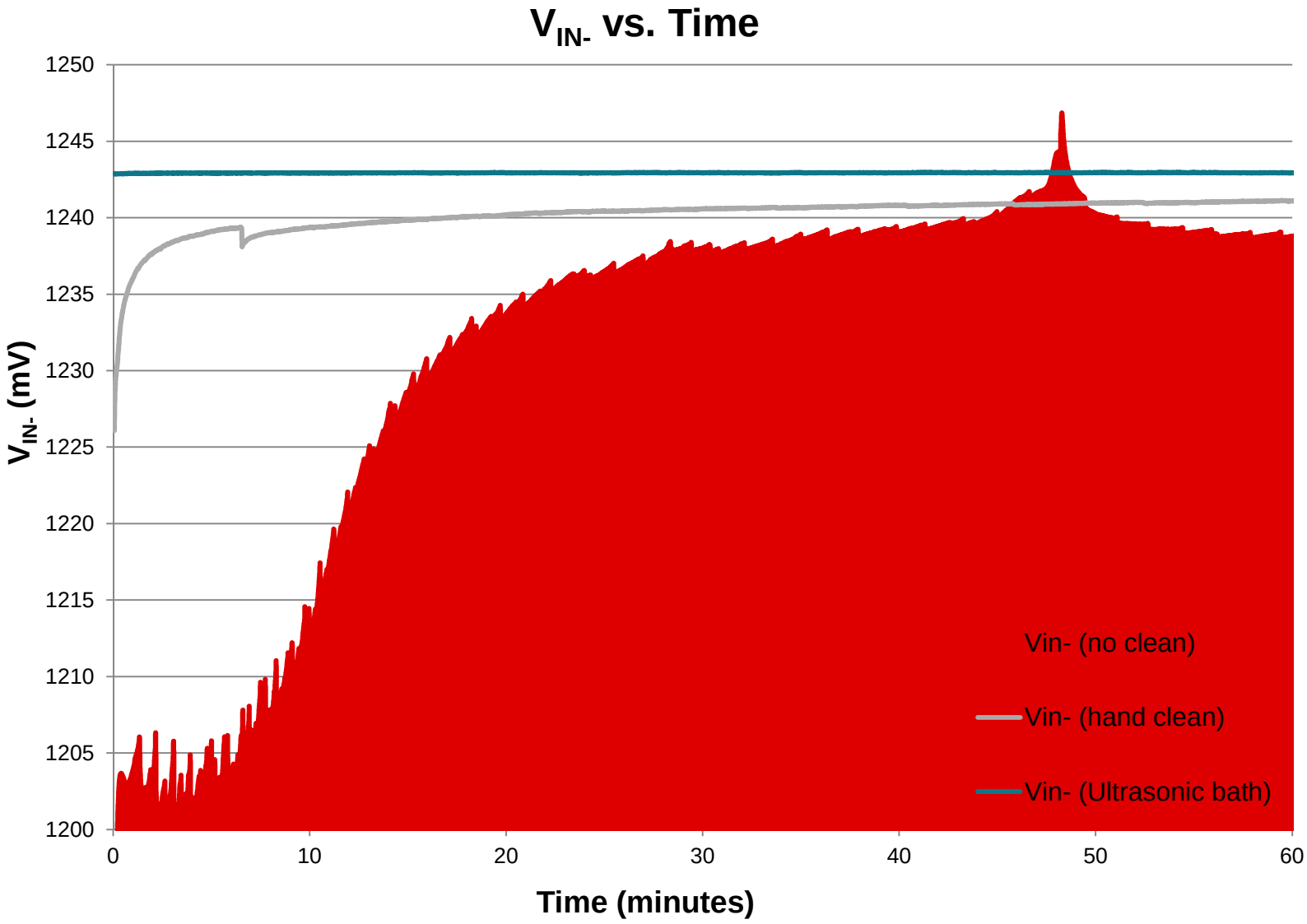




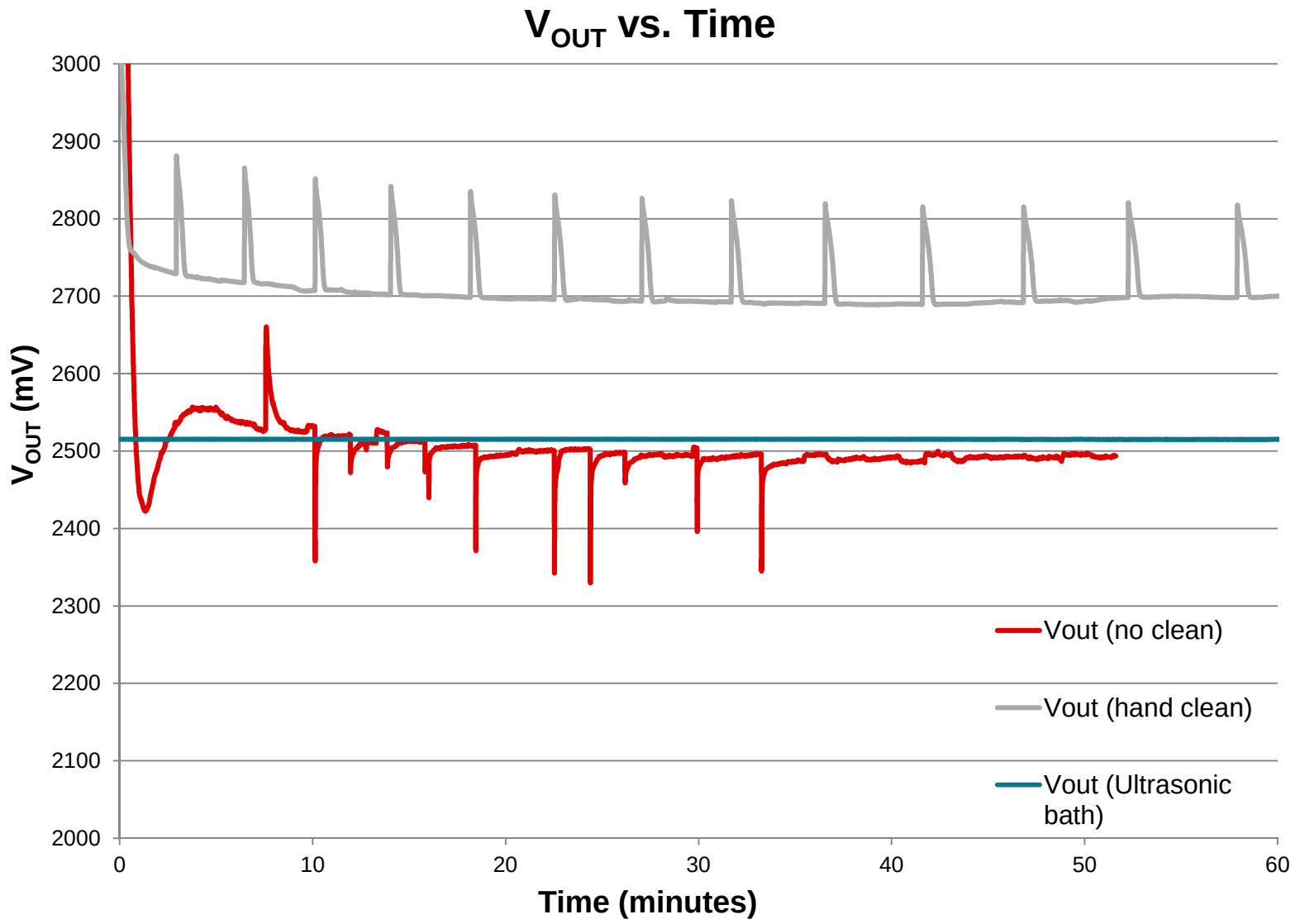


Area most sensitive
to flux contamination

INA333 Bridge Sensor Circuit Results



INA333 Bridge Sensor Circuit Results



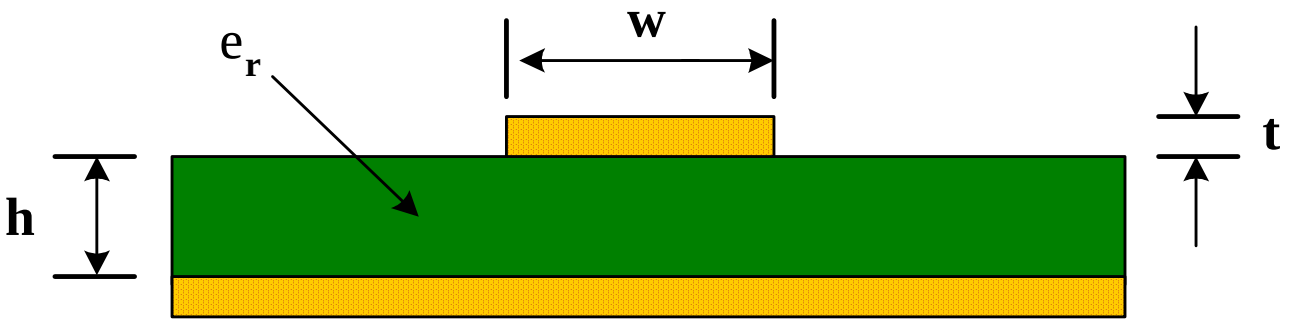
Solder Flux – Conclusions & Recommendations

- Improper cleaning of solder flux can cause **huge** DC voltage errors!
  - These errors are random in nature and are nearly impossible to predict
- Use an Ultrasonic bath (or similar) for final cleaning of all hand-assembled or reworked PCBs
  - PCBs assembled by a contracted assembly house should already use suitable post-assembly cleaning methods
- Bake assembled and cleaned PCBs at slightly elevated temperature to remove any residual moisture
  - e.g. 70°C, 10 minutes
- Place guard rings around critical signal traces to reduce PCB surface leakage currents
  - See "Op Amp Precision Design: PCB Layout Techniques" for more information

Capacitance & Inductance

Microstrip Copper Traces

- Used to connect critical signals on the PCB
  - May create parasitic inductance and capacitance



x = length of trace (cm)
w = width of trace (cm)
h = thickness of board (cm)
t = thickness of trace (cm)
e_r = PCB dielectric constant (FR-4 ≈ 4.5)

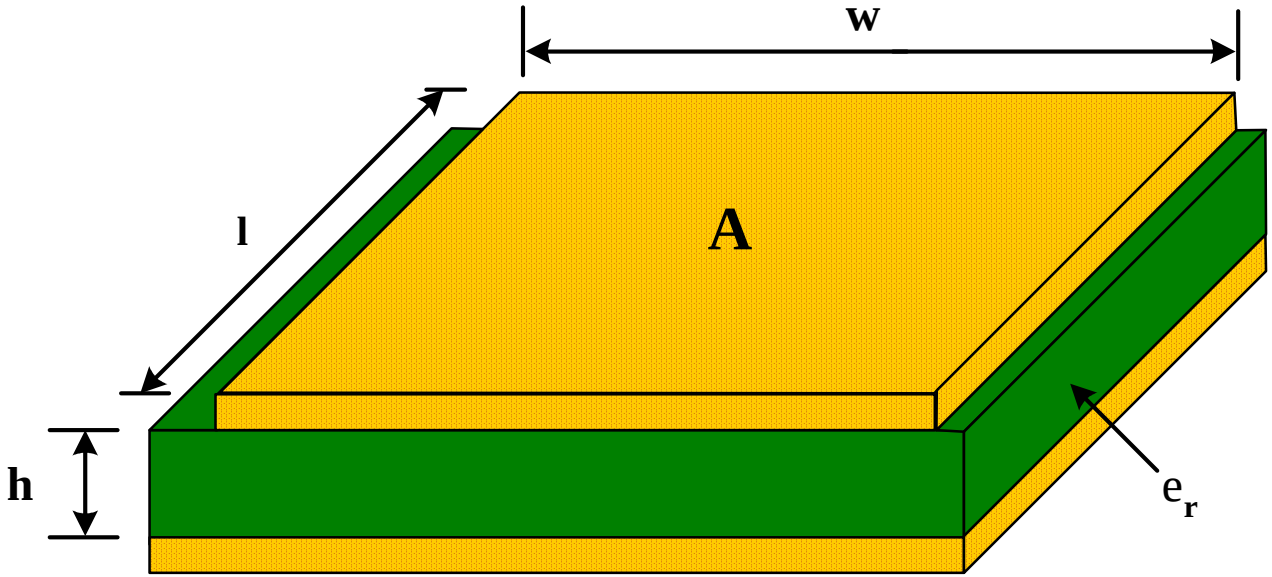
$$C(pF) \approx \frac{0.264x\ (\varepsilon_r + 1.41)}{ln\left(\frac{5.98\ h}{0.8\ w + t}\right)}$$

$$L(nH) \approx 2x\ ln\left(\frac{5.98\ h}{0.8\ w + t}\right)$$

$$Z_0(W) = 31.6\sqrt{\frac{L(nH)}{C(pF)}}$$

Parallel Copper Planes

- Used to provide convenient, low-impedance access to power or ground
  - Creates parasitic capacitance (may be desirable for “free” supply filtering)
- Often employed as a heat sink

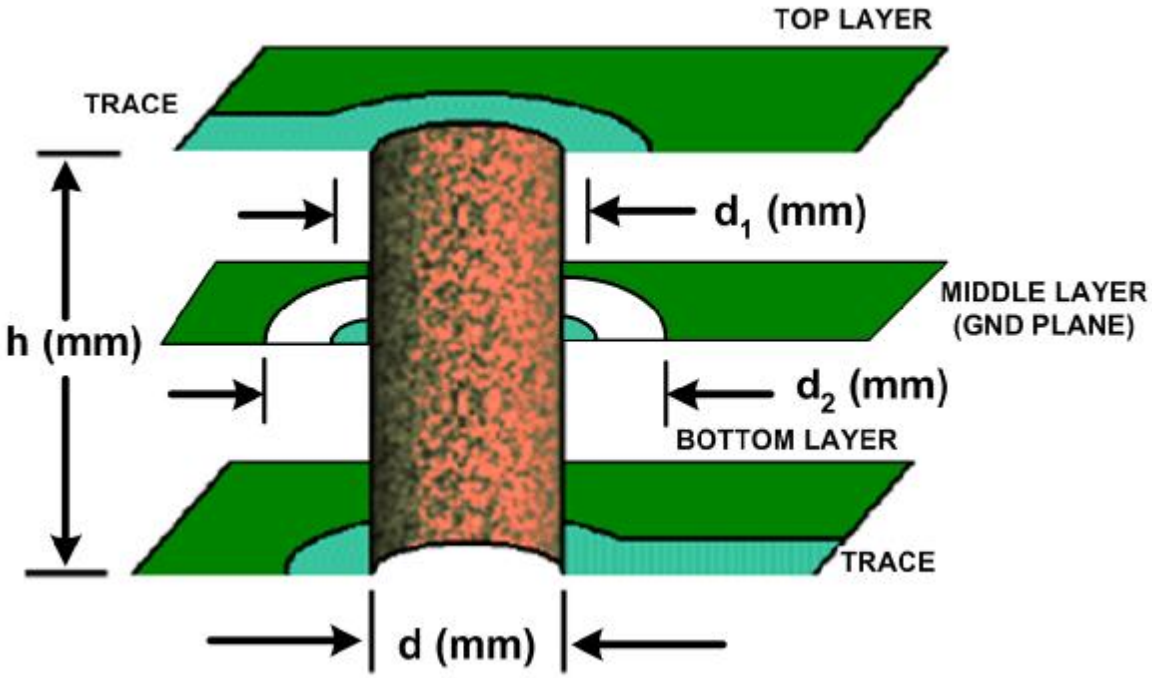


h = separation between planes (cm)
A = area of common planes = l*w (cm^2)
e_r = PCB dielectric constant (FR-4 ≈ 4.5)

$$C(pF) \approx \frac{0.0886\ \varepsilon_r\ A}{h}$$

Vias

- Used to connect signals on different PCB layers
  - Creates parasitic inductance and capacitance
  - Avoid or minimize using for signal traces, especially at high frequencies

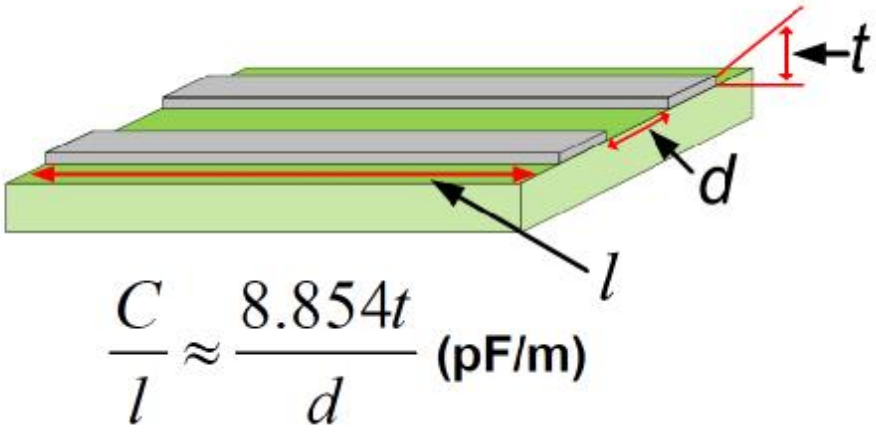


$$L(nH) \approx \frac{h}{5}\left[1 + \ln\left(\frac{4h}{d}\right)\right]$$

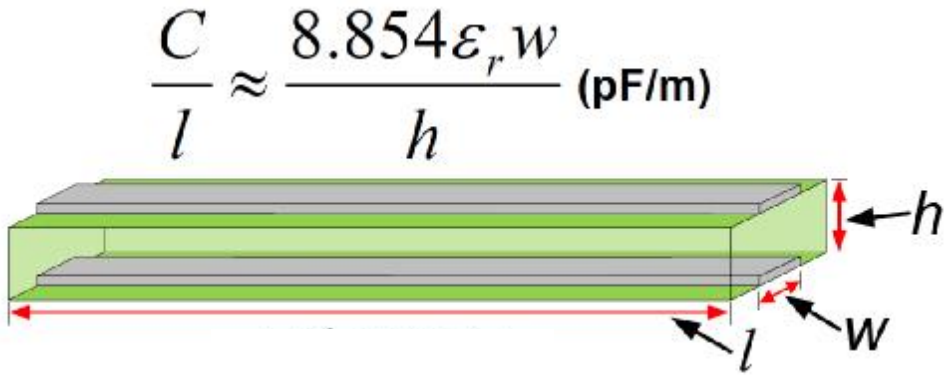
$$C(pF) \approx \frac{0.0555\ e_r\ h\ d_1}{d_2 - d_1}$$

Adjacent Copper Traces

- Used to route related groups of signals around the PCB
  - Amplifier inputs, digital communications buses, etc.
  - Creates parasitic capacitance
  - Allows capacitive coupling of signals between the traces (cross talk)



Same layer

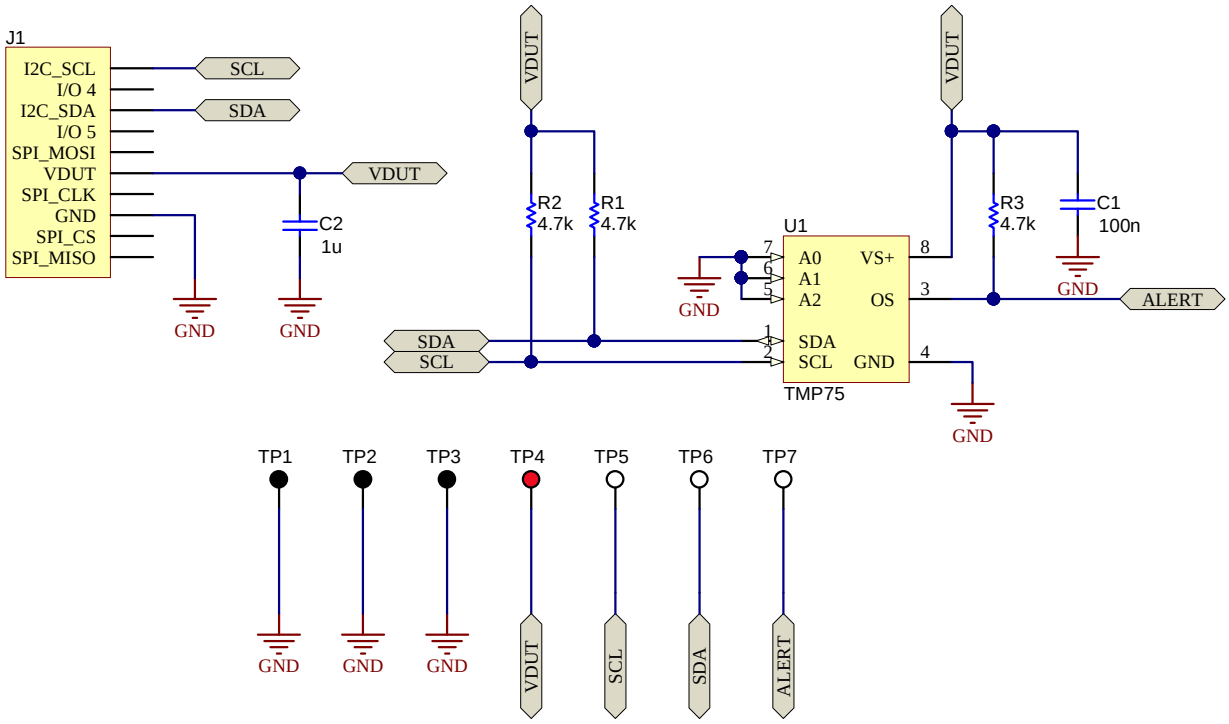


Different layers

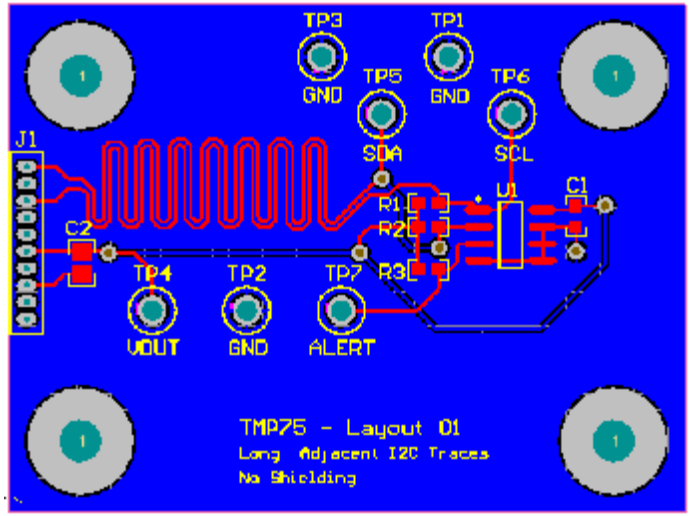
- Adjacent traces on different (adjacent) layers typically create much higher capacitance than traces on the same layer

Test Case 1: TMP75 I²C Bus

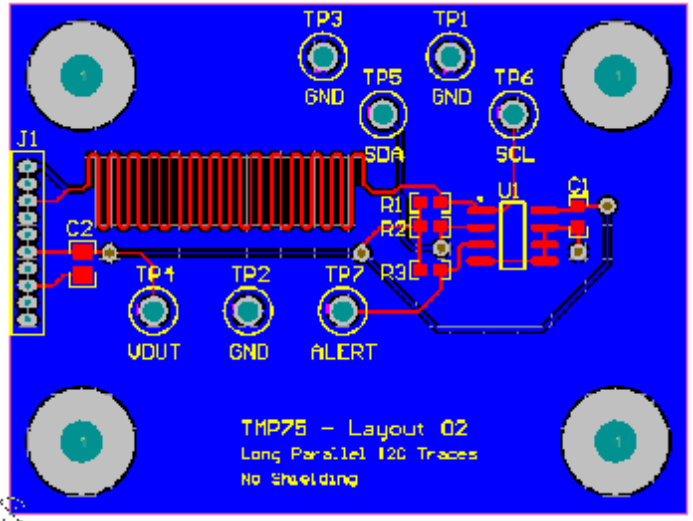
- Typical TMP75 circuit with adjacent I²C (SCL, SDA) traces
- 4 variations of PCB layout
  - Short vs. long traces, same layer vs. adjacent layers, GND vs. no GND
- I²C read/write operations were performed to determine the impact of parasitic trace capacitance



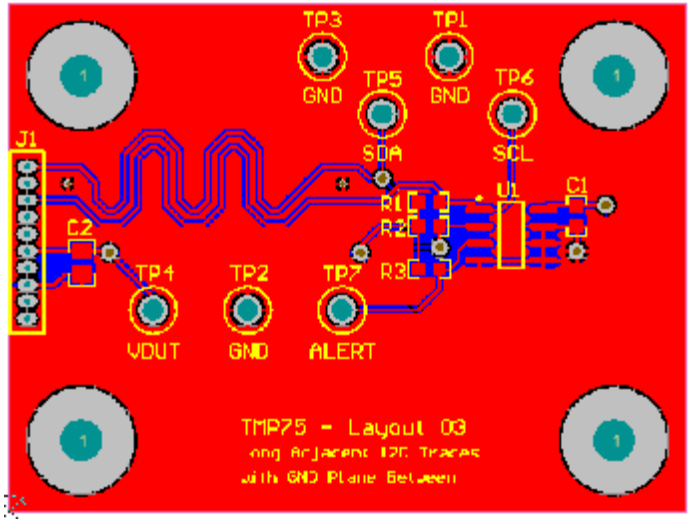
Test Case 1: TMP75 I²C Bus



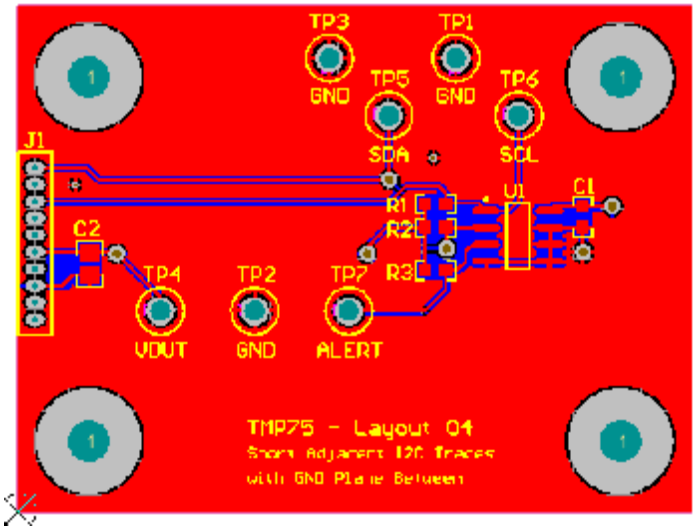
Adjacent lines, GND pour bottom layer



Lines in adjacent layers, GND pour bottom layer

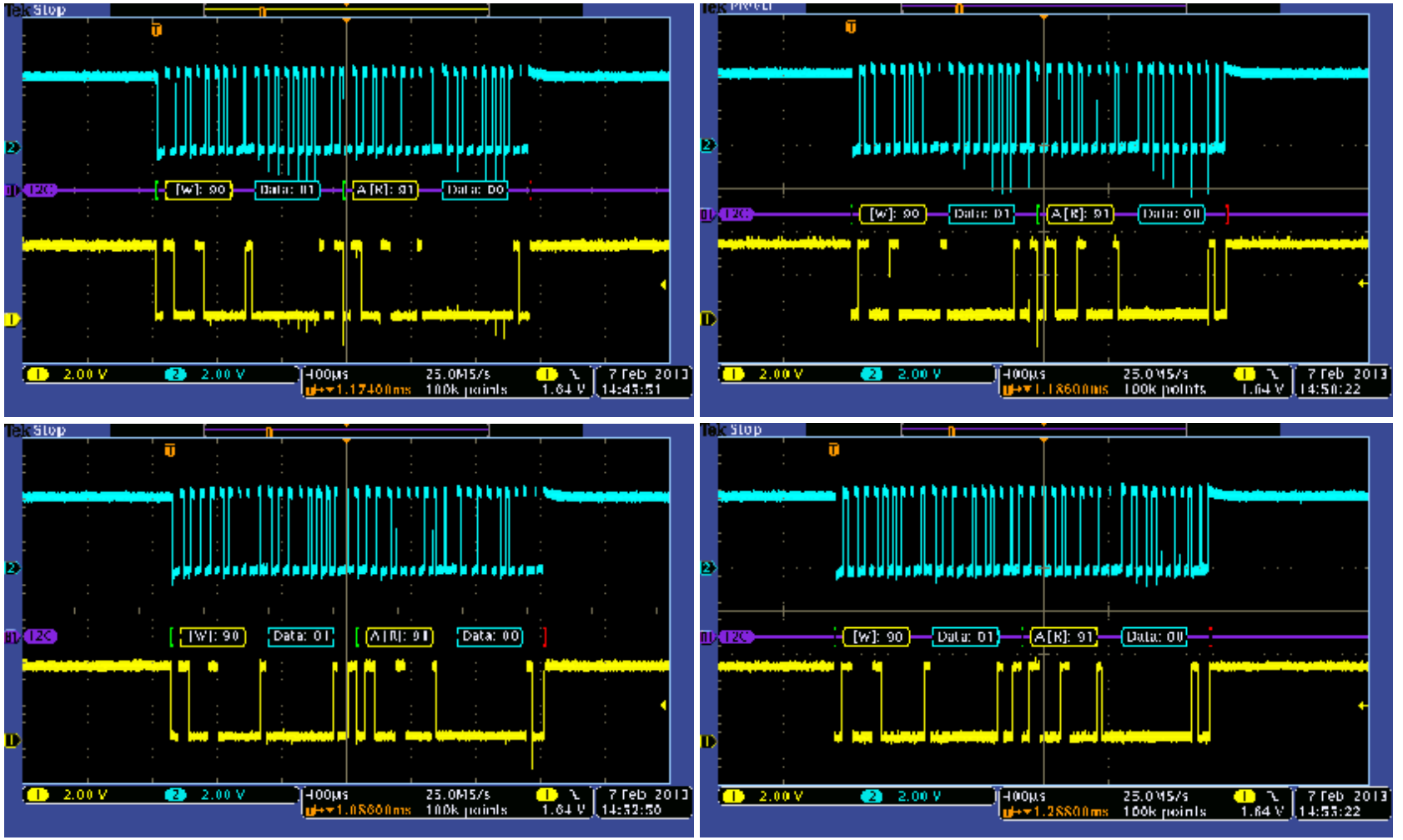


Adjacent lines with GND, GND on both layers



Direct adjacent lines with GND, GND on both layers

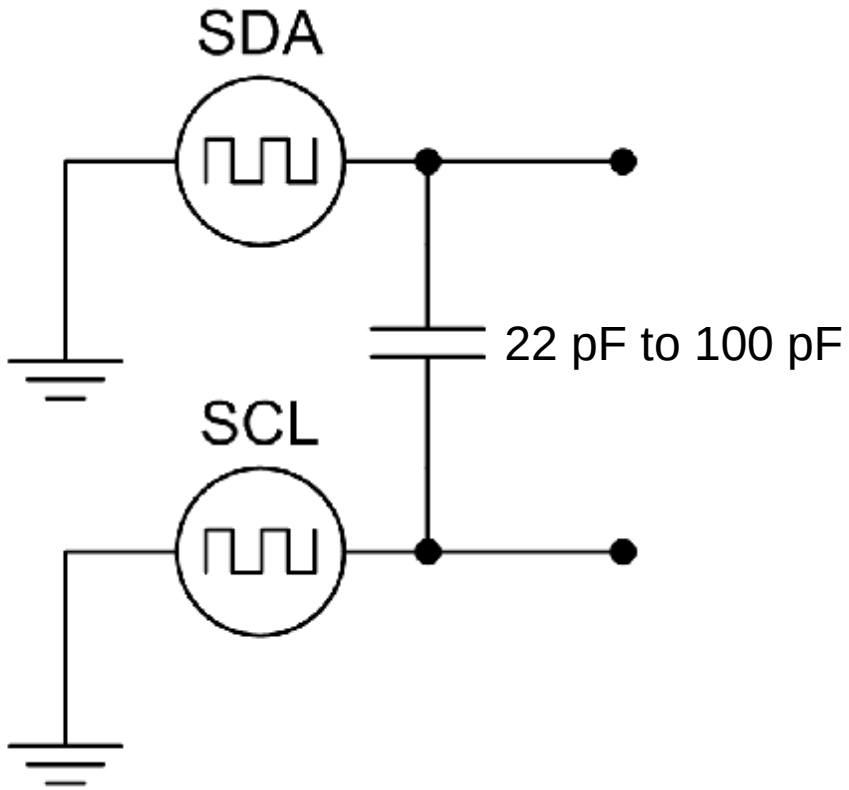
TMP75 I²C Bus Results



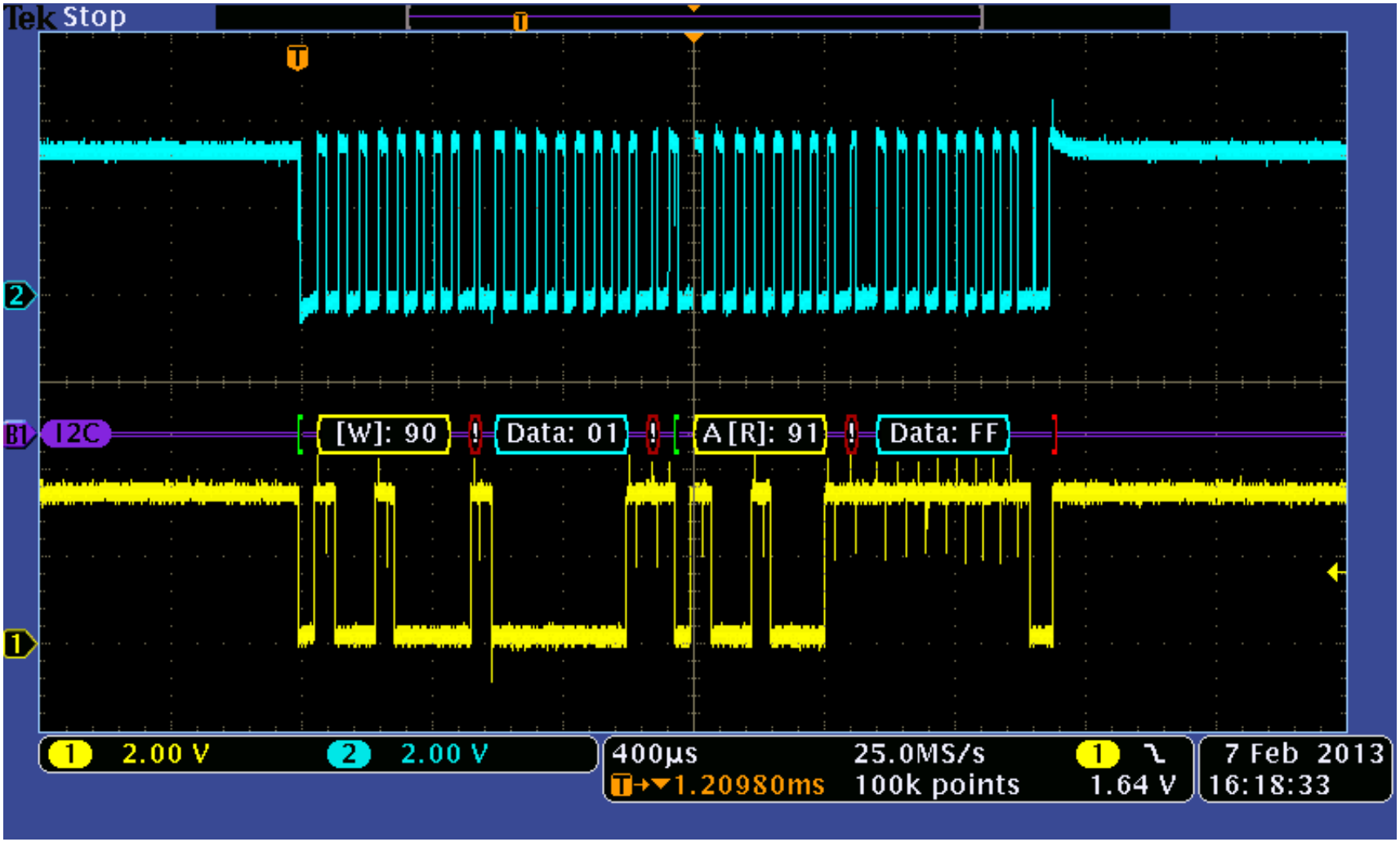
Some cross talk observed, but no communication issues on any of the layouts!

TMP75 I²C Bus Results – Test to Failure

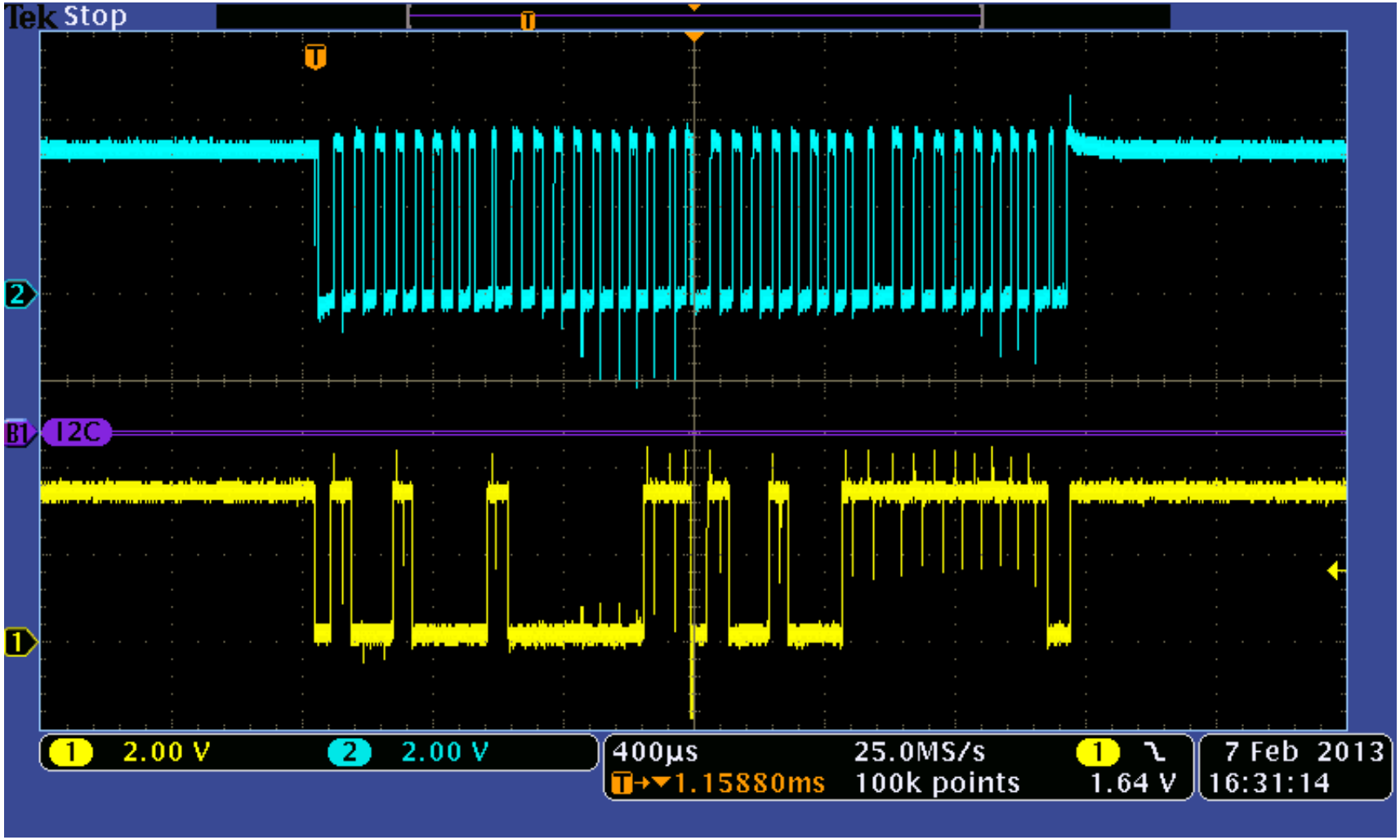
- Additional capacitance was added between SDA and SCL to determine the thresholds of failure
  - Bit read/write errors
  - Total I²C bus failure



Threshold 1 – Bit R/W Errors – 27 pF

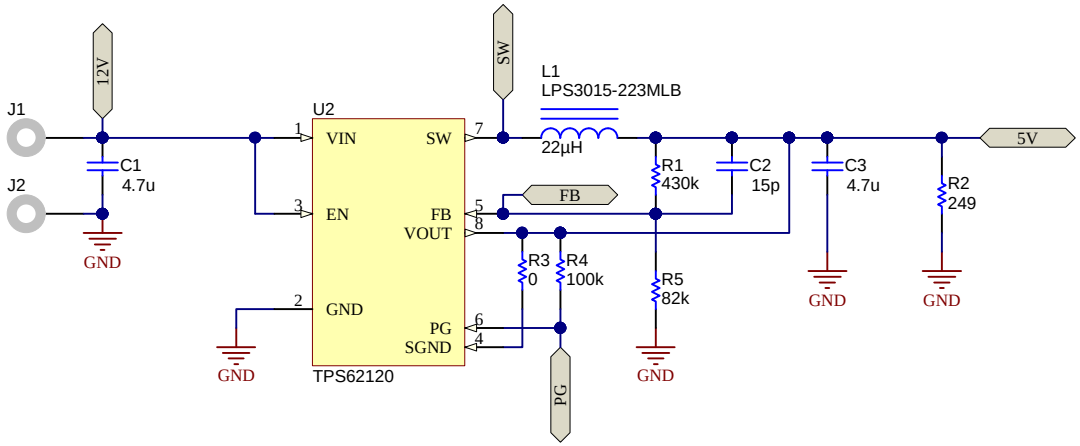


Threshold 2 – Bus Failure – 39 pF

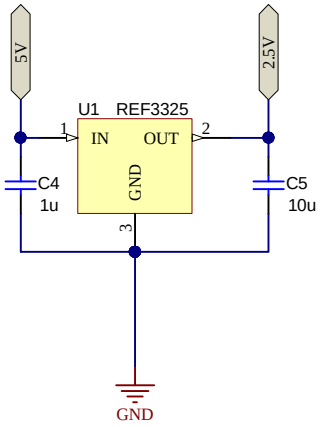


Test Case 2: TPS62120 SW Noise + INA333

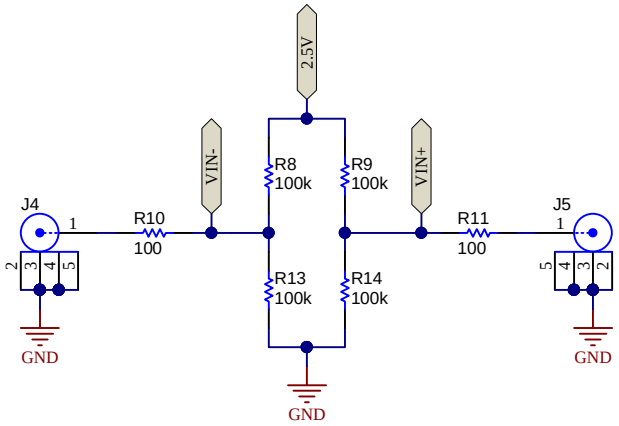
12Vin, 5Vout SMPS



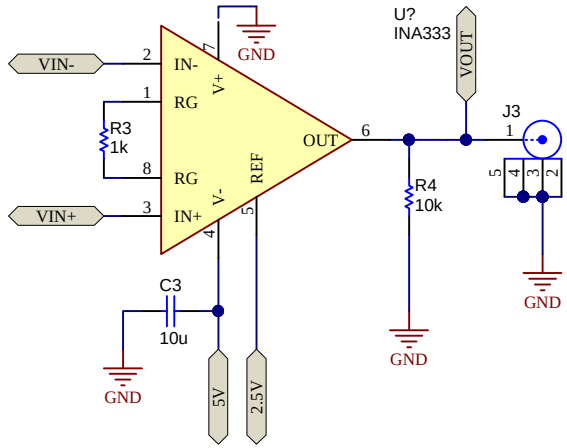
5Vin, 2.5Vout Reference



Bridge Sensor

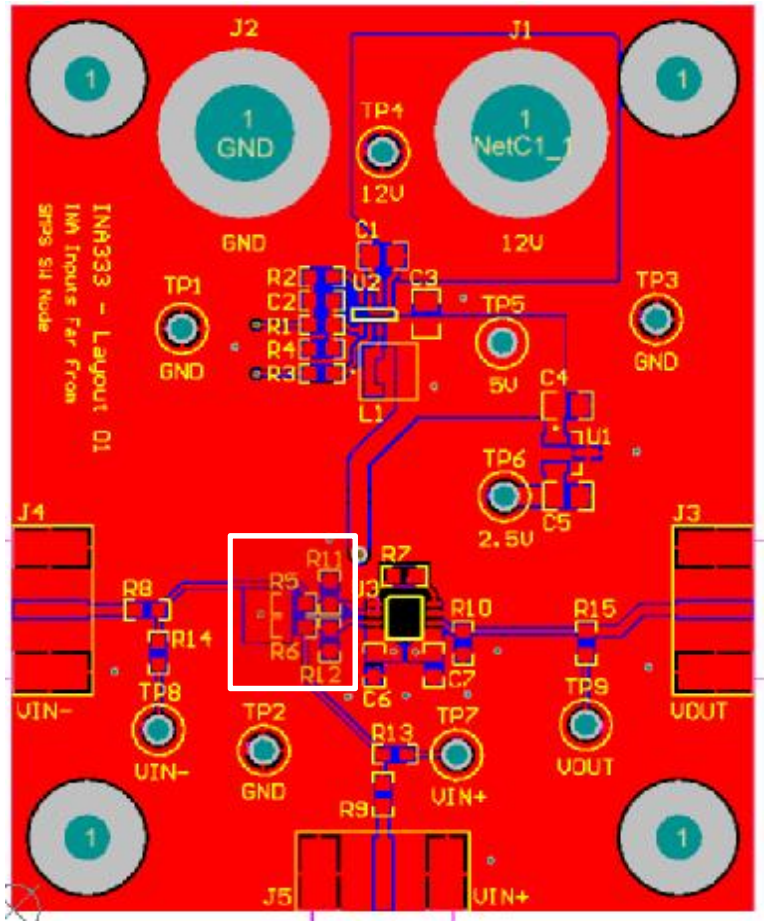


INA333, Gain=101

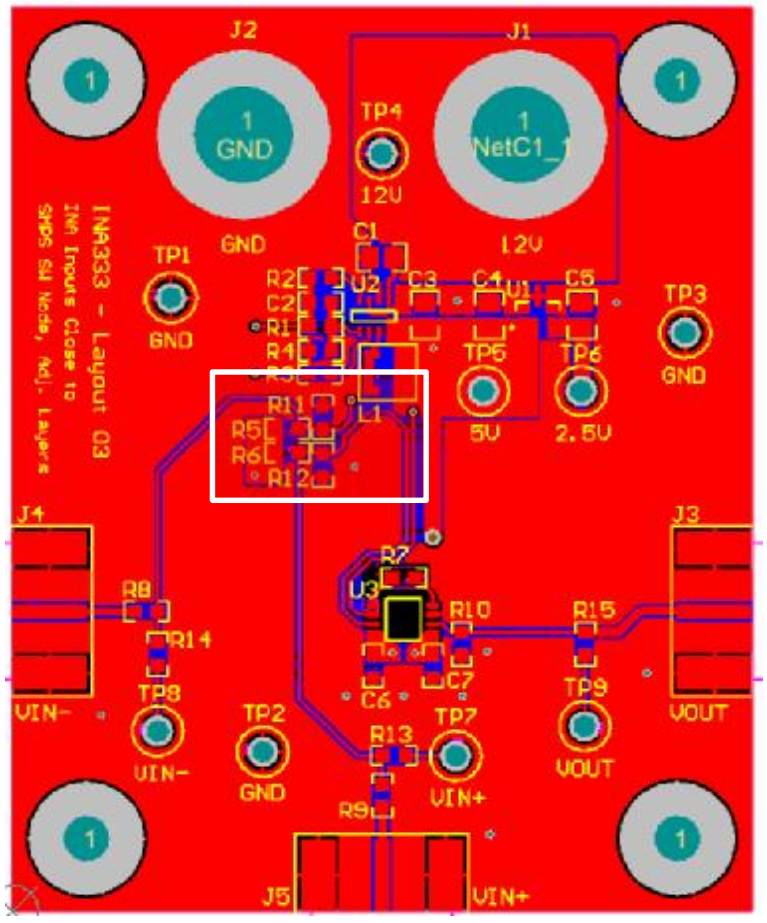


Texas Instruments

Test Case 2: TPS62120 SW Noise + INA333

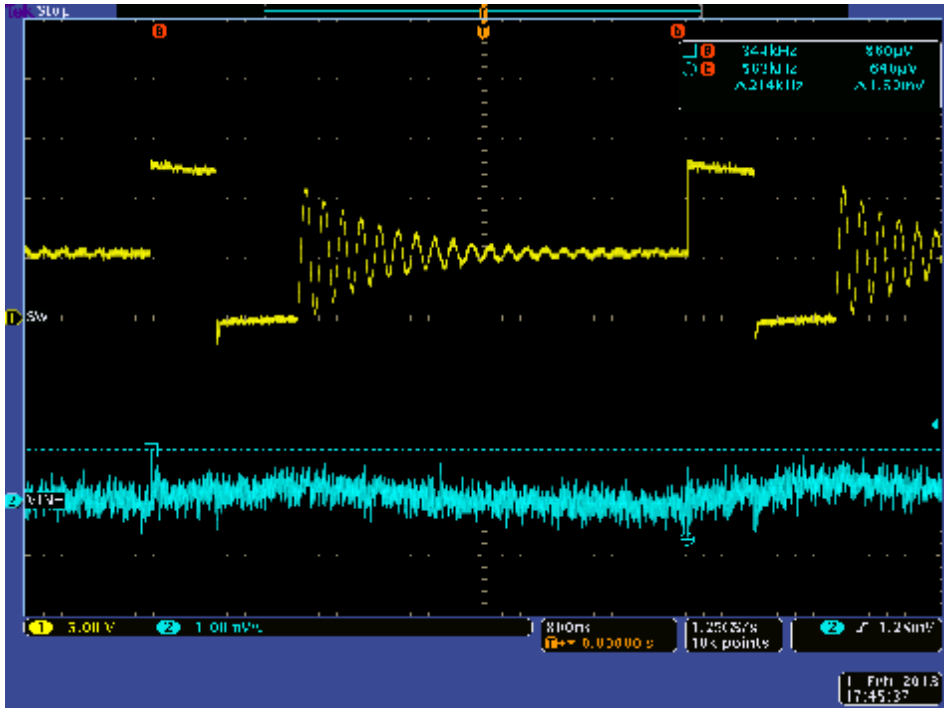


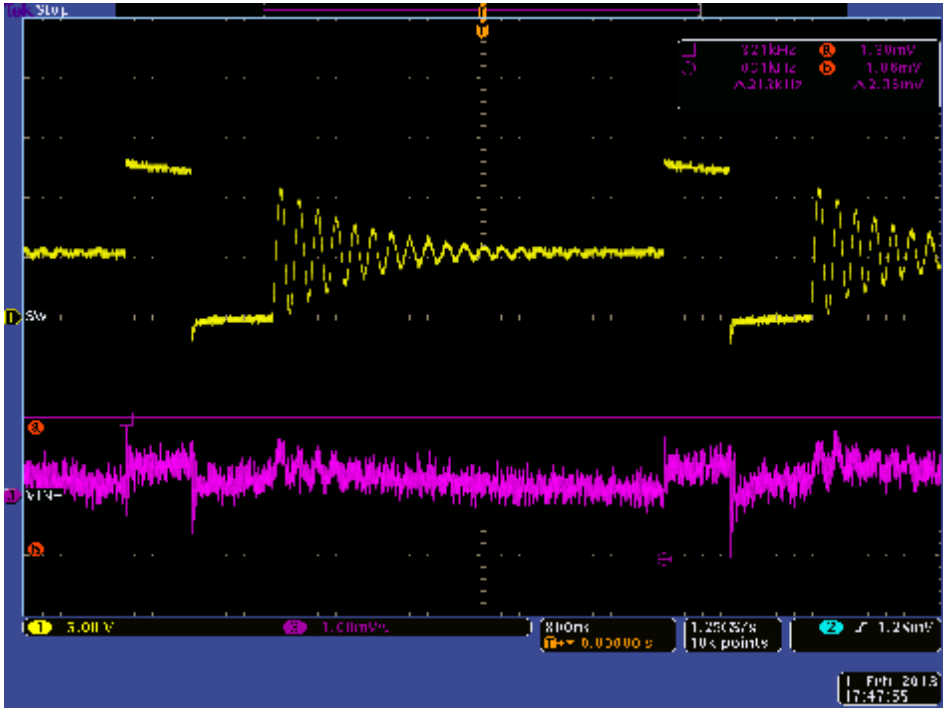
Layout 1 – V_{IN+}, V_{IN-} far from SW node



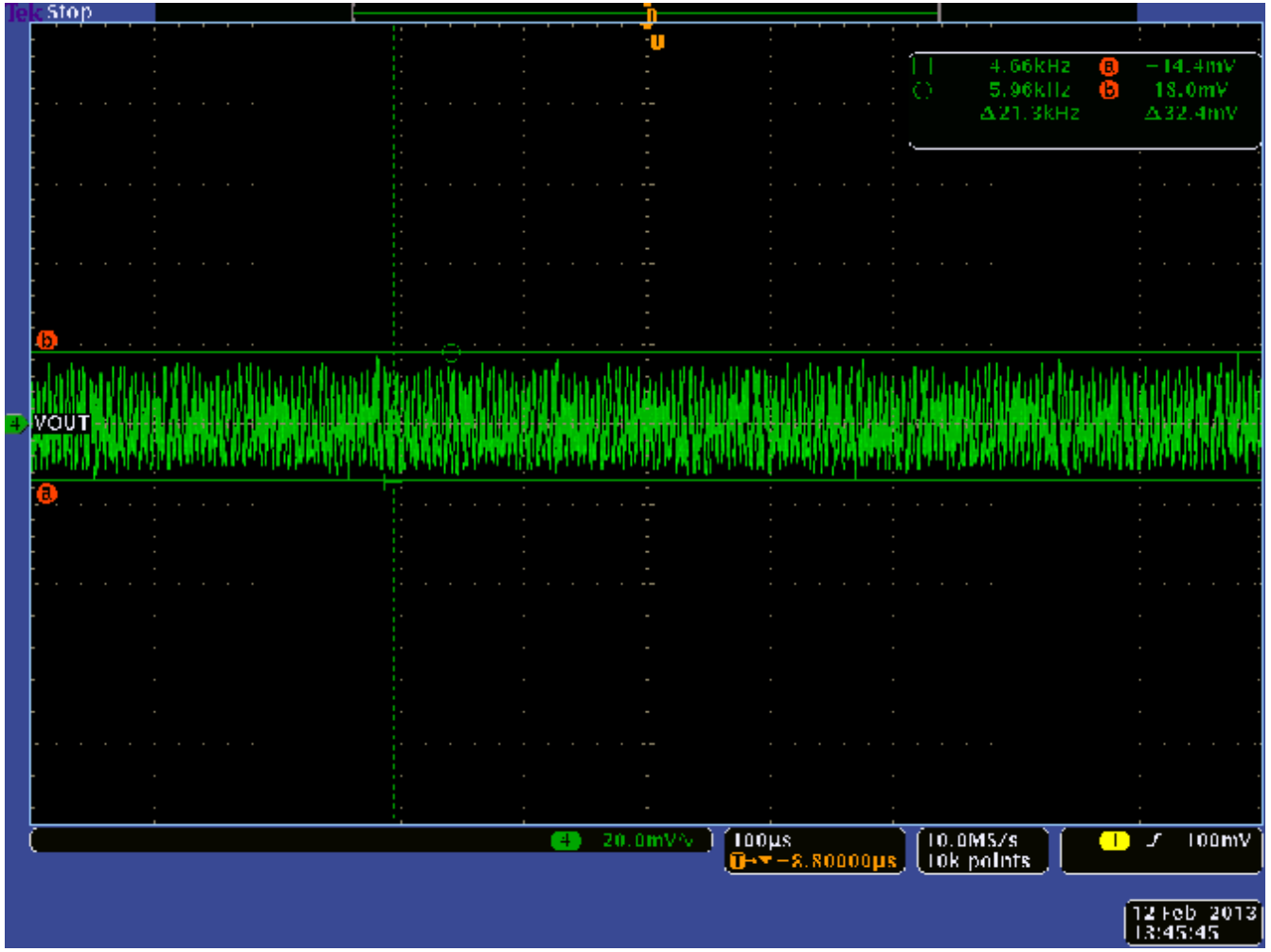
Layout 3 – V_{IN+}, V_{IN-} adjacent to and underneath SW node

Layout 1 Results – V_{IN-} & V_{IN+} Noise

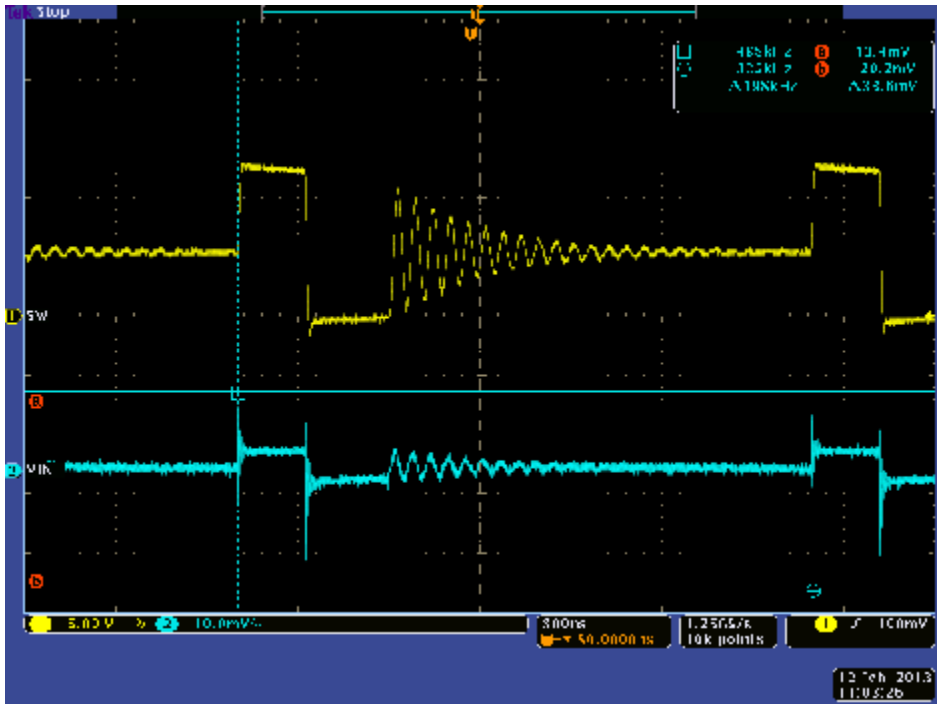


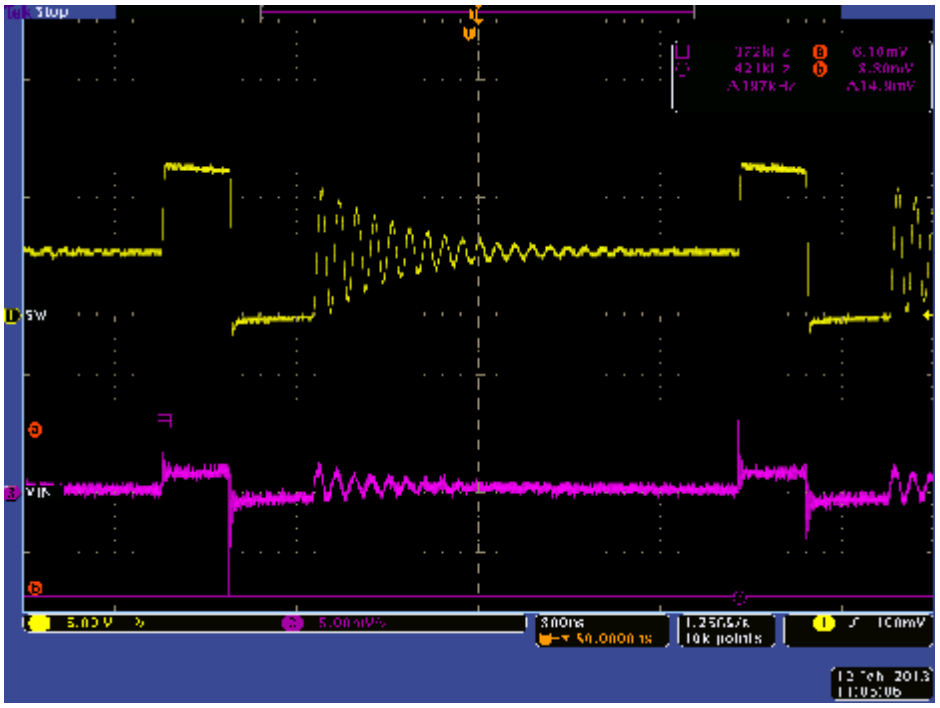


Layout 1 Results – V_{OUT} Noise



Layout 3 Results – V_{IN-} & V_{IN+} Noise

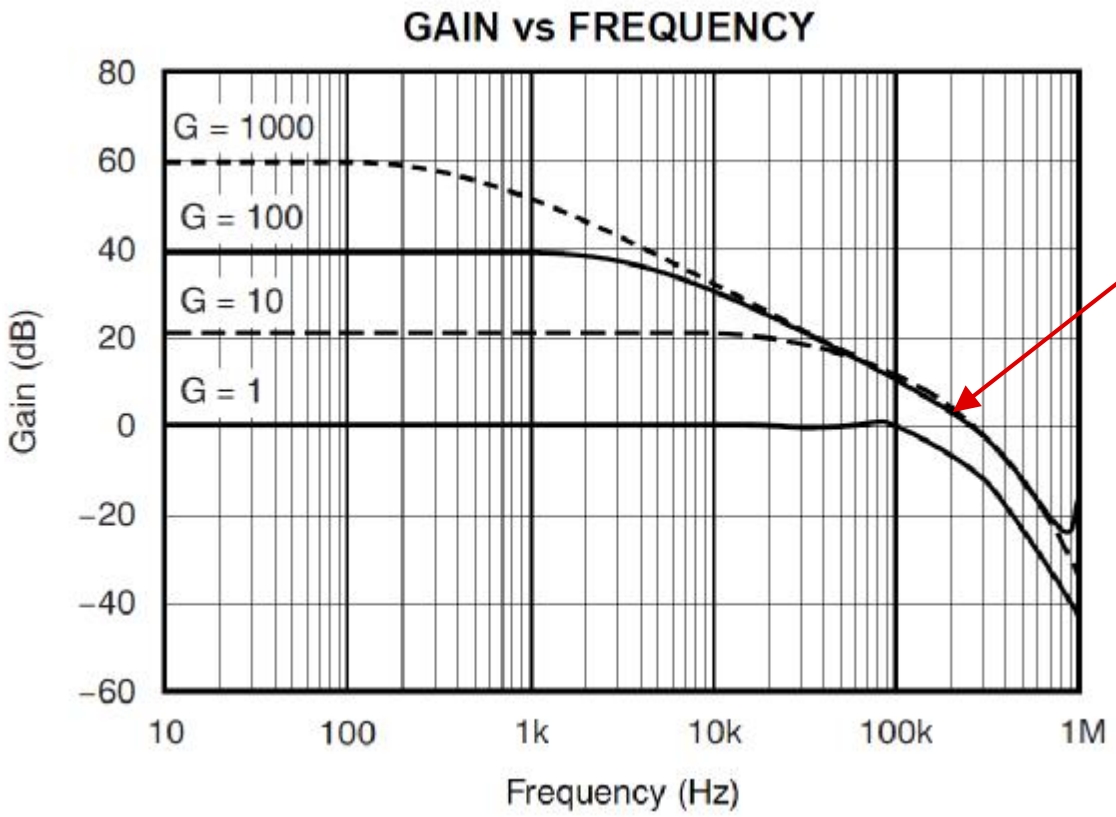




Layout 3 Results – V_{OUT} Noise

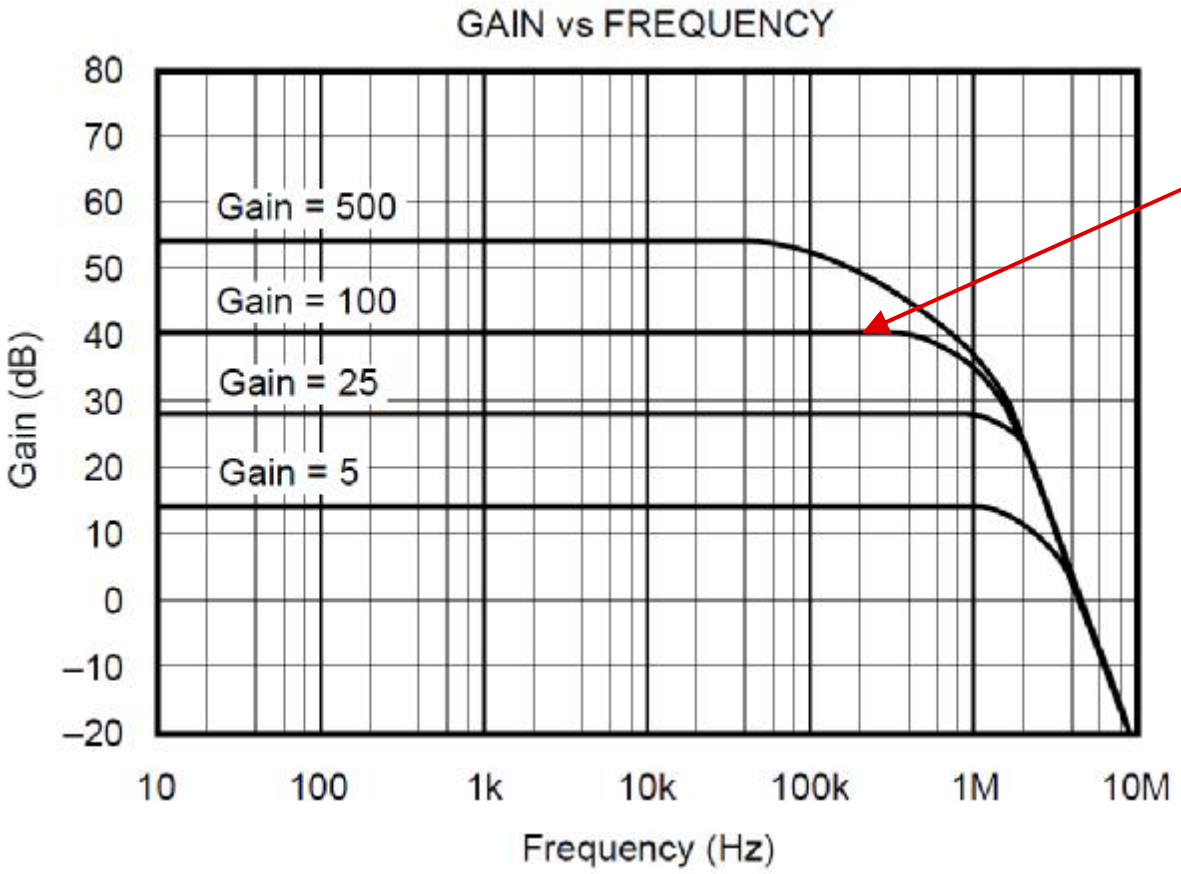
Layout 3 Results – V_{OUT} Noise

- Other than slightly higher output ripple, why does the “bad” layout look almost the same as the “good” layout?



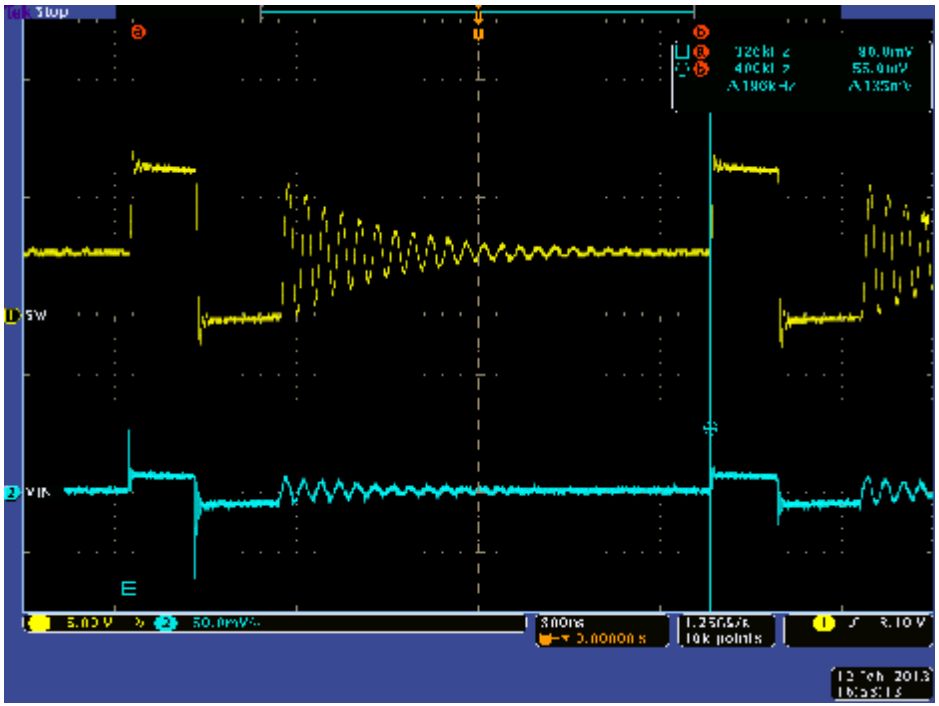
When set to G = 100, the INA333 has only ~5 dB of gain at 200 kHz!

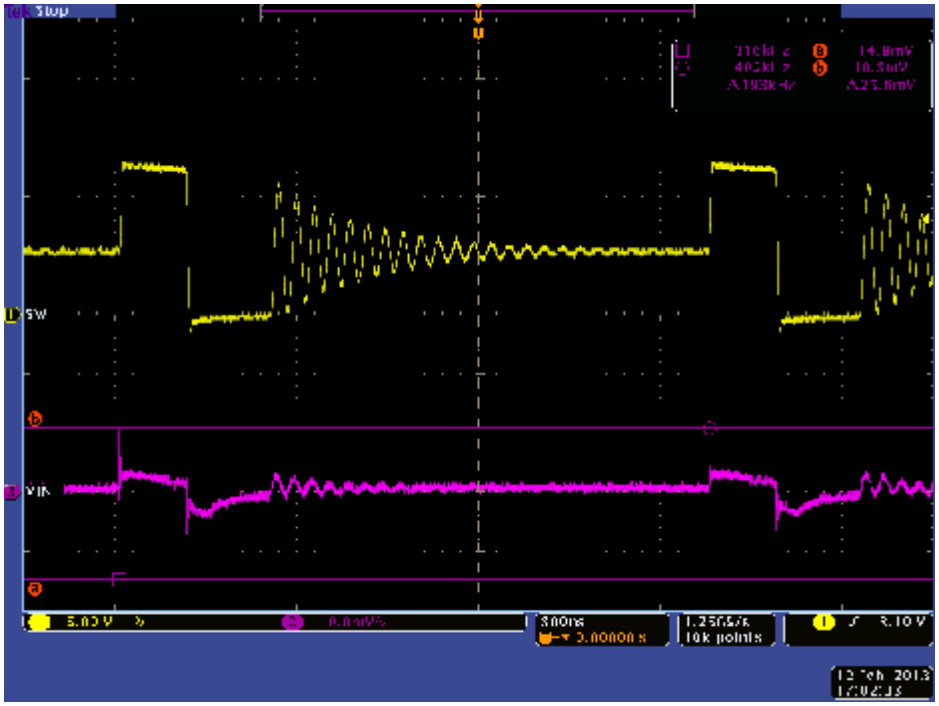
Test Case 3: INA331



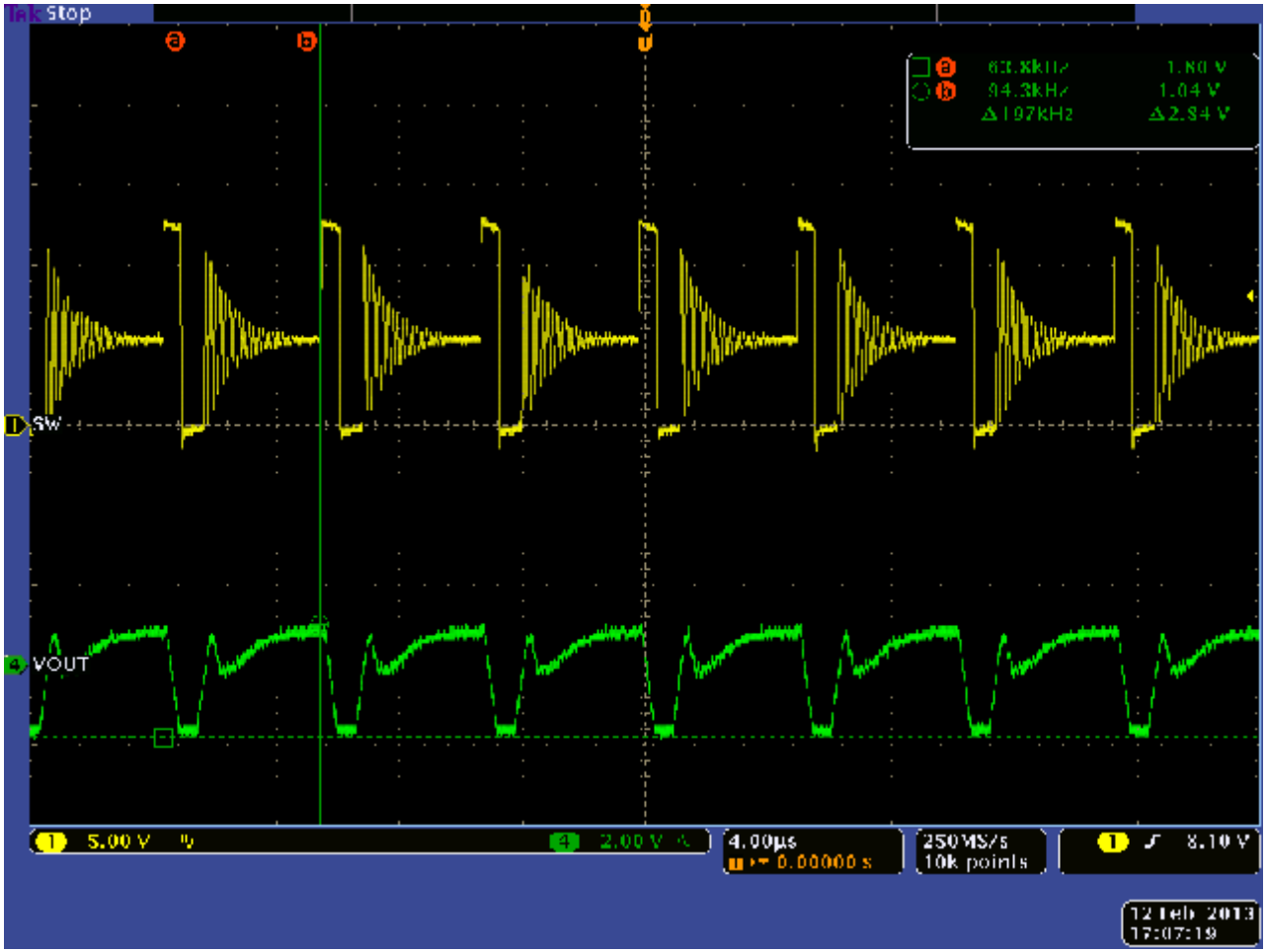
When set to G = 100, the INA331 has enough bandwidth to properly amplify a 200 kHz signal

Layout 3a Results – V_{IN-} & V_{IN+} Noise

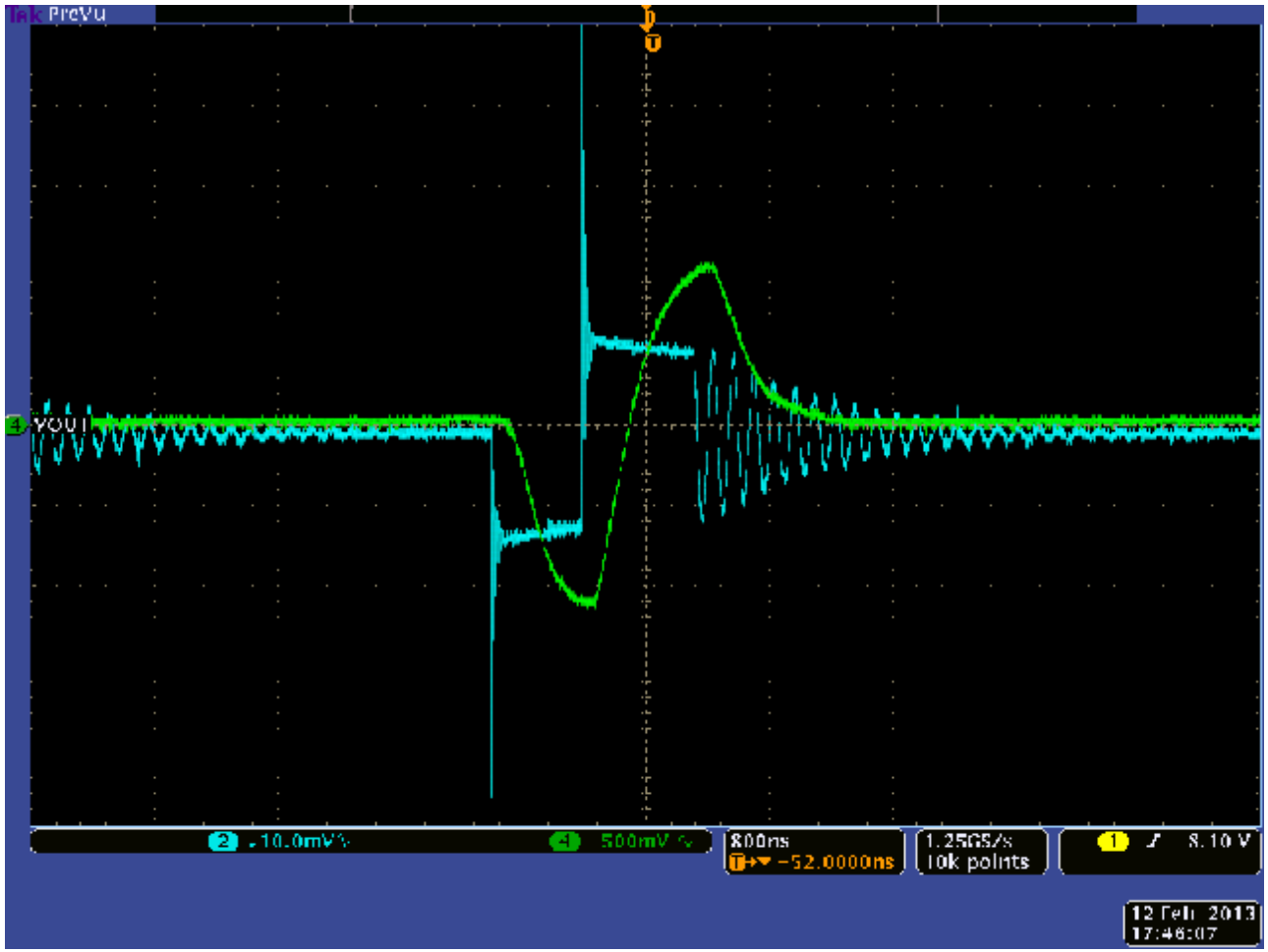




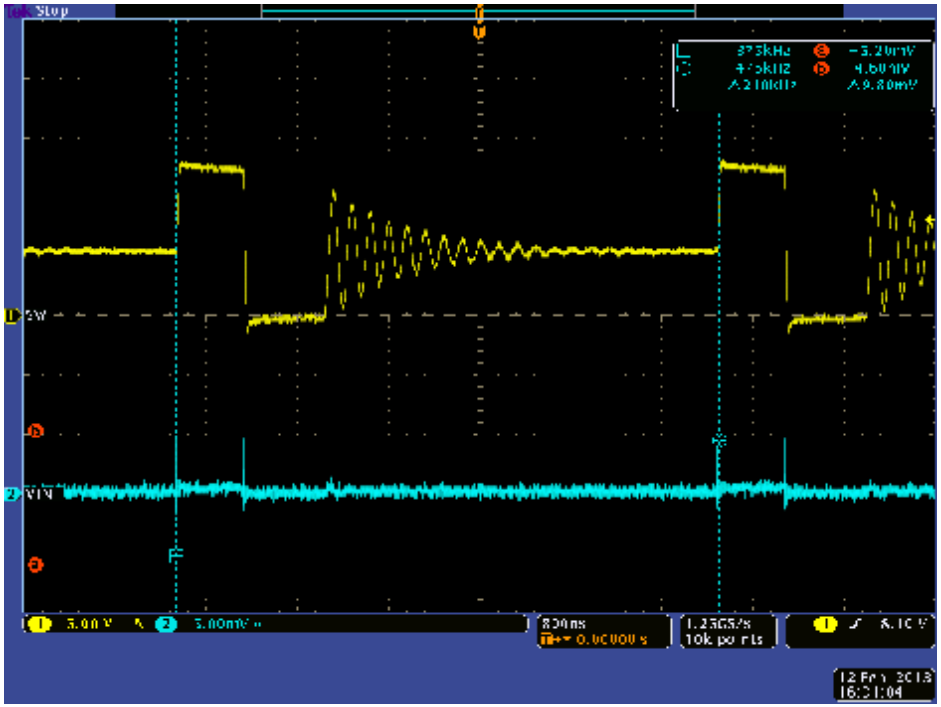
Layout 3a Results – V_{OUT} Noise

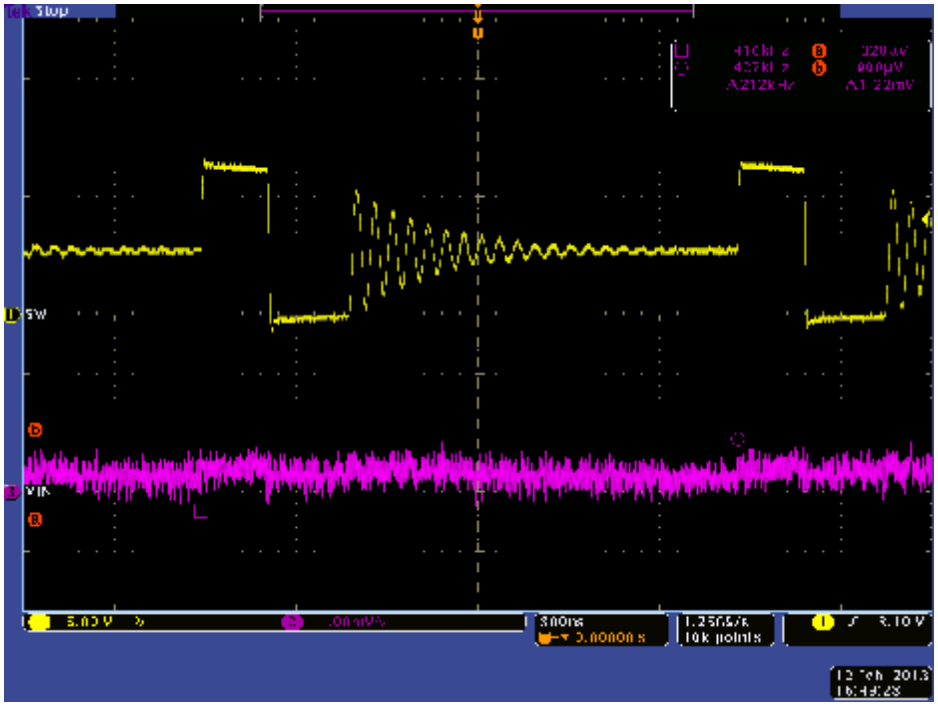


Layout 3a Results – V_{OUT} Noise



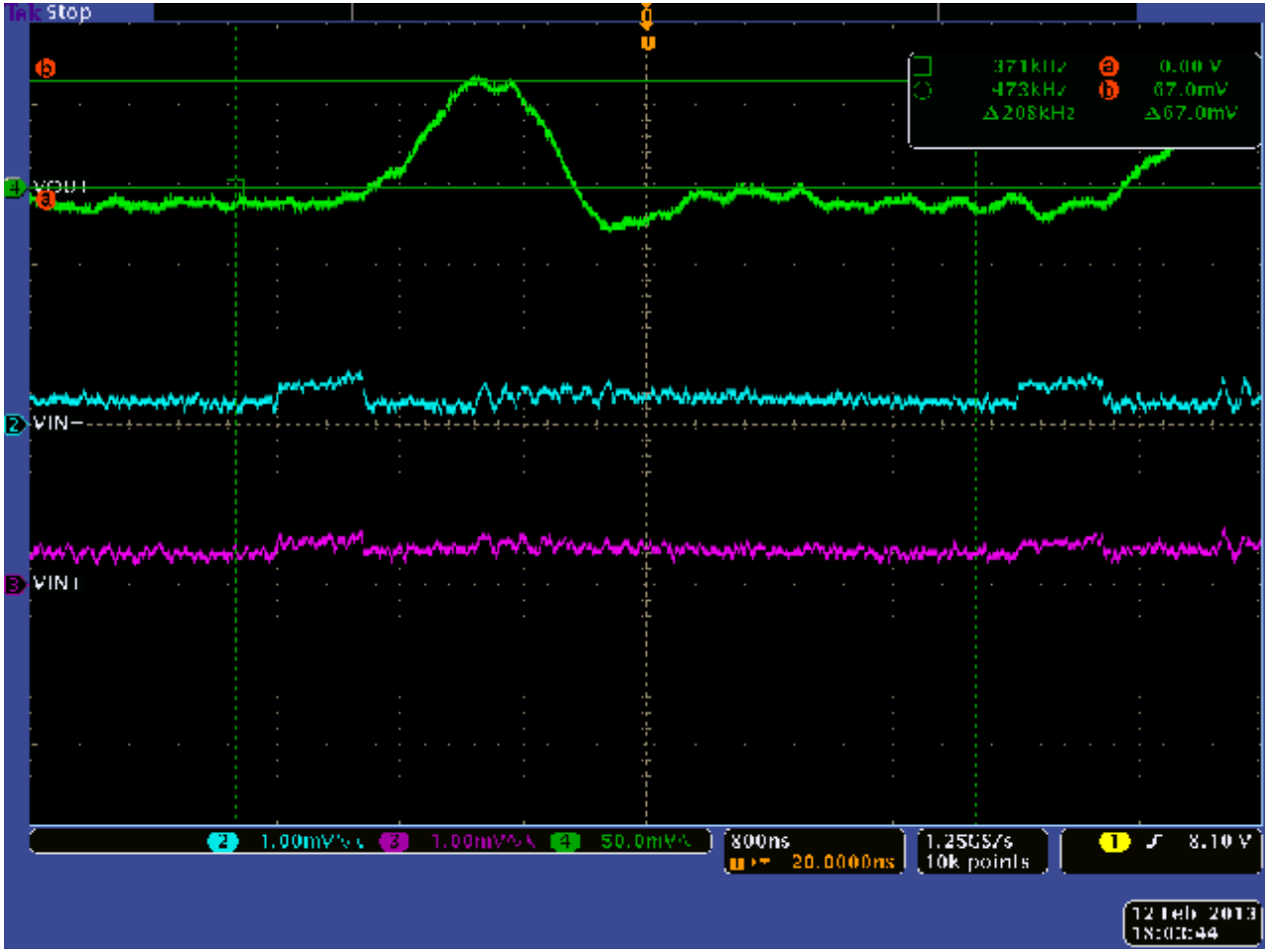
Layout 1a Results – V_{IN-} & V_{IN+} Noise





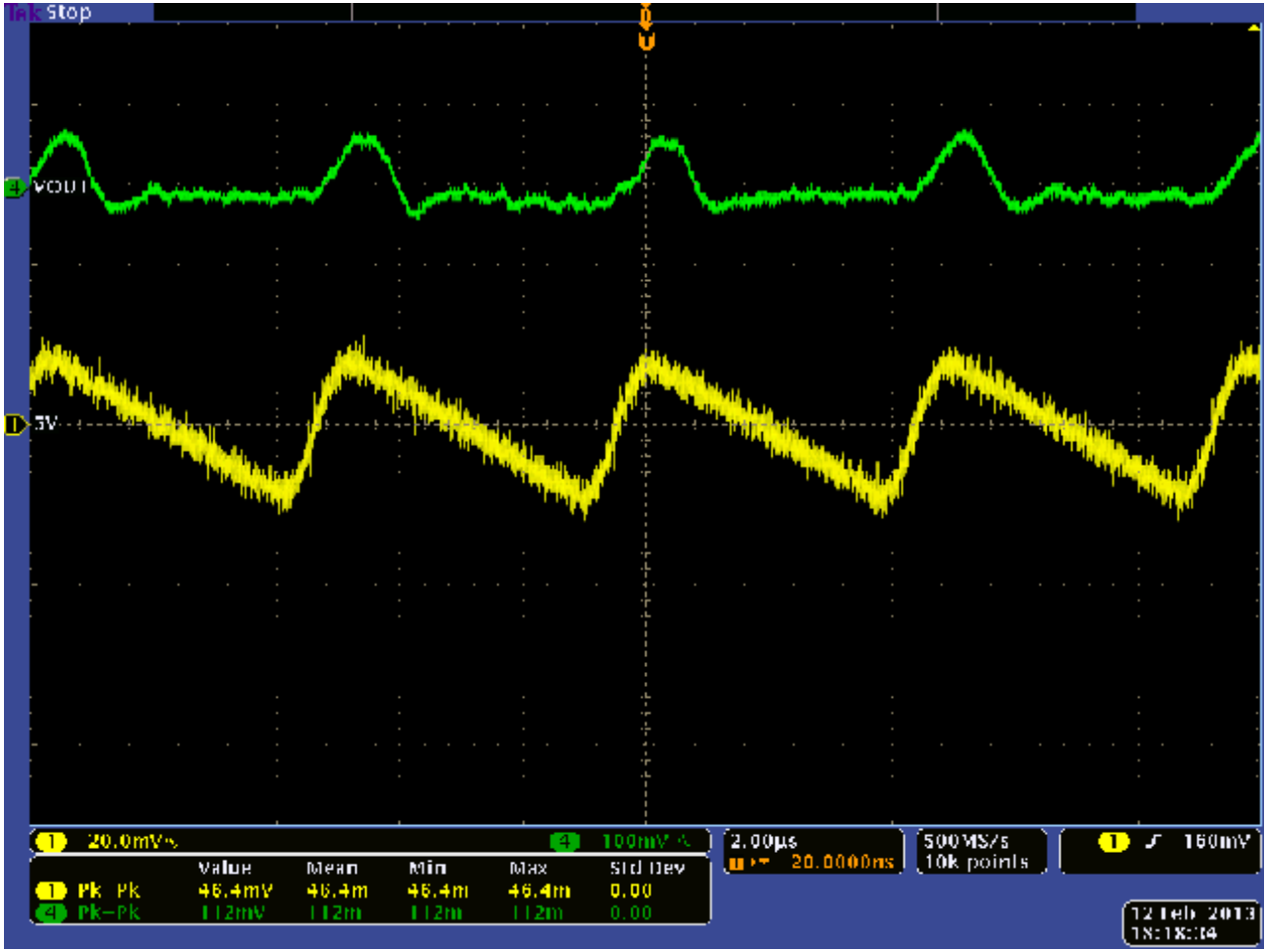
- Some switching noise is able to couple into the signal traces
- Most likely by capacitive coupling to the ground plane

Layout 1a Results – V_{OUT} Noise



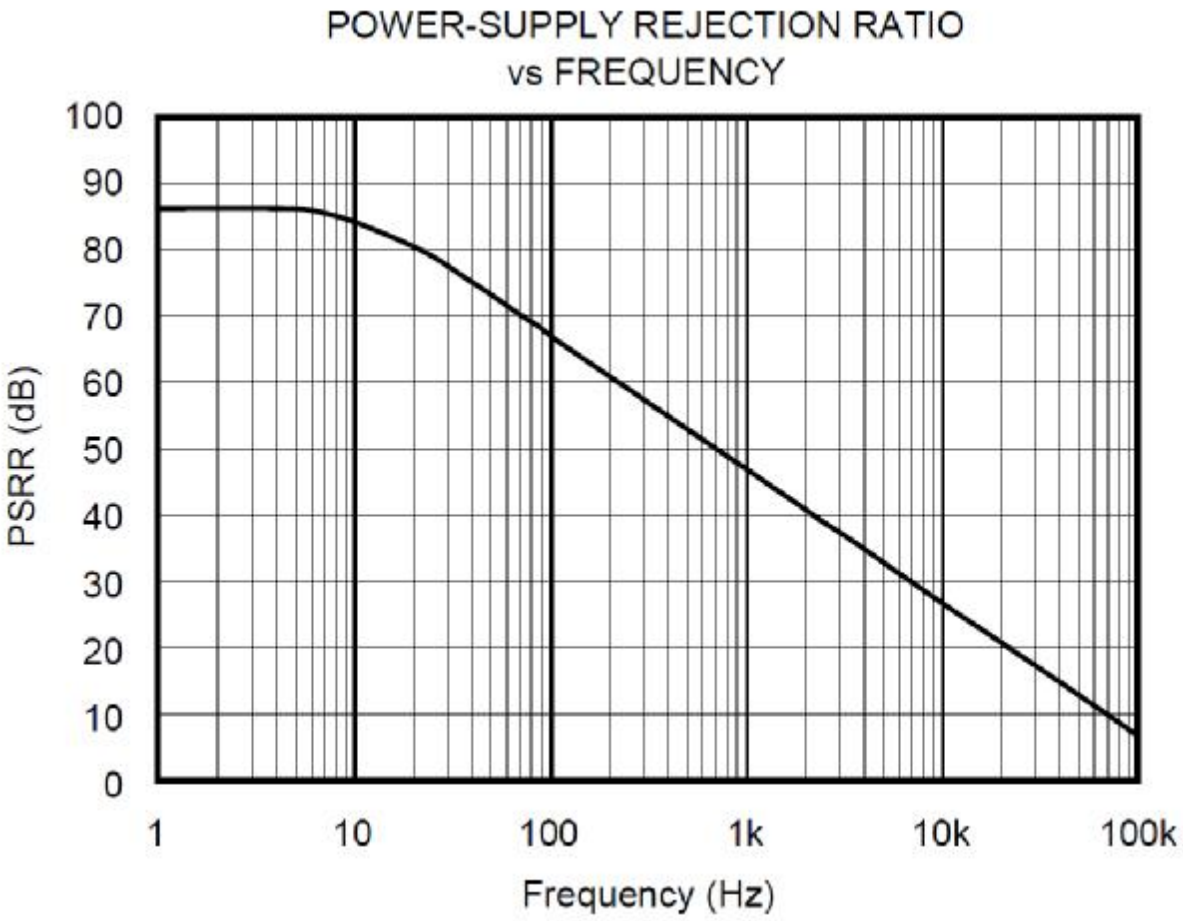
Some periodic noise on V_{OUT} is present, but strangely, it does not appear to be correlated to (V_{IN+} - V_{IN-})

Layout 1a Results – V_{OUT} Noise



If we probe VOUT and the 5V power rail, we can see that the VOUT noise spikes are in phase with the switching power supply's AC ripple

Layout 1a Results – V_{OUT} Noise



The INA331 has no power-supply rejection at 200 kHz!

Conclusions

- On most PCBs, trace-to-trace capacitance will not be large enough to cause I^2C bus failures
- Analog signal traces can easily pick up large amounts of AC noise through capacitive coupling, especially through adjacent PCB layers
- If capacitively-coupled input noise is within the gain-bandwidth of an amplifier, huge errors may be observed at the amplifier's output
  - High gain configurations are especially susceptible to this issue
- Even "good" layouts can experience unwanted noise coupling through the ground plane or power supply

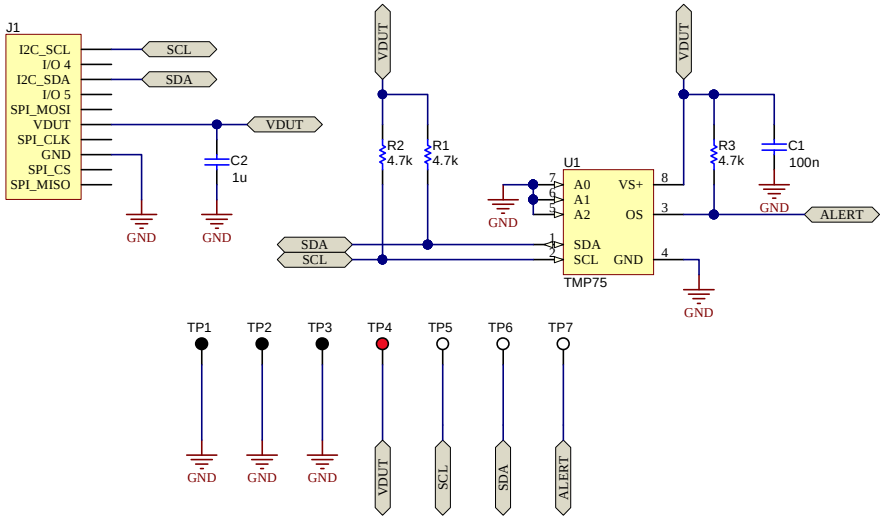
Recommendations

- Use short, direct signal routing to minimize unwanted noise pickup
  - Place ground copper between adjacent traces to minimize cross talk
  - Use filtering on signal paths if required
- Control parasitic capacitance and inductance
  - Cut out copper planes and traces under sensitive nodes
  - Minimize use of vias on critical signal traces
- Ideally, select an amplifier with sufficient bandwidth for your input signals but lower bandwidth than the noise sources in your system
- Be mindful of any switching power supply's switching frequency compared to the PSRR of the amplifiers in your system
- Use adequate supply bypass capacitors

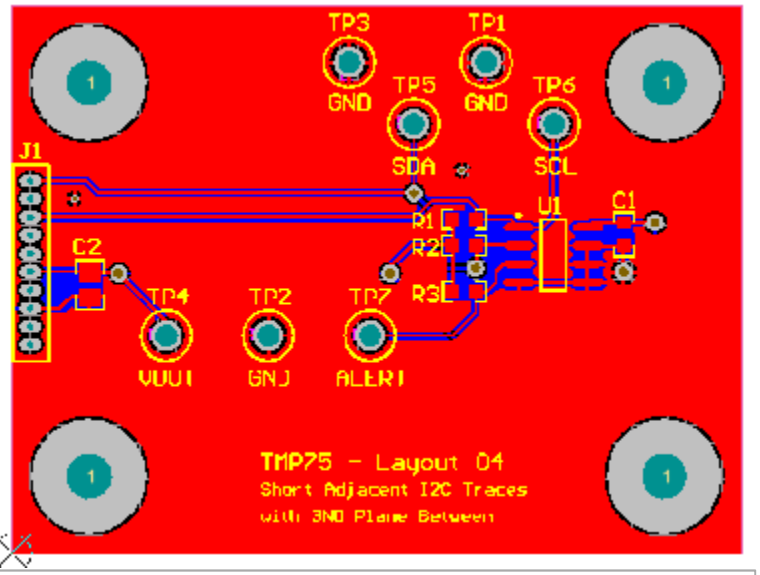
Summary

Summary

- Real-world printed circuit boards have a significant impact on a circuit's measured performance
- **Parasitics** - capacitors, inductors, resistors, thermocouples, and leakage paths - can be formed by certain processes and layout techniques
- The effects of these parasitics **must** be minimized in order to maintain acceptable circuit performance



≠



References

- K. Blake, "Op Amp Precision Design: PCB Layout Techniques," Microchip Technology Inc., Chandler, AZ, AN1258, 2009.
- J. Ardizzoni, "A Practical Guide to High-Speed Printed-Circuit-Board Layout", *Analog Dialogue*, vol. 39, no. 9, Sept. 2005.
- R. Downs, "Precision Analog Designs Demand Good PCB Layouts," Texas Instruments Inc., Dallas, TX, presented at TI Tech Days, 2009.
- T. Kuehl, "Thermocouple Applications," Texas Instruments Inc., Dallas, TX, presented at TI Precision Analog Applications Seminar, 2006.
- K. Mitzner, "PCB Design for Signal Integrity," in *Complete PCB Design Using OrCAD® Capture and PCB Editor*. Oxford, UK: Elsevier, 2009, ch. 6, pp. 97-157.
- J. Karki, "Effect of Parasitic Capacitance in Op Amp Circuits," Texas Instruments Inc., Dallas, TX, SLOA013A, 2000.
- R. Schmid, "Measuring Board Parasitics in High-Speed Analog Design," Texas Instruments Inc., Dallas, TX, SBOA094, 2003.

Special thanks to Collin Wells and Pete Semig for their work on I^2C bus capacitance!