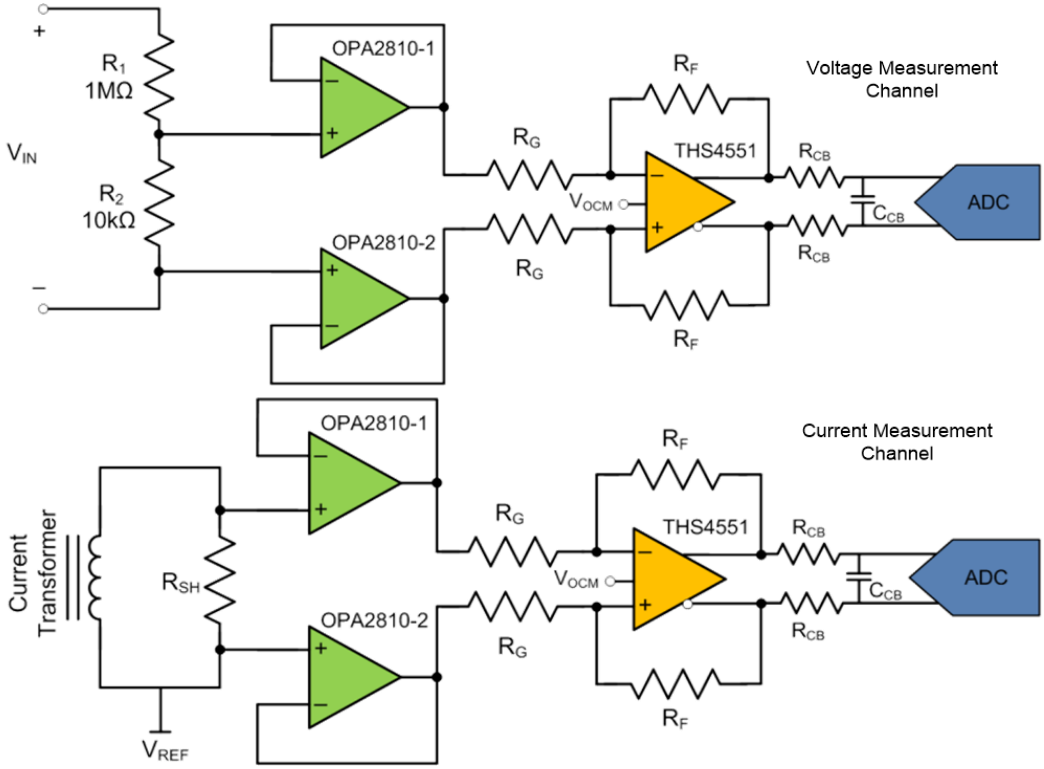
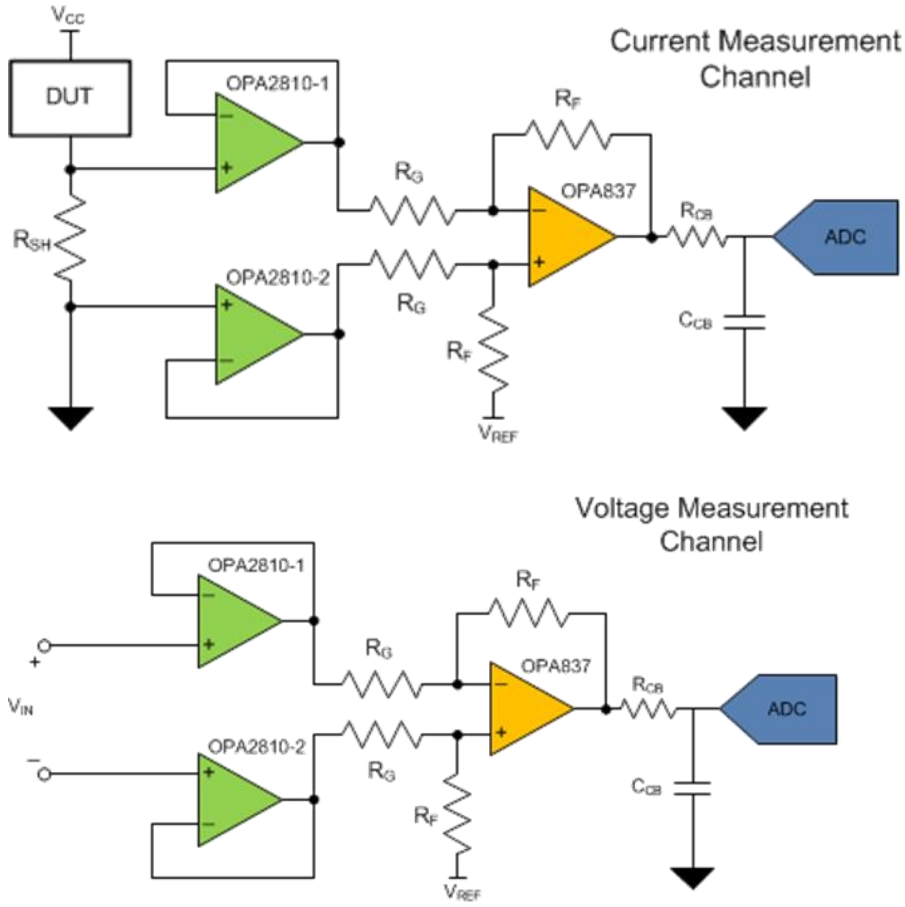
Check out TI's JFET amplifiers for **High Voltage, High-Input Impedance front-end** systems for Power Analyzers. The OPA2810 is a dual-channel and OPA810 is the single-channel version. The OPAx810 offers 70MHz, FET-input, Rail to Rail Input & Output, and a 24V amplifier with 2x performance over similar competition devices.

Voltage & Current measurement channels in Power Analyzers will require low noise and large input impedance with low distortion for a high-fidelity signal chain.

Example Block Diagram with Differential ADC:



Generic Block Diagram Single ended ADC:



ADC Driver:

- **Single Ended Output:**
  - **OPA863A is a 12V supply voltage RRIO feedback amplifier which offer great precision (0.095µV/C), low power (0.8mA) and 50MHz**
- **Differential Output:**
  - **An FDA is needed to attenuate the voltage & drive the Precision or High-Speed ADCs to perform the single-ended to differential signal conversion, TI offers several FDAs with a variety of BW and voltage ranges depending on the system need.**
  - **Check out the TIDA-00187: *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts***
  - **For a fully differential input ADC check out the latest fully differential ADC drivers for your application below: (THS4531A, THS4551, THS4561, THS4541, THS4509)**

Parameter	THS4531A	THS4561	THS4551	THS4541	THS4509
ADC Pairing	> 14-bit, 500kSPS-1MSPS	> 14-bit, 1 – 2 MSPS	> 16-bit, 1 – 4 MSPS	> 10-MSPS	>100-MSPS
Gain Bandwidth Product (MHz)	36	68	135	850	3000
Quiescent Current, I_Q (typ) (mA)	0.25	0.775	1.37	10.1	37.7
e_{noise} (nV/√Hz) (1/f corner frequency)	10 (45Hz)	4 (8Hz)	3.3 (150Hz)	2.2 (30kHz)	1.9(10kHz)
Slew Rate (V/µs)	200	230	220	1500	6600
V_{OS} (25°C, Max) (µV)	400	250	175	450	4
V_{OS} drift (typ) (µV/°C)	3	0.5	1.8	0.5	2.6
THD (dB), V_{OUT} = 2 V_{PP} @ 100kHz	-102	-117	-128	-93 (@ 5MHz)	-104 (@10MHz)
Output Voltage Swing (V)	V_{S-} +0.2, V_{S+} – 0.11	V_{S-} +0.25, V_{S+}-0.1	V_{S-}+0.2, V_{S+} – 0.2	V_{S-} +0.2, V_{S+} – 0.2	V_{S-} +1.1, V_{S+} – 1.1
Differential Output Impedance (Ω) f= 100kHz, G= 1)	0.25	0.06	0.02	0.1	0.3
Settling Time (G=1, 0.1%, V_{OUT}=2V step) (ns)	60	40	30	8 (G=2)	10
Temperature Range (°C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Features	Low Iq	Feedback Pin	Feedback Pin	Bare Die Option Feedback Pin Auto Q100	Shutdown

Additional Signal Conditioning:

- **May be needed if the signal has to be attenuated to compensate for the ADC input voltage range**

Reference Buffer:

- **Need for reference buffers for ADCs with external reference for multichannel and fast sampling rates.**
- **OPA863A- Reference buffer: Precision(95uV), Low power(0.8mA), 50MHz, RRIO voltage feedback amplifier.**
  - **Check out the TIDA-01055: *ADC Voltage Reference Buffer Optimization Reference Design for High-Performance DAQ Systems***

Additional Collateral:

- **Check out this BLOG for more information on JFET amplifiers in different types of applications.**
- **Check out this TIDA-01057: *Reference Design Maximizing Signal Dynamic Range for True 10 Vpp Differential Input to 20-bit ADC***
- **SBOT049: *Pairing High-speed JFET Amplifiers with Hi-Z DAQ Systems***
- **SBOT050: *Pairing ADC Drivers with Fully-Differential Input ADCs for Wide Bandwidth Data Acquisition***