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Power-Saving Topologies for TI Current Shunt Monitors

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ABSTRACT

Power demands of today's modern systems have created the need for sensors to shut down when not in use. Through the strategic placement of TI's FemtoFET product line, significant power savings can be realized for several parts in the TI current sensing product line.

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1   Background and Motivation [(1)]

Current monitors are continually used in today's most advanced technologies at an increased rate. Current monitors fulfill multiple roles, providing information that ranges from feedback in motor control systems to overcurrent fault detection in protection circuitry. However, in many of these applications, the current sensor may not continually send information; instead the current sensor may be polled every minute, second, or fraction of a second. This gap leaves downtime in the current sensing circuit where the device continues to consume power, but does not provide a tangible benefit to the system.

Aside from the INA190, most of the current sensors in the TI parts portfolio do not include an internal ability to disable the part. However, the rapidly evolving embedded systems of today are revealing a need for expanded battery life: drones must fly longer, smartphones need additional energy to accommodate massive data demands, and invasive medical devices must maximize battery life, to cite a few examples. A challenge arises because there are several ways to implement a current sensor in these applications; a single solution is insufficient for all cases. This guide examines several leading devices of the TI current sensing parts catalog, and analyzes specific ways to incorporate the FemtoFET product line from TI to reduce power consumption in the parts when they are not needed by the system. These parts are designed and optimized to minimize the footprint of today's field-effect transistor (FET), providing a reduction in footprint size up to 60%. Figure 1 shows an example of the CSD25481F4 dimensions.

In addition to shutting down current sensors with the FemtoFET products, the INA190 and its internal enable/disable feature will be considered. Both methods of shutting down the INA190 (using its logic enable pin and using an external FET) will analyzed for comparison.
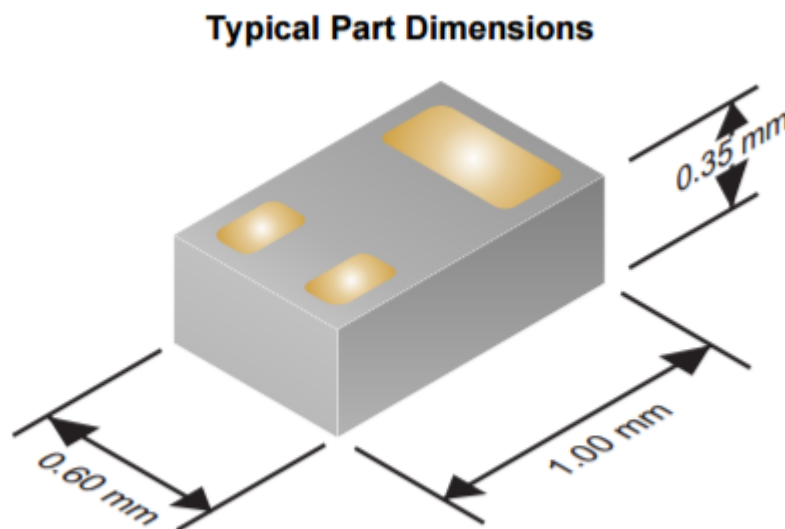

Figure 1. CSD25481F4 Dimensions

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2   Devices

In each of the following cases a variety of data is examined, including multiple common-mode voltages, varying levels of differential input, and different orientations of the reference pin. In each case, the metric of interest is the current consumed by the device. The output voltage is examined to provide information on that pin, because resistive paths are present in the devices. These voltages often collapse when a load is applied. Therefore, each device was also examined driving a 10 kΩ load. These two cases demonstrate the intended isolation alongside each device's ability to interact with high impedance networks, as well as their capabilities to drive resistive loads. In each of these diagrams, all passive components are not mounted, but provide options to configure different parameters for testing, such as input filtration, gain settings, and reference levels.

2.1   INA190 and Enable Pin

The INA190A5RSW was tested with the setup in Figure 2. The ENABLE pin was toggled by shorting it to either VS5 or GND5 planes on INA190EVM J45 header. Standard power and meter lab instruments were used with the INA190A5 (gain = 500V/V) EVM panel.
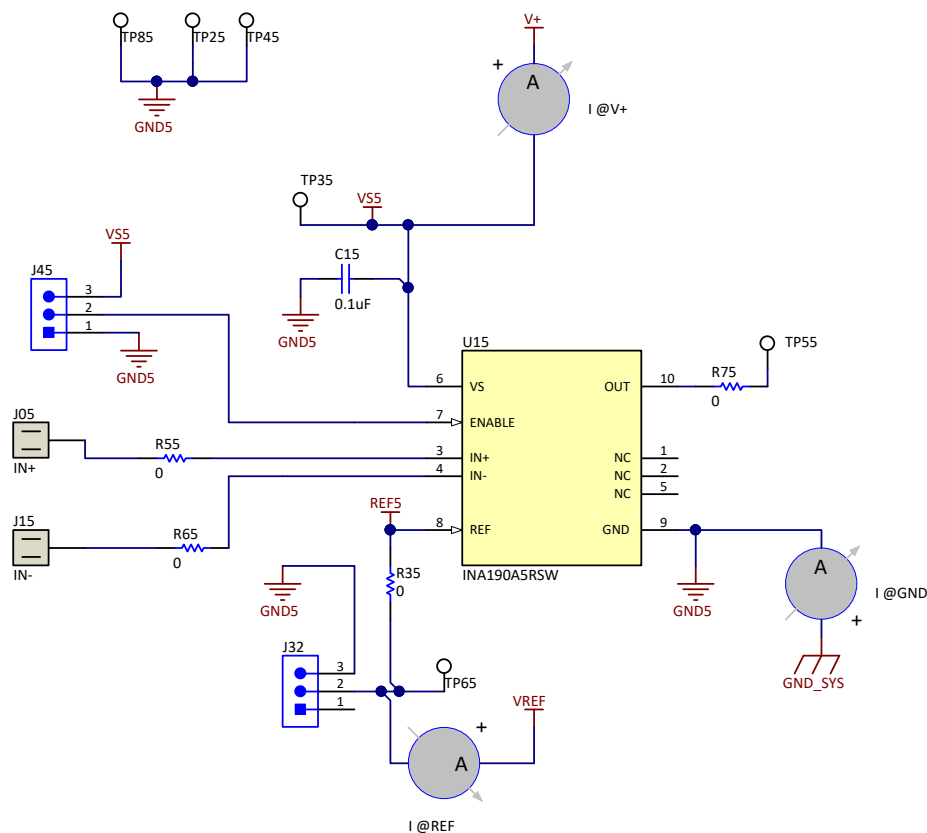
Figure 2. INA190 and Enable Pin Functionality Test Set Up Using INA190EVM

INA190 supply voltage (V+) was set to 1.8V for entire experiment. Two separate voltage sources set input differential voltage (V_{SENSE}) and input common voltage (V_{CM}). Measurements were recorded for two reference voltage levels (VREF): mid-supply and system ground. When the reference pin (REF) was grounded, VREF was driven to system ground (GND_SYS) of external power sources and not shorted to GND5 plane on the PCB. This is because when the ammeter was measuring I @GND, the GND5 could be millivolts above GND_SYS due to ammeter instrument sensing voltage and impedance loading. Ensuring a central ground for device shows true application performance. Note that current measurements were not taken simultaneously as to avoid loading effects from ammeters.

This ammeter interference is also why the input bias currents into IN+ and IN- pins were not measured. The INA190 I_B only significantly changes tens of nano-amps with V_{SENSE} (see INA190 datasheet). Thus, the introduction of an ammeter voltage will increase I_B and possible skew results. Furthermore, the INA190 input bias currents (iBias or I_B) were not measured since they are already very small (+-500pA typical ENABLED and 20 pA DISABLED). The INA190 capacitive input stage increases input impedance and thus reduces the I_B by almost three orders of magnitude compared to most other current sensors. Overall, the input bias currents are guaranteed by design and left out of this analysis for the INA190.

The INA190EVM did not have a load resistor for Table 1 and Table 2, but did have a 10 kΩ through-hole resistor as a load for Table 3 and Table 4. All measurements are at DC and sometimes required seconds of wait time for measurement to settle after adjusting the V_{CM}.

Table 1. INA190 Power with Enable Pin; Measurements With No Output Load (Enable Off)

ENABLE OFF								
V_{CM} (V)	V_{SENSE} (mV)	iBias IN+ (nA)	iBias IN- (nA)	I(nA) @V+	I(nA) @REF	I(nA) @GND	REF	V_{OUT} (mV)
0	1	<10	<10	0.05	0	0.07	V+/2	797.65
0	1	<10	<10	0.14	0.001	0.09	GND	-0.002
5	1	<10	<10	0.06	-0.003	0.08	V+/2	797.64
5	1	<10	<10	0.09	-0.01	0.1	GND	-0.001
12	1	<10	<10	0.05	-0.006	0.11	V+/2	797.65
12	1	<10	<10	0.07	-0.14	0.2	GND	0.005
42	1	<10	<10	0.04	-0.03	0.14	V+/2	797.63
42	1	<10	<10	0.04	-0.22	0.22	GND	0.001

Table 2. INA190 Power with Enable Pin; Measurements With No Output Load (Enable On)

ENABLE ON								
V_{CM} (V)	V_{SENSE} (mV)	iBias IN+ (nA)	iBias IN- (nA)	I(µA) @V+	I(µA) @REF	I(µA) @GND	REF	V_{OUT} (V)
0	1	<10	<10	49.95	0.029	50.185	V+/2	1.4013
0	1	<10	<10	50.37	-0.888	49.42	GND	0.5005
5	1	<10	<10	49.97	0.0289	50.18	V+/2	1.4015
5	1	<10	<10	50.37	-0.888	49.43	GND	0.5008
12	1	<10	<10	49.96	0.0289	50.18	V+/2	1.4016
12	1	<10	<10	50.38	-0.888	49.44	GND	0.5007
42	1	<10	<10	49.94	0.029	50.18	V+/2	1.4015
42	1	<10	<10	50.38	-0.888	49.43	GND	0.50056

Table 3. INA190 Power with Enable Pin; Measurements With 10 kΩ Output Load (Enable Off)

ENABLE OFF									
V_{CM} (V)	V_{SENSE} (mV)	iBias IN+ (nA)	iBias IN- (nA)	I(nA) @V+	I(nA) @REF	I(nA) @Load	I(nA) @GND	REF	V_{OUT} (mV)
0	1	<10	<10	0.11	696.42	698.8	0.08	V+/2	6.988
0	1	<10	<10	0.15	0.01	0	0.05	GND	0.000
5	1	<10	<10	0.15	696.42	698.8	0.09	V+/2	6.988
5	1	<10	<10	0.06	0.01	0	0.05	GND	0.000
12	1	<10	<10	0.08	696.4	698.9	0.07	V+/2	6.989
12	1	<10	<10	0.05	-0.01	0	0.05	GND	0.000
42	1	<10	<10	0.03	696.25	698.9	0.09	V+/2	6.989
42	1	<10	<10	0.03	-0.02	0	0.07	GND	0.000

Table 4. INA190 Power with Enable Pin; Measurements With 10 kΩ Output Load (Enable On)

ENABLE ON									
V_{CM} (V)	V_{SENSE} (mV)	iBias IN+ (nA)	iBias IN- (nA)	I(µA) @V+	I(µA) @REF	I(µA) @Load	I(µA) @GND	REF	V_{OUT} (V)
0	1	<10	<10	183.63	0.0292	140.12	43.44	V+/2	1.4012
0	1	<10	<10	93.4	-0.8881	50.014	42.7	GND	0.50014
5	1	<10	<10	183.7	0.029	140.17	43.447	V+/2	1.4017
5	1	<10	<10	93.4	-0.8884	49.975	42.7	GND	0.49975
12	1	<10	<10	183.7	0.029	140.16	43.45	V+/2	1.4016
12	1	<10	<10	93.4	-0.8883	50.072	42.69	GND	0.50072
42	1	<10	<10	183.65	0.0289	140.13	43.454	V+/2	1.4013
42	1	<10	<10	93.4	-0.8884	50.1	42.693	GND	0.501

According to Table 2 and Table 4, the lowest total currents (or I@GND) with ENABLE ON are achieved with 0-V VCM and 0-V REF; although, the difference in total current over VREF and V_{CM} are minimal. One reason for this is as the V_{CM} increases so do the input bias currents, which when positive will sink into the INA190 IN+ and IN- pins and then exit through the GND pin. The second reason is when the REF pin is grounded; it will source current (~888 nA) and thus divert current away from GND pin.

When the amplifier is driving a load, the disabled I@REF current will increase to about 698 nA and this is the limiting factor in reducing current draw from disabled INA190 at mid-supply reference. So when INA190 is disabled, even though the supply current, or I_{QDIS} in the datasheet, is reduced to around 100 pA, the OUT pin of the device is weakly driven by REF pin through approximately 1 MΩ of resistance. Note that when INA190 is disabled, the output pin becomes a high-impedance node and thus can be driven to any voltage within the INA190 voltage supply range.

According to Table 1, Table 2, Table 3, and Table 4 the greatest reduction in total current comes at 0-V V_{CM} and V+/2 REF with no load and 0-V V_{CM} and 0-VREF with a load. The reduction of INA190 Enabled current to INA190 Disabled current is as follows in Equation 1 and Equation 2.

With no load:

$$i_{total,ON}/i_{total, OFF}= 50.185 \ \mu A/0.07 \ nA = 716,929 \quad (1)$$

With load:

$$i_{total, ON}/i_{total, OFF} = 42.7 \ \mu A/0.05 \ nA = 854,000 \quad (2)$$

2.2 *INA190 and FET*

The INA190A5RSW was tested with the setup in Figure 3. The INA190 was isolated by placing FemtoFET CSD23280F3 (Q1) in line with the supply V+. The Q1 FET was turned on by shorting the gate to GND_SYS V+ and turned off by shorting gate to the source pin. Standard power and meter lab instruments were used with the INA190A5 (gain = 500V/V) EVM panel.
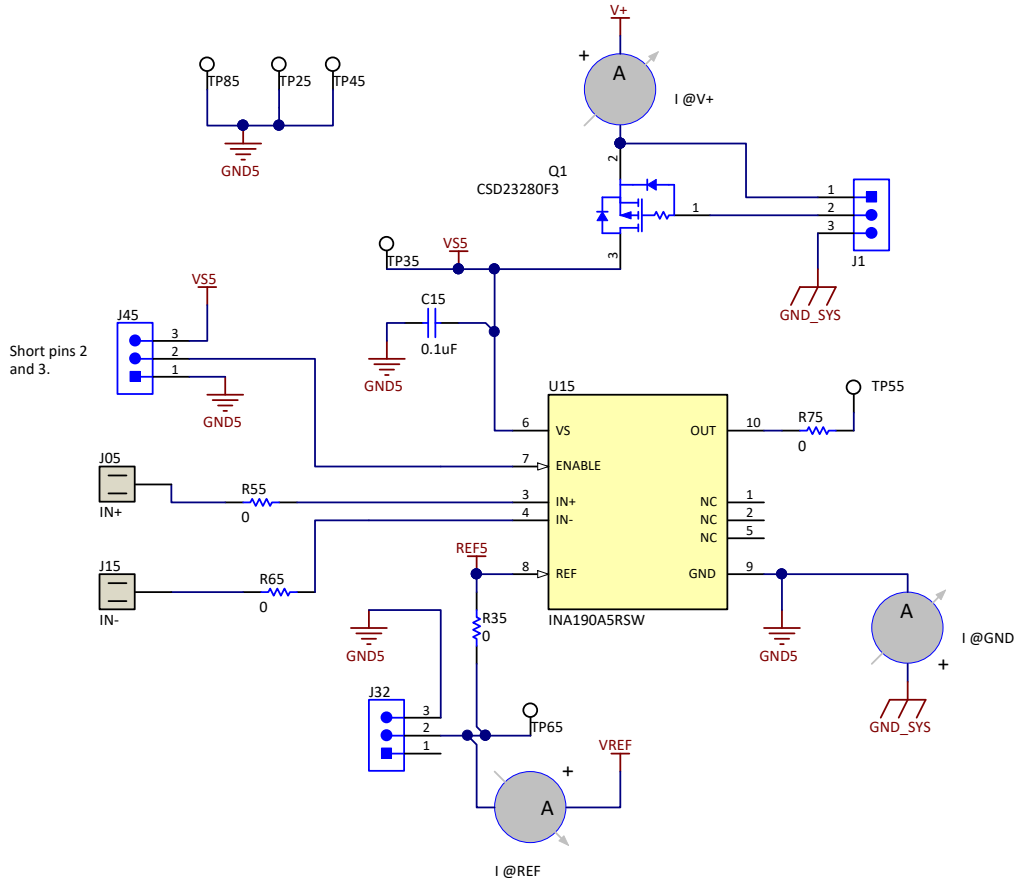

Figure 3. INA190 and Power Shutdown with CSD23280F3 FET

INA190 supply voltage (V+) was set to 1.8V and ENABLE pin was shorted to VS pin for entirety of these measurements. Two separate voltage sources set V_{SENSE} and input common voltage (V_{CM}). Measurements were made with two VREF levels and also with and without a 10 kΩ load. Equipment and test methodology are all the same as what was described in Section 2.1.

Table 5. INA190 with FemtoFET; Measurements with No Output Load (FET Off)

FET OFF								
V_{CM} (V)	V_{SENSE} (mV)	iBias IN+ (nA)	iBias IN- (nA)	I(nA) @V+	I(nA) @REF	I(nA) @GND	REF	V_{OUT} (V)
0	1	<10	<10	0.2	76	57.7	V+/2	0.776
0	1	<10	<10	0.07	-1.3	0.28	GND	0.000
5	1	<10	<10	0.089	76	57.6	V+/2	0.776
5	1	<10	<10	0.18	-1.4	0.4	GND	0.000
12	1	<10	<10	0.15	76	57.55	V+/2	0.776
12	1	<10	<10	0.3	-1.6	0.4	GND	0.000
42	1	<10	<10	0.2	76	57.55	V+/2	0.776
42	1	<10	<10	0.17	-1.4	0.35	GND	0.000

Table 6. INA190 with FemtoFET; Measurements with No Output Load (FET On)

FET ON								
V_{CM} (V)	V_{SENSE} (mV)	iBias IN+ (nA)	iBias IN- (nA)	I(μA) @V+	I(μA) @REF	I(μA) @GND	REF	V_{OUT} (V)
0	1	<10	<10	52.00	0.0303	51.89	V+/2	1.4015
0	1	<10	<10	52.36	-0.887	51.44	GND	0.5003
5	1	<10	<10	52.01	0.0303	51.90	V+/2	1.4019
5	1	<10	<10	52.39	-0.887	51.43	GND	0.5007
12	1	<10	<10	52.00	0.0302	51.90	V+/2	1.4017
12	1	<10	<10	52.39	-0.887	51.43	GND	0.5009
42	1	<10	<10	51.99	0.0302	51.90	V+/2	1.4012
42	1	<10	<10	52.39	-0.887	51.43	GND	0.5010

Table 7. INA190 with FemtoFET; Measurements with 10 kΩ Output Load (FET Off)

FET OFF									
V_{CM} (V)	V_{SENSE} (mV)	iBias IN+ (nA)	iBias IN- (nA)	I(nA) @V+	I(nA) @REF	I(nA) @Load	I(nA) @GND	REF	V_{OUT} (V)
0	1	<10	<10	0.13	706.7	710	3.17	V+/2	0.007
0	1	<10	<10	0.11	-0.26	-1	0.2	GND	0.000
5	1	<10	<10	0.12	706.9	710	3.21	V+/2	0.007
5	1	<10	<10	0.108	-0.143	-1	0.3	GND	0.000
12	1	<10	<10	0.093	706.8	710	3.24	V+/2	0.007
12	1	<10	<10	0.1	-0.35	-1	0.3	GND	0.000
42	1	<10	<10	0.087	706.8	710	3.31	V+/2	0.007
42	1	<10	<10	0.084	-0.2	-1	0.5	GND	0.000

Table 8. INA190 with FemtoFET; Measurements with 10 kΩ Output Load (FET On)

FET ON									
V_{CM} (V)	V_{SENSE} (mV)	iBias IN+ (nA)	iBias IN- (nA)	I(μA) @V+	I(μA) @REF	I(μA) @Load	I(μA) @GND	REF	V_{OUT} (V)
0	1	<10	<10	185.33	0.0304	140.13	45.82	V+/2	1.4015
0	1	<10	<10	95.15	-0.8869	50.00	44.77	GND	0.50007
5	1	<10	<10	185.27	0.0303	140.12	45.83	V+/2	1.4014
5	1	<10	<10	95.11	-0.8873	50.05	45.77	GND	0.50060
12	1	<10	<10	185.21	0.0303	140.19	45.83	V+/2	1.4021
12	1	<10	<10	95.05	-0.8871	50.07	44.77	GND	0.50080
42	1	<10	<10	185.12	0.0304	140.20	45.83	V+/2	1.4022
42	1	<10	<10	95.01	-0.887	50.09	44.78	GND	0.50100

According to Table 6, and Table 8, the lowest total FET ON currents (I@GND) are achieved with 0-V V_{CM} and 0-V REF for similar as explained in Section 2.1; although, the difference between FET ON ground currents are minimal.

From Table 5 through Table 8, the greatest reduction in total current comes at 0-V V_{CM} and 0-V REF with a load and without a load. The reduction of total current from FET ON to FET OFF is determined by Equation 3 and Equation 4.

With no load:

$$i_{total,\ ON}/i_{total,OFF} = 51.44\ \mu A/0.28\ nA = 183,714 \tag{3}$$

With load:

$$i_{total,\ ON}/i_{total,\ OFF} = 44.77\ \mu A/0.20\ nA = 223,850 \tag{4}$$

If Table 1, Table 2, Table 3, and Table 4 are compared with Table 5, Table 6, Table 7, and Table 8, there is essentially no difference in power consumption when INA190 is operational and powered on. However, there is a difference in the total I@GND currents when INA190 is OFF. When using the ENABLE pin, the I@GND currents were always around 100 pA, but when using the FET to turn off the power supply, I@GND became 3 nA with a load and 57 nA without a load and at mid-supply. Additionally, with reference grounded the I@GND was around 100pA to 300pA higher when using the FET to turn INA190 off. The reason for this is that in Figure 3 the VS and ENABLE pins are essentially floating when the FET is off. In Figure 2, the ENABLE pin is actually driven to ground and this is what effectively shuts down the amplifier. When amplifier is properly disabled, the I_B and I_Q (or I@V+) drop significantly; I_Q will drop to I_{QDIS} where it will be 100pA to 10nA typically at room temperature and I_B will be less than 25 pA over VCM.

Another difference between Figure 2 and Figure 3 is how the supply current (I@V+) will change over temperature. If using the ENABLE pin, the supply current will conform to the I_{QDIS} specification and will increase to a maximum 500 nA at 150C. This behavior relates back to the reverse bias leakage current of the internal FET responsible for disabling the INA190. As temperature increases the diode's leakage current will increase similarly to most diodes. If using the FET as in Figure 3, as temperature increases so will the drain-to-source leakage current (I_{DSS}) of the Q1 FET. Leakage current is related to FET size, V_{GS} and V_{DS}. OFF leakage current for CSD23280F3 is specified as -50 nA at 25C, but will increase significantly over temperature and most certainly more than the INA190 I_{QDIS} since it is a bigger FET that can handle a maximum continuous drain current of 1.8 A.

In conclusion, disabling the INA190 with the ENABLE pin is more effective at reducing current consumption than using a FET at the supply pin because the ENABLE pin can shutdown the INA190 input and reference stages, as well as, maintain lower leakage current over temperature.

2.3 INA225

The INA225 was isolated by placing a CSD25484F4 in line with the supply pin V_S, as shown in Figure 4.
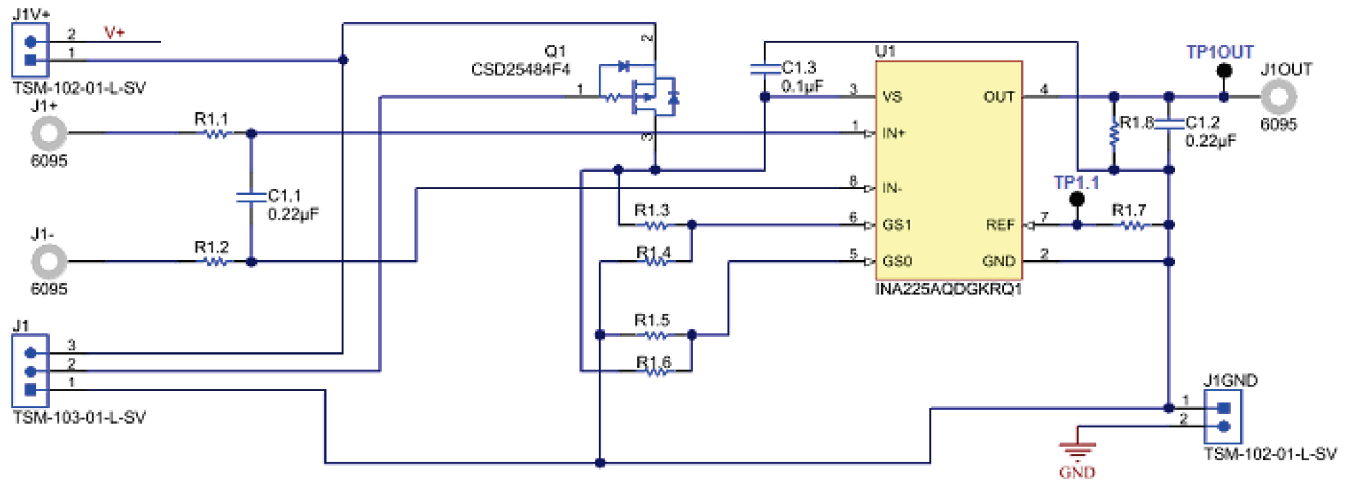
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Not all passive components are mounted simultaneously.

Figure 4. INA225 Schematic

The measurements in Table 9, Table 10, Table 11, and Table 12 were taken with the INA225 gain set to 200 and the supply voltage (V+) set to 5 V. The measurements were taken with the reference both at mid-supply and grounded. Resistor 1.8 was removed in Table 9 and Table 10, and set to 10 kΩ in Table 11 and Table 12.

Table 9. INA225 Measurements With No Output Load (FET Off)

FET OFF							
V_{CM} (V)	V_{Sense} (mV)	iBias IN+(µA)	iBias IN–(µA)	I(µA) @V+	I(µA) @GND	REF	V_{Out} (V)
5	8	54.9	49.3	–0.1	2302.9	V+/2	0.002
5	8	12.9	5.1	–0.2	5.0	GND	0.002
12	12	70.9	62	–0.2	2216.7	V+/2	0.002
12	12	29.5	17.9	–0.2	20.1	GND	0.001
36	8	118.5	113	–0.2	1889.4	V+/2	0.002
36	8	77	69.2	–0.2	71.7	GND	0.001

Table 10. INA225 Measurements With No Output Load (FET On)

FET ON							
V_{CM} (V)	V_{Sense} (mV)	iBias IN+(µA)	iBias IN–(µA)	I(µA) @V+	I(µA) @GND	REF	V_{Out} (V)
5	8	56.4	49.1	279.3	374.4	V+/2	4.1
5	8	61.5	54.2	288.7	386.5	GND	1.6
12	12	72.5	61.7	274.3	379.3	V+/2	4.91
12	12	77.6	66.6	287.7	397.5	GND	2.41
36	8	119.9	112.5	269.8	427.5	V+/2	4.15
36	8	125.1	117.7	281.6	444.3	GND	1.65

Table 11. INA225 Measurements With 10 kΩ Output Load (FET Off)

FET OFF								
V_{CM} (V)	V_{Sense} (mV)	iBias IN+(µA)	iBias IN−(µA)	I(µA) @V+	I(µA) @Load	I(µA) @GND	REF	V_{Out} (V)
5	8	54.8	49.4	−0.2	0.2	2289.9	V+/2	0.002
5	8	12.9	5.1	−0.2	0	4.9	GND	0.001
12	12	70.9	62.0	−0.2	0.2	2203.9	V+/2	0.003
12	12	29.4	17.9	−0.2	−0.1	20	GND	0
36	8	118.5	112.8	−0.2	0.2	1874.9	V+/2	0.002
36	8	77.1	69.3	−0.2	−0.1	71.6	GND	0

Table 12. INA225 Measurements With 10 kΩ Output Load (FET On)

FET ON								
V_{CM} (V)	V_{Sense} (mV)	iBias IN+(µA)	iBias IN−(µA)	I(µA) @V+	I(µA) @Load	I(µA) @GND	REF	V_{Out} (V)
5	8	56.3	49.1	674.8	410.1	357.9	V+/2	4.09
5	8	61.5	54.2	433.2	160.7	372.7	GND	1.6
12	12	72.5	61.6	753.8	491.2	367.0	V+/2	4.9
12	12	77.6	66.7	514.9	241.7	382.7	GND	2.41
36	8	119.8	112.6	669.4	415.0	411.7	V+/2	4.14
36	8	125.0	117.7	432.2	165.5	429.2	GND	1.65

From the data captured, in almost all cases applying a FemtoFET in the given configuration results in current reduction. The greatest benefit was seen when V_{CM} is 5 V, because the ratio of total current from FET OFF to FET ON is as follows in Equation 5.

$$i_{total,\ ON}\ /\ i_{total,\ OFF} = 386.5\ \mu A\ /\ 5.0\ \mu A = 77.3 \tag{5}$$

Equation 5 shows that the introduction of this topology can result in a reduction in current of greater than 77x. The output has been driven to nearly zero in all cases, effectively shutting down the INA225. The INA225 actually increases current consumption when the reference is placed at mid-supply. This increase is due to an internal property of the device that allows a large amount of current to flow through the reference pin when the supply pin is not being driven. Therefore, this topology is recommended only for unidirectional cases.

2.4   INA199

The INA199 was isolated by placing a CSD25480F3 in line with the supply V+, as shown in Figure 5.
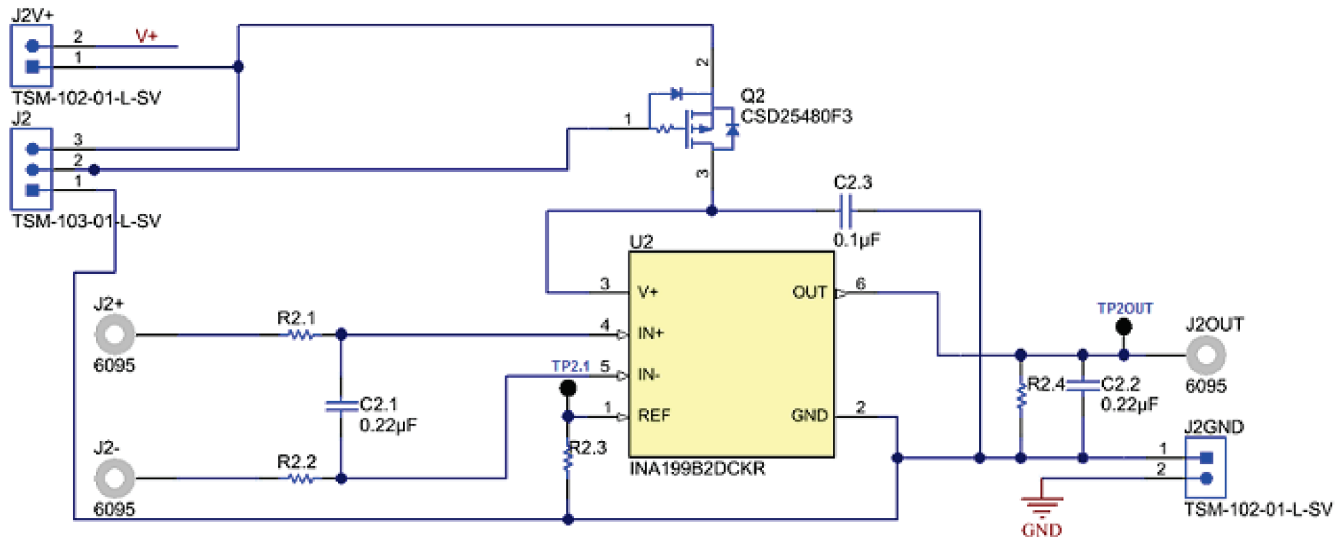
Not all passive components are mounted simultaneously

Figure 5. INA199 Schematic

The measurements in Table 13, Table 14, Table 15, and Table 16 were taken with the INA199B2 gain set to 100 and the supply voltage (V+) set to 5 V. The measurements were taken with the reference both at mid-supply and grounded. Resistor 2.4 was removed in Table 13 and Table 14, and set to 10 kΩ in Table 15 and Table 16.

Table 13. INA199 Measurements With No Output Load (FET Off)

FET OFF							
V$_{CM}$ (V)	V$_{Sense}$ (mV)	iBias IN+(µA)	iBias IN–(µA)	I(µA) @V+	I(µA) @GND	REF	V$_{Out}$ (V)
5	18	10.6	−2.1	−0.2	6.3	V+/2	.987
5	18	13.0	−2.1	−0.2	6.3	GND	.989
12	12	18.6	10.6	−0.1	20.3	V+/2	1.166
12	12	21.0	10.5	−0.2	20.3	GND	1.168
26	20	41.8	27.3	−0.1	46.9	V+/2	1.355
26	20	44.1	27.3	−0.1	47.0	GND	1.335

Table 14. INA199 Measurements With No Output Load (FET On)

FET ON							
V$_{CM}$ (V)	V$_{Sense}$ (mV)	iBias IN+(µA)	iBias IN–(µA)	I(µA) @V+	I(µA) @GND	REF	V$_{Out}$ (V)
5	18	26.7	11.1	60.9	96.5	V+/2	4.3
5	18	29.1	13.4	62.5	100.4	GND	1.797
12	12	31.0	20.6	59.6	102.5	V+/2	3.70
12	12	33.4	23.0	60.1	105.3	GND	1.198
26	20	48.1	30.7	54.7	111.6	V+/2	4.49
26	20	50.5	33.1	57.8	117.0	GND	1.996

Table 15. INA199 Measurements With 10 kΩ Output Load (FET Off)

FET OFF								
V$_{CM}$ (V)	V$_{Sense}$ (mV)	iBias IN+(µA)	iBias IN–(µA)	I(µA) @V+	I(µA) @Load	I(µA) @GND	REF	V$_{Out}$ (V)
5	18	9.2	−2.4	−0.1	4.6	−0.2	V+/2	.046
5	18	11.8	−2.5	−0.2	4.6	−0.2	GND	.046
12	12	13.6	6.5	−0.2	11.2	−0.2	V+/2	.112
12	12	16.0	6.6	−0.2	11.2	−0.2	GND	.112
26	20	30.0	16.5	−0.2	24.3	−0.2	V+/2	.244
26	20	32.3	16.5	−0.2	24.4	−0.2	GND	.244

Table 16. INA199 Measurements With 10 kΩ Output Load (FET On)

| FET ON								
V$_{CM}$ (V)	V$_{Sense}$ (mV)	iBias IN+(µA)	iBias IN–(µA)	I(µA) @V+	I(µA) @Load	I(µA) @GND	REF	V$_{Out}$ (V)
5	18	26.7	11.0	479.9	429.8	85.4	V+/2	4.29
5	18	29.0	13.4	227.8	179.8	85.6	GND	1.79
12	12	31.0	20.6	412.7	369.8	85.4	V+/2	3.69
12	12	33.4	22.9	160.8	119.9	85.9	GND	1.19
26	20	48.1	30.7	480.0	449.7	86.8	V+/2	4.49
26	20	50.5	33.1	227.9	199.8	87.1	GND	1.99

From the data captured, in all cases applying a FET in the given configuration results in current reduction. The greatest benefit was seen when V_{CM} is 5 V, because the ratio of total current from FET OFF to FET ON is as follows in Equation 6

$$i_{total,\ ON} / i_{total,\ OFF} = 100.4\ \mu A / 6.3\ \mu A = 15.94 \tag{6}$$

Equation 6 shows that the introduction of this topology can result in a reduction in current of 15x. However, some leakage propagates through the output pin due to resistive paths present throughout the part.

2.5 INA240

The INA240 was isolated by placing a CSD23280F3 in line with the supply pin V_S, as shown in Figure 6.
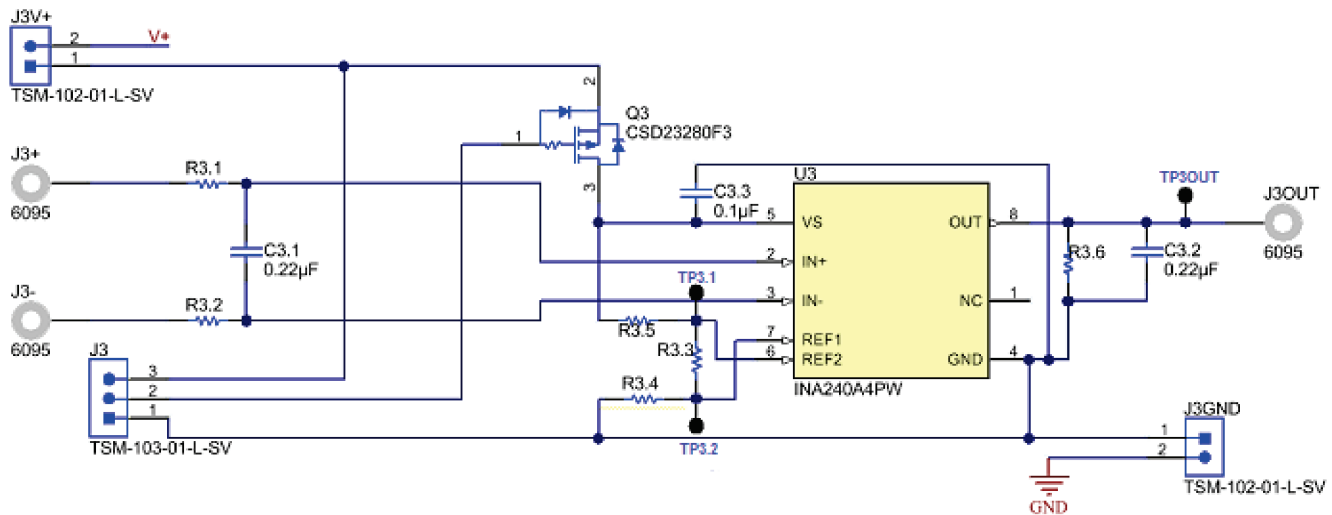
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Not all passive components are mounted simultaneously.

Figure 6. INA240 Schematic

The measurements in Table 17, Table 18, Table 19, and Table 20 were taken with the INA240A4 gain set to 200 and the supply voltage set to 5 V. The measurements were taken with the reference both at mid-supply and grounded. Resistor 3.6 was removed in Table 17 and Table 18, and set to 10 kΩ in Table 19 and Table 20. For the grounded case, REF1 and REF2 are both grounded. For the V+/2 case, REF1 is set to V+, and REF2 is grounded.

Table 17. INA240 Measurements With No Output Load (FET Off)

FET OFF							
V_{CM} (V)	V_{Sense} (mV)	iBias IN+(μA)	iBias IN−(μA)	I(μA) @V+	I(μA) @GND	REF	V_{Out} (V)
12	12	23.5	20.0	.1	43.4	V+/2	.474
12	12	23.6	19.9	.1	43.4	GND	.567
24	12	46.3	42.7	.1	89.1	V+/2	.605
24	12	46.4	42.7	.1	89.0	GND	.611
48	12	92.1	88.3	.1	180.6	V+/2	.636
48	12	92.4	88.4	.1	180.6	GND	.639
80	12	153.3	149.3	.1	302.7	V+/2	.671
80	12	154.2	149.3	.1	302.9	GND	.678

Table 18. INA240 Measurements With No Output Load (FET On)

FET ON							
V_{CM} (V)	V_{Sense} (mV)	iBias IN+(µA)	iBias IN–(µA)	I(µA) @V+	I(µA) @GND	REF	V_{Out} (V)
12	12	89.9	85.9	1847.7	2023.7	V+/2	4.91
12	12	90.0	85.9	1810.6	1986.4	GND	2.40
24	12	112.8	108.8	1826.7	2048.3	V+/2	4.91
24	12	112.9	108.7	1788.9	2010.7	GND	2.40
48	12	158.6	154.5	1791.5	2104.9	V+/2	4.91
48	12	158.9	154.5	1752.7	2066.0	GND	2.40
80	12	219.8	215.5	1757.9	2193.4	V+/2	4.91
80	12	220.4	215.5	1717.7	2153.0	GND	2.40

Table 19. INA240 Measurements With 10 kΩ Output Load (FET Off)

FET OFF								
V_{CM} (V)	V_{Sense} (mV)	iBias IN+(µA)	iBias IN–(µA)	I(µA) @V+	I(µA) @Load	I(µA) @GND	REF	V_{Out} (V)
12	12	23.3	19.8	–0.2	1.1	41.9	V+/2	.012
12	12	23.4	19.8	–0.2	1.1	41.9	GND	.012
24	12	46.1	42.6	–0.2	1.3	87.4	V+/2	.013
24	12	46.2	41.9	–0.2	1.3	85.3	GND	.013
48	12	91.0	88.2	–0.2	2.1	178.8	V+/2	.015
48	12	91.9	87.4	–0.2	1.4	176.4	GND	.014
80	12	152.1	149.1	–0.2	2.4	300.7	V+/2	.016
80	12	153.0	148.4	–0.2	1.5	298.4	GND	.015

Table 20. INA240 Measurements With 10 kΩ Output Load (FET On)

FET ON								
V_{CM} (V)	V_{Sense} (mV)	iBias IN+(µA)	iBias IN–(µA)	I(µA) @V+	I(µA) @Load	I(µA) @GND	REF	V_{Out} (V)
12	12	89.7	85.6	2270.1	491.3	1954.9	V+/2	4.90
12	12	89.7	85.7	1986.7	239.0	1922.9	GND	2.38
24	12	112.6	108.6	2248.8	491.2	1979.6	V+/2	4.90
24	12	112.6	108.5	1964.8	238.9	1947.1	GND	2.38
48	12	158.4	154.3	2213.3	491.1	2035.8	V+/2	4.90
48	12	158.4	154.4	1928.6	238.8	2002.4	GND	2.38
80	12	219.4	215.2	2179.1	491.0	2123.7	V+/2	4.89
80	12	219.4	215.3	1893.0	238.6	2089.5	GND	2.38

From the data captured, in all cases applying a FET in the given configuration results in current reduction. The greatest benefit was seen when V_{CM} is 12 V, because the ratio of total current from FET OFF to FET ON is as follows in Equation 7.

$$i_{total,\,ON} / i_{total,\,OFF} = 1954.9\ µA / 41.9\ µA = 46.66 \qquad (7)$$

Equation 7 shows that the introduction of this topology can result in a reduction in current of 46x.

2.6 INA212

The INA212 was isolated by placing a CSD25480F3 in line with the supply V$^+$, as shown in Figure 7.
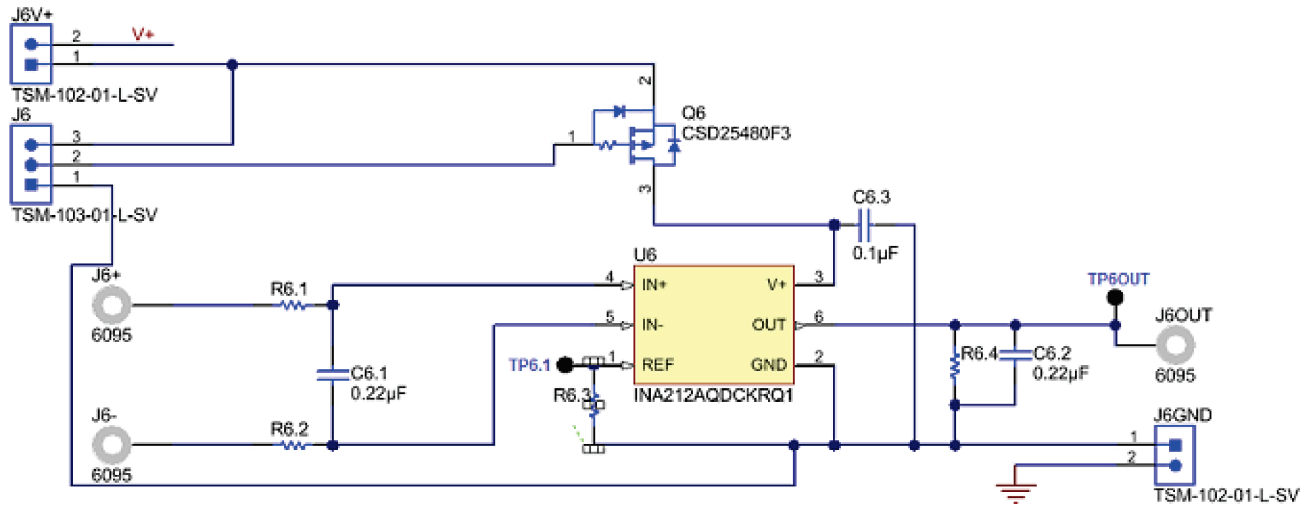
Not all passive components are mounted simultaneously.

Figure 7. INA212 Schematic

The measurements in Table 21, Table 22, Table 23, and Table 24 were taken with the INA212 set to a gain of 1000 and the supply voltage (V+) set to 5 V. The measurements were taken with the reference both at mid-supply and grounded. Resistor 6.4 was removed in Table 21 and Table 22, and set to 10 kΩ in Table 23 and Table 24.

Table 21. INA212 Measurements With No Output Load (FET Off)

FET OFF							
V$_{CM}$ (V)	V$_{Sense}$ (mV)	iBias IN+(μA)	iBias IN–(μA)	I(μA) @V+	I(μA) @GND	REF	V$_{Out}$ (V)
5	1.5	2.9	3.3	–0.2	3.8	V+/2	0.994
5	1.5	5.4	3.2	–0.2	3.8	GND	0.994
12	1.5	9.7	9.9	–0.2	10.6	V+/2	1.060
12	1.5	12.1	9.9	–0.2	10.6	GND	1.060
26	4	24.3	22.6	–0.2	24.2	V+/2	1.128
26	4	26.8	22.6	–0.2	24.2	GND	1.128

Table 22. INA212 Measurements With No Output Load (FET On)

FET ON							
V$_{CM}$ (V)	V$_{Sense}$ (mV)	iBias IN+(μA)	iBias IN–(μA)	I(μA) @V+	I(μA) @GND	REF	V$_{Out}$ (V)
5	1.5	18.1	15.4	66.7	98.2	V+/2	3.99
5	1.5	20.6	17.9	67.1	100.9	GND	1.490
12	1.5	24.9	22.2	63.2	101.5	V+/2	3.99
12	1.5	27.4	24.5	64.0	104.6	GND	1.490
26	4	40.1	34.6	34.2	86.5	V+/2	4.99
26	4	42.6	35.4	58.6	111.7	GND	3.98

Table 23. INA212 Measurements With 10 kΩ Output Load (FET Off)

FET OFF								
V$_{CM}$ (V)	V$_{Sense}$ (mV)	iBias IN+(μA)	iBias IN–(μA)	I(μA) @V+	I(μA) @Load	I(μA) @GND	REF	V$_{Out}$ (V)
5	1.5	2.9	4.1	–0.2	4.7	–0.2	V+/2	.048
5	1.5	5.3	4.1	–0.2	4.7	–0.1	GND	.048
12	1.5	9.7	10.9	–0.2	11.4	–0.2	V+/2	.108
12	1.5	12.2	10.9	–0.2	11.4	–0.2	GND	.115
26	4	24.3	23.4	–0.2	24.0	1.0	V+/2	.232
26	4	26.8	23.4	–0.2	24.9	1.2	GND	.241

Table 24. INA212 Measurements With 10 kΩ Output Load (FET On)

FET ON								
V$_{CM}$ (V)	V$_{Sense}$ (mV)	iBias IN+(μA)	iBias IN–(μA)	I(μA) @V+	I(μA) @Load	I(μA) @GND	REF	V$_{Out}$ (V)
5	1.5	18.1	15.4	455.4	399.0	87.4	V+/2	3.98
5	1.5	20.5	17.8	203.3	149.2	87.8	GND	1.49
12	1.5	25.0	22.2	448.4	399.1	87.4	V+/2	3.98
12	1.5	27.3	24.6	196.5	149.2	87.9	GND	1.49
26	4	40.2	34.6	535.0	500.7	86.4	V+/2	5.00
26	4	42.6	35.5	434.5	398.7	88.8	GND	3.98

From the data captured, in all cases applying a FET in the given configuration results in current reduction. The greatest benefit was observed when V_{CM} is 5 V, because the ratio of total current from FET OFF to FET ON is as defined in Equation 8.

$$i_{total,\ ON} / i_{total,\ OFF} = 100.9\ \mu A / 3.8\ \mu A = 26.55 \tag{8}$$

Equation 8 shows that the introduction of this topology can result in a reduction in current of greater than 26x.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2017) to A Revision   **Page**