SLG7AD45191

GreenPAK ™

Flash Button Reset

General Description

Dialog SLG7AD45191 is a low power and small form device. The SoC is housed in a 1mm x 1.2mm STQFN package which is optimal for using with small devices.

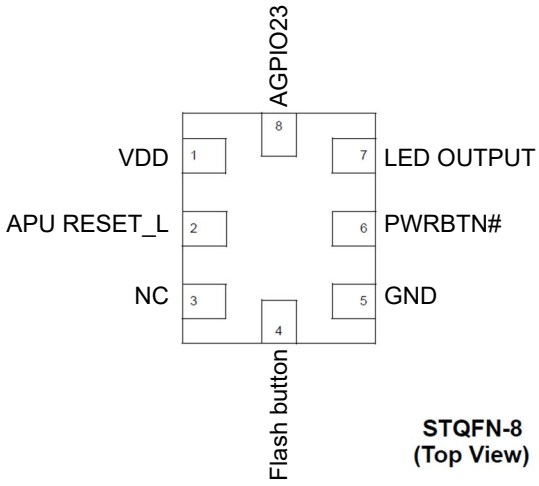
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 8 Package

Output Summary

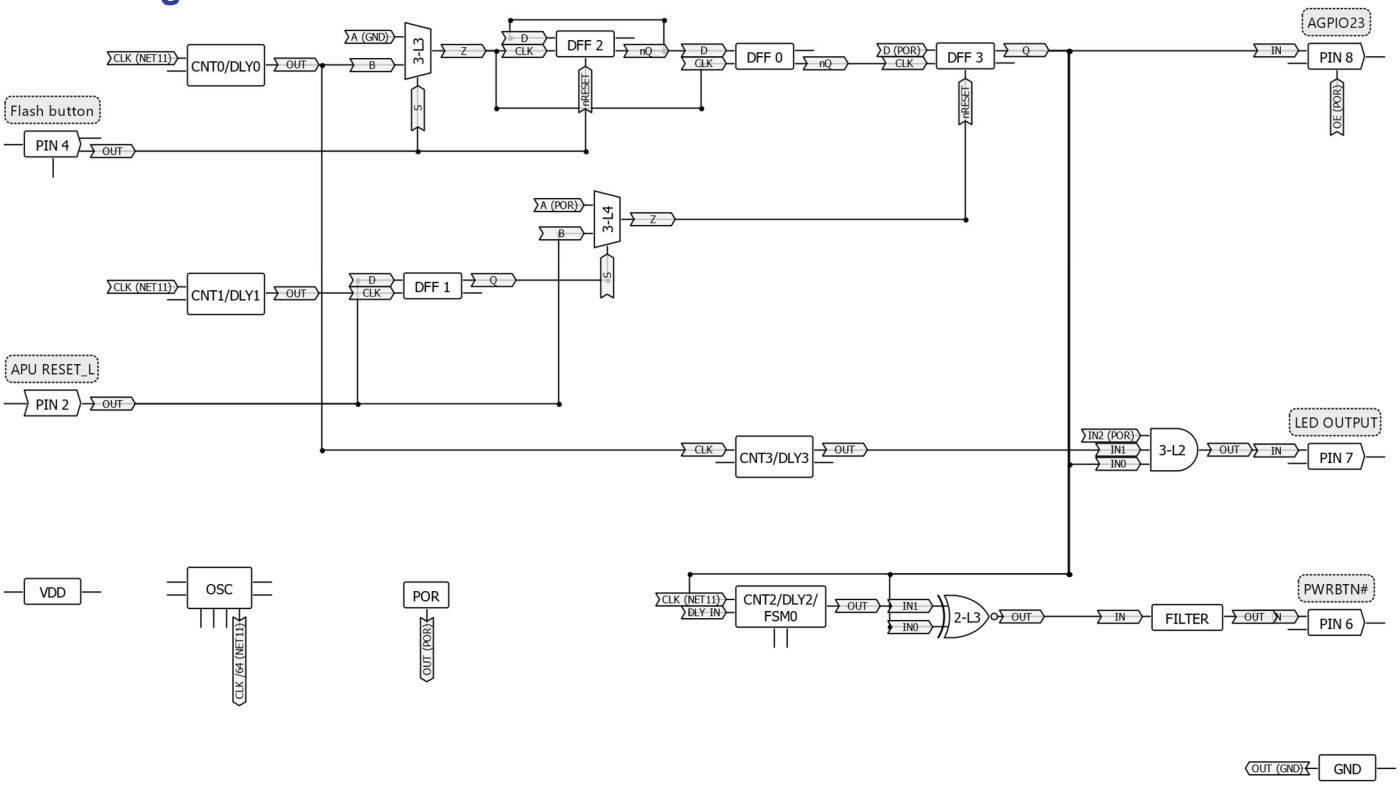
1 Output - Open Drain NMOS 2X
1 Output - Push Pull 1X
1 Output - Push Pull 2X

Pin Configuration



STQFN-8
(Top View)

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	APU RESET_L	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
3	NC	--	Keep Floating or Connect to GND	--
4	Flash button	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
5	GND	GND	Ground	--
6	PWRBTN#	Digital Output	Push Pull 1X	floating
7	LED OUTPUT	Digital Output	Open Drain NMOS 2X	1MΩ pullup
8	AGPIO23	Digital Output	Push Pull 2X	floating

Ordering Information

Part Number	Package Type
SLG7AD45191V	8-pin STQFN
SLG7AD45191VTR	8-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	8	mA
	Push-Pull 2x	--	10	
	OD 2x	--	12	
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

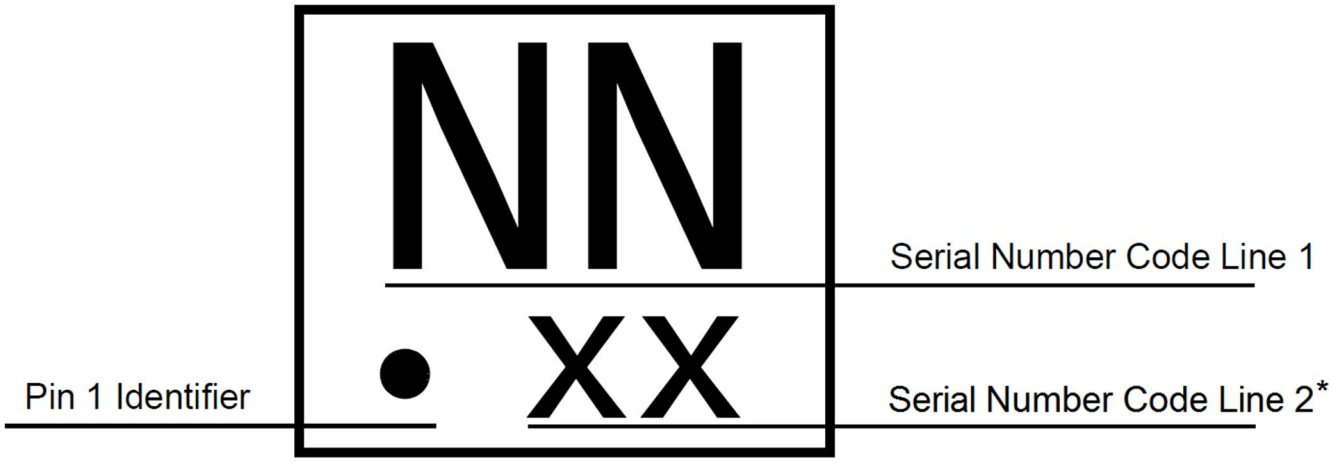
Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	3.3	5.5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	15	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	84	mA
		T_J = 110°C	--	--	40	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input at VDD=1.8V	1.071	--	VDD	V
		Logic Input at VDD=3.3V	1.84	--	VDD	V
		Logic Input at VDD=5.0V	2.744	--	VDD	V
V_{IL}	LOW-Level Input Voltage	Logic Input at VDD=1.8V	0	--	0.73	V
		Logic Input at VDD=3.3V	0	--	1.255	V
		Logic Input at VDD=5.0V	0	--	1.877	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH}=100µA, at VDD=1.8V	1.692	1.788	--	V
		Push-Pull 1X, Open Drain PMOS 1X, I_{OH}=3mA, at VDD=3.3V	2.721	3.108	--	V
		Push-Pull 1X, Open Drain PMOS 1X, I_{OH}=5mA, at VDD=5.0V	4.171	4.761	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH}=100µA, at VDD=1.8V	1.7	1.794	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH}=3mA, at VDD=3.3V	2.864	3.204	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH}=5mA, at VDD=5.0V	4.336	4.879	--	V

V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=100µA, at VDD=1.8V	--	0.01	0.016	V
		Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V	--	0.175	0.257	V
		Push-Pull 1X, I_{OL}=5mA, at VDD=5.0V	--	0.225	0.325	V
		Push-Pull 2X, I_{OL}=100µA, at VDD=1.8V	--	0.005	0.007	V
		Push-Pull 2X, I_{OL}=3mA, at VDD=3.3V	--	0.086	0.122	V
		Push-Pull 2X, I_{OL}=5mA, at VDD=5.0V	--	0.111	0.156	V
		Open Drain NMOS 2X, I_{OL}=100µA, at VDD=1.8V	--	0.003	0.003	V
		Open Drain NMOS 2X, I_{OL}=3mA, at VDD=3.3V	--	0.043	0.061	V
		Open Drain NMOS 2X, I_{OL}=5mA, at VDD=5.0V	--	0.057	0.08	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH}=VDD-0.2V, at VDD=1.8V	1.045	1.506	--	mA
		Push-Pull 1X, Open Drain PMOS 1X, V_{OH}=2.4V, at VDD=3.3V	5.774	11.066	--	mA
		Push-Pull 1X, Open Drain PMOS 1X, V_{OH}=2.4V, at VDD=5.0V	20.656	30.203	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH}=VDD-0.2V, at VDD=1.8V	2.097	2.982	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH}=2.4V, at VDD=3.3V	11.351	21.73	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH}=2.4V, at VDD=5.0V	40.17	56.319	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL}=0.15V, at VDD=1.8V	0.984	1.363	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V	4.491	6.438	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=5.0V	6.087	8.611	--	mA
		Push-Pull 2X, V_{OL}=0.15V, at VDD=1.8V	2.011	2.743	--	mA
		Push-Pull 2X, V_{OL}=0.4V, at VDD=3.3V	9.124	12.884	--	mA
		Push-Pull 2X, V_{OL}=0.4V, at VDD=5.0V	12.321	17.147	--	mA
		Open Drain NMOS 2X, V_{OL}=0.15V, at VDD=1.8V	4.02	5.471	--	mA
		Open Drain NMOS 2X, V_{OL}=0.4V, at VDD=3.3V	17.995	25.459	--	mA
		Open Drain NMOS 2X, V_{OL}=0.4V, at VDD=5.0V	24.032	33.581	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PIN 7	700	1000	1300	kΩ
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 2, 4	700	1000	1300	kΩ

T_{DLY2}	Delay2 Time	At temperature 25°C	492.93	515.84	532.95	ms
		At temperature -40 +85°C (Note 3)	474.45	515.84	559.17	ms
T_{CNT0}	Counter0 Period	At temperature 25°C	541.98	565.76	583.08	ms
		At temperature -40 +85°C (Note 3)	521.66	565.76	611.77	ms
T_{CNT1}	Counter1 Period	At temperature 25°C	247.69	258.56	266.48	ms
		At temperature -40 +85°C (Note 3)	238.40	258.56	279.59	ms
T_{CNT3}	Counter3 Period	At temperature 25°C	1.08	1.13	1.17	s
		At temperature -40 +85°C (Note 3)	1.04	1.13	1.23	s
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	--	0.54	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.303	1.506	1.707	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.675	0.901	1.174	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3 and 4 are connected to one side, pins 6, 7 and 8 to another.
3. Guaranteed by Design.

Package Top Marking



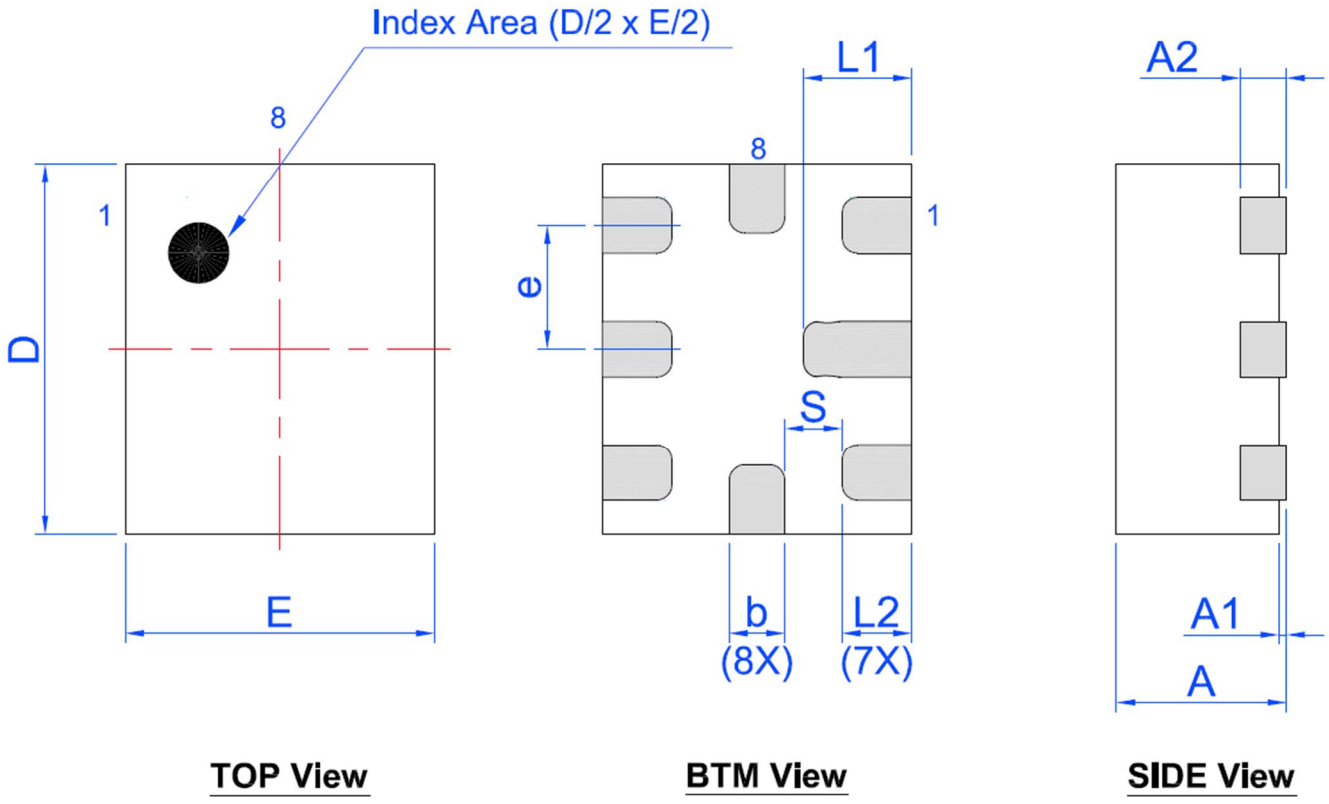
* xx only consists of the special characters +, -, and = for a total of 9 different combinations

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	002	L	0xF8DE3C6D	2D	B	04/05/2022

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

8 Lead STQFN Package 1.0 x 1.2 mm



TOP View **BTM View** **SIDE View**

Unit: mm

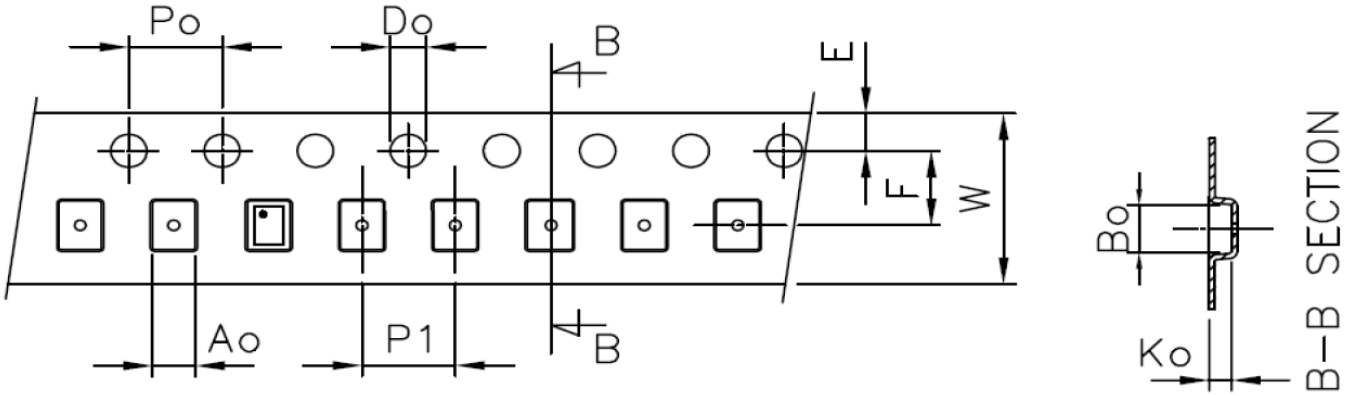
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.15	1.20	1.25
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L1	0.30	0.35	0.40
b	0.13	0.18	0.23	L2	0.175	0.225	0.275
e	0.40 BSC			S	0.185 REF		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 8L 0.4P FC Green	8	1.0x1.2x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 8L 0.4P FC Green	1.16	1.38	0.71	4	4	1.5	1.75	3.5	8



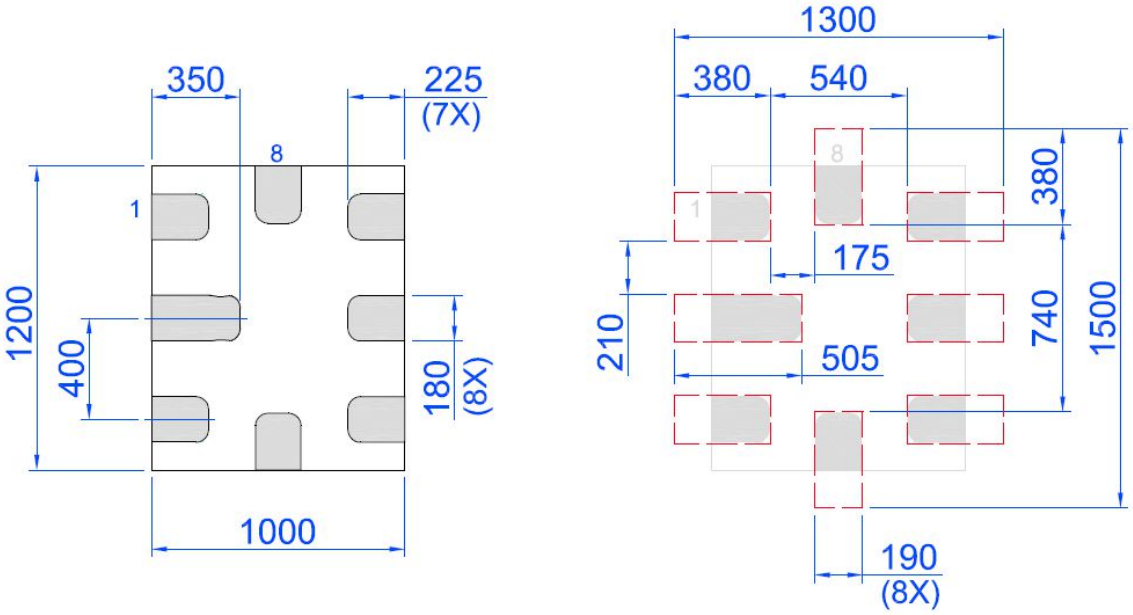
Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.66 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern

Exposed Pad
(PKG face down)

Recommended Landing Pattern
(PKG face down)



Unit: um

Datasheet Revision History

Date	Version	Change
08/19/2021	0.10	New design for SLG46108 chip
08/25/2021	0.11	Change PIN#2 name to APU_RESET_L
09/14/2021	0.12	Updated Device Revision Table
03/29/2022	0.13	Changed logo and updated Lock status
04/01/2022	0.14	Updated DRS Table
04/05/2022	1.00	Production Release