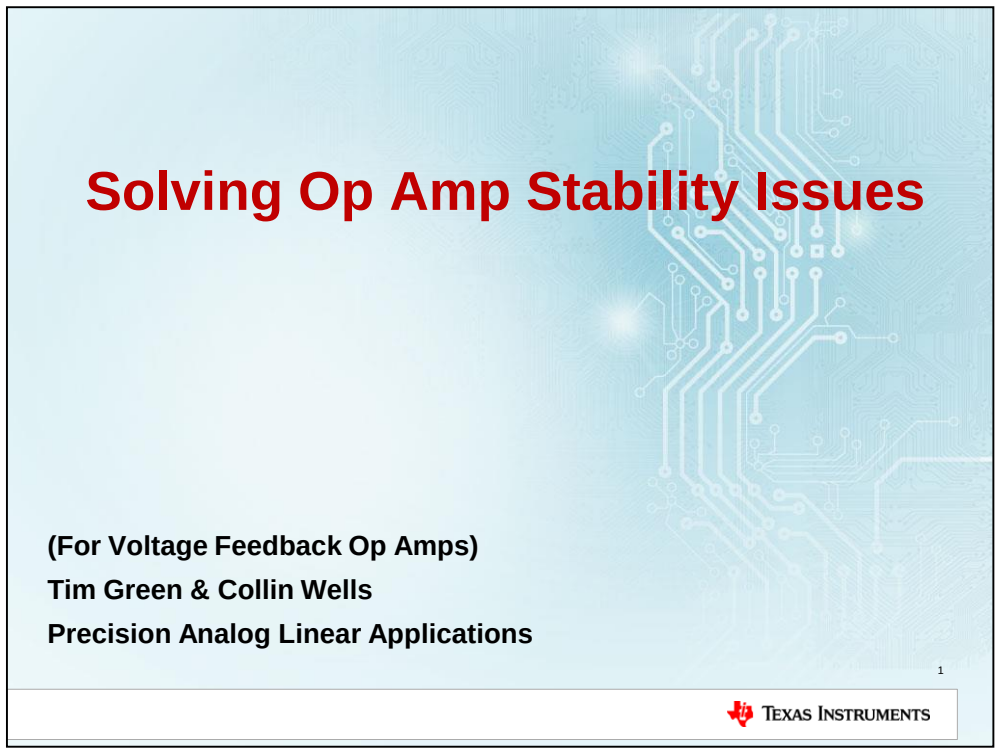


This presentation will focus on techniques to solve voltage feedback op amp stability problems. The content is intended to teach any range of professional, from technician to PHD, to become an op amp stability expert!

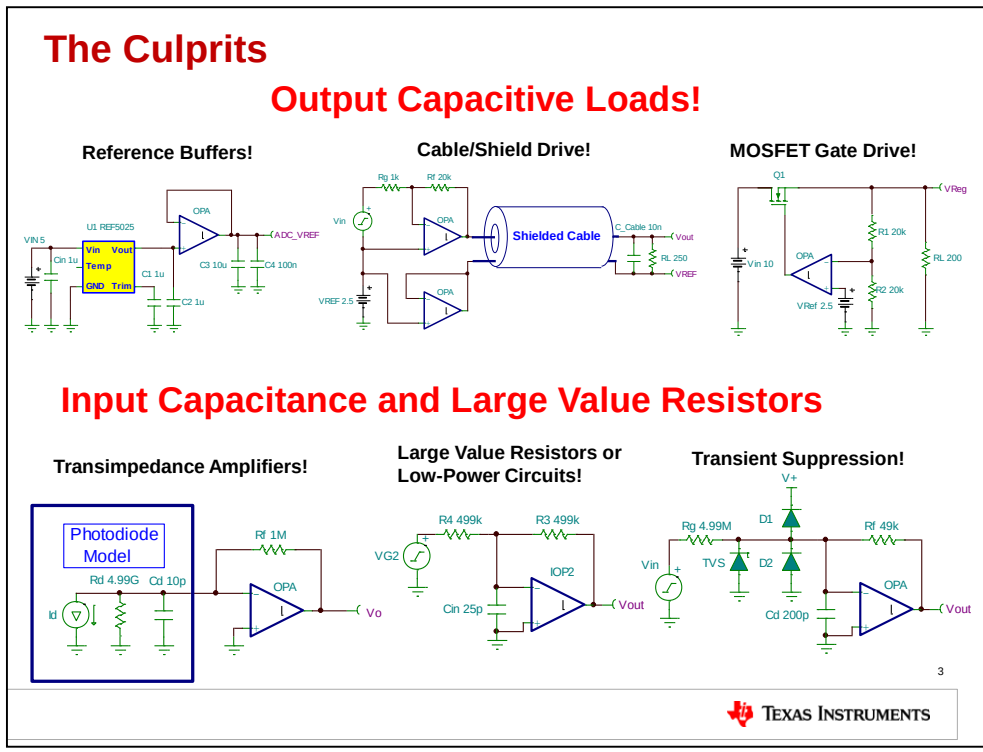
Overview

Main Presentation Focus:

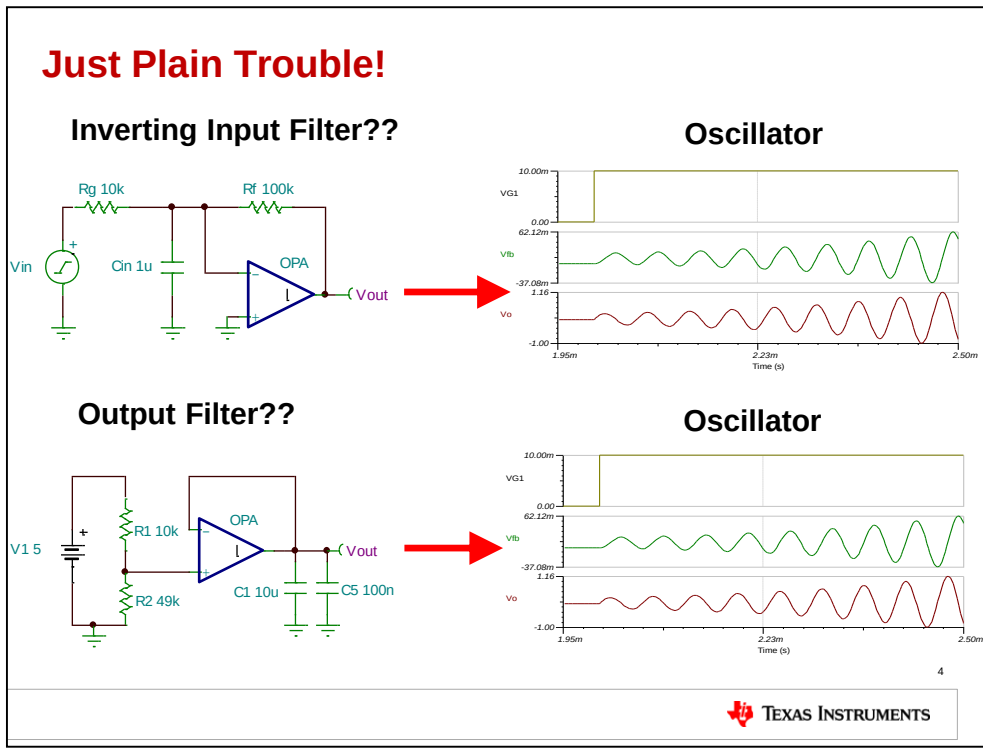
1) Op Amp Stability Basics
2) Stability Analysis – Method 1 : Loaded Aol & 1/β Technique
   A) Riso Compensation Technique for Output Capacitive Loads
3) Stability Analysis – Method 2 : Aol & 1/β Technique
   A) CF Compensation Technique for Input Capacitance
4) Stability Tricks and Rules of Thumb

Appendix:

1) Additional Useful Tools for your Analog Stability Toolbox
   A) Op Amp Output Impedance
   B) Pole and Zero: Magnitude and Phase on Bode Plots
   C) Dual Feedback Paths and 1/β
   D) Non-Loop Stability Problems
2) Nine different ways to stabilize op amps with capacitive loads
   A) Definition by example using TINA-TI simulations



For small signal op amps the most common cause of op amp instability is capacitance on the output or input. Sometimes output capacitive loads are obvious, such as a reference buffer loaded by an output capacitor, for high frequency filtering, and as a charge reservoir for load transients. Other output capacitive loads can often be overlooked, such as, cable capacitance and MOSFET gate capacitance. Input capacitance is easy to overlook, since it is usually parasitic capacitance, such as, op amp input capacitance, photodiode capacitance, or diode/transient voltage suppressor capacitance. Both input and output capacitance are often the culprits of unstable op amp circuits.



For an inverting gain configuration, as shown here, some engineers will add a filter, Cin, which will result in a nice oscillatory behavior unless proper compensation is added for stability. Output capacitance on an op amp should always be of concern from a stability concern. Even if it is not a sustained oscillation, a response to a transient step excitation can result in undesired overshoot and ringing on the output. This becomes more of concern as we designs systems with 12 bit and higher resolution A/D Converters with sample rates fast enough to capture the ringing.

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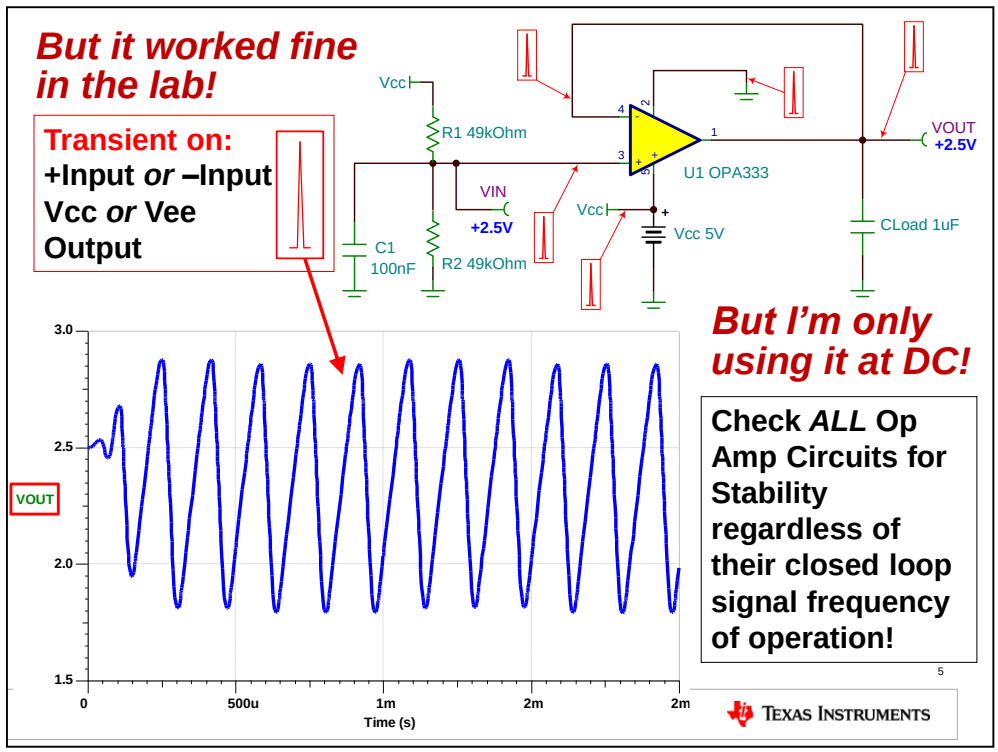
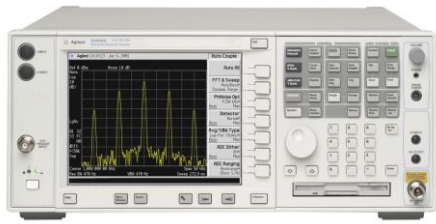


A typical "Supply Splitter" is shown above. Many an engineer has built one of these for a mid-supply reference point in a single supply system. A large capacitance is put on the output to provide a local charge reservoir for load transients on VOUT, and to also provide good high frequency bypassing in the form of a low impedance to ground at high frequencies, should loads connected generate noise or high frequency spikes. Then, in the lab, he has connected a DC meter and confirmed that the output voltage, VOUT, is indeed mid-supply. Now the supply splitter circuit goes into production. Best case the product passes final test and is shipped to the customer. Worst case production fall-out happens and yields go down. Worst, worst case the product ships to the end customer and the end customer starts to have intermittent performance problems All of this due to a marginally stable or unstable mid-supply reference circuit which could have been avoided by proper stability analysis at the design phase! Regardless of the final signal frequency of operation, including DC only, op amps have usable bandwidth and are happy to oscillate under the right conditions. Check stability on all op amp circuits.

Treat all op amp pins as inputs. A transient on +input, -input, output, or power supplies (Vcc or Vee) can set an unstable or marginally stable into an undesired, burst, oscillatory state that may eventually recover. However, during the oscillatory response due to a transient, the end application may read false data, make wrong decisions, or even cause unwanted shutdowns.

Recognize Amplifier Stability Issues on the Bench

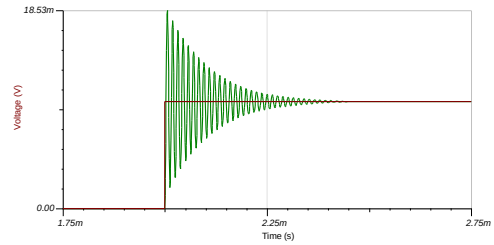
- Required Tools:
  - Oscilloscope
  - Signal Generator
- Other Useful Tools:
  - Gain / Phase Analyzer
  - Network / Spectrum Analyzer

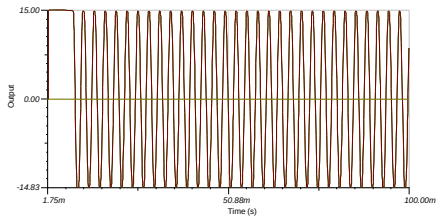


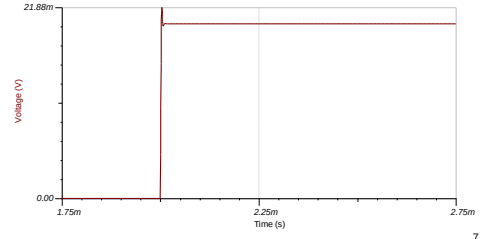
Your lab contains instruments that can help you check prototype circuits for stability problems. Most labs will have a Signal Generator and an Oscilloscope. Techniques will be shown later in this presentation on how to easily check op amp stability using these instruments in the time domain. If a Gain/Phase Analyzer or Network/Spectrum Analyzer are available they can be used to check op amp stability in the frequency domain.

Recognize Amplifier Stability Issues

- Oscilloscope - Transient Domain Analysis:
  - Oscillations or Ringing
  - Overshoots
  - Unstable DC Voltages
  - High Distortion







7

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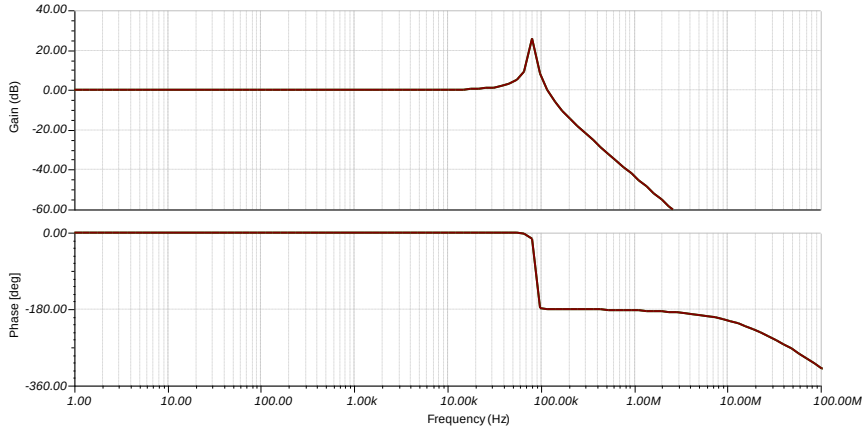
In the time domain, a transient analysis in the lab, with the results displayed on and oscilloscope, can indicate whether there is a stability problem in the op amp circuit. On the output waveform, oscillations or ringing, overshoots, unstable DC voltages or high distortion are all indicators of stability issues.

Recognize Amplifier Stability Issues

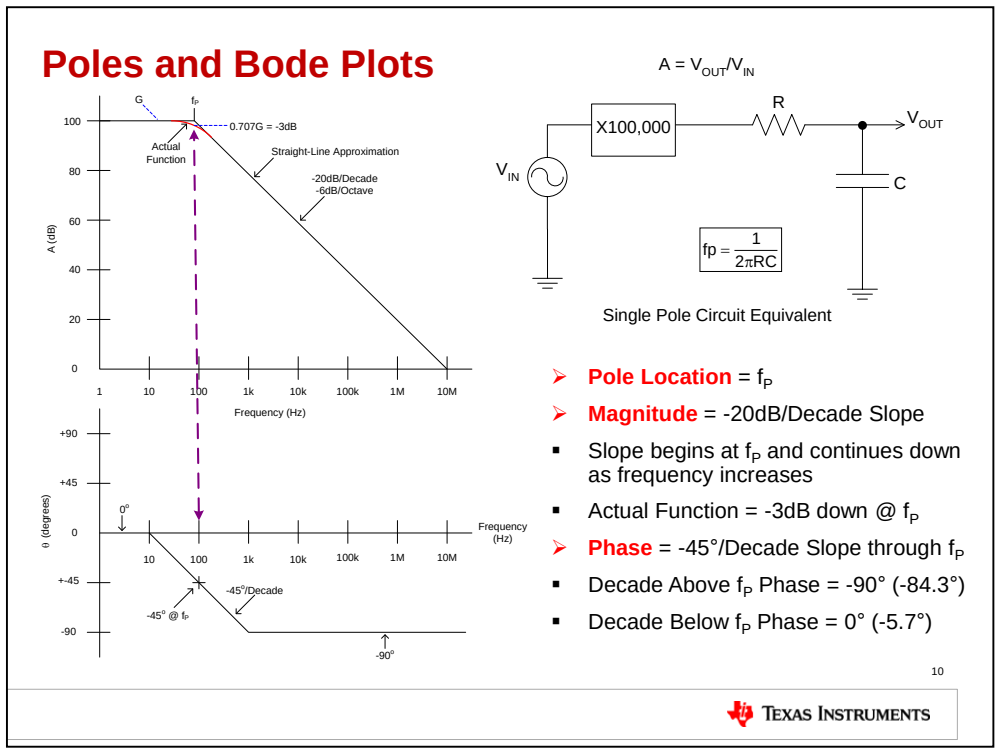
- Gain / Phase Analyzer - Frequency Domain:

  - Peaking, Unexpected Gains, Rapid Phase Shifts

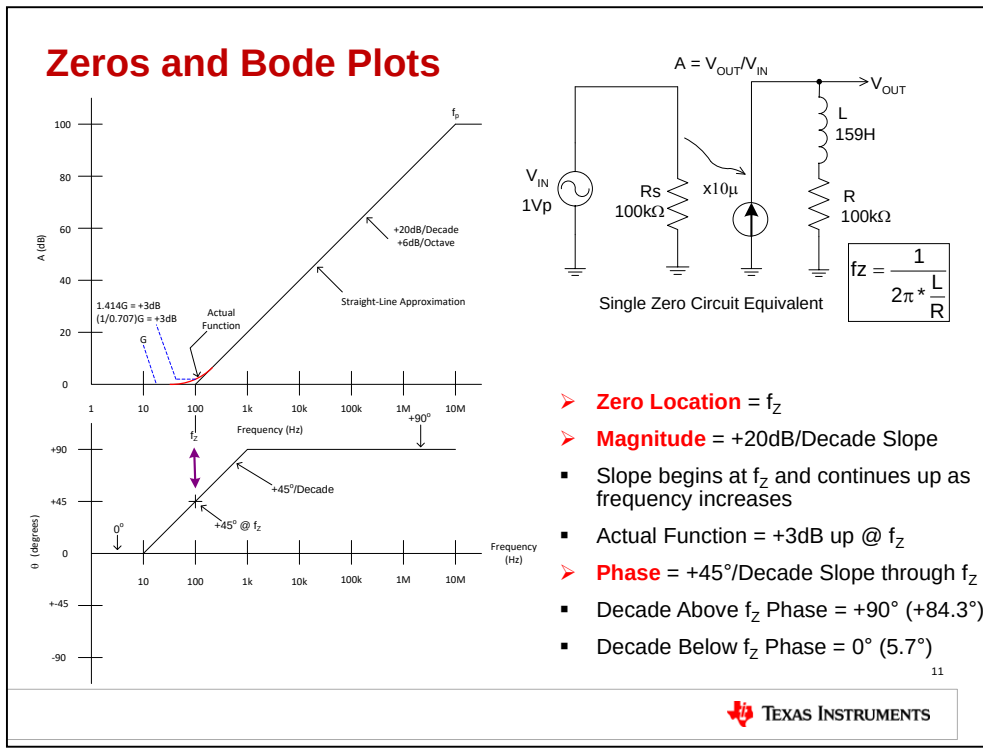


In the frequency domain, a Gain/Phase Analyzer output waveform will have peaking in the magnitude plot and rapid phase shifts in the phase plot, if there are stability issues with the op amp circuit.

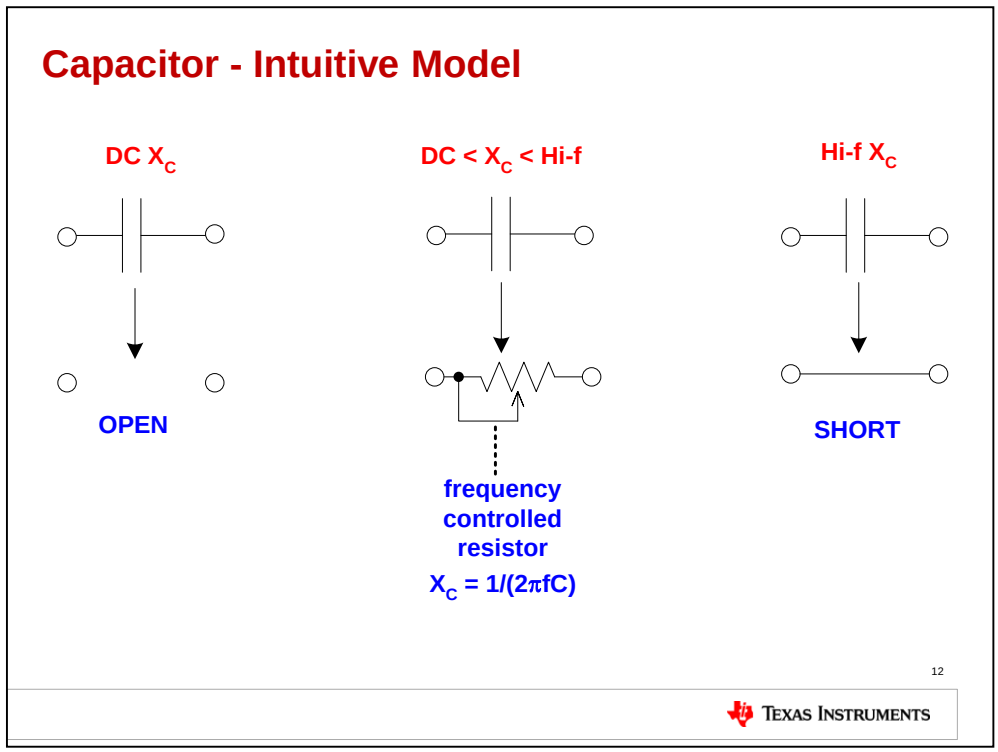
Quick Op-Amp Theory
Bode Plot Review
Basic Stability Tools



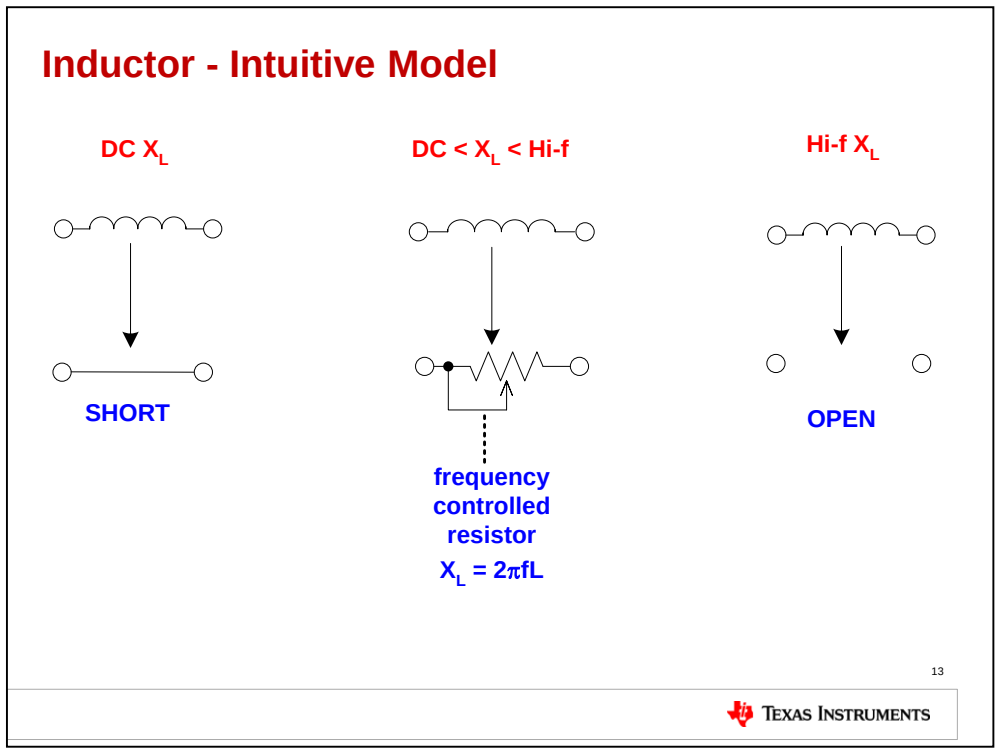
Pole → A single pole response has a -20dB/decade, -6db/octave roll-off in the Bode plot (magnitude or gain plot). At the pole location the gain is reduced by -3dB from the previous flat-band gain. In the phase plot the pole has a -45° phase shift at f_P, the frequency of the pole location. The phase extends on either side of f_P to roughly 0° and -90° at a -45°/decade slope. A single pole may be represented by a simple RC low pass network as shown. Recall that at low frequencies a capacitor is an open and at high frequencies a capacitor is a short. Hence at high frequencies V_{OUT} is shorted to ground and gain goes to zero.



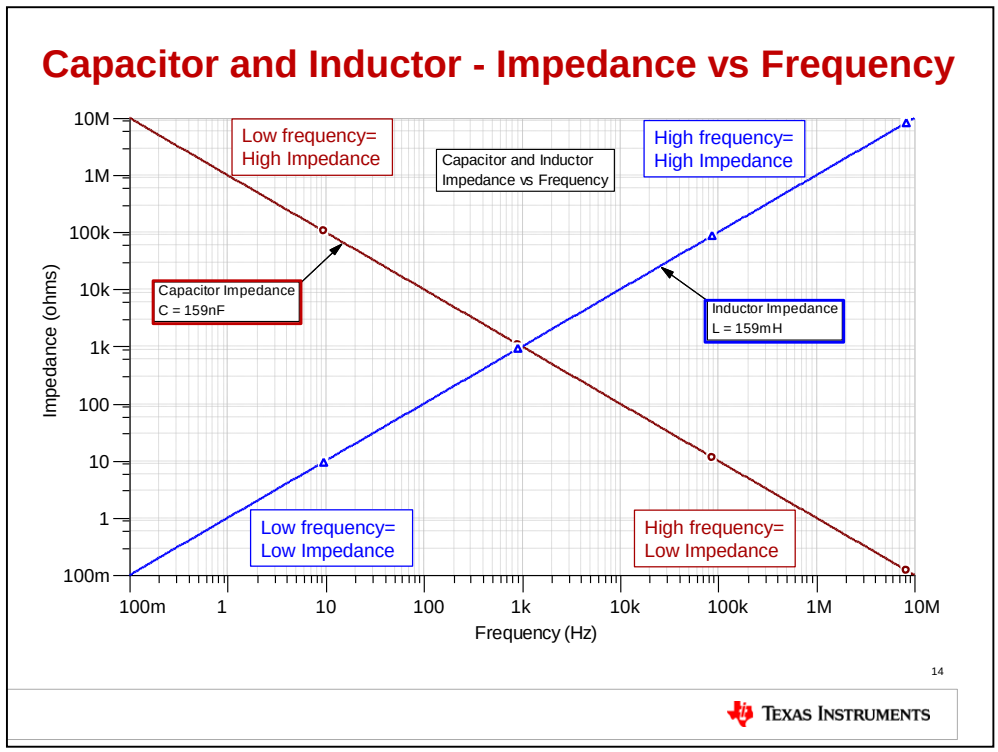
Zero → A single zero response has a +20dB/decade, +6db/octave "roll-on" (opposite of roll-off?) in the Bode plot (magnitude or gain plot). At the zero location the gain is increased by +3dB from the previous flat-band gain. In the phase plot the pole has a +45° phase shift at f_Z, the frequency of the zero location. The phase extends on either side of f_Z to roughly 0° and +90° at a +45°/decade slope. A single zero may be represented by a simple LR high pass network, driven by a current sources, as shown. Recall that at low frequencies an inductor is a short and at high frequencies a inductor is an open, or a very large value of impedance. Hence at low frequencies L is shorted and the current gain of x10uA/V into the R of 100k-ohm yields a gain =1 for V_{OUT}/V_{IN}. As frequency increases the impedance of the inductor increases which will increase the V_{OUT}/V_{IN} gain at a rate of +20dB/decade for the fixed current gain of x10uA/V times the increasing impedance of L as frequency increases.



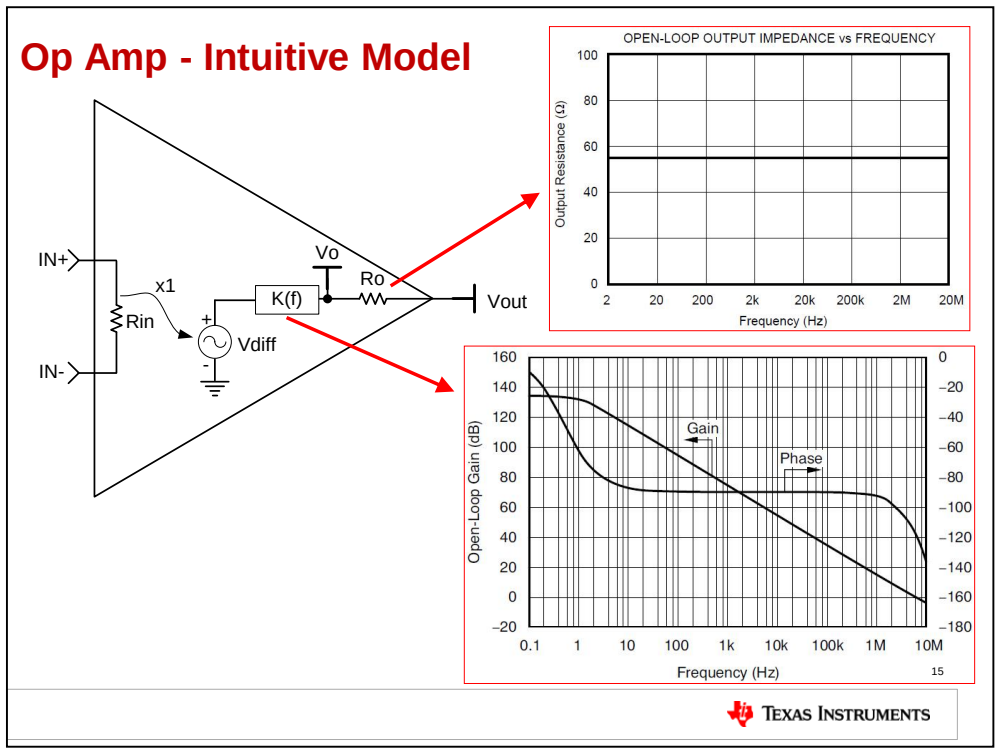
Our Intuitive Capacitive Model for AC Stability Analysis is defined above and contains three distinct operating areas. At “DC” the capacitor will be viewed as an open circuit. At “High Frequency” the capacitor will be viewed as a short circuit. In between the capacitor will be viewed as a frequency controlled resistor with a 1/2πfC decrease in impedance as frequency increases.



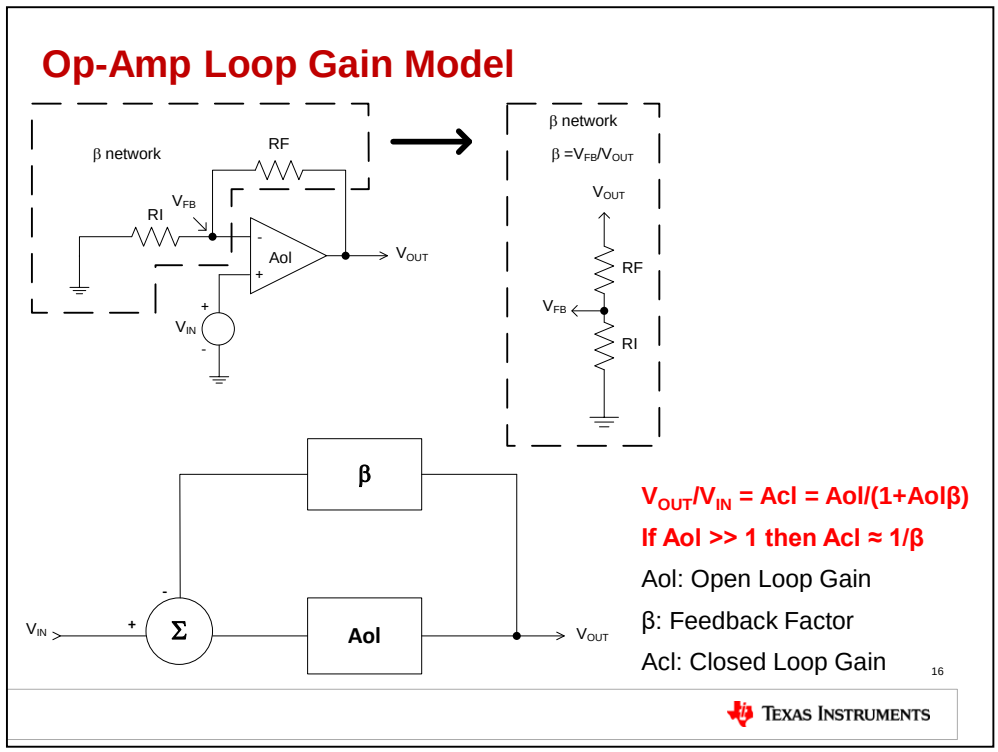
Our Intuitive Inductor Model for AC Stability Analysis is defined above and contains three distinct operating areas. At “DC” the inductor will be viewed as a short circuit. At “High Frequency” the inductor will be viewed as an open circuit. In between the inductor will be viewed as a frequency controlled resistor with a 2πfL increase in impedance as frequency increases.



SPICE simulation confirms the impedance effects for a capacitor as Low Frequency = High Impedance and High Frequency = Low Impedance. Spice simulation also confirms the impedance effects for an inductor as Low Frequency = Low Impedance and High Frequency = High Impedance.



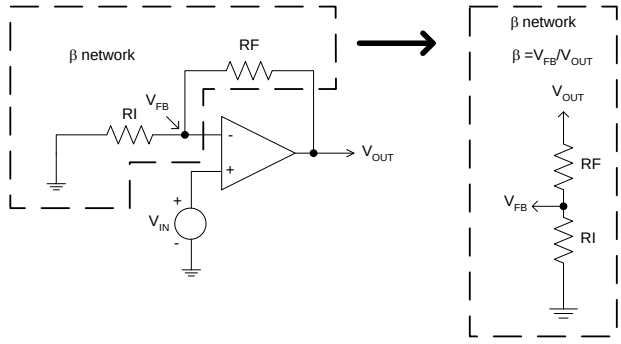
Our Intuitive Op Amp Model for AC Stability Analysis is defined above. The differential voltage between the IN+ and IN- terminals will be amplified by x1 and converted to a single-ended AC Voltage Source, Vdiff. Vdiff is then amplified by K(f). K(f) represents the data sheet Aol Curve (Open Loop Gain vs Frequency Plot). This resultant voltage, Vo, is then followed by the Op Amp Open Loop, AC Small Signal, Output Impedance, Ro. After passing through Ro the voltage, Vo, appears as Vout.



The lower diagram is the traditional control loop model which represents an op amp circuit with feedback. The top diagram depicts the sections of a typical op amp circuit with feedback which correspond to the control loop model. This model of an op amp circuit with feedback we will call the Op Amp Loop Gain Model. Notice that the Aol is the Op Amp data sheet parameter Aol, and is the open loop gain of the op amp. β (Beta) is the amount of output voltage from V_{OUT} which gets fed back as feedback to the op amp -input. The β network in this example is a resistor feedback network.

In the derivation of V_{OUT}/V_{IN} we see that the closed loop gain function is directly defined by Aol and β.

β and 1/β



- β is easy to calculate as feedback network around the Op Amp
- 1/β is reciprocal of β
- Easy Rules-Of-Thumb and Tricks to Plot 1/β on Op Amp Aol Curve
- Plotting Aol Curve and 1/β Curve shows Loop Gain

17

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Before we simulate a circuit in SPICE we will want to know what the approximate outcome will be. Remember GIGO (Garbage In Garbage Out)!!

Beta (β) and its reciprocal 1/Beta (1/β) along with the data sheet Aol Curve will provide a powerful method for first-order approximations of Loop Gain analysis before we run SPICE. Beta (β) is easy to compute and its reciprocal even easier to plot!

Amplifier Stability Criteria

V_{OUT}/V_{IN} = Aol / (1+ Aolβ)
If: Aolβ = -1
Then: V_{OUT}/V_{IN} = Aol / 0 → ∞

If V_{OUT}/V_{IN} = ∞ → Unbounded Gain

Any small changes in V_{IN} will result in large changes in V_{OUT} which will feed back to V_{IN} and result in even larger changes in V_{OUT} → *OSCILLATIONS* → *INSTABILITY !!*

Aolβ: Loop Gain
Aolβ = -1 → Phase shift of ±180°, Magnitude of 1 (0dB)
fcl: frequency where Aolβ = 1 (0dB)

Stability Criteria:
At fcl, where Aolβ = 1 (0dB), Phase Shift < ±180°
Desired Phase Margin (distance from ±180° Phase Shift) ≥ 45°

18

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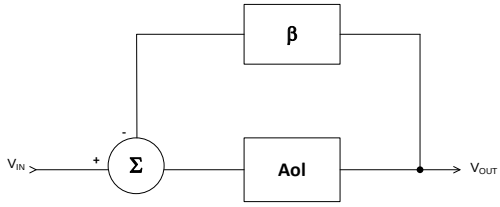
From our Op Amp Loop Gain Model we can derive the criteria for a stable, closed loop, op amp circuit.

At the frequency fcl, where Loop Gain (Aolβ) goes to 1 or 0dB, if the Loop Gain Phase Shift is +/-180°, then we have instability!!

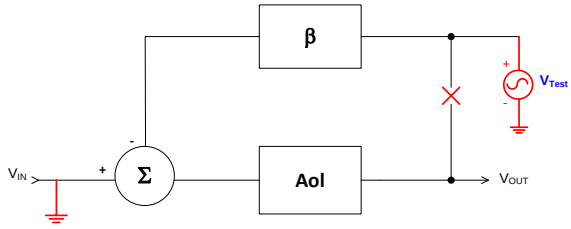
At fcl the distance the Loop Gain Phase Shift is from 180° is called the Loop Gain Phase Margin. Our desired Loop Gain Phase Margin is >45° for an acceptably damped, well-behaved, closed loop response.

Traditional Loop Gain Test



Op Amp Loop Gain Model

Op Amp is “Closed Loop”



Loop Gain Test:

(An Open Loop Test)

Break the Closed Loop at β

Ground V_{IN}

Inject AC Source, V_{Test}, into β

$A_{OL}\beta = V_{OUT}$

19

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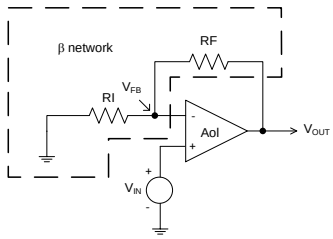
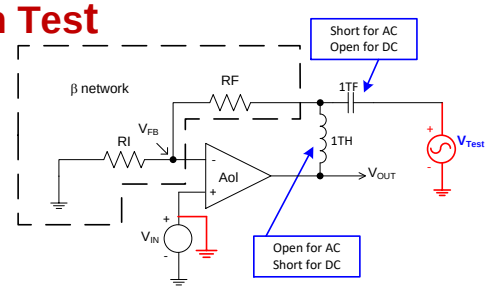
Since stability is defined by the magnitude and phase plot of Loop Gain ($A_{OL}\beta$) then we will need to know how to easily analyze Loop Gain ($A_{OL}\beta$) magnitude and phase. To do this we will break the closed loop op amp circuit and inject a small signal AC source into the loop and measure amplitude and phase to plot the complete loop gain picture. It is key to understand that Loop Gain is an open loop analysis as shown here.

Traditional Loop Gain Test





Op Amp Loop Gain Model

Op Amp is "Closed Loop"

V_{OUT}/V_{IN} = AoI / (1+AoIβ)

SPICE Loop Gain Test:

Op Amp Loop Gain Test is an "Open Loop" Test

SPICE finds a DC Operating Point before it does an AC Analysis so loop must be closed for DC and open for AC.

Break the Closed Loop at V_{OUT}

Ground V_{IN} → source impedance low for AC analysis

Inject: AC Source, V_{Test}, into RF

(Inject: AC Source into High Impedance Node)

Read: AoIβ = Loop Gain = V_{OUT}

(Read: Loop Gain from Low Impedance Node)

20

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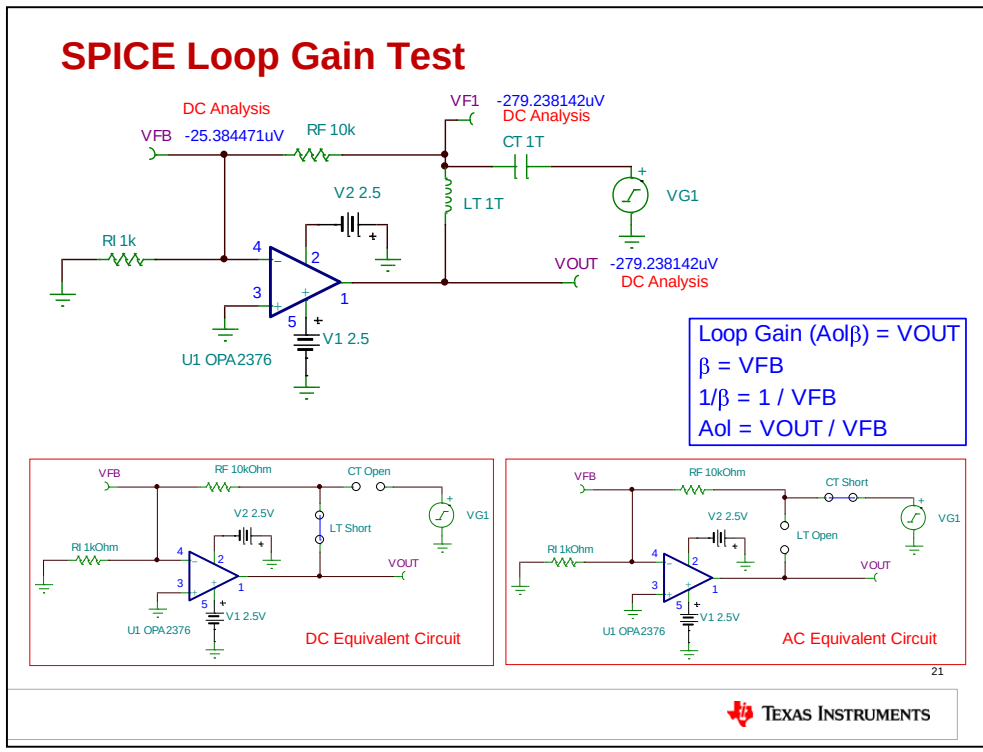
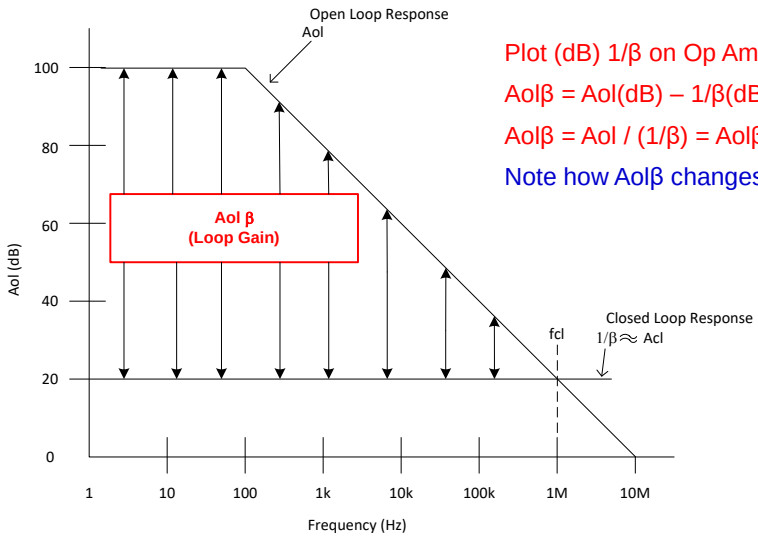
Loop Gain is an Open Loop Gain Test which looks at magnitude and phase around the entire loop starting on one side of where the loop is broken open and ending at the other side where it is broken open. The loop can be broken anywhere but the break shown here will account for both input capacitance effects and the interaction of the op amp open loop output impedance, Zo, with any capacitive loading on the output. When breaking the loop open remember to inject the test signal into the highest impedance side of the break and read out from the lowest impedance side of the break. This makes intuitive sense since you cannot excite a circuit if the source is being shorted out by a low impedance. When analyzing a circuit built in SPICE for simulation the traditional Loop Gain Test breaks the closed loop op amp circuit through the use of an inductor and capacitor. A very large value of inductance ensures the loop is closed at DC (a requirement for SPICE simulation is to be able to calculate a DC Operating Point first before performing an AC Analysis) but open at AC frequencies of interest. A very large value of capacitance ensures that our AC Small Signal Source is not connected at DC but is directly connected at the frequencies of interest.



The SPICE loop gain circuit above is the preferred way to break open the loop for loop gain analysis for most applications. It will account for both input capacitance and any open loop output impedance, Zo, interactions with capacitive output loading. The DC Equivalent Circuit shows that the loop will be closed by the inductor, LT, being a short at DC and the capacitor, CT, being an open so our test generator, VG1, will not be connected. SPICE must find a DC operating point as a requirement before any AC Analysis will run. It is important to check the DC Operating point before running an AC Analysis. If an op amp output is saturated for example SPICE will use this condition to build its AC Equivalent Models and they will not be correct since the op amp will have a different AC Equivalent Model in saturation than in normal linear operation. AC Analysis is only valid when the op amp is in a linear operating condition. The AC Equivalent Circuit shows what SPICE will use during its AC Analysis. For all frequencies of interest the capacitor CT is a short and our test generator, VG1, injects the signal into the open loop since for all frequencies of interest the inductor, LT, is an open.

Loop Gain (Aolβ) from Aol and 1/β



Plot (dB) 1/β on Op Amp Aol (dB)

Aolβ = Aol(dB) – 1/β(dB)

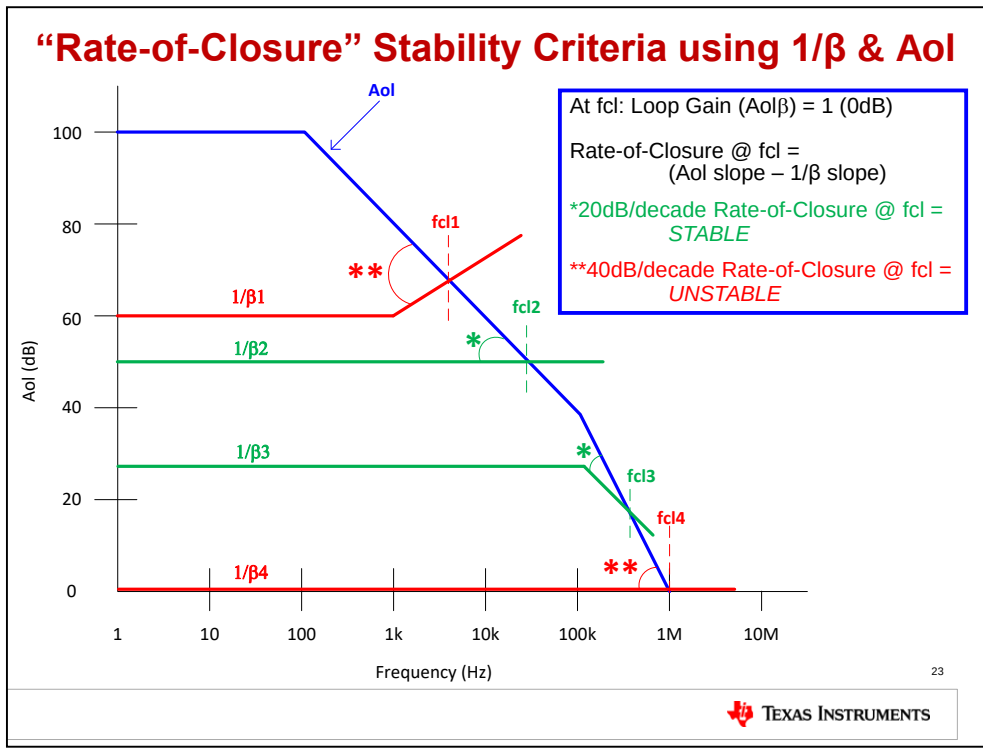
Aolβ = Aol / (1/β) = Aolβ

Note how Aolβ changes with frequency

22

TEXAS INSTRUMENTS

The 1/β plot plotted on the Aol curve will provide a clear picture of exactly what the Loop Gain (Aolβ) plot is. From our derivation above we clearly see that the Aolβ magnitude plot is simply the difference between Aol and 1/β when we plot 1/β in dB on an Aol curve. Note that as frequency increases Aolβ decreases. Aolβ is the gain left to correct for errors in the V_{OUT}/V_{IN} or Closed Loop response. So as Aolβ decreases the V_{OUT}/V_{IN} response will become less accurate until the point where Aolβ goes to 0dB where from then on the V_{OUT}/V_{IN} response will simply follow the Aol curve.



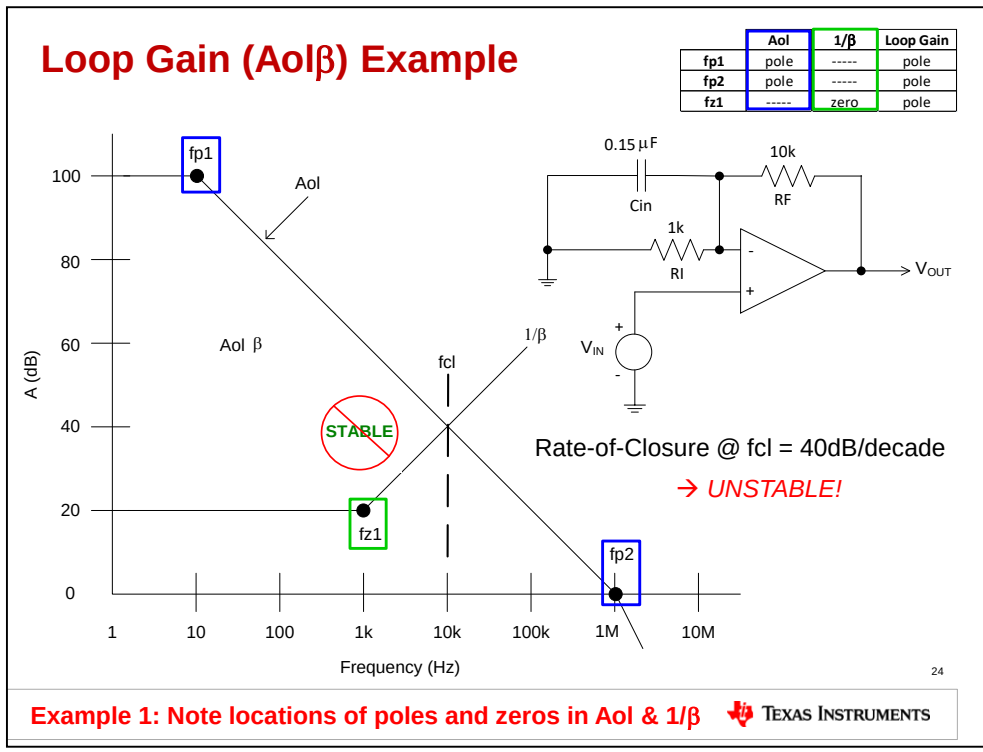
Once we plot 1/β on the Aol curve there is an easy first-order check for stability called Rate-Of-Closure. This Rate-Of-Closure stability check is defined as the "rate of closure" of the 1/β curve with the Aol curve at fcl, where loop gain goes to 0dB. A 40db/decade rate-of-closure implies an UNSTABLE circuit and a 20dB/decade rate-of-closure implies a STABLE circuit. The 40dB/decade rate-of-closure implies instability because it implies two poles in the Aolβ plot before fcl which can mean a 180 phase shift. Four examples are shown above with their respective rate-of-closure computed below.

fcl1: Aol-1/β1 = -20dB/decade - +20dB/decade = -40dB/decade → 40dB/decade rate-of-closure & UNSTABLE

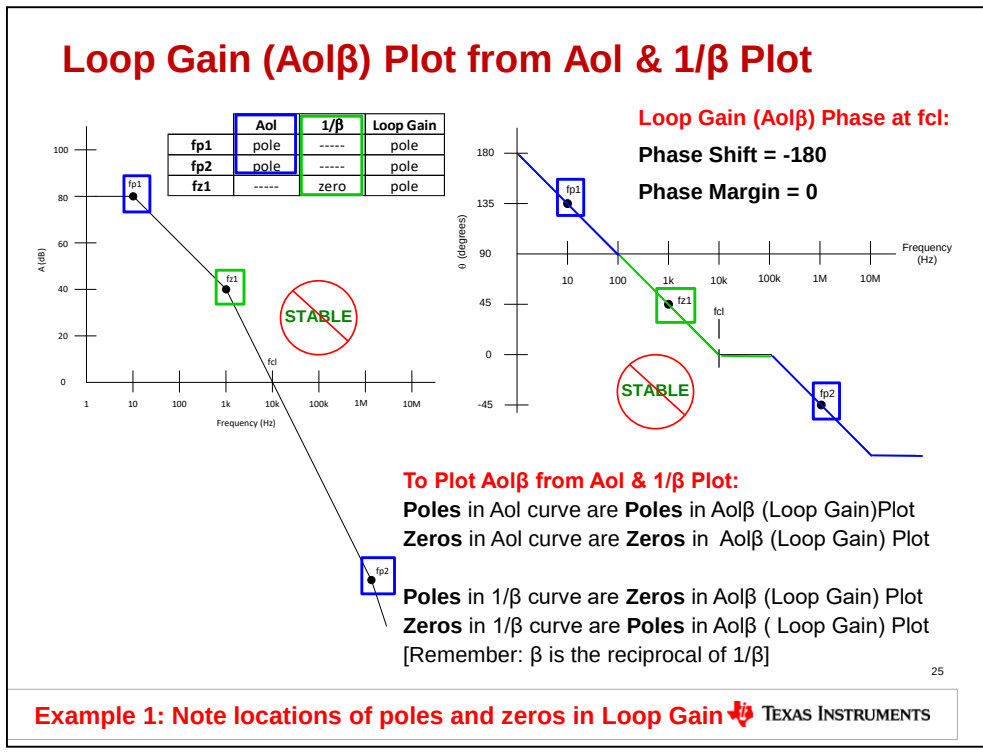
fcl2: Aol-1/β2 = -20dB/decade - 0dB/decade = -20dB/decade → 20dB/decade rate-of-closure & STABLE

fcl3: Aol-1/β3 = -40dB/decade – (-20dB/decade) = -20dB/decade → 20dB/decade rate-of-closure & STABLE

fcl4: Aol-1/β4 = -40dB/decade - 0dB/decade = -40dB/decade → 40dB/decade rate-of-closure & UNSTABLE



A loop gain analysis example serves to relate how we can analyze the stability of an op amp circuit from the 1/β curve plotted on the Aol curve. Here as frequency increases the capacitor Cin goes towards a short in impedance thereby lowering the magnitude of the β plot with frequency (less voltage feedback as frequency increases) and respectively raising the 1/β curve as frequency increases. From our rate-of-closure criteria we predict an UNSTABLE circuit. Note the locations of poles, fp1 and fp2, in the Aol curve and the zero, fz1, in the 1/β plot.



From our 1/β plot on the Aol curve we can plot the Aolβ (Loop Gain) magnitude plot. From the Aolβ (Loop Gain) magnitude plot we can then plot the Aolβ (Loop Gain) phase plot. The rules to create an Aolβ (Loop Gain) plot from the 1/β plot on the Aol curve are simple: Poles and zeros from the Aol curve are poles and zeros in the Aolβ (Loop Gain) plot. Poles and zeros from the 1/β plot are opposite in the Aolβ (Loop Gain) plot. One easy way to remember this is β is used in the Aolβ (Loop Gain) plot and 1/β is the reciprocal of β and so we would expect the Aolβ (Loop Gain) curve to use the reciprocal of poles and zeros from the 1/β plot. Reciprocal of a pole is a zero and reciprocal of a zero is a pole.

Phase shift at fcl (Θcl) can be seen to be -180° which is UNSTABLE. Mathematically the complete Phase Shift is calculated as:

$\Theta cl = -\tan^{-1}(fcl/fp1) - \tan^{-1}(fcl/fz1) - \tan^{-1}(fcl/fp2)$

$\Theta cl = -\tan^{-1}(10k/10) - \tan^{-1}(10k/1k) - \tan^{-1}(10k/1M)$

Θcl = -89.94° -84.29°-0.57°

Θcl = -174.8°

Note that in the Aolβ (Loop Gain) plot there are all poles (fp1, fz1, fp2)

First order approximation errors for magnitude plots:

Actual Pole is -3dB down from ideal at fp

Actual Zero is +3dB up from ideal at fz

First order approximation errors for phase plots:

Actual Pole Phase is 6° lower than 0° a decade less than fp

Actual Pole Phase is 6° higher than -90° a decade more than fp

Actual Zero Phase is 6° higher than 0° a decade less than fz

Actual Pole Phase is 6° lower than +90° a decade more than fz

Phase margin is a definition used to describe how close closed loop op amp configuration is to oscillation (how far away from 180° Θcl is) . A positive phase margin is an indication of stability. A phase margin of about 45° is desirable for maximum response to a pulse input without ringing or instability.

Θpm (phase margin) = 180 + Θcl

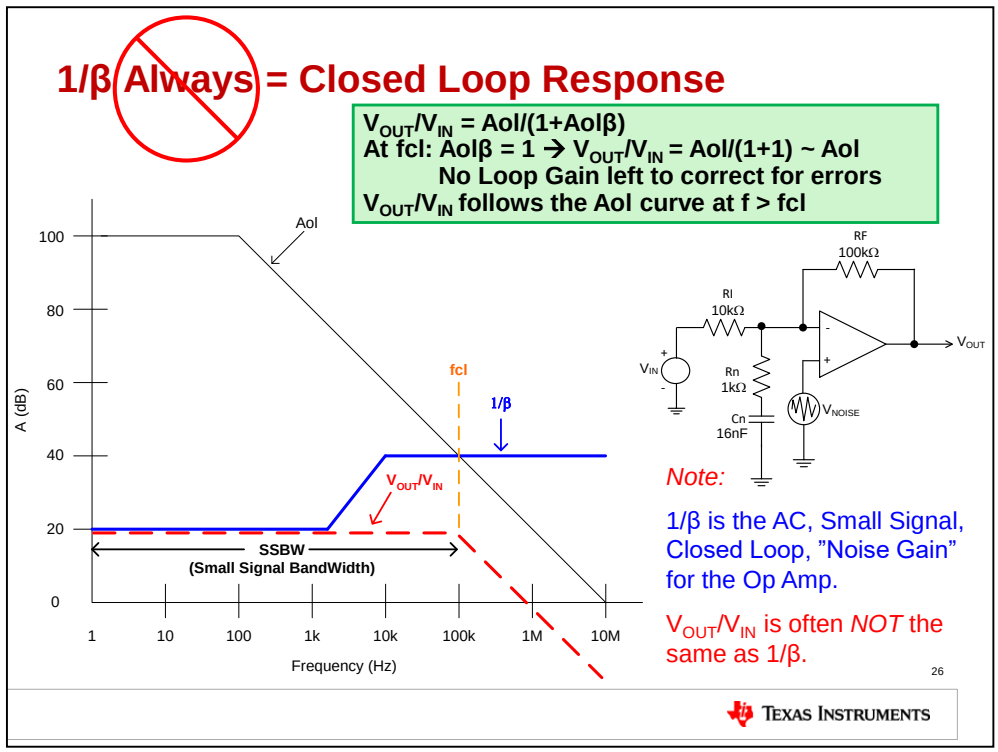
First Order Approximation Phase Margin:

Θpm (phase margin) = 180° + Θcl

Θpm = 180° + (-180°) = 0°

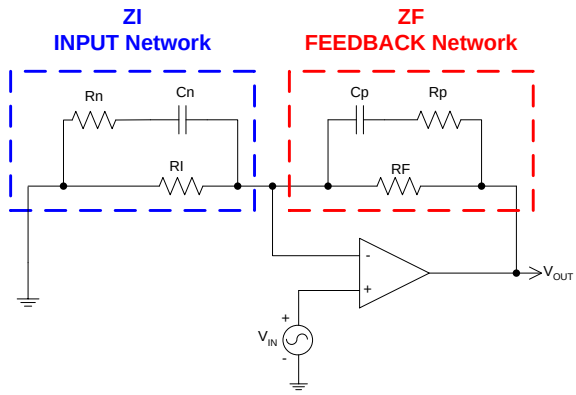
Actual Phase Margin:

Θpm (phase margin) = 180° + Θcl
Θpm = 180° + (-174.8°) = 5.2°



The V_{OUT}/V_{IN} closed loop response is not always the same as 1/β. In the example above we see that the AC small signal feedback is modified by the Rn-Cn network in parallel with RI. As frequency increases we see the results of this network reflected in the 1/β plot on the Aol curve. Think of this example as an inverting summing op amp circuit. We are summing in V_{IN} through RI and Ground through the Rn-Cn netowrk. V_{OUT}/V_{IN} will not be affected by this Rn-Cn network at low frequencies and the desired gain is seen as 20dB. As Loop Gain (Aolβ) is forced to 1 (0dB) by the Rn-Cn network there is no Loop Gain (Aolβ) left to correct for errors and V_{OUT}/V_{IN} will follow the Aol curve at frequencies above fcl. In this example the closed loop gain is inverting but the 1/β will reflect a non-inverting gain equivalent number at DC. One way to view this is that the 1/β gain is the "noise gain" and a noise source could appear on the +input of the op amp. In essence the op amp always runs in its "noise gain" for loop stability considerations.

How to Modify 1/β for Stable Circuits

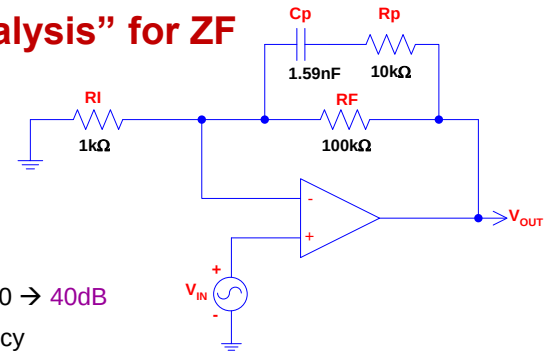


27

Texas Instruments

Two common op amp networks, ZI and ZF are shown above. We will perform a 1st Order Analysis on each of these networks independently and then use Tina SPICE to simulate the op amp circuit and check if our predicted results agree! The key to our 1st Order Analysis will be to use our Intuitive Component Models (capacitor and inductor) from earlier in this presentation and a little intuition.

1/β "First Order Analysis" for ZF



- 1/β Low Frequency = RF/RI = 100 → 40dB
  Cp = Open at Low Frequency
- 1/β High Frequency = (Rp//RF)/RI ≈ Rp/RI = 10 → 20dB
  Cp = Short at High Frequency
- Pole in 1/β when Magnitude of X_{Cp} = RF
  Magnitude X_{Cp} = 1/(2·π·f·Cp)
  fp = 1/(2·π·RF·Cp) = 1kHz
- Zero in 1/β when Magnitude of X_{Cp} = Rp
  fz = 1/(2·π·Rp·Cp) = 10kHz

ZF Exact equations :

$$fp = \frac{1}{2\pi * Cp * (RF + Rp)}$$

$$fz = \frac{1}{2\pi * Cp * [Rp + (RI // RF)]}$$

28

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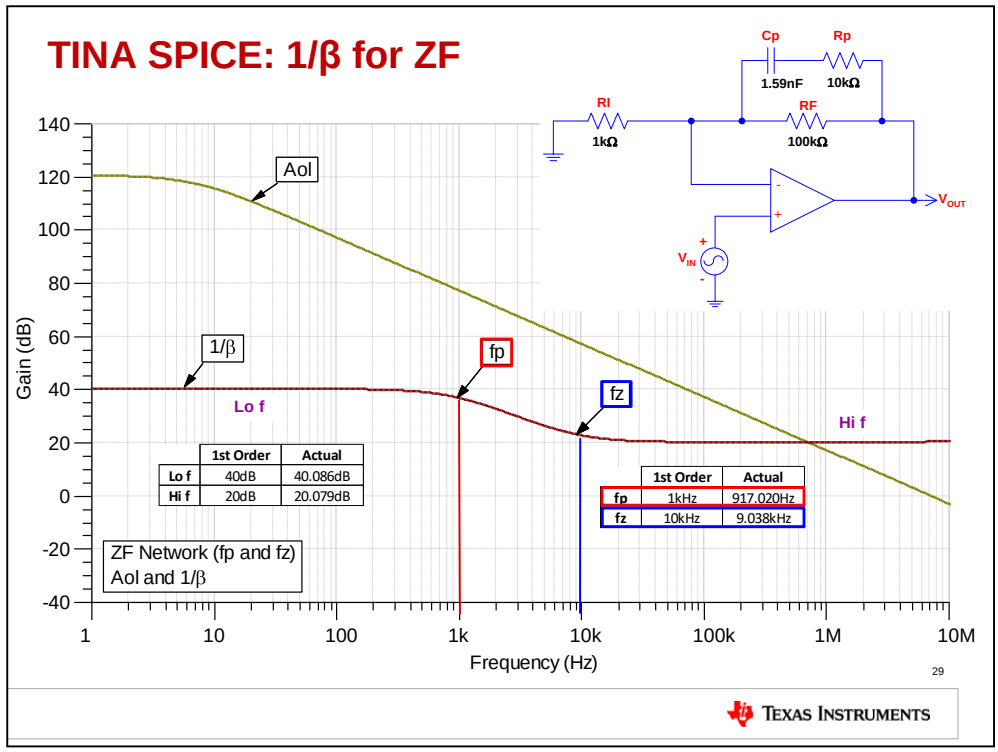
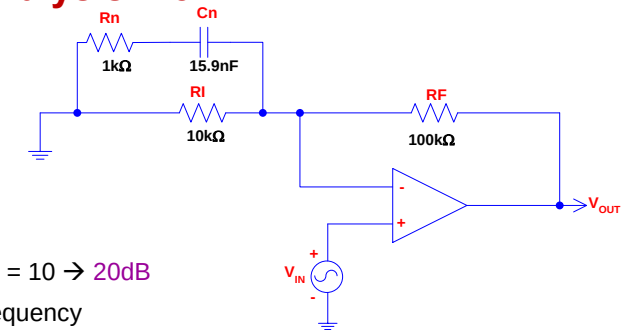
Let's perform our 1st Order Analysis for the ZF network above. This is a feedback network in the op amp circuit. Cp is open at low frequency and the Low Frequency 1/β becomes simply RF/RI as shown. At the other frequency extreme, high frequency, Cp is a short and the High Frequency 1/β becomes (Rp//RF)/RI. However, when Cp is a short Rp<<RF and Rp should dominate the feedback resistance and so we approximate high frequency gain to be Rp/RI. We note there is a reactive element in the feedback path of the op amp, a capacitor, and therefore know there has to be some poles and/or zeros somewhere in the transfer function. At the frequency where the magnitude of Cp matches that of the parallel impedance with it (dominated here by RF) we anticipate a pole in the 1/β plot. Feedback resistance will be getting smaller and therefore V_{OUT} must start to reduce. Now the frequency where the magnitude of Cp matches that of the impedance in series with it, Rp, we expect a zero since as Cp approaches a short the net feedback resistance can become no smaller and V_{OUT} must flatten out as frequency increases. So we have predicted by our 1st order analysis where a pole and zero exists as well as the Low Frequency and High Frequency 1/β levels.



Our optimally scaled Tina SPICE simulation results are displayed above. Our First Order analysis results are shown along with the actual measured results. Our 1st Order Analysis results and predictions are not exact but certainly more than acceptable for a powerful and intuitive analysis for the 1/β curve for AC Stability Analysis.

1/β "First Order Analysis" for ZI



- 1/β Low Frequency = RF/RI = 10 → 20dB
  Cn = Open at Low Frequency
- 1/β High Frequency = RF/(RI//Rn) ≈ RF/Rn =100 → 40dB
  Cn = Short at High Frequency
- Zero in 1/β when Magnitude of X_{Cn} = RI
  Magnitude X_{Cn} = 1/(2·π·f·Cn)
  fz = 1/(2·π·RI·Cn) = 1kHz
- Pole in 1/β when Magnitude of X_{Cn} = Rn
  fp = 1/(2·π·Rn·Cn) = 10kHz

ZI Exact equations :

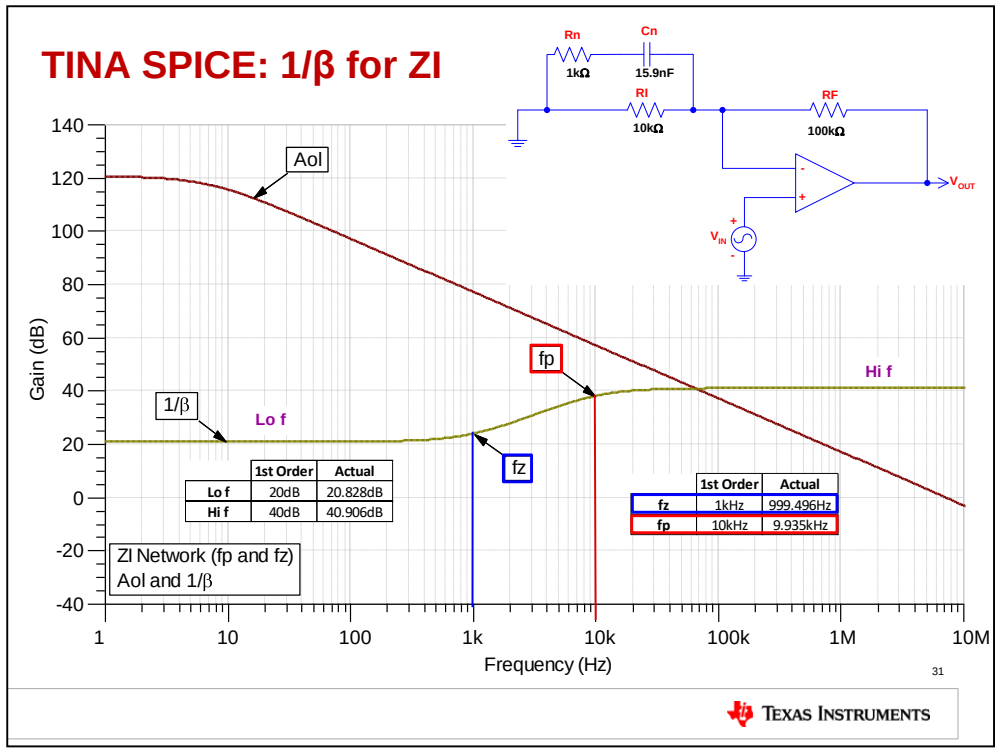
$$fp = \frac{1}{2\pi RnCn}$$

$$fz = \frac{1}{2\pi Cn * [Rn + (RI // RF)]}$$

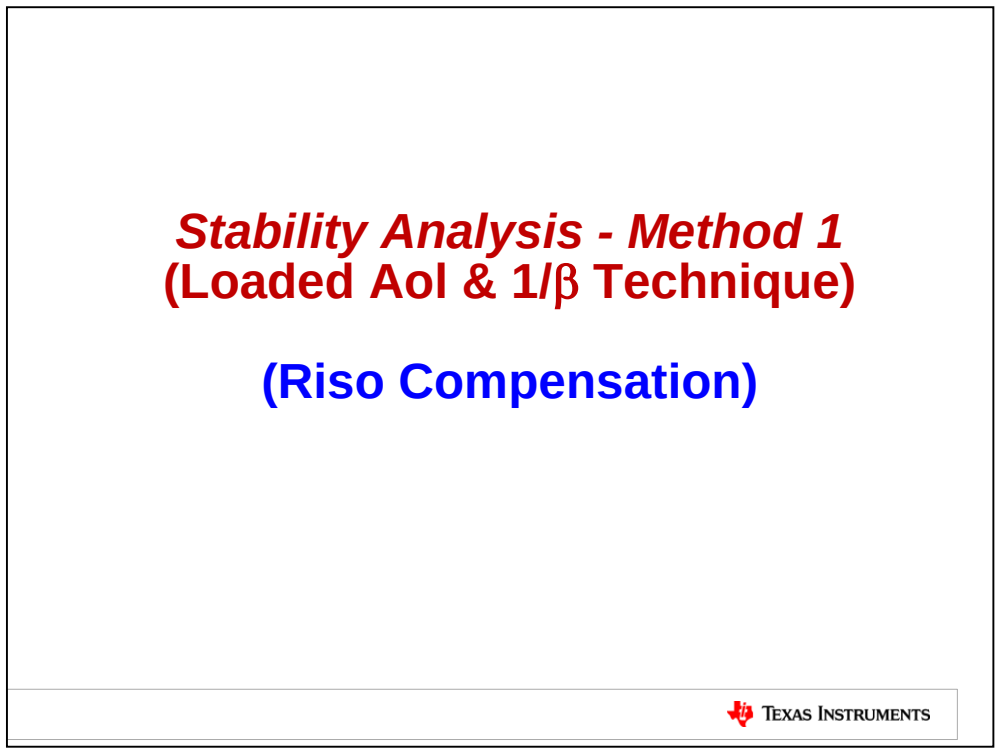
30

Texas Instruments

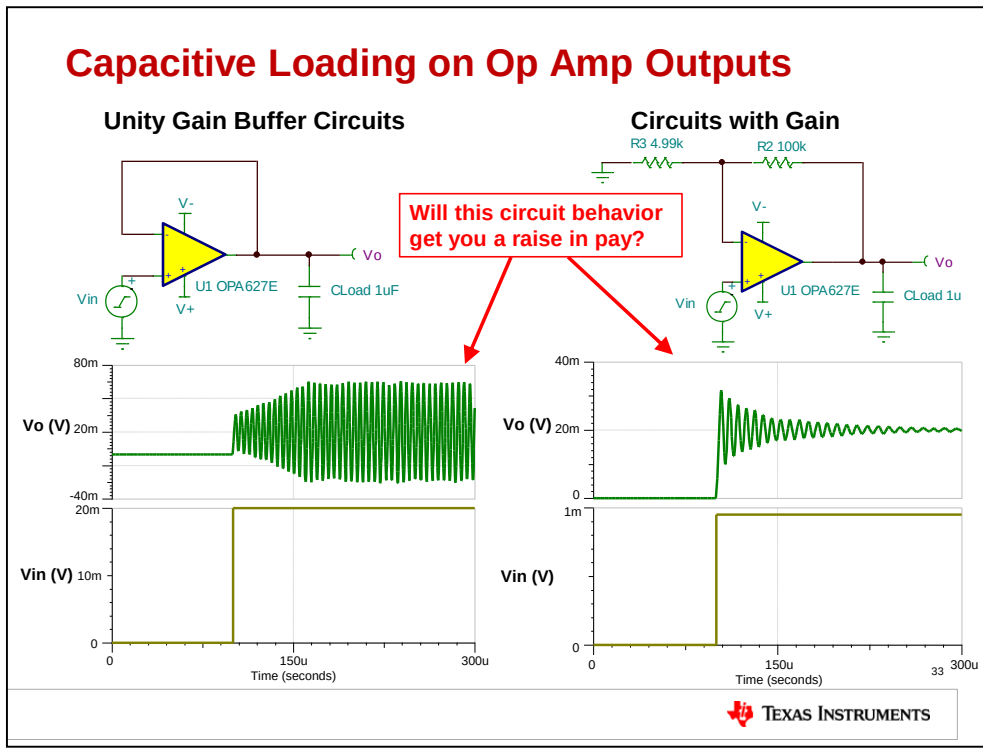
Let's perform our 1st Order Analysis for the ZI network above. This is an input network in the op amp circuit. Cn is open at low frequency and the Low Frequency 1/β becomes simply RF/RI as shown. At the other frequency extreme, high frequency, Cn is a short and the High Frequency 1/β becomes RF/(RI//Rn). However, when Cp is a short Rn<<RI and Rn should dominate the input resistance and so we approximate high frequency gain to be RF/Rn. We note there is a reactive element in the input path of the op amp, a capacitor, and therefore know there has to be some poles and/or zeros somewhere in the transfer function. At the frequency where the magnitude of Cn matches that of the parallel impedance with it (dominated here by RI) we anticipate a zero in the 1/β plot. Input resistance will be getting smaller and therefore V_{OUT} must start to increase. Now the frequency where the magnitude of Cn matches that of the impedance in series with it, Rn, we expect a pole since as Cn approaches a short the net input resistance can become no smaller and V_{OUT} must flatten out as frequency increases. So we have predicted by our 1st order analysis where a pole and zero exists as well as the Low Frequency and High Frequency 1/β levels.



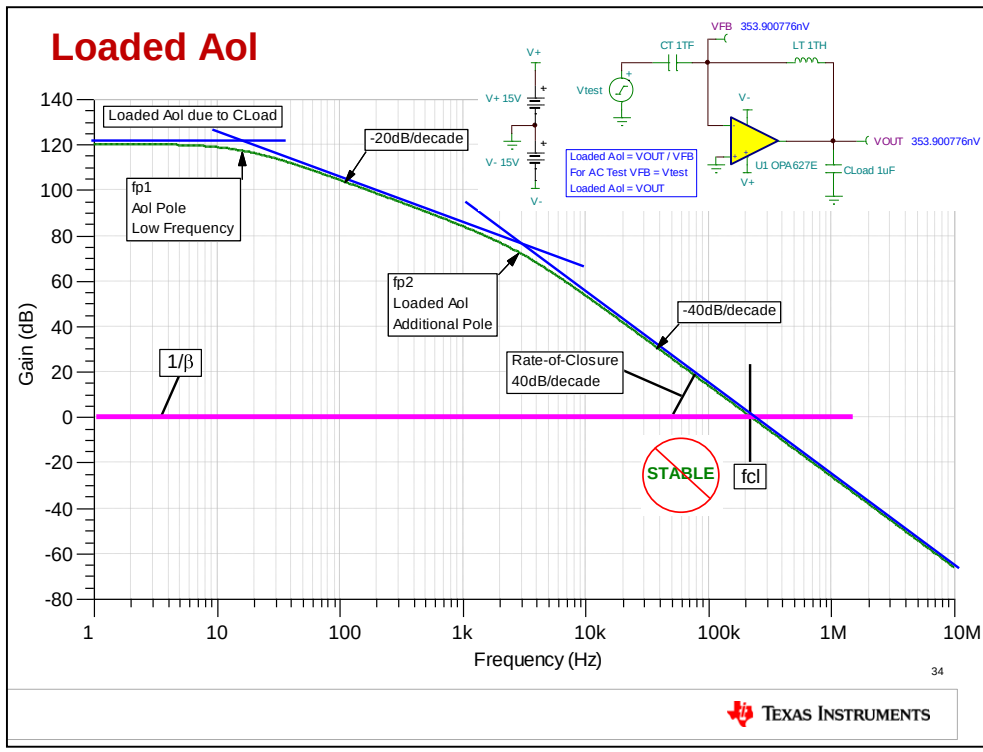
Our optimally scaled Tina SPICE simulation results are displayed above. Our First Order analysis results are shown along with the actual measured results. Our 1st Order Analysis results and predictions are not exact but certainly more than acceptable for a powerful and intuitive analysis for the 1/β curve for AC Stability Analysis.



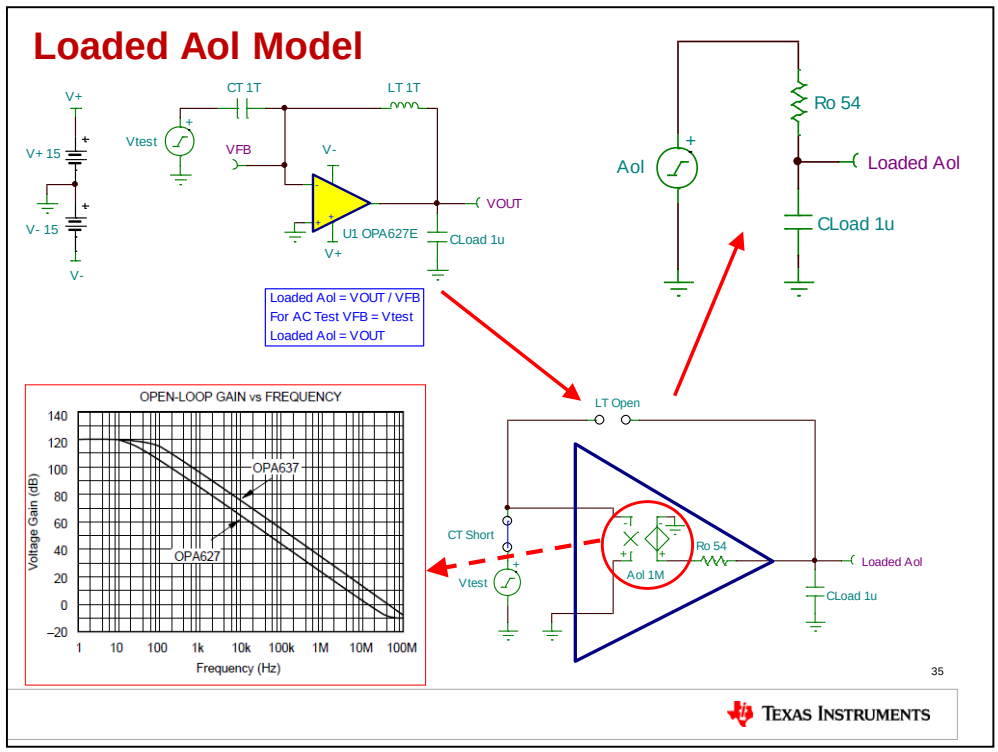
There are two basic methods for analyzing op amp stability problems. The first method, Method 1, will use the Loaded Aol and 1/β Technique to analyze stability problems due to capacitive loading of an op amp output. The compensation used for this example will be Riso Compensation.



Capacitive loading on op amp outputs without proper stability considerations can lead to undesired oscillations on the op amp outputs as shown here. The worst case will be for a unity gain buffer as shown on the left, since phase margin will be lowest for this configuration. On the right is the transient response for a higher gain circuit with the same op amp and same capacitive load, with less oscillation, since phase margin is increased as closed loop gain is increased. Higher closed loop gain will also result in a decrease in closed loop bandwidth as well.

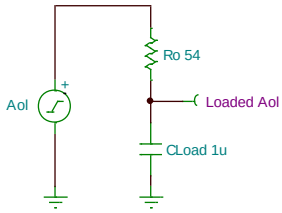


A loop gain analysis circuit can be used to analyze the “Loaded Aol” due to CLoad. As shown here the “Loaded Aol” curve due to CLoad,1uF, has an additional pole in it around 3kHz, fp2. fp1 is the original pole in the Aol curve of the op amp before CLoad is applied. Since the circuit is running as a unity gain follower 1/β is 0dB and at fcl, where 1/β intersects the Loaded Aol curve, we see a 40dB/decade rate-of-closure, which is UNSTABLE by our rate-of-closure criteria.



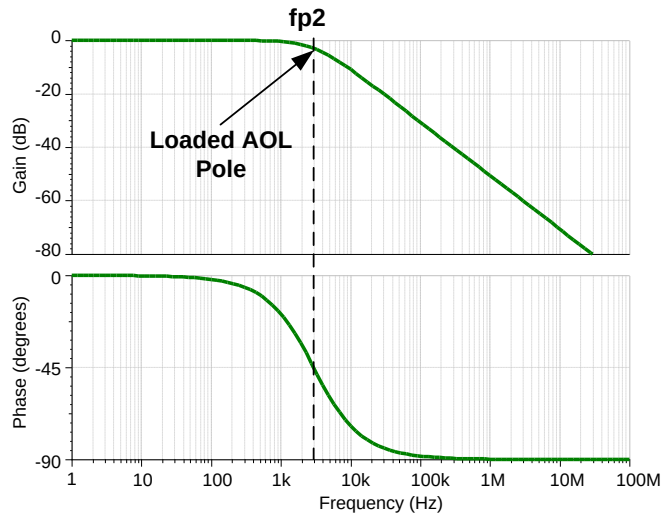
Our stability analysis of the effects of capacitive loading on an op amp will be simplified by the introduction of the “Loaded Aol Model”. As shown in this slide the data sheet Aol curve is followed by the op amp output resistance, Ro. The capacitive load, CLoad, in conjunction with Ro will form an additional pole in the Aol plot and may be represented by a new “Loaded Aol” plot. The Ro-CLoad network form the “Aol Load” on the original op amp “Aol”.

Loaded Aol Model



Loaded Aol Pole Equation

$$fp2 = \frac{1}{2 * \pi * Ro * CLoad}$$



36

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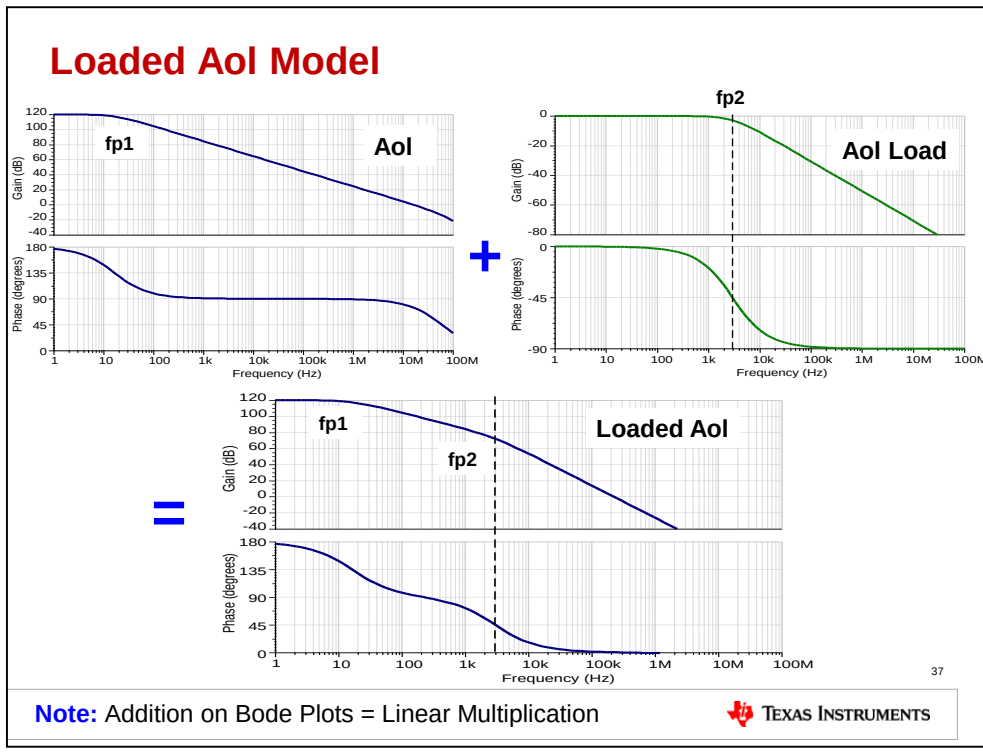
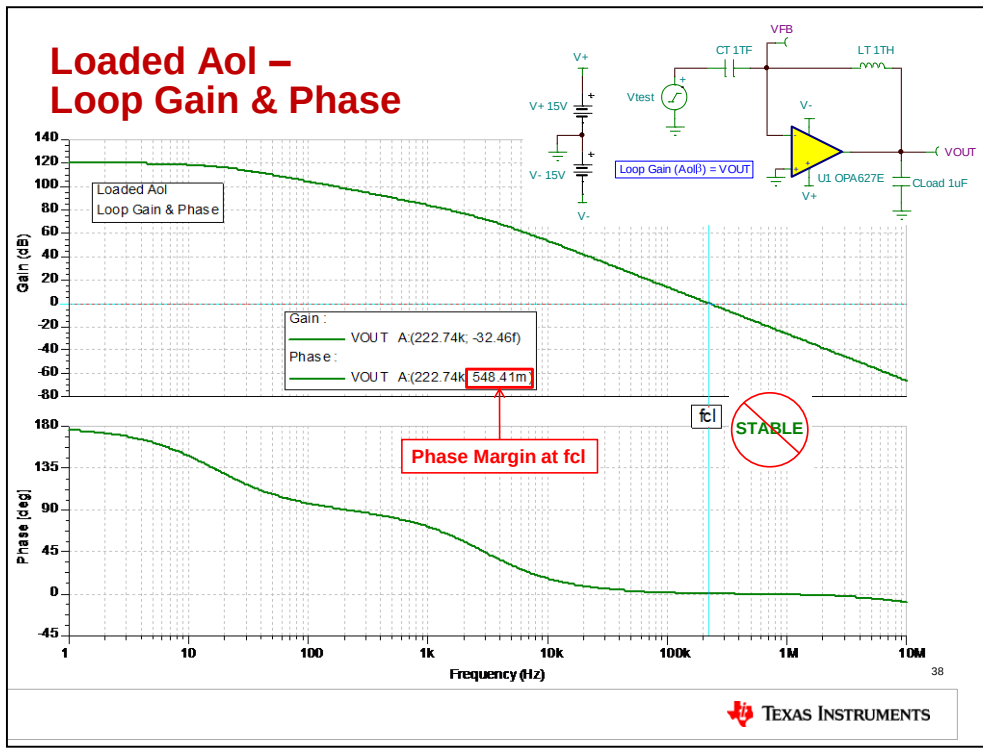
The data sheet Aol is loaded by the Ro-CLoad load network as shown here. The additional pole, fp2, due to Ro and CLoad is computed here.



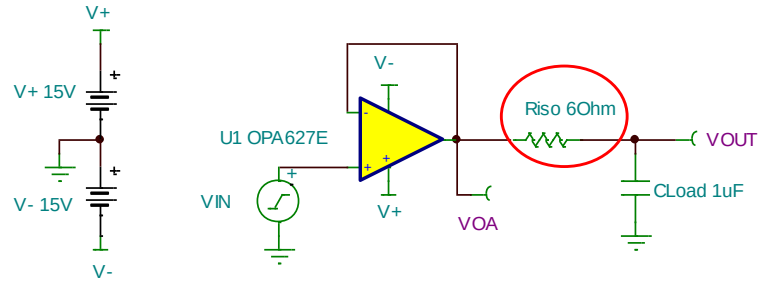
The op amp original “Aol” is “multiplied” by the “Aol Load” to yield the resultant “Loaded Aol” curve. On dB plots linear multiplication is performed by adding the curves in dB. As shown above it becomes easy to see the resultant “Loaded Aol” by adding the op amp original “Aol” plus the “Aol Load” formed by Ro-CLoad.



The Loaded AoI caused by CLoad, 1uF, will result in Loop Gain phase margin at fcl of only 0.548 degrees. This is definitely an UNSTABLE circuit as it stands here.

Riso Compensation

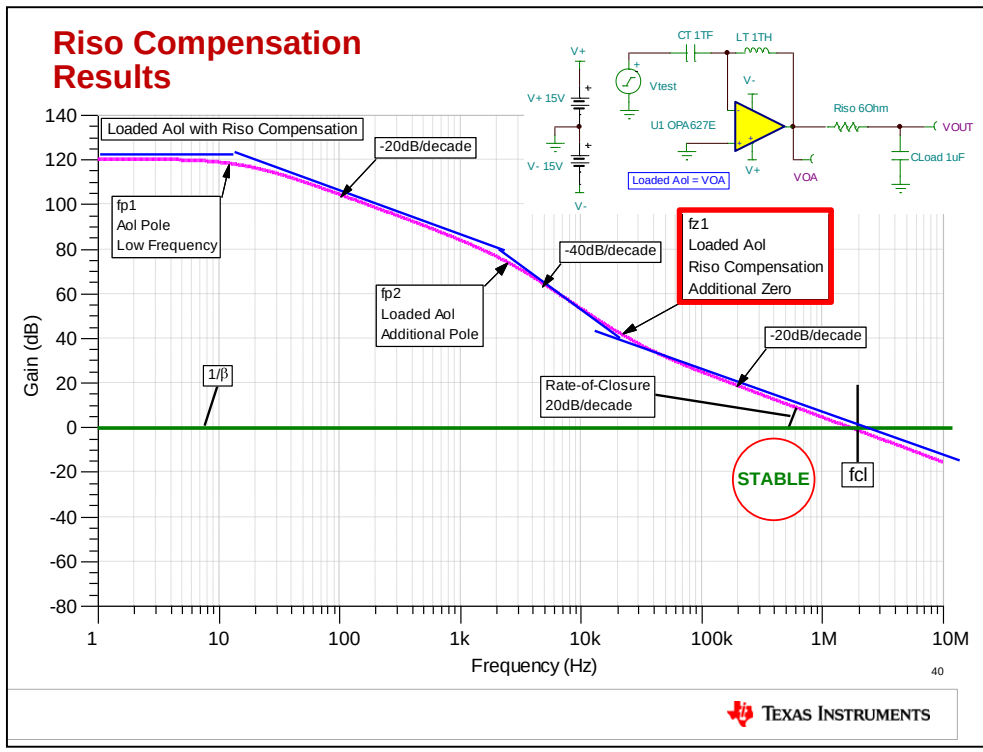
Riso will add a zero in the Loaded Aol Curve



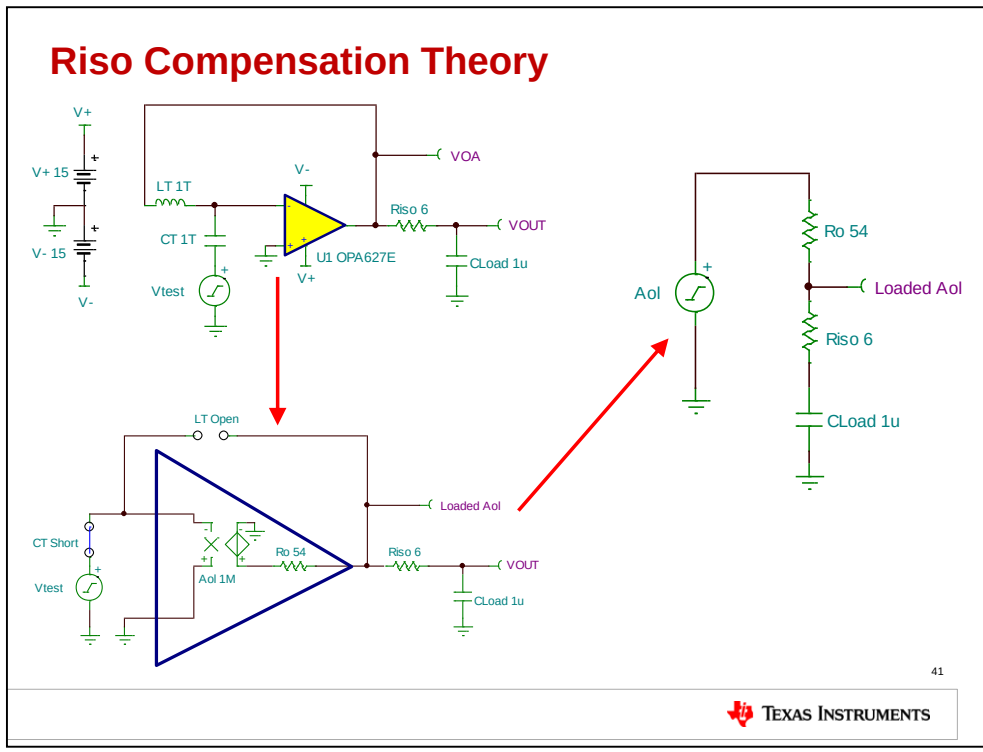
39

TEXAS INSTRUMENTS

One way to compensate the op amp circuit for CLoad is to add Riso Compensation. Note the point of feedback for the circuit is still taken directly at the output of the op amp. The addition of Riso will add a zero into the “Loaded Aol” curve and stabilize the circuit.

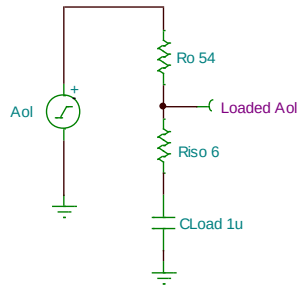


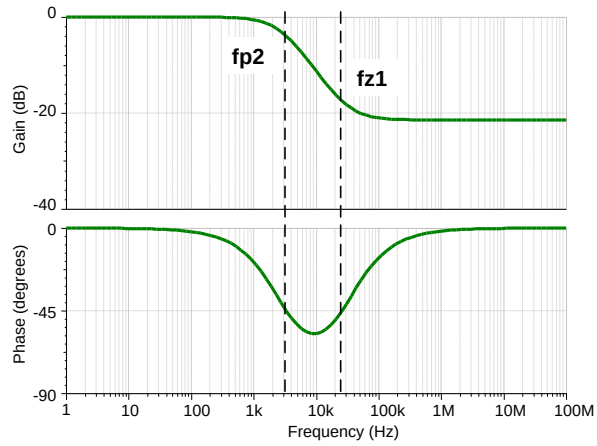
The Riso Compensation will add fz1 into the “Loaded Aol” which will result in a -20dB/decade slope crossing 0db at fcl. This will result in a stable circuit by our rate-of-closure criteria of 20dB/decade indicating stability.



Our stability analysis using the “Loaded Aol Model” will be analyzed for the addition of the Riso Compensation. The data sheet Aol curve is followed by the op amp output resistance, Ro, Riso Compensation, Riso, and load capacitance, CLoad. Note the point of feedback is between Ro and Riso. The capacitive load, CLoad, in conjunction with Ro and Riso will form an additional pole in the Loaded Aol plot. The capacitive load, CLoad, in conjunction with Riso will add a zero in the Loaded Aol plot.

Riso Compensation Theory





Transfer Function

$$\text{Loaded Aol}(s) = \frac{1 + \text{CLoad} * \text{Riso} * s}{1 + (\text{Ro} + \text{Riso}) * \text{CLoad} * s}$$

Pole :

$$fp2 = \frac{1}{2\pi(\text{Ro} + \text{Riso}) * \text{CLoad}}$$

Zero :

$$fz1 = \frac{1}{2\pi * \text{Riso} * \text{CLoad}}$$

42

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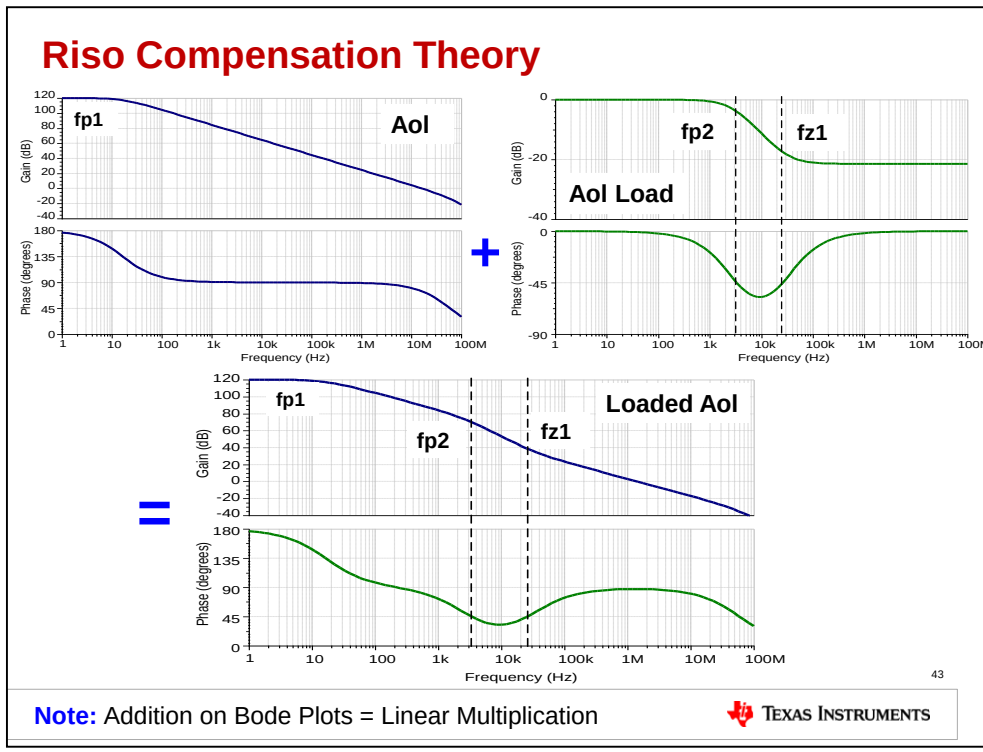
The data sheet Aol is loaded by the Ro-Riso-CLoad load network as shown here. The additional pole, fp2, due to Ro + Riso and CLoad is computed here. Also we see a zero, fz1, formed by Riso and Cload.



The op amp original “Aol” is “multiplied” by the “Aol Load” with Riso Compensation to yield the resultant “Loaded Aol” curve. On dB plots linear multiplication is performed by adding the curves in dB. As shown above, it becomes easy to see the resultant “Loaded Aol”, by adding the op amp original “Aol” plus the “Aol Load”, formed by the Ro-Riso-CLoad combination.

Riso Compensation Design Steps

1) Determine fp2 in Loaded Aol due to CLoad
   A) Measure in SPICE with CLoad on Op Amp Output
2) Plot fp2 on original Aol to create new Loaded Aol
3) Add Desired fz2 on to Loaded Aol Plot for Riso Compensation
   A) Keep fz1 $\leq$ 10*fp2 *(Case A)*
   B) Or keep the Loaded Aol Magnitude at fz1 $\geq$ 0dB *(Case B)*
   (fz1$\geq$10dB will allow for Aol variation of ½ Decade in Unity Gain Bandwidth)
4) Compute value for Riso based on plotted fz1
5) SPICE simulation with Riso for Loop Gain (Aolβ) Magnitude and Phase
6) Adjust Riso Compensation if greater Loop Gain (Aolβ) phase margin desired
7) Check closed loop AC response for VOUT/VIN
   A) Look for peaking which indicates marginal stability
   B) Check if closed AC response is acceptable for end application
8) Check Transient response for VOUT/VIN
   A) Overshoot and ringing in the time domain indicates marginal stability
   B) Determine if settling time is acceptable for end application

44

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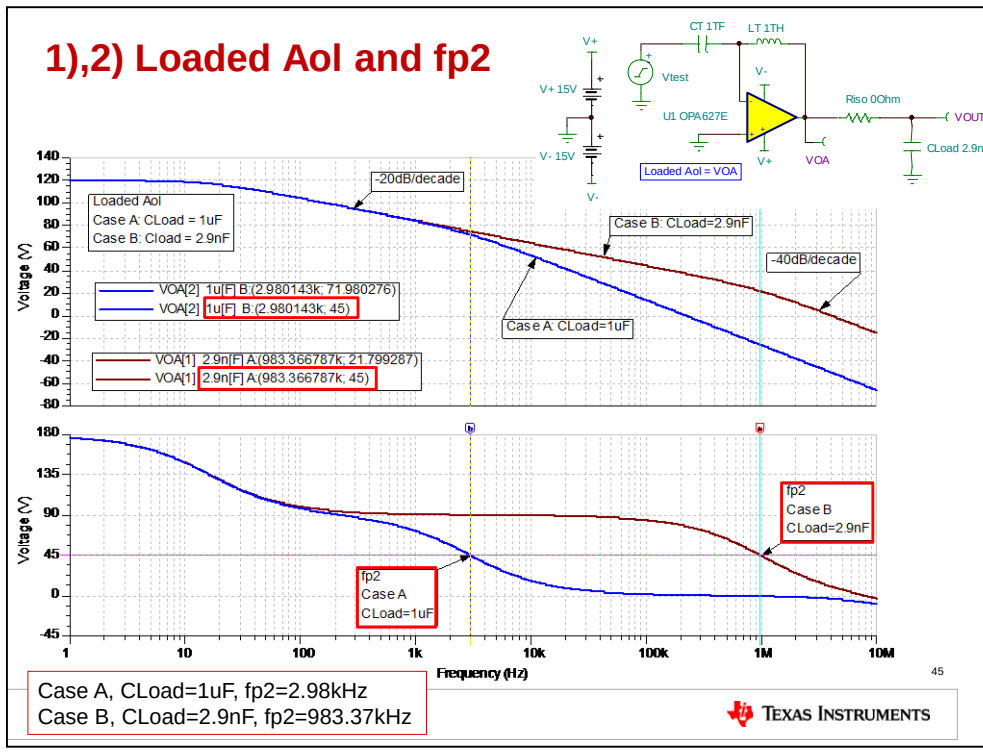
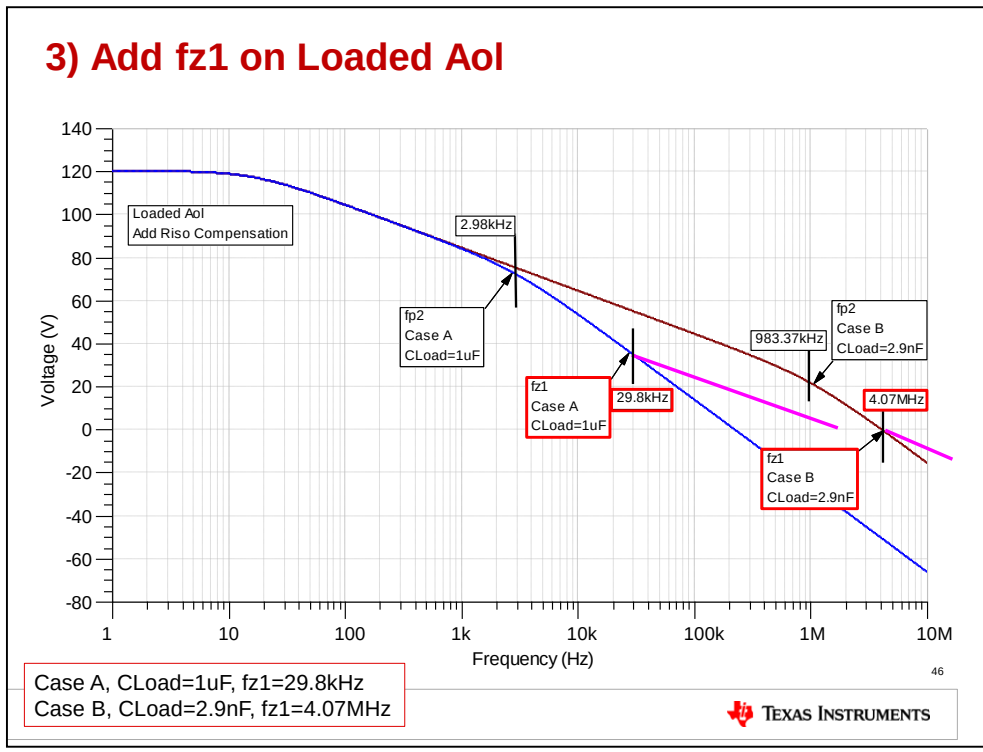
The Riso Compensation design steps are outlined here. Two cases, Case A and Case B, will be presented. Rules-of-thumb will be presented to yield best stability on first pass analysis.



Two different CLoads will be analyzed to show rules-of-thumb to get the best stability using Riso Compensation. Case A will use CLoad = 1uF and Case B will used CLoad = 2.9nF. By setting Riso = 0 ohms we can easily analyze the Loaded Aol for each case without Riso Compensation. From above Loaded Aol plots we can use the phase plots to determine the pole locations of fp2 for each of Case A, CLoad=1uF and Case B, CLoad=2.9nF.

From above we have completed Steps 1 and 2 for the Riso Compensation Design:

1) Determine fp2 in Loaded Aol due to CLoad
   A) Measure in SPICE with CLoad on Op Amp Output
2) Plot fp2 on original Aol to create new Loaded Aol



Our Loaded Aol curves for Case A, CLoad=1uF and Case B, CLoad=2.9nF, found using Step 1 and Step 2, are shown above. We can add straight line approximations to the magnitude plot (-20dB/decade slope) to indicate how and where we want to modify the Loaded Aol curve so the unity gain buffer (1/β = 0dB) will be stable with each respective capacitive load. These lines are added per the recommended rules-of-thumb below in Step 3.

From above we have completed Step 3 for the Riso Compensation Design:

3) Add Desired fz2 on to Loaded Aol Plot for Riso Compensation

   A) Keep fz1 $\leq$ 10*fp2 *(Case A)*

   B) Or keep the Loaded Aol Magnitude at fz1 $\geq$ 0dB *(Case B)*

   (fz1$\geq$10dB will allow for Aol variation of ½ Decade in Unity Gain Bandwidth)

4) Compute Value for Riso

Case A, CLoad=1uF, fz1=29.8kHz
Case B, CLoad=2.9nF, fz1=4.07MHz

Zero :

$$fz1 = \frac{1}{2\pi * Riso * CLoad}$$

$$Riso = \frac{1}{2\pi * fz1 * CLoad}$$

Zero, Case A, CLoad = 1μF, fz1 = 29.8kHz :

$$fz1 = \frac{1}{2\pi * Riso * CLoad}$$

$$Riso = \frac{1}{2\pi * 29.8kHz * 1\mu F} = 5.34\Omega \rightarrow \textbf{use 5.36Ω}$$

Zero, Case B, CLoad = 2.9nF, fz1 = 4.07MHz :

$$fz1 = \frac{1}{2\pi * Riso * CLoad}$$

$$Riso = \frac{1}{2\pi * 4.07MHz * 2.9nF} = 13.48\Omega \rightarrow \textbf{use 13.7Ω}$$

47

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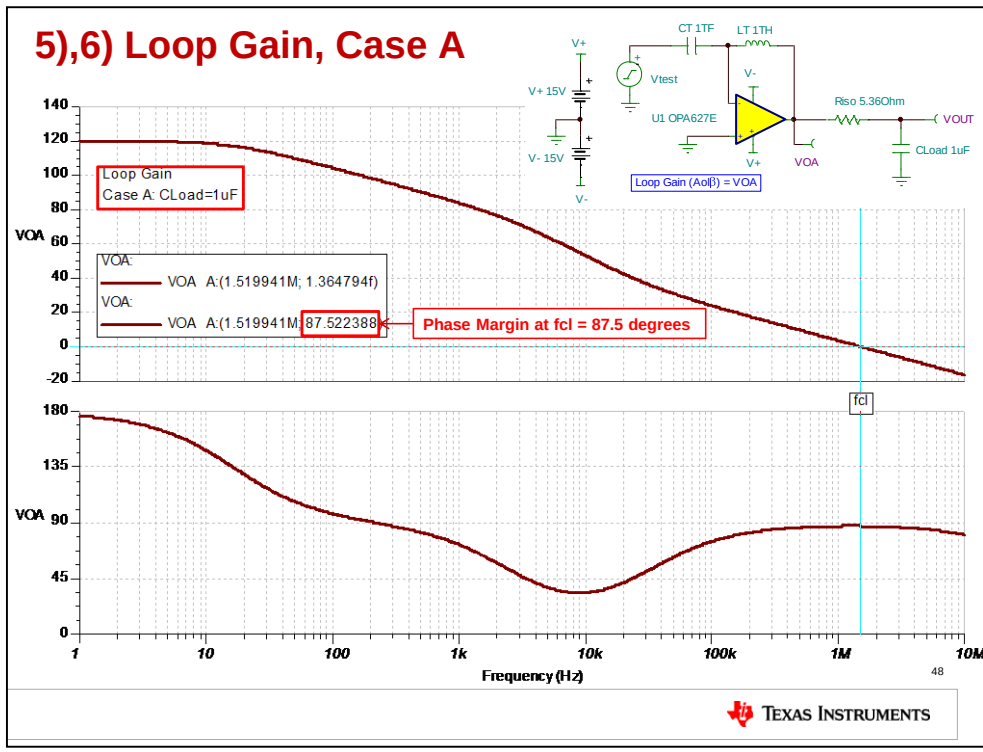
From Riso Compensation Design Step 3 we know the respective locations we want for fz1. From that we can compute Riso and choose a standard resistor value.

From above we have completed Step 4 for the Riso Compensation Design:

4) Compute value for Riso based on plotted fz1

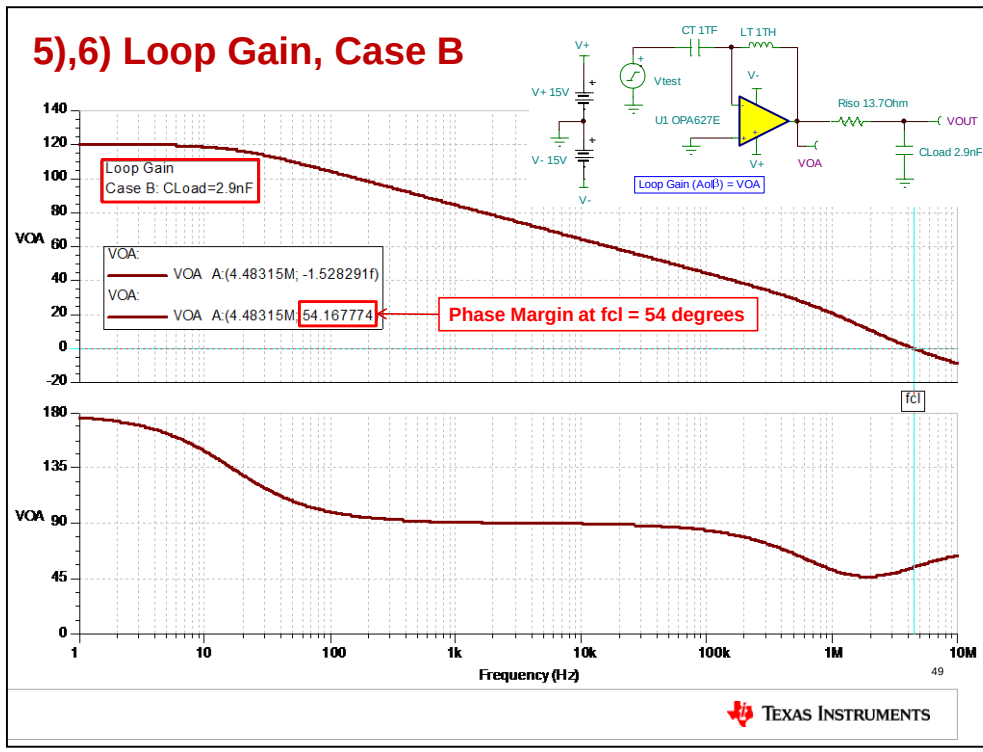


Design Step 5 for Riso Compensation is to check the final Riso value chosen by a loop gain plot on the complete op amp circuit. We see from above that for Case A, CLoad=1uF, at fcl, where Loop Gain (Aolβ) goes to zero, the phase margin is 87.5 degrees. Step 6 is to adjust Riso for more phase margin if we are not satisfied with our first analysis and re-run the loop gain and phase plot to check the final design. Here we are happy with 87.5 degrees of Loop Gain (Aolβ) phase margin.

From above we have completed Steps 5 & 6 for the Riso Compensation Design:

5) SPICE simulation with Riso for Loop Gain (Aolβ) Magnitude and Phase

6) Adjust Riso Compensation if greater Loop Gain (Aolβ) phase margin desired

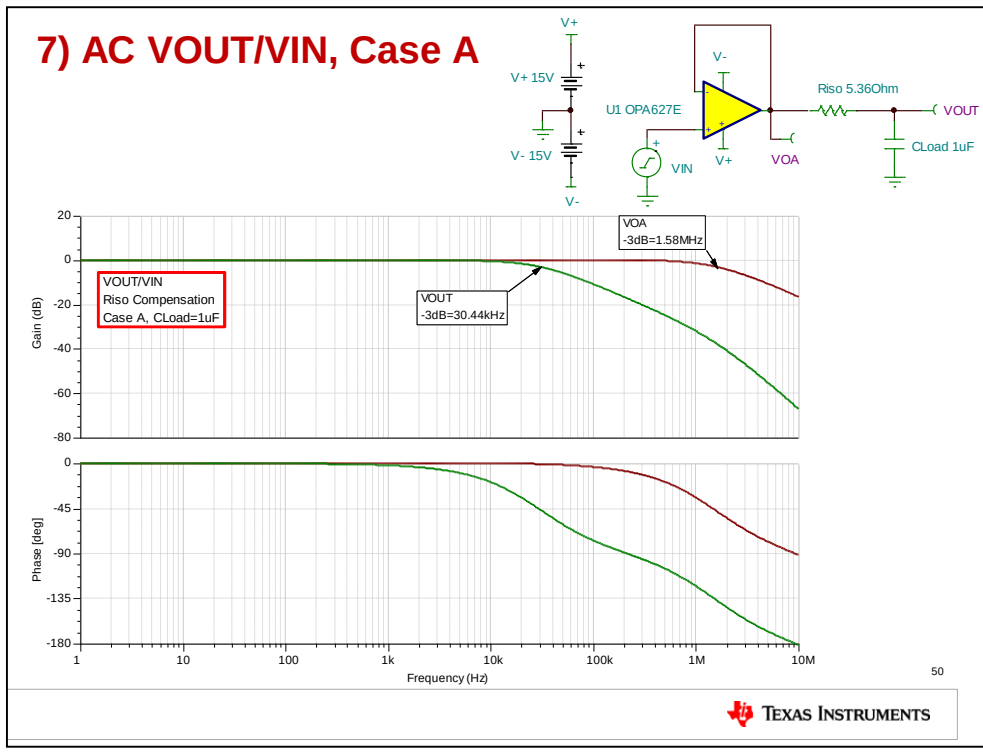


Design Step 5 for Riso Compensation is to check the final Riso value chosen by a loop gain plot on the complete op amp circuit. We see from above that for Case B, CLoad=2.9nF, at fcl, where Loop Gain (Aolβ) goes to zero, the phase margin is 54.2 degrees. Step 6 is to adjust Riso for more phase margin if we are not satisfied with our first analysis and re-run the loop gain and phase plot to check the final design. Here we are happy with 54.2 degrees of Loop Gain (Aolβ) phase margin.

From above we have completed Steps 5 & 6 for the Riso Compensation Design:

5) SPICE simulation with Riso for Loop Gain (Aolβ) Magnitude and Phase

6) Adjust Riso Compensation if greater Loop Gain (Aolβ) phase margin desired



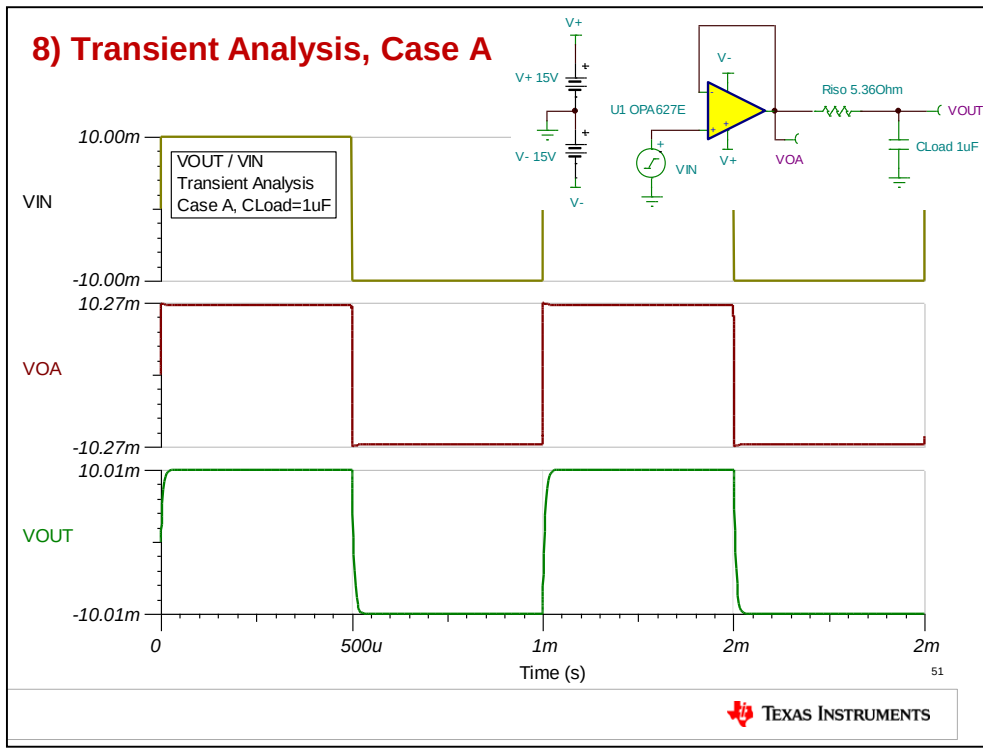
Design Step 7 for Riso Compensation is to check the closed loop AC response over frequency. From above, for Case A, CLoad=1uF, we see the closed loop AC response for both the output of the op amp, VOA, and the output after Riso, VOUT. If this closed loop bandwidth is not acceptable for the final application we will need to consider other capacitive stability techniques (see Appendix) or a different op amp or different load capacitance value.

From above we have completed Step 7 for the Riso Compensation Design:

7) Check closed loop AC response for VOUT/VIN

   A) Look for peaking which indicates marginal stability

   B) Check if closed AC response is acceptable for end application

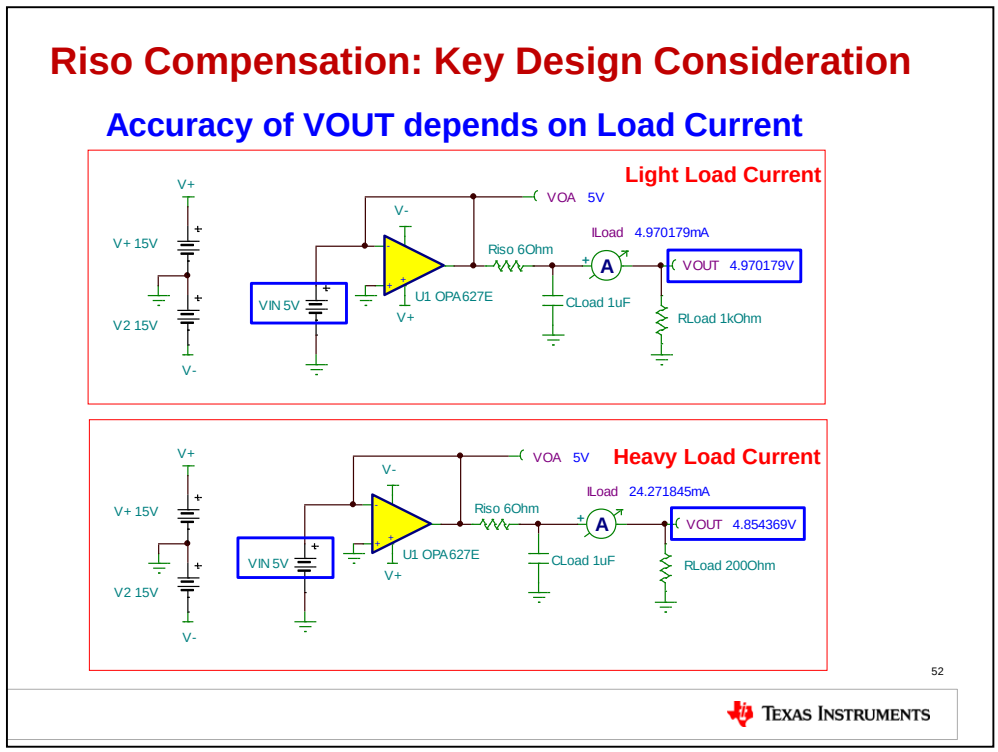


Design Step 8 for Riso Compensation is to check the closed loop transient response. From above, for Case A, CLoad=1uF, we see the closed loop Transient response for both the output of the op amp, VOA, and the output after Riso, VOUT show no signs of excessive overshoot or ringing before settling.

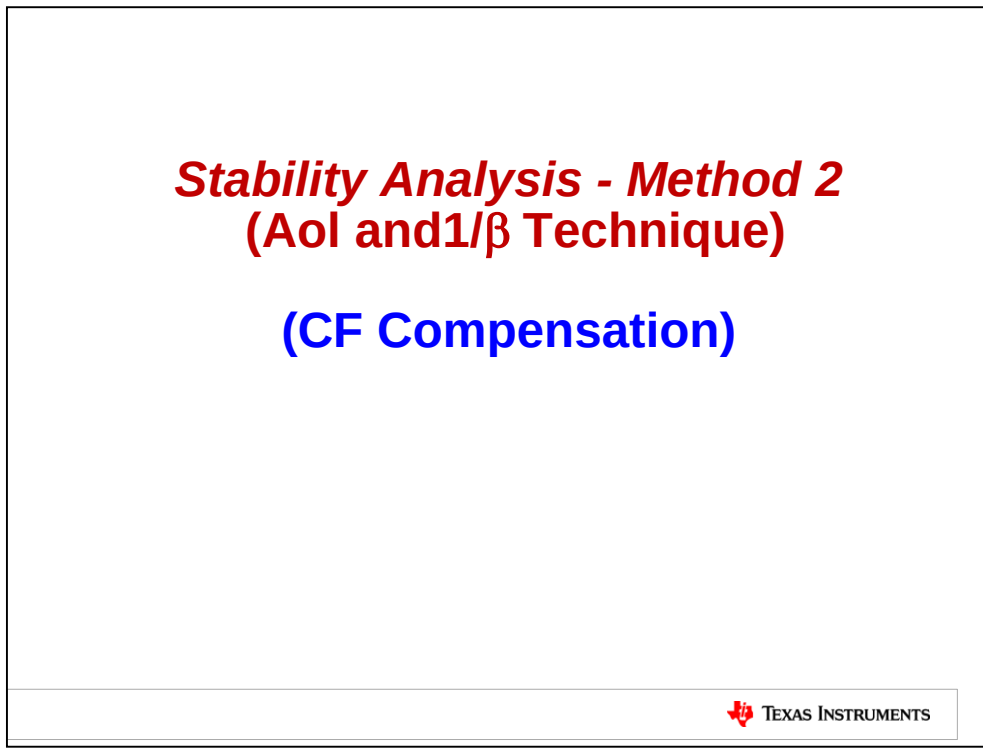
From above we have completed Step 7 for the Riso Compensation Design:

8) Check Transient response for VOUT/VIN

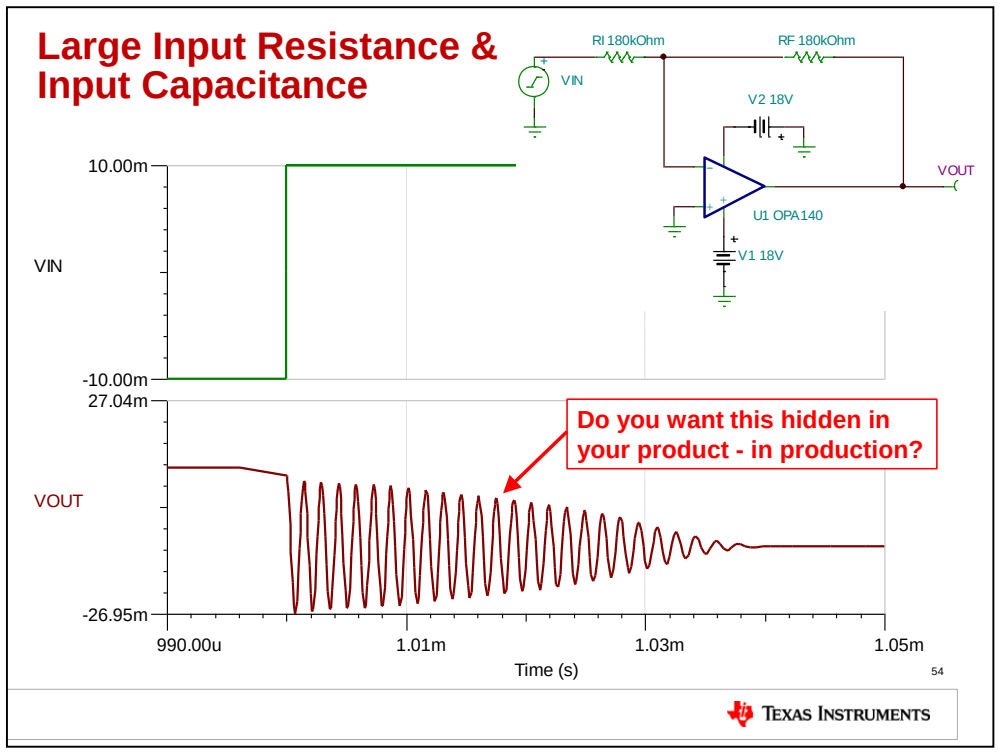
A) Overshoot and ringing in the time domain indicates marginal stability



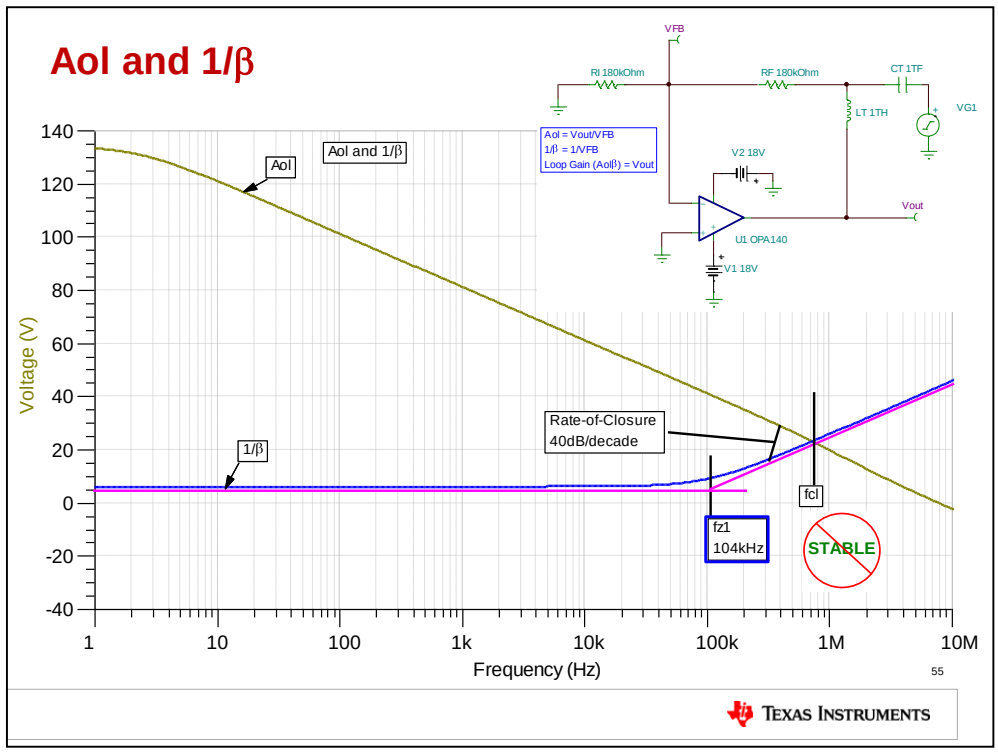
The Riso Compensation has one key design consideration with regards to accuracy at VOUT for heavy loads. The feedback for voltage accuracy is directly at the output of the op amp and the VOUT at the load is isolated by Riso. If output currents are large and depending upon the value of Riso the voltage at VOUT will not be the voltage at VIN for the unity gain follower shown above. If this is a problem in the end application a different compensation technique for the CLoad will need to be used (see Appendix for alternative compensation methods for output capacitive loads).



There are two basic methods for analyzing op amp stability problems. The second method, Method 2, will use the Aol and 1/β Technique to analyze stability problems due to capacitive loading of an op amp input. The compensation used for this example will be CF Compensation.



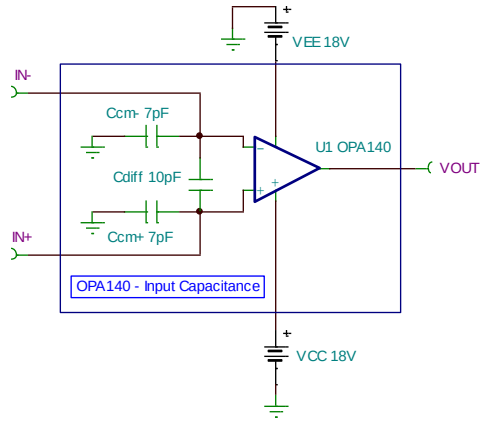
Large input resistances can combine with op amp input capacitance to create unanticipated and undesired instabilities as shown above in the transient response of the OPA140 in an inverting Gain = -1 configuration with RF=RI=180k ohms.



We can use our SPICE Loop Gain Test circuit above to plot Aol and 1/β for this Gain = -1 circuit. Note that the 1/β curve has a zero in it at 104kHz. At fcl, where Loop Gain (Aolβ) goes to zero, we see that the 1/β curve intersects the Aol at a rate-of-closure that is 40dB/decade which by our criteria implies an UNSTABLE circuit.

Op Amp Input Capacitance

PARAMETER	CONDITIONS	OPA140, OPA2140, OPA4140 MIN	TYP	MAX	UNIT
INPUT IMPEDANCE					
Differential			10^{13} || 10		Ω || pF
Common-Mode	V_{CM} = (V–) –0.1V to (V+) –3.5V		10^{13} || 7		Ω || pF



56

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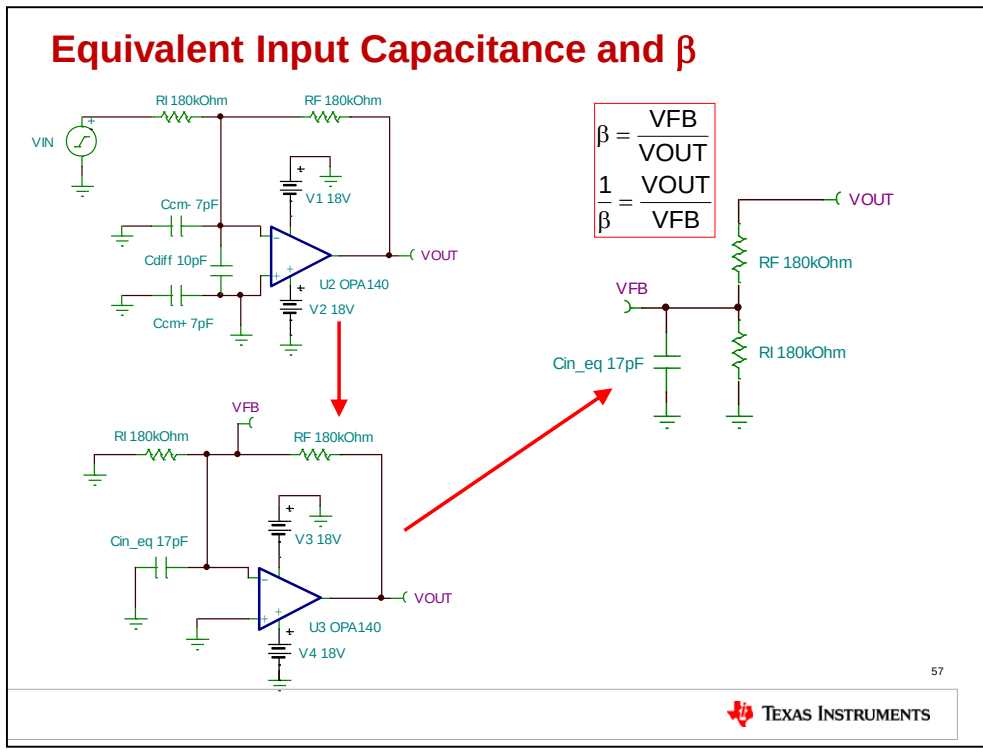
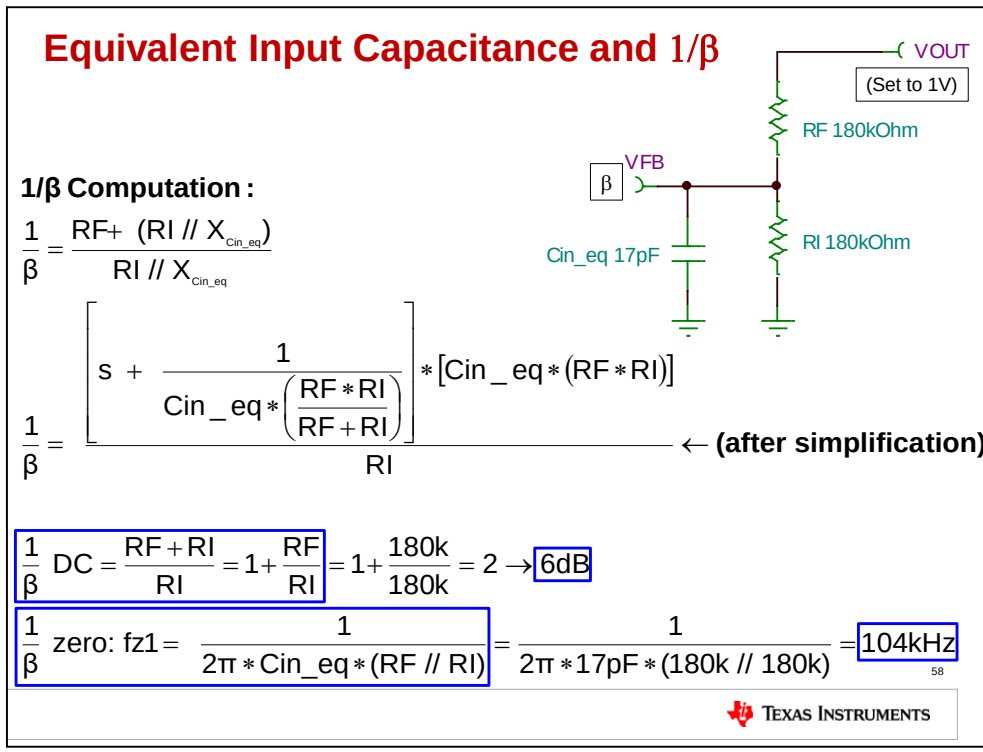
To properly analyze this circuit and thus properly compensate it for stability we first must analyze the OPA140 op amp input capacitance. The datasheet excerpt for the OPA140 is shown here with Input Impedance parameters for Differential and Common-Mode. The input capacitance model for the OPA140 is also shown. From the data sheet we can assign values for the capacitances shown, Ccm+, Ccm-, and Cdiff.



From our input capacitance model for the OPA140 and the circuit topology it is configured in we see there is a net input capacitance, Cin_eq which will affect our feedback factor, β, over frequency. Since the Cin_eq capacitor is buffered by RF, 180k ohm resistor, there are no loading effects on Aol with this circuit topology and so the Aol remains unchanged.



Our β network is shown above. β is easy to compute if one sets VOUT = 1. β=(input impedance)/(feedback impedance + input impedance). Recall that 1/β is just the reciprocal of β. From our derived and simplified equations above we see a zero, fz1, in the 1/β plot due to RF, RI and Cin_eq. Note that although our closed loop gain is -1 our 1/β is at 6dB or x2. Remember our earlier discussion of noise gain and to view the op amp, from a loop gain view, to always be running in a noise gain equivalent to putting a noise source on the +input of the op amp and running in the non-inverting gain based on feedback and input impedances from output to –input.

CF Compensation Design Steps

1) Determine fz1 in 1/β due to Cin_eq
   A) Measure in SPICE
      OR
   B) Compute by Datasheet C_{DIFF} and C_{CM} and Circuit RF and RI
2) Plot 1/β with fz1 on original Aol
3) Add Desired fp1 on 1/β for CF Compensation
   A) Keep fp1 ≤ 10*fz1
   B) Keep fp1 ≤ 1/10 * fcl
4) Compute value for CF based on plotted fp1
5) SPICE simulation with CF for Loop Gain (Aolβ) Magnitude and Phase
6) Adjust CF Compensation if greater Loop Gain (Aolβ) phase margin desired
7) Check closed loop AC response for VOUT/VIN
   A) Look for peaking which indicates marginal stability
   B) Check if closed AC response is acceptable for end application
8) Check Transient response for VOUT/VIN
   A) Overshoot and ringing in the time domain indicates marginal stability

59

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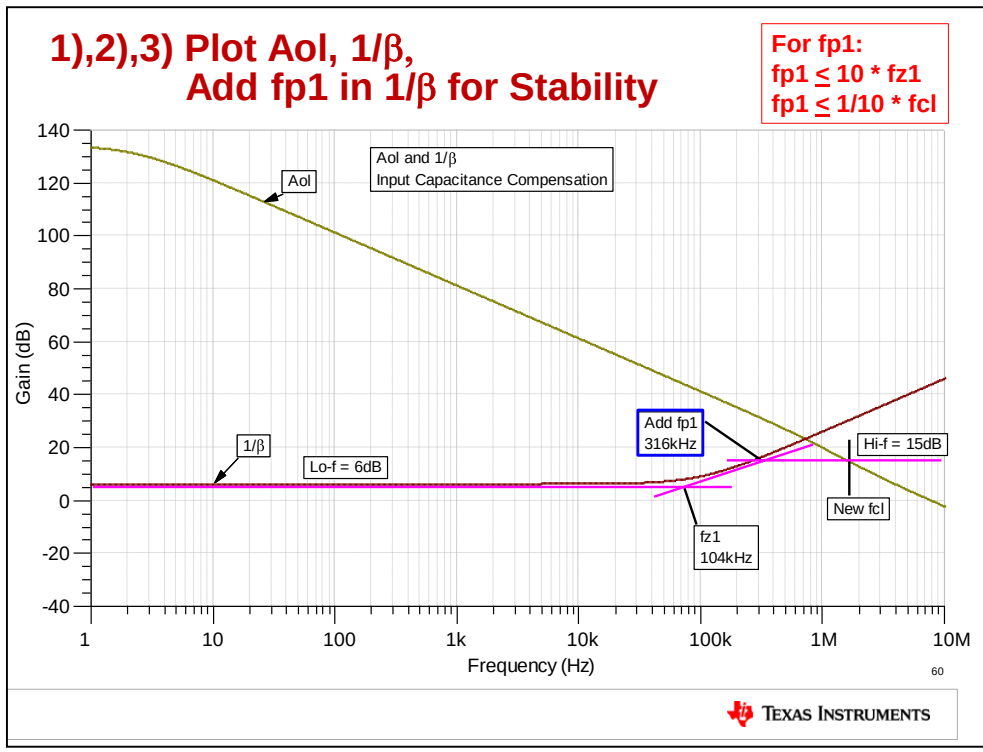
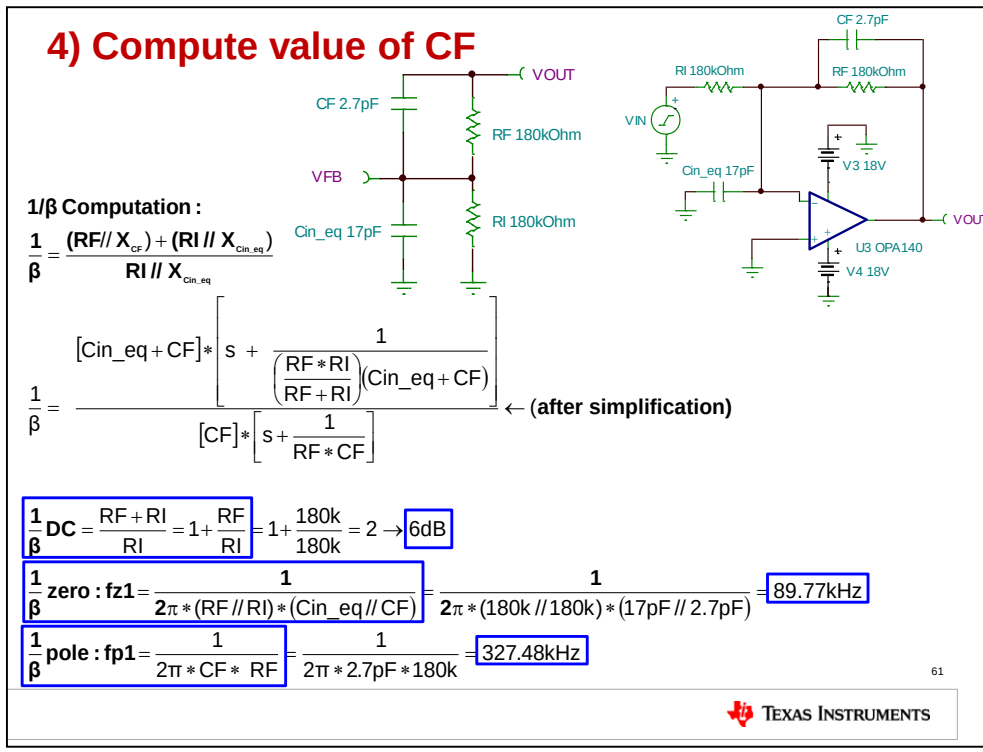
The CF Compensation design steps are outlined here. Rules-of-thumb are presented to yield best stability on first pass analysis.



Using our Loop Gain Test circuit in SPICE we can plot the Aol and 1/β for the uncompensated circuit as shown above. For best stability results on first pass we use the recommended rules-of-thumb shown and draw in what we want the final 1/β curve to look like. Based on this graphical approach we see we need a pole, fp1, added into the 1/β curve to allow the compensated 1/β to intersect the Aol at a rate-of-closure which is 20db/decade and thus stable by our criteria.

From above we have completed Steps 1, 2, and 3 for the CF Compensation Design:

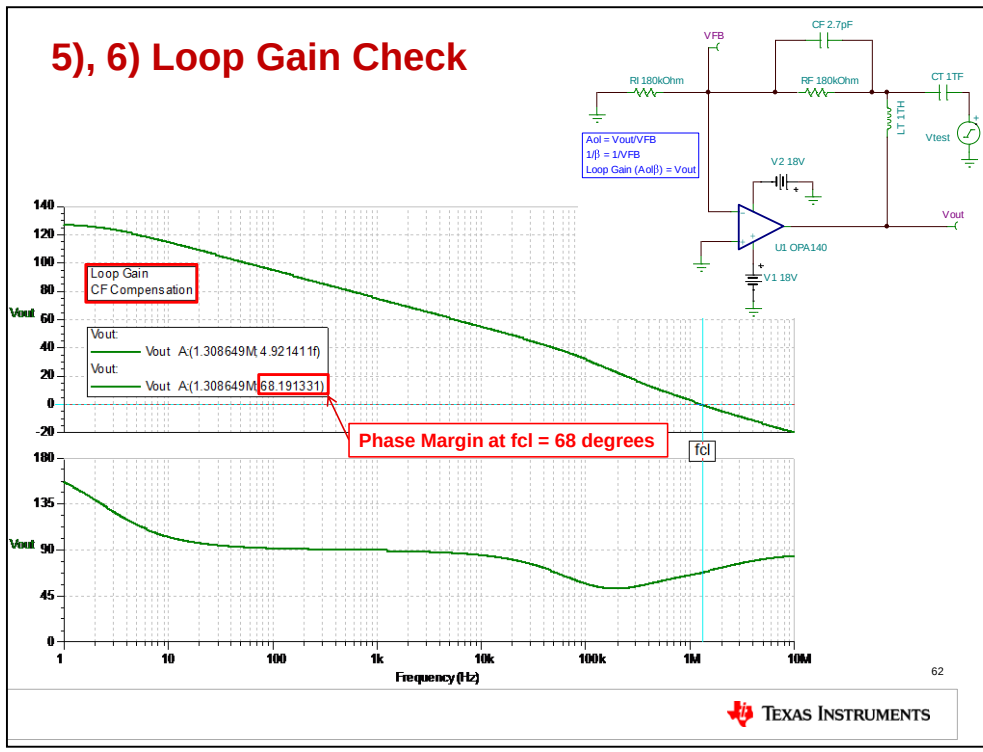
1) Determine fz1 in 1/β due to Cin_eq
   - A) Measure in SPICE
   - B) Compute by Datasheet C_{DIFF} and C_{CM} and Circuit RF and RI
2) Plot 1/β with fz1 on original Aol
3) Add Desired fp1 on 1/β for CF Compensation
   - A) Keep fp1 $\leq$ 10*fz1
   - B) Keep fp1 $\leq$ 1/10 * fcl



Our β network is shown above. β is easy to compute if one sets VOUT = 1. β=(input impedance)/(feedback impedance + input impedance). Recall that 1/β is just the reciprocal of β. From our derived and simplified equations above we see a zero, fz1, in the 1/β plot due to RF, RI, Cin_eq, and CF. Note that although our closed loop gain is -1 our 1/β is at 6dB or x2. Remember our earlier discussion of noise gain and to view the op amp, from a loop gain view, to always be running in a noise gain equivalent to putting a noise source on the +input of the op amp and running in the non-inverting gain based on feedback and input impedances from output to –input. Note that with the addition of CF Compensation the 1/β zero, fz1, is moved to a lower frequency since CF is in parallel with Cin_eq to determine the location of fz1. However, to choose the CF Compensation pole, fp1, it is only dependent upon Rf and CF.

From above we have completed Step 4 for the CF Compensation Design:

4) Compute value for CF based on plotted fp1

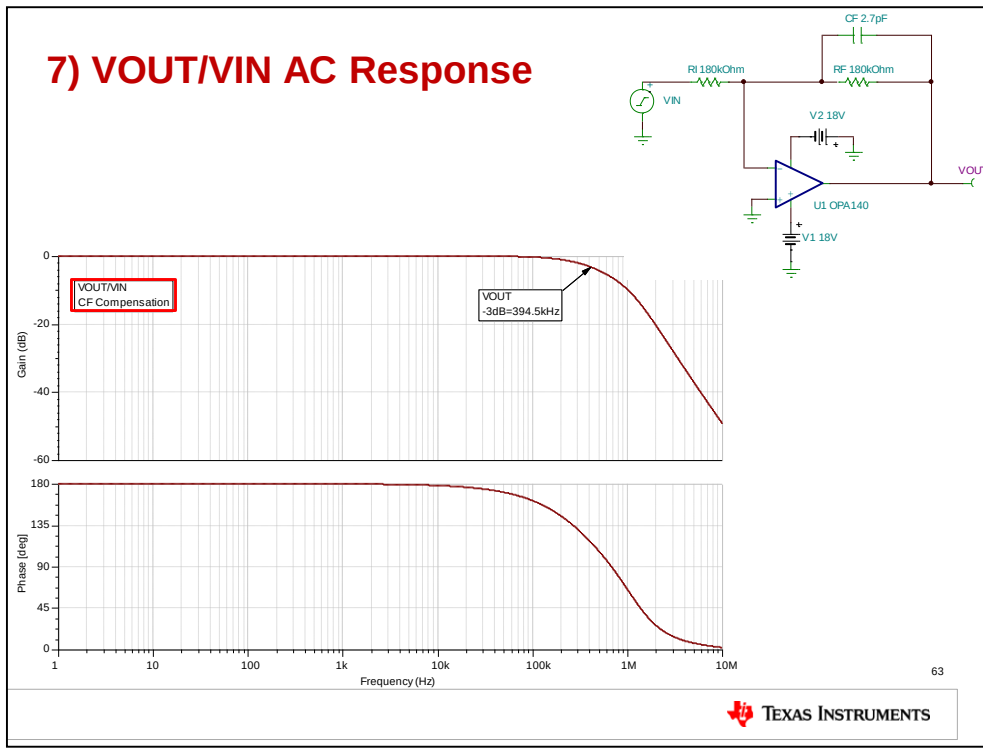


Design Step 5 for CF Compensation is to check the final CF value chosen by a loop gain plot on the complete op amp circuit. We see from above that at fcl, where Loop Gain (Aolβ) goes to zero, the phase margin is 68 degrees. Step 6 is to adjust CF for more phase margin if we are not satisfied with our first analysis and re-run the loop gain and phase plot to check the final design. Here we are happy with 68 degrees of Loop Gain (Aolβ) phase margin.

From above we have completed Steps 5 & 6 for the CF Compensation Design:

5) SPICE simulation with CF for Loop Gain (Aolβ) Magnitude and Phase

6) Adjust CF Compensation if greater Loop Gain (Aolβ) phase margin desired



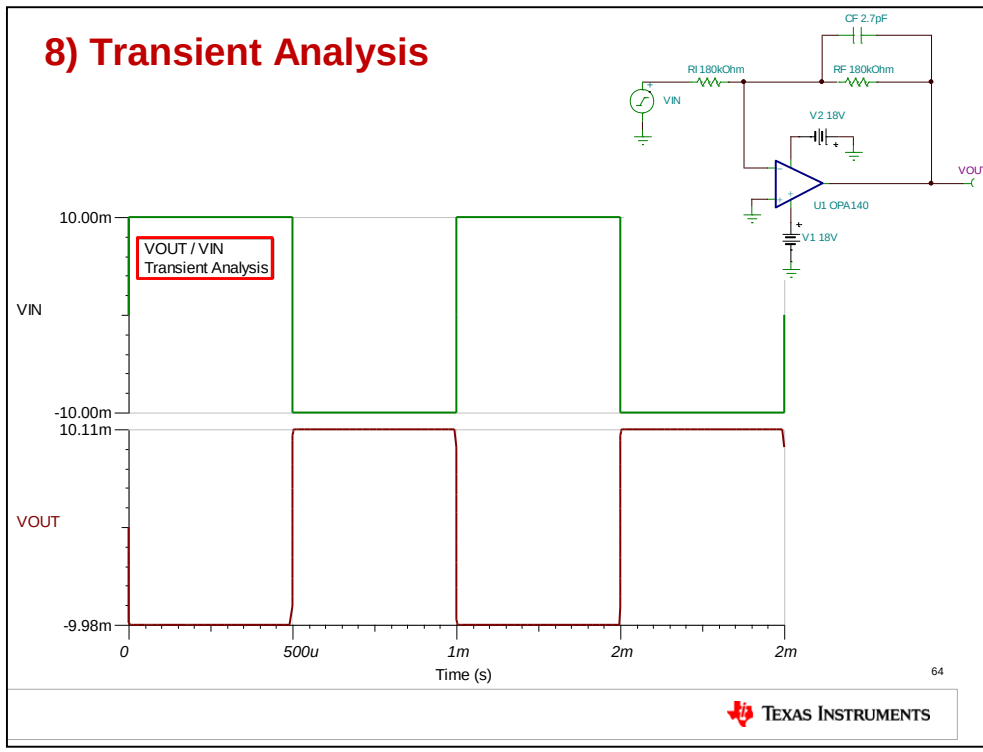
Design Step 7 for CF Compensation is to check the closed loop AC response over frequency. From above, see the closed loop AC response for both the output of the op amp, VOUT. If this closed loop bandwidth is not acceptable for the final application we will need to consider other capacitive stability techniques (see Appendix) or a different op amp or different feedback and input resistor values of lower values.

From above we have completed Step 7 for the CF Compensation Design:

7) Check closed loop AC response for VOUT/VIN

   A) Look for peaking which indicates marginal stability

   B) Check if closed AC response is acceptable for end application



Design Step 8 for CF Compensation is to check the closed loop transient response. From above we see the closed loop Transient response for VOUT shows no signs of excessive overshoot or ringing before settling.

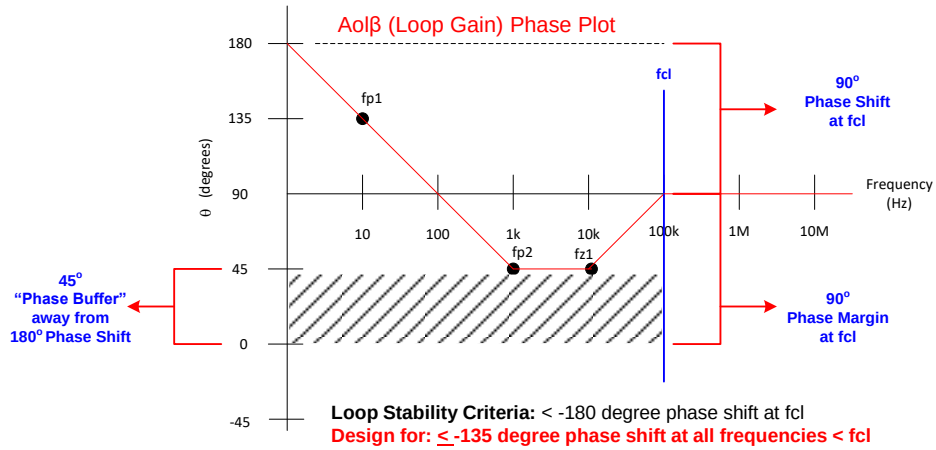
From above we have completed Step 7 for the CF Compensation Design:

8) Check Transient response for VOUT/VIN

A) Overshoot and ringing in the time domain indicates marginal stability

There are some handy stability tricks and rules-of-thumb that have been developed based on experience in stabilizing hundreds of op amp circuits. They are presented here to help you get op amp stability done quickly and right the first time.

Loop Gain Bandwidth Rule: 45 degrees for f ≤ fcl



Loop Stability Criteria: < -180 degree phase shift at fcl
Design for: ≤ -135 degree phase shift at all frequencies < fcl
Why?:
Because Aol is not always "Typical"
Power-up, Power-down, Power-transient → Undefined "Typical" Aol
Allows for phase shift due to real world Layout & Component Parasitics
Prevent excessive ringing due to phase margin dip near fcl

66

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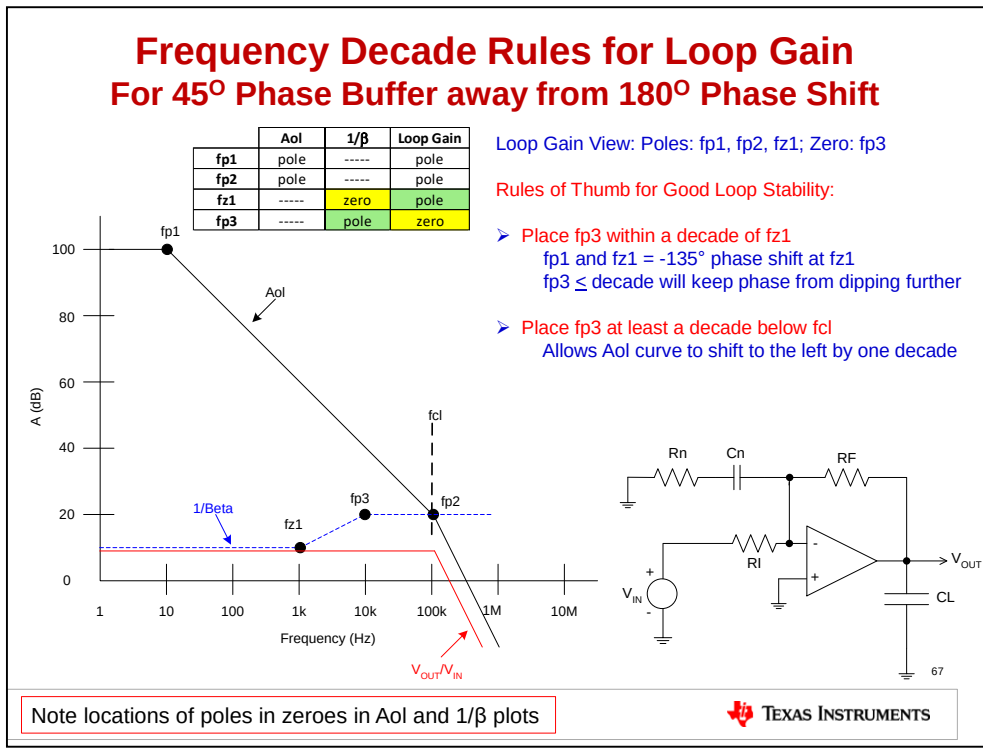
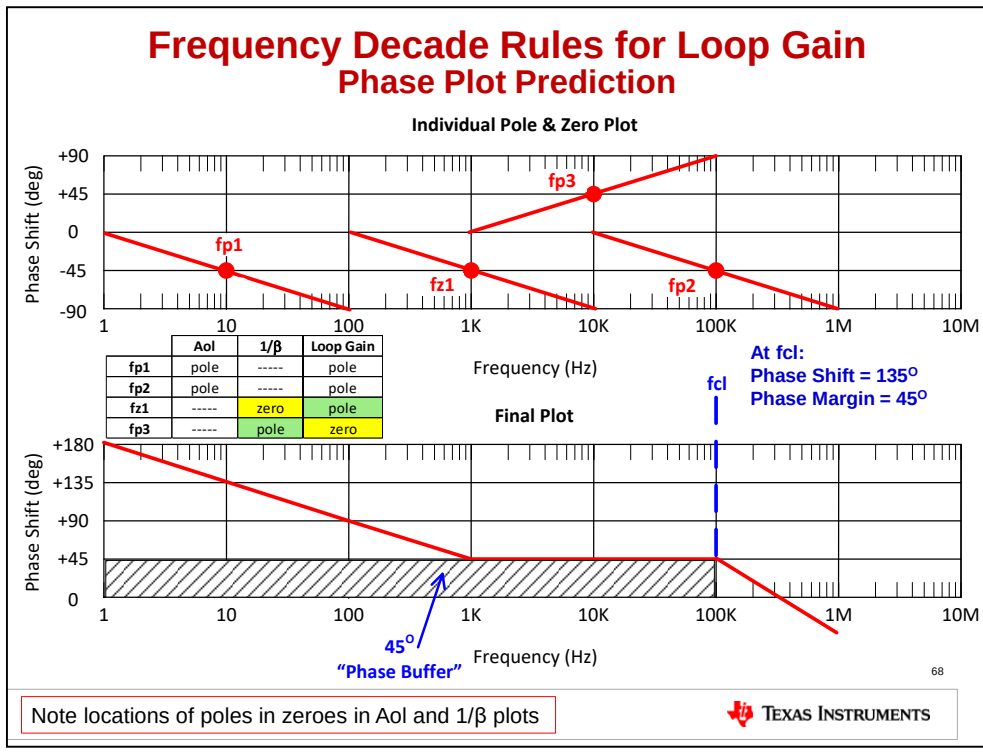
The established loop stability criteria is less than a 180 degree phase shift at fcl, the frequency at which loop gain goes to zero. How close the phase shift is to a full 180 degrees phase shift at fcl is defined as phase margin. As detailed in this slide the recommended rule-of-thumb for real world circuits is to design for 135 degree phase buffer (45 degree away from 180 degrees phase shift) throughout the loop gain bandwidth (f ≤ fcl). This allows for the real world cases of power-up, power-down and power-transient conditions where the op amp can have changes in its Aol curve which may result in transient oscillations. This is especially undesirable in power op amp circuits. This rule-of-thumb also allows for extra phase buffer in the loop gain bandwidth to account for additional real world phase shifts due to parasitic capacitances and PCB layout parasitics. Also, a phase buffer less than 45 degrees within the loop gain bandwidth can result in undesired peaking in the closed loop transfer function. The lower the phase buffer dip and the closer the dip is to fcl, the more pronounced the closed loop peaking will be.



The “decade rules” for frequency in the Loop Gain plot are detailed in the slide above. These frequency decade rules will be used for 1/β plots and Aol plots as well as Aolβ, loop gain plots, which we can predict directly from the Aol and 1/β plots. For the circuit shown in this slide the Aol curve contains a second pole, fp2, around 100kHz due to the capacitive load, CL, and the op amp’s Ro. We will create a feedback network that will meet our Loop Gain Bandwidth rule of 45 degrees margin for f≤ fcl. We will analyze and synthesize the feedback network using the 1/β plot and Aol plot with the knowledge of what we are doing to the Loop Gain plot, Aolβ. fp1 gives us a first pole at 10Hz in the Loop Gain plot which implies a 45 degree phase shift at 10Hz with phase shifting to a 90 degrees by 100Hz. At 1kHz, fz1, a zero in the 1/β plot, we add a pole in the Loop Gain plot and another 45 degree phase shift at 1kHz. Our total phase shift now is -135 degrees at 1kHz. But if we continue on in frequency with just fz1 we will reach -180 phase shift at 10kHz!! So we add fp3, a pole in the 1/β plot, which is a zero in the Loop Gain plot at 10kHz. This keeps the phase shift at 1kHz to -135 degrees and flattens the phase plot to -135 degrees phase shift from 1kHz to 10kHz (remember poles and zeros have an effect a decade above and a decade below their actual frequency location). fp2 adds another pole in the Loop Gain plot at 100kHz since fp2 is from the Aol plot. Between 10kHz, where fp3 is, and 100kHz, where fp2 is, we expect no change in phase shift since fp3 is a Loop Gain plot zero and fp2 is a Loop Gain plot pole.

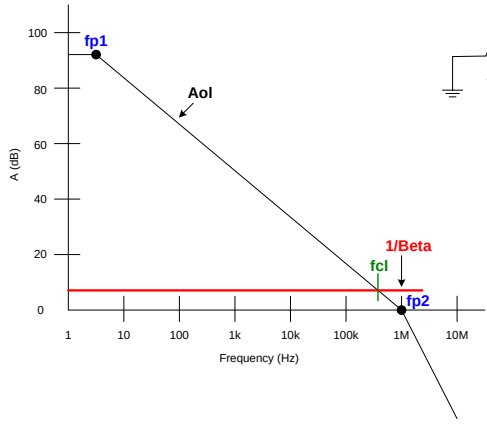
So if we keep poles and zeros spaced a decade away from each other they will keep the phase shift from dipping between them since each has an effect on one another a decade above and a decade below their location. The final key part of the Frequency Decade Rules for Loop Gain is to place fp3 no closer than a decade away from fcl. This allows for a decade shift in Aol towards the lower frequency range before we would be in a marginal stability condition. Typical Aol curves may shift as much as ½ decade in the real world.

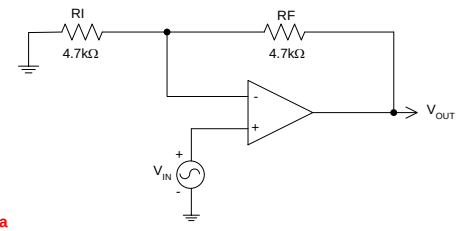
The V_{OUT}/V_{IN} for this circuit is predicted to be flat until loop gain goes away at 100kHz, at which point it will then follow the Aol curve on down.



This is the first order hand analysis prediction for the Loop Gain phase plot of the circuit described in the previous slide.

Op Amp Circuits & Second Order Systems





Most Op Amp Circuits are adequately analyzed, simulated, and real world tested using well-known second order system response behavior.

Most Op Amps are dominated by Two Poles:
Aol curve shows a low frequency pole, fp1
Aol curve also has a high frequency pole, fp2
Often fp2 is at fcl for unity gain
This yields 45 degrees phase margin at unity gain

69

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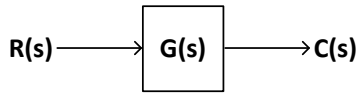
Most real world op amp circuits are dominated by a two pole, second order, system response. A typical op amp Aol has a low frequency pole in the 10Hz to 100Hz region and another high frequency pole at its unity gain crossover frequency, or soon after that in frequency. If pure resistive feedback is used we can see that the loop phase plot would demonstrate the effects of a two pole system. For more complicated op amp circuits the resultant loop gain and loop phase plots are usually dominated by a two pole response. Closed loop behavior of a second order system is well defined and offers us a powerful technique for a real world stability check.

Control Loop - Second Order System



$$\frac{C(s)}{R(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

where :

ω_n = **natural frequency (rad/s)**

ζ = **damping ratio**

Closed Loop Response (Step and AC) :

Underdamped : $0 < \zeta < 1$

Marginally Stable : $\zeta = 0$

Critically Damped : $\zeta = 1$

Overdamped : $\zeta > 1$

70

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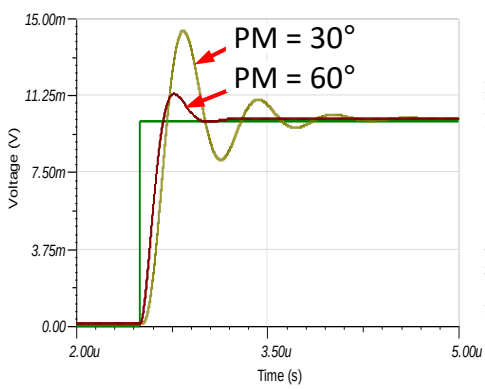
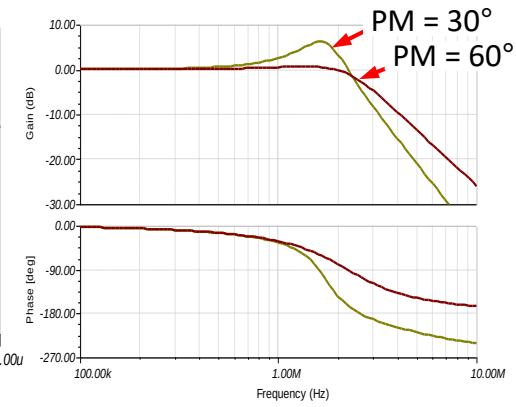
The traditional second order system control loop block diagram and characteristic equation are shown above. G(s) for us represents our closed loop, 2-pole dominant, op amp circuit. There are well established, documented, and derived behaviors for such a 2-pole dominant system that we can use to help us assess most op amp stability problems.

Indirect Phase Margin Measurements

Phase Margin can be measured indirectly on closed-loop circuits!



Time Domain → Percent Overshoot



AC Gain/Phase → AC Peaking

71

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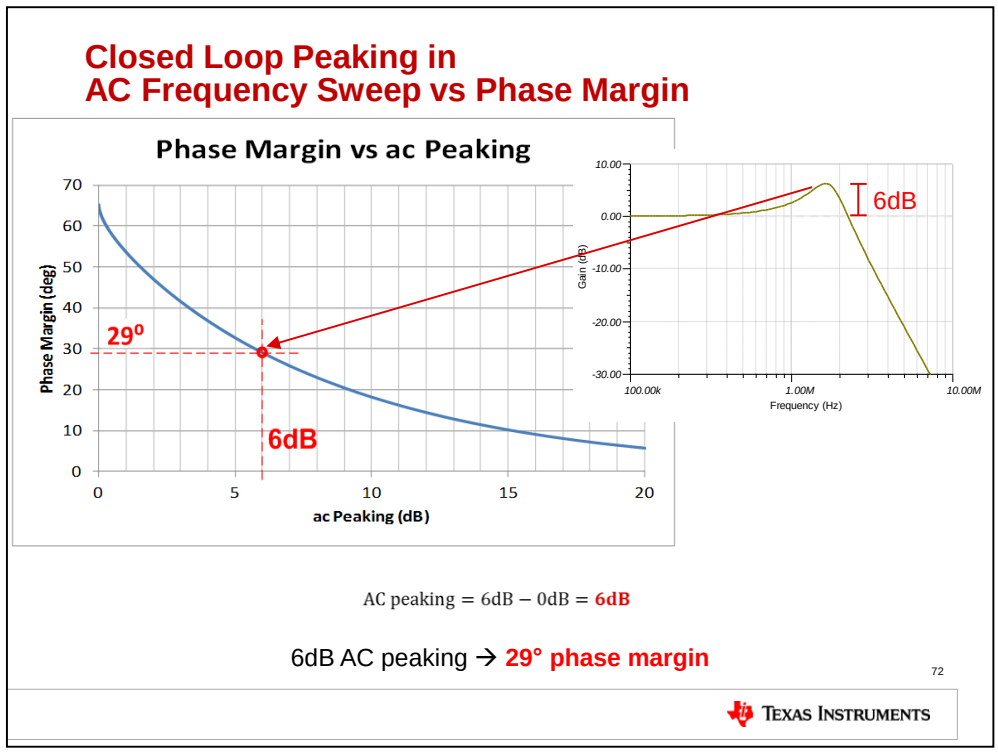
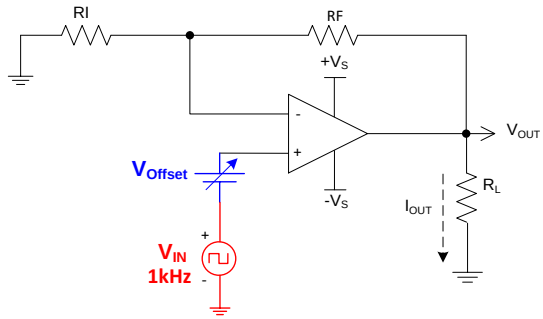
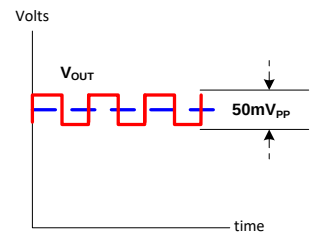
Phase Margin can also be indirectly measured on closed-loop circuits in the time domain and in ac gain/phase measurements. In the time domain, we can observe phase margin based on the overshoot of an op amp's output relative to a small-signal step input. In the frequency domain, we can observe phase margin based on the maximum AC peaking in the circuit's transfer function compared to the DC gain.



In AC Gain/Phase plots, the amount of ac peaking relative to the DC gain can be used to indirectly measure the phase margin of a circuit. In this example, the AC transfer function is peaking at 6dB, while the DC gain is 0dB. A total peaking of 6dB again results in 29 degrees of phase margin.

Transient Real World Stability Test





Test Tips:

- Choose test frequency << fcl
  "Small Signal" AC Output Square Wave (1kHz usually works well)
- Adjust V_{IN} amplitude to yield output ≤50mVpp
- Worst case is usually when $V_{Offset} = 0$ → Largest Op Amp R_O ($I_{OUT} = 0$)
- Use V_{Offset} as desired to check all output operating points for stability
- Set scope = AC Couple & expand vertical scope scale to look for amount of overshoot, undershoot, ringing on V_{OUT} small signal square wave
- Use X1 Scope Probe on V_{OUT} for best resolution

73

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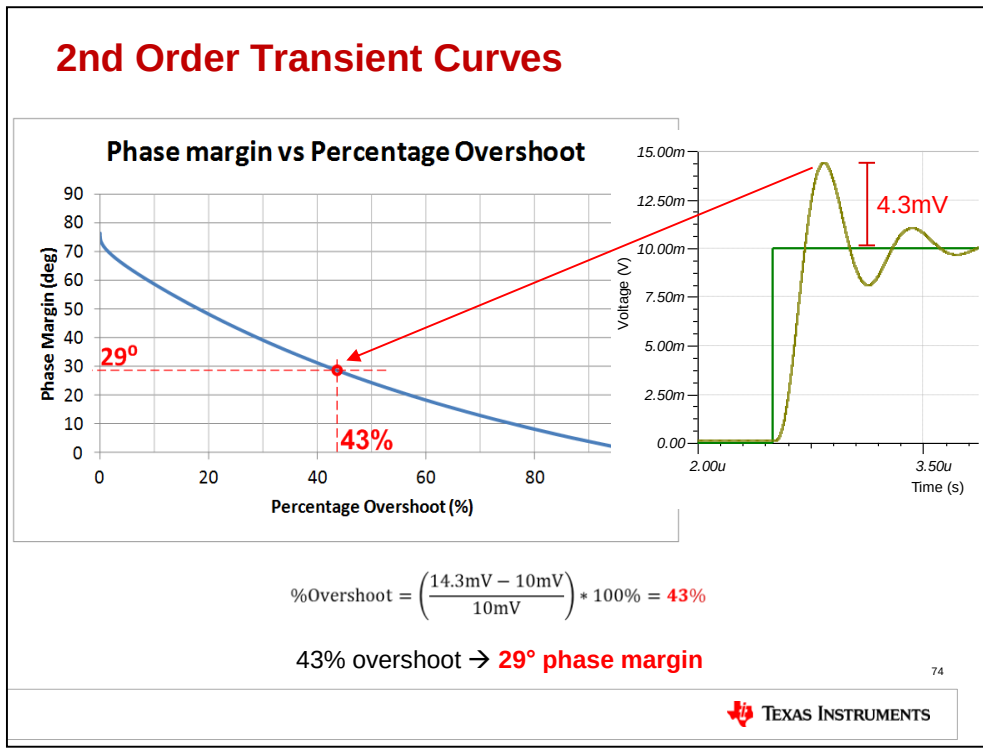
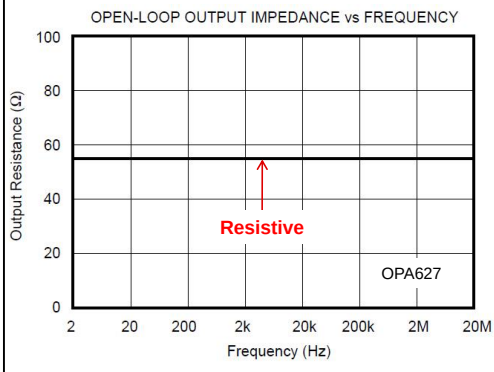
This slide details the Transient Real World Stability Test. A small amplitude square wave is injected into the closed loop op amp circuit as the V_{IN} source. A frequency is chosen well within the loop gain bandwidth but also high enough to make triggering with an oscilloscope easy. 1kHz is a good test frequency for most applications. V_{IN} is adjusted such that V_{OUT} is 50mVpp or less. We are interested in the small signal AC behavior of the circuit to look for AC stability. To that end we do not want a large signal swing on the output which could also contain large signal limitations such as slew rate or output current limitations or output stage voltage saturation. V_{offset} provides a mechanism to move the output voltage up and down through its entire output voltage range to look for AC stability under all operating point conditions. For many circuits, especially those that drive capacitive loads, the worst case for stability is when the output is near zero (for a dual supply op amp application) and there is little or no DC load current since this results in the highest value of R_O, the op amp's open loop small signal resistance. Record the amount of overshoot and ringing on the square wave output and compare it to the 2nd Order Transient Curves in the Slide 75 to derive the phase margin for stability.



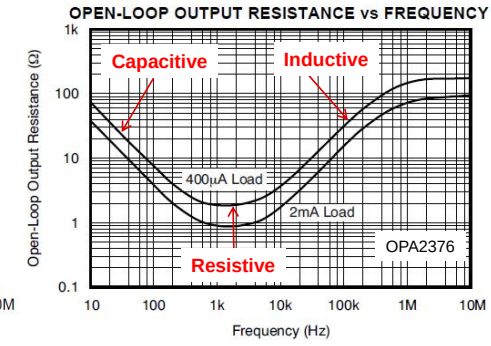
In the time domain the percent overshoot to a step input can be used to indirectly calculate the phase margin. In this example, a 10mV step was applied. The output overshoot reached 14.3mV, or 4.3mV above the intended output. This corresponds to a percent overshoot of 43%. Using the phase margin vs. percentage overshoot plot, we can see that 43% of overshoot results in only 29 degrees of phase margin.

When R_O is really Z_O!!

OPA627 has R_O

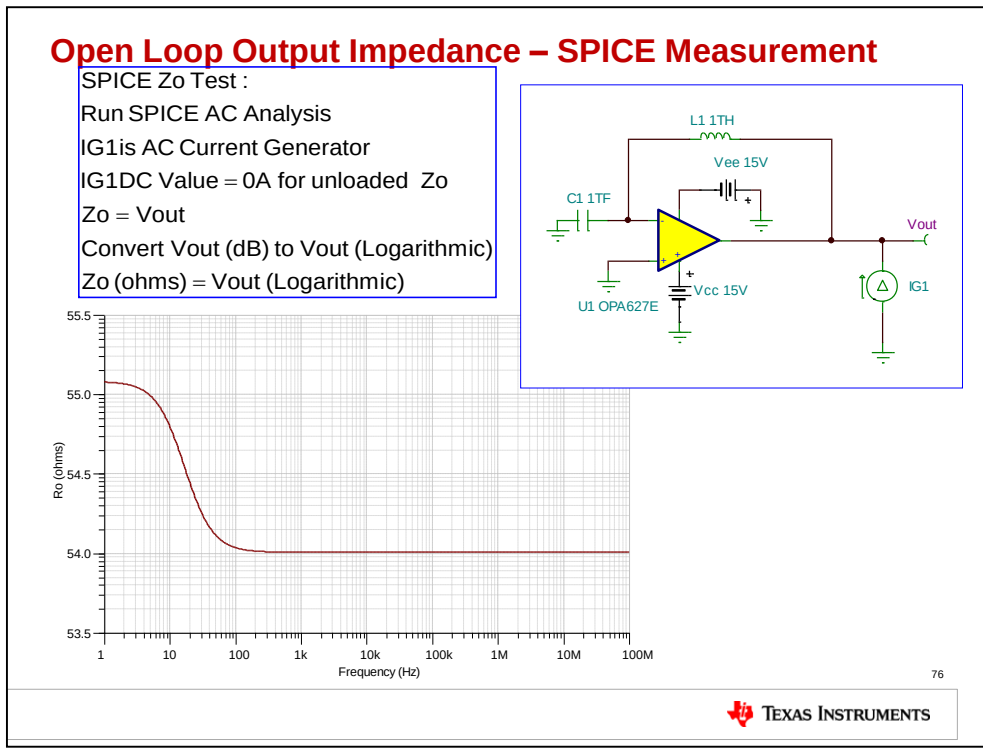


OPA2376 has Z_O



Note: **Some op amps have Z_O characteristics other than pure resistance – consult data sheet / manufacturer / SPICE Model**

Not all op amps have open loop output impedance that is purely resistive. If it is not clear in the data sheet consult the manufacturer for the true unloaded Zo curve. Check the SPICE macromodel before relying on it for stability analysis in circuits where the correct Zo is critical for stability such as capacitive loading on the op amp output. See Appendix for a more detailed discussion of “Op Amp Output Impedance”.



For many op amp application circuits is will be necessary to know the op amp Open Loop Small Signal AC Output Impedance, Zo. Often this can be obtained from the op amp data sheet. Many op amp SPICE macromodels properly model Zo. If the data sheet contains a Zo curve we can easily check the macromodel for Zo accuracy. The test circuit here uses inductor, LT, in the feedback path to act as a short for the DC Operating Point analysis. The capacitor, CT, on the – input to ground is open for DC Analysis and will be a short for all frequencies of interest during the AC Analysis. Current Generator, IG1, is set to DC Current =0 and selected as AC Current of 1. During the AC Analysis IG1 injects current into the output, Vout, and the op amp is open loop. AC Analysis reports Vout in dB over frequency as a ratio of Vout/IG1 which is Zo, in dB. To convert Zo in dB to Zo in ohms simply change the y-axis scaling from dB-Linear to logarithmic.

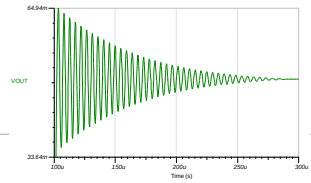
Summary for Stability

For *Stability Loop Gain Analysis* all we need is:

1) **AoI** – from op amp data sheet or macromodel
2) **Zo** – Op Amp open loop, small signal AC output impedance
   from op amp data sheet or macromodel
3) **1/β** – basic by application, modified for stability
4) **Z_Load** – given by application

Stability General Comments:

1) Stability by modifying 1/β will decrease closed loop bandwidth
2) Stability compensation can slow large signal response (charging of caps) – check it
3) Simulate AC Transfer function (Closed Loop AC Response) as final check
4) Simulate Small Signal Transient Response as final check
5) DC operation in the lab does not guarantee stability
6) Marginal stability can cause undesired overshoot and ringing
7) DC circuits can get real world transient inputs from supplies, inputs, or output
8) That ringing in your circuit is *not* your Grandmother's dial telephone



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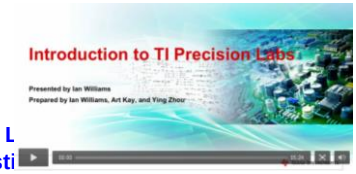
Additional Analog Design Resources:

TI Precision Designs
http://www.ti.com/ww/en/analog/precision-designs/
Three design levels from the desks of our analog experts.

TI Precision Hub blog
http://e2e.ti.com/blogs_/b/precisionhub/

Get tips, tricks and techniques from TI precision analog experts

Additional Analog Design Resources:



TI Precision Labs

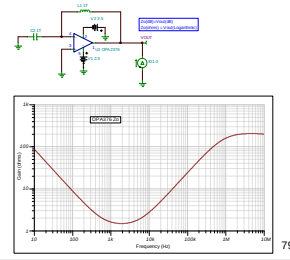
A new technical learning experience: Theory, Simulation, L
Short videos focusing on a dedicated op amp characteristi
Labs can be run with regular lab equipment or National Instruments VirtualBench.

www.ti.com/precisionlabs

TINA-TI

TINA-TI is an easy-to-use, powerful circuit simulation tool based on a SPICE engine. TINA-TI is a fully functional version of TINA, loaded with a library of TI macromodels plus passive and active models.

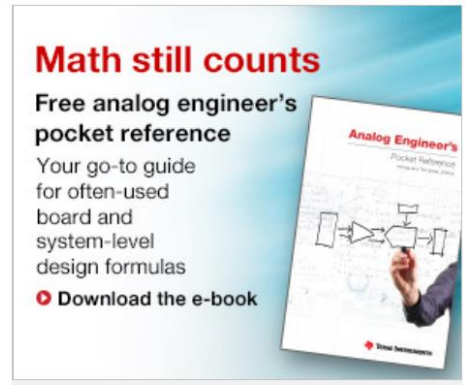
http://www.ti.com/tool/tina-ti



Additional Analog Design Resources:

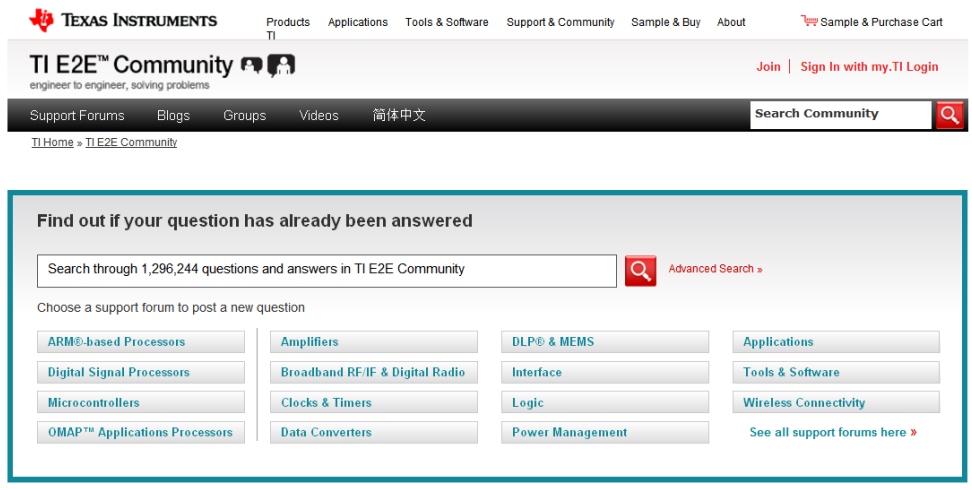
Analog Engineer's Pocket Reference

Written by op amp experts Art Kay and Tim Green, the *Analog Engineer's Pocket Reference* covers a wide variety of popular precision signal chain topics – from op amp bandwidth and stability to analog-to-digital and digital-to-analog conversions and more. Download your free copy today to put this handy, tried-and-true reference guide at your fingertips.



http://www.ti.com/lsds/ti/amplifiers-linear/precision-amplifier-support-community.page#pocketref

Technical Support: http://e2e.ti.com/



Acknowledgements

A special thanks to Jerald Graeme, whom we honorably dub "The Godfather of 1/β" for his work at Burr-Brown Corporation, et ali, in research and writing about Op Amp Stability using 1/β.

Jerald Graeme Brief Biography:
From: http://electronicdesign.com/analog/jerald-graeme

When ICs and op amps were separate devices, Jerald Graeme was among the first to develop a combined IC op amp while at Burr-Brown, in a 1968 team effort with Motorola. He designed many more op amps and video amplifiers whose precision, high speed, or low drift amplification made them a very useful component in a variety of analog applications. Nine U.S. patents and numerous foreign counterparts resulted from these designs. The internationally acknowledged authority on electronic amplifiers wrote five very popular books about op amps, the latest being Photodiode Amplifiers: Op Amp Solutions and Optimizing Op Amp Performance. The latter, subtitled "A new approach for maximizing op amp behavior in circuit designs without extensive mathematical analysis," offers design equations and models that reflect real-world op amp behavior and makes analysis of difficult-looking configurations easy. Graeme's earlier books are: Op Amps: Design and Application, Designing with Operational Amplifiers, and Amplifier Applications of Op Amps. He expects signal processing with op amps to be the domain of digital devices, but they will still require an analog interface to integrate with real-world items like process control or avionics.

Jerald Graeme Books:
http://www.amazon.com/Jerald-G.-Graeme/e/B001HO9X60

Appendix

Appendix Index

Appendix Index

Appendix No.	Title	Description/*Stability* Technique	When to use the *Stability* Technique
1	Op Amp Output Impedance	Zo vs Zout difference and datasheet curves	Zo is a key parameter for stability analysis
2	Pole and Zero: Magnitude and Phase on Bode Plots	Closed loop magnitude and phase shifts of a signal frequency due to poles and zeroes on a Bode Plot	Magnitude and phase shift at a frequency of interest for closed loop poles and zeroes
3	Dual Feedback Paths and 1/β	How to avoid problems when using dual feedback paths for stability compensation	Key tool in analyzing op amp circuits that use dual feedback for stability
4	Non-Loop Stability Problems	Oscillations and causes not seen in loop gain stability simulations	Check all designs to avoid oscillations that do not show up in SPICE simulation
5	Riso (Output Cload)	*Stability:* Isolation resistor with feedback at op amp	Output Cload, Note: accuracy of output is dependent upon load current
6	High Gain and CF (Output Cload)	*Stability* : High gain circuits and a feedback capacitor	Output Cload, closed loop gain >20dB
7	CF Non-Inverting (Input Cload)	*Stability* : Non-inverting gain and feedback capacitor	Input Cload, non-inverting gain, large value input resistor
8	CF Inverting (Input Cload)	*Stability:* Inverting gain and feedback capacitor	Input Cload, non-inverting gain, large value input resistor, photodiode type circuits
9	Noise Gain Inverting and Non-Inverting (Output Cload)	*Stability:* Noise Gain added by input R-C network	Output Cload, closed loop gain <20dB
10	Noise Gain and CF (Output Cload)	*Stability:* Noise Gain (input R-C) and feedback capacitor	Output Cload, Loaded Aol has a second pole located >20dB
11	Output Pin Compensation (Output Cload)	*Stability:* Series R-C on op amp output to ground	Output Cload, no access to -input, monolithic, integrated difference amplifiers, complex feedback where not practical to use -input
12	Riso w/Dual Feedback (Output Cload) - Zo, 1/β, Aol Technique	*Stability:* Isolation resistor with two feedback paths - analysis by Zo, 1/β, and Aol technique	Output Cload, some additional Vdrop across isolation resistor is okay, accurate Vout at load
13	Riso w/Dual Feedback (Output Cload) - 1/β, Loaded Aol Technique	*Stability:* Isolation resistor with two feedback paths - analysis by 1/β, and Loaded Aol technique	Output Cload, some additional Vdrop across isolation resistor is okay, accurate Vout at load
14	Riso w/Dual Feedback plus RFx (Output Cload) - 1/β, Loaded Aol Technique	*Stability:* Isolation resistor with two feedback paths - analysis by 1/β, and Loaded Aol technique	Output Cload, some additional Vdrop across isolation resistor is okay, accurate Vout at load. RFx can provide wider BW control at output load.
15	Discrete Difference Amplifier (Output Cload)	*Stability:* Balanced use of noise gain (series R-C)	Output Cload, difference amp configuration, any closed loop gain

1) Op Amp Output Impedance

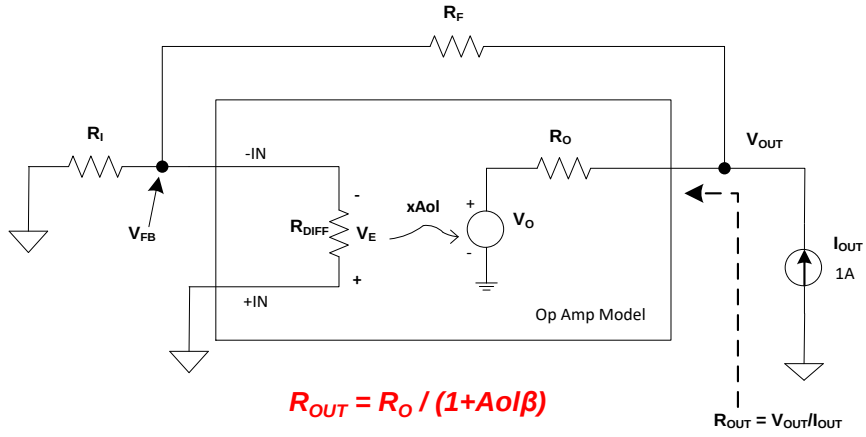
Open Loop (Z_O)
&
Closed Loop (Z_{OUT})

Op Amps and "Output Resistance"

Definition of Terms:

R_O = Op Amp ***Open Loop*** Output Resistance

R_{OUT} = Op Amp ***Closed Loop*** Output Resistance



$R_{OUT} = R_O / (1+AolB)$

$R_{OUT} = V_{OUT}/I_{OUT}$

87

From: Frederiksen, Thomas M. Intuitive Operational Amplifiers. McGraw-Hill Book Company. New York. Revised Edition. 1988.

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R_O is the Open Loop Output Resistance of an op amp. R_{OUT} is defined as the Closed Loop Output Resistance of an op amp. This slide emphasizes the important difference between these two different resistances.

R_O and R_{OUT} are related. R_{OUT} is R_O reduced by loop gain. This slide will define the op amp model used for the derivation of R_{OUT} from R_O. This simplified op amp model focuses solely on the basic DC characteristics of an op amp. A high input resistance (100mΩ to GΩ), R_{DIFF} develops an error voltage across it, V_E, due to the voltage differences between -IN and +IN. The error voltage , V_E, is amplified by the open loop gain factor Aol and becomes V_O. In series with V_O to the output, V_{OUT}, is R_O, the open loop output resistance.

Derivation of R_{OUT} (Closed Loop Output Resistance)

1) $\beta = V_{FB} / V_{OUT} = [V_{OUT} (R_I / \{R_F + R_I\})]/V_{OUT} = R_I / (R_F + R_I)$

2) $R_{OUT} = V_{OUT} / I_{OUT}$

3) $V_O = -V_E$ Aol

4) $V_E = V_{OUT} [R_I / (R_F + R_I)]$

5) $V_{OUT} = V_O + I_{OUT}R_O$

6) $V_{OUT} = -V_E$Aol + $I_{OUT}R_O$ *Substitute 3) into 5) for V_O*

7) $V_{OUT} = -V_{OUT} [R_I/(R_F + R_I)]$ Aol+ $I_{OUT}R_O$ *Substitute 4) into 6) for V_E*

8) $V_{OUT} + V_{OUT} [R_I/(R_F + R_I)]$ Aol = $I_{OUT}R_O$ *Rearrange 7) to get V_{OUT} terms on left*

9) $V_{OUT} = I_{OUT}R_O / \{1+[R_IAol/(R_F+R_I)]\}$ *Divide in 8) to get V_{OUT} on left*

10) $R_{OUT} = V_{OUT}/I_{OUT} =[I_{OUT}R_O / \{1+[R_I$Aol $/ (R_F+R_I)]\}] / I_{OUT}$

Divide both sides of 9) by I_{OUT} to get R_{OUT} [from 2)] on left

11) $R_{OUT} = R_O / (1+$Aol$\beta)$ *Substitute 1) into 10)*

→ $R_{OUT} = R_O / (1+$Aol$\beta)$ ←

88

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Using the op amp model in the previous slide we can solve for R_{OUT} as a function of R_O and Aolβ. We see that Aolβ, loop gain, reduces R_O so that the output resistance of the op amp with feedback, R_{OUT}, will be much lower than R_O, for large values of Aolβ.

R_{OUT} vs R_O

- R_O does *NOT* change when Closed Loop feedback is used
- R_{OUT} is the effect of R_O, Aol, and β controlling V_O
  - ✓ Closed Loop feedback (β) forces V_O to increase or decrease as needed to accommodate V_O loading
  - ✓ Closed Loop (β) increase or decrease in V_O appears at V_{OUT} as a reduction in R_O
  - ✓ R_{OUT} increases as Loop Gain (Aolβ) decreases

89

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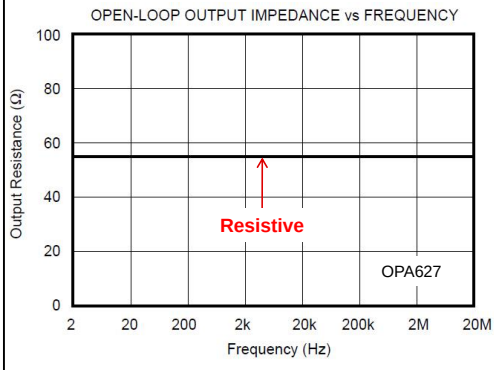
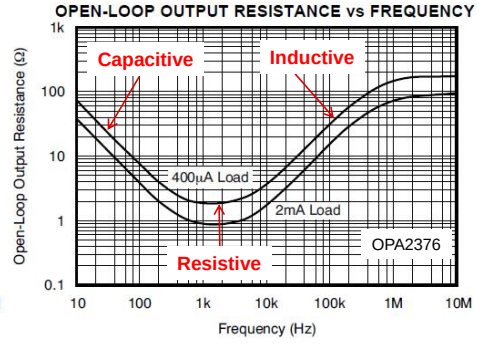
This slide emphasizes the differences between R_O and R_{OUT}.

When R_O is really Z_O!!

OPA627 has R_O

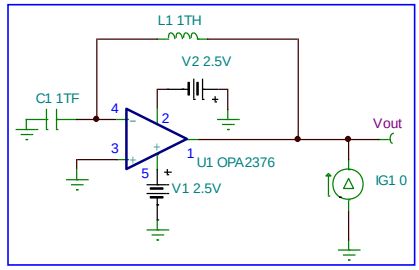


OPA2376 has Z_O

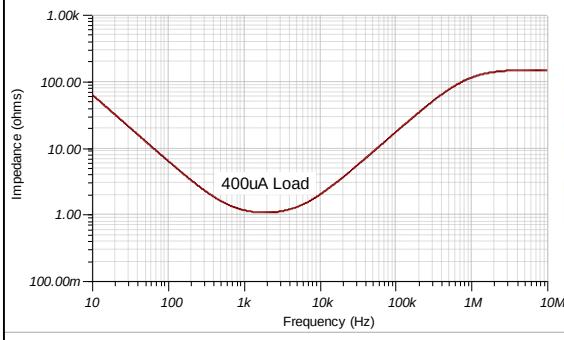


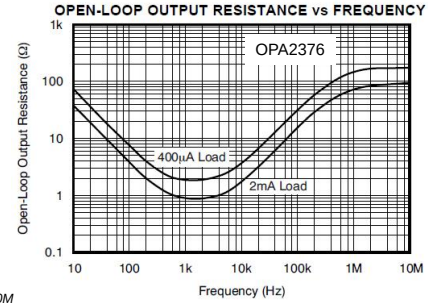
Note: **Some op amps have Z_O characteristics other than pure resistance – consult data sheet / manufacturer**

With Complex Z_O, Accurate Models are Key!



SPICE Test of Op Amp Macro Zo :
Run SPICE AC Analysis
IG1is AC Current Generator
IG1DC Value = 0A for unloaded Zo
Zo = Vout
Convert Vout (dB) to Vout (Logarithmic)
Zout (ohms) = Vout (Logarithmic)





Some Data Sheets Specify Z_{OUT} *NOT* Z_O

Recognize R_{OUT} instead of R_O:
R_{OUT} inversely proportional to Aol
R_{OUT} typically <100Ω at high frequency

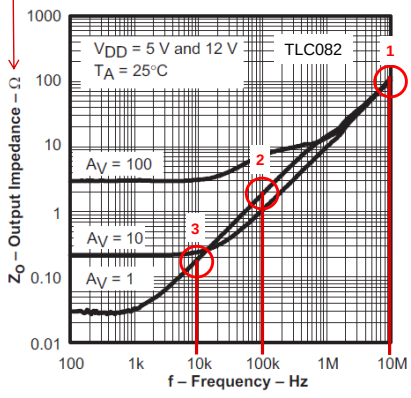
R_{OUT} is Inverse of Aol :

$$R_{OUT} = \frac{R_O}{1 + Aol\beta}$$

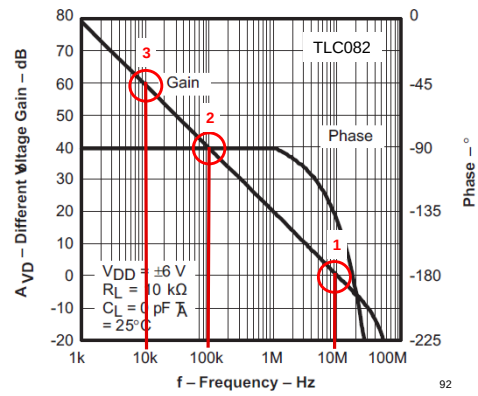
$$R_{OUT} \propto \frac{1}{Aol}$$

This is really Z_{OUT} or R_{OUT}!

OUTPUT IMPEDANCE vs FREQUENCY



DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY



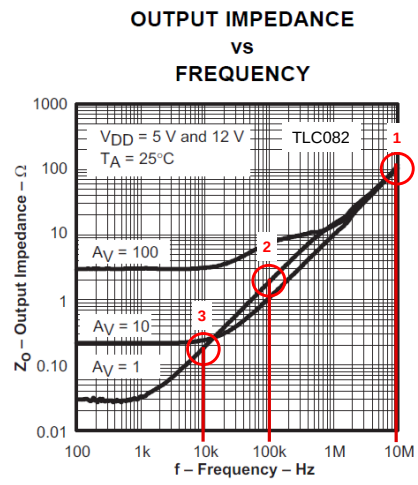
Some Data Sheets Specify Z_{OUT} *NOT* Z_O

Point	frequency (Hz)	Aol (dB)	R_{OUT} (A_V=1) Datasheet (ohms)	R_{OUT} (A_V=1) Computed (ohms)
1	10M	0	100	$R_O = 200$
2	100k	40	2	2
3	10k	60	0.2	0.2

Compute R_o from R_{OUT} where $Aol\beta = 1$(0dB):
$R_{OUT} = 100\Omega$ for $A_v = 1$, $f = 10MHz$, $Aol\beta = 1$(0dB)

$$R_{OUT} = \frac{R_O}{1 + Aol\beta}$$

$$100\Omega = \frac{R_O}{1+1} \rightarrow R_O = 200\Omega$$



2) Pole and Zero:
Magnitude & Phase on Bode Plots

Formulae for Pole and Zero Calculations

Pole Magnitude for f
where :
f = **frequency of signal**
fp = **frequency of pole**

$$\text{Magnitude(dB)} = +20 \times \text{LOG}_{10} \sqrt{\frac{1}{1+\frac{f^2}{fp^2}}}$$

Pole Phase Shift for f
where :
f = **frequency of signal**
fp = **frequency of pole**

$$\text{Phase(deg)} = -\tan^{-1}\left(\frac{f}{fp}\right)$$

Zero Magnitude for f
where :
f = **frequency of signal**
fz = **frequency of pole**

$$\text{Magnitude(dB)} = +20 \times \text{LOG}_{10} \sqrt{1+\frac{f^2}{fz^2}}$$

Zero Phase Shift for f
where :
f = **frequency of signal**
fz = **frequency of pole**

$$\text{Phase(deg)} = +\tan^{-1}\left(\frac{f}{fz}\right)$$

Closed Loop Gain: Magnitude and Phase

Closed Loop Magnitude and Phase for frequency f :
where :
f = frequency of signal
fp1 = frequency of pole 1
fp2 = frequency of pole 2
fz1 = frequency of zero 1
fz2 = frequency of zero 2
K = DC Gain in V/V

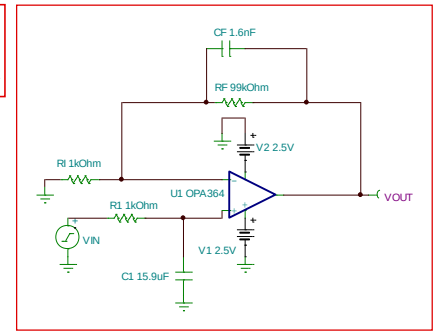
$$\text{Magnitude(dB)} = 20\times\text{LOG}_{10}K + 20\times\text{LOG}_{10}\sqrt{\frac{1}{1+\frac{f^2}{fp1^2}}} + 20\times\text{LOG}_{10}\sqrt{\frac{1}{1+\frac{f^2}{fp2^2}}} + 20\times\text{LOG}_{10}\sqrt{1+\frac{f^2}{fz1^2}} + 20\times\text{LOG}_{10}\sqrt{1+\frac{f^2}{fz2^2}}$$

$$\text{Phase(deg)} = -\tan^{-1}\left(\frac{f}{fp1}\right) - \tan^{-1}\left(\frac{f}{fp2}\right) + \tan^{-1}\left(\frac{f}{fz1}\right) + \tan^{-1}\left(\frac{f}{fz1}\right)$$

Closed Loop Gain: Magnitude and Phase

$$fp1 = \frac{1}{2\pi * R1 * C1} = \frac{1}{2\pi * 1k\Omega * 15.9\mu F} = 10.00974485Hz$$

$$fp2 = \frac{1}{2\pi * RF * CF} = \frac{1}{2\pi 99k\Omega * 1.6nF} = 1.004766055kHz$$



Closed Loop Magnitude and Phase for frequency f :
where :
f = frequency of signal
fp1 = frequency of pole 1
fp2 = frequency of pole2
K = DC Gain in V/V

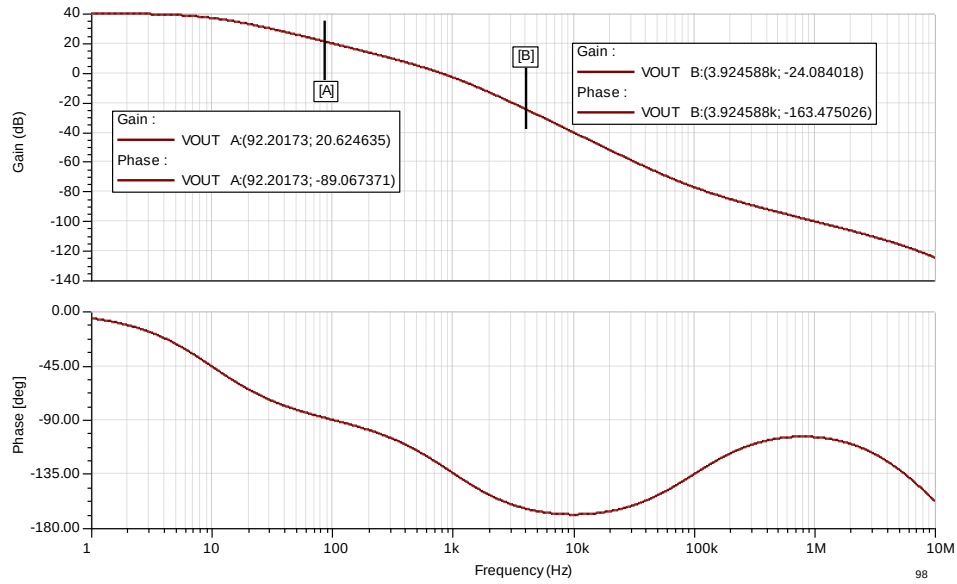
$$Magnitude(dB) = 20 \times LOG_{10}K + 20 \times LOG_{10}\sqrt{\frac{1}{1+\frac{f^2}{fp1^2}}} + 20 \times LOG_{10}\sqrt{\frac{1}{1+\frac{f^2}{fp2^2}}}$$

$$Phase(deg) = -\tan^{-1}(\frac{f}{fp1}) - \tan^{-1}(\frac{f}{fp2})$$

$$Magnitude(dB) = 20 \times LOG_{10}(100) + 20 \times LOG_{10}\sqrt{\frac{1}{1+\frac{f^2}{(10.00974485)^2}}} + 20 \times LOG_{10}\sqrt{\frac{1}{1+\frac{f^2}{(1.004766055e3)^2}}}$$

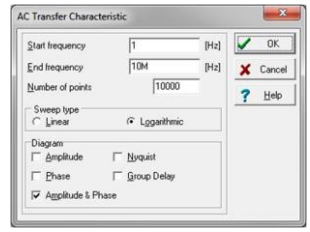
$$Phase(deg) = -\tan^{-1}(\frac{f}{10.00974485}) - \tan^{-1}(\frac{f}{1.004766055e3})$$

Closed Loop Gain: Magnitude and Phase



Spice Compared with Calculated Analysis

SPICE AC Analysis:
For best accuracy use highest resolution
i.e. maximum "Number of Points"

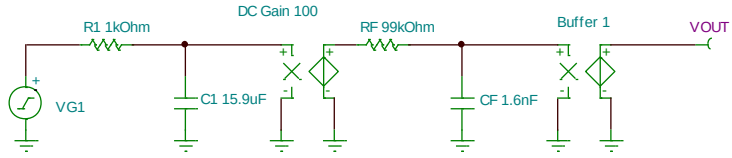


f	Magnitude	Magnitude		Phase	Phase
(Hz)	(dB)	(dB)		(deg)	(deg)
----------	***Calculated***	***SPICE***		***Calculated***	***SPICE***
9.22017300E+01	20.6263744	20.624635		-89.04706182	-89.067371
3.92458800E+03	-23.97775119	-24.084018		-165.49354967	-163.475026

Note:
1) SPICE analysis accounts for loop gain effects and closed loop phase shifts due to op amp AoI.
2) Calculated results do not account for loop gain effects and closed loop phase shifts due to op amp AoI.

Closed Loop Gain: Magnitude and Phase

SPICE Ideal Op Amp & Poles: Equivalent Circuit

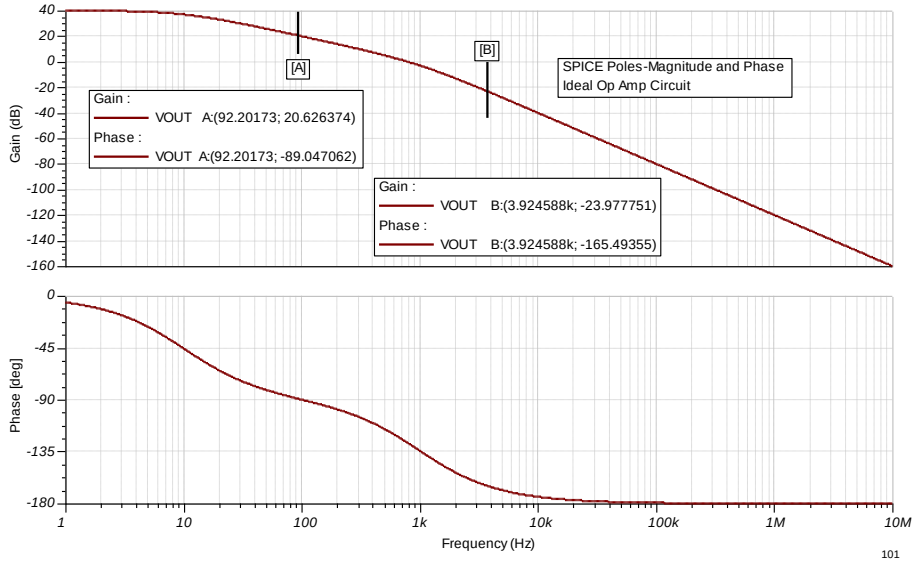


f	Magnitude	Magnitude		Phase	Phase
(Hz)	(dB)	(dB)		(deg)	(deg)
----------	Calculated	SPICE - Ideal		Calculated	SPICE - Ideal
9.22017300E+01	20.6263744	20.626374		-89.04706182	-89.047062
3.92458800E+03	-23.97775119	-23.977751		-165.49354967	-165.49355

Note:
1) SPICE - Ideal Circuit analysis matches Calculated results.
2) No loop gain effect or closed loop phase shifts due to op amp Aol.

Closed Loop Gain: Magnitude and Phase

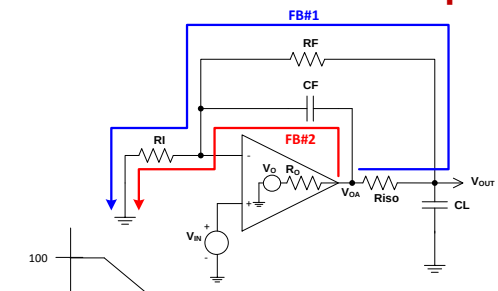
SPICE Ideal Op Amp & Poles: Equivalent Circuit



101

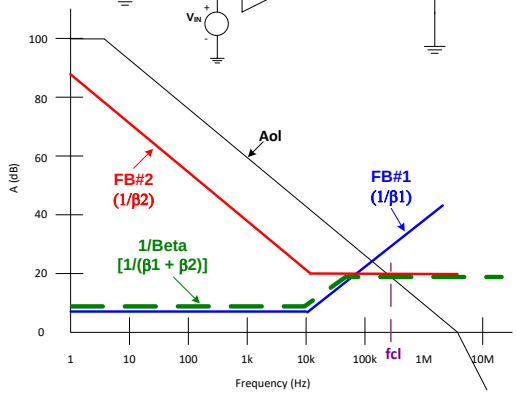
3) Dual Feedback Paths and 1/β

Dual Feedback and 1/β Concept



Analogy: Two people are talking in your ear. Which one do you hear? The one talking the loudest!

Dual Feedback: Op amp has two feedback paths talking to it. It listens to the one that feeds back the largest voltage ($\beta = V_{FB} / V_{OUT}$). This implies the smallest 1/β!



Dual Feedback Networks:

- Analyze & Plot each FB#? 1/β
- Smallest FB#? dominates 1/β
- 1/β = 1 / (β1 + β2)
- 1/β relative to V_O
  Note: V_O = Op Amp Aol Output before Ro for this Dual Feedback Example

103

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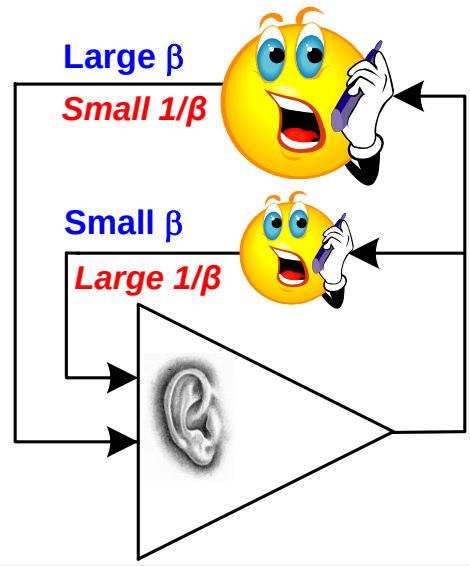
In this slide we see an op amp circuit which uses two feedback paths. The first feedback path, FB#1, is out of the op amp, through Riso and CL back through RF and RI to the –input of the op amp. The second feedback, FB#2, is out of the op amp, through CF and back to the –input of the op amp. The equivalent 1/β plots for each of these feedbacks are plotted separately. When more than one feedback path is used around an op amp the feedback path which feeds back the largest voltage to the op amp's input will become the dominant feedback path. This implies that if 1/β is plotted for each feedback that the feedback with the lowest 1/β at a given frequency will dominate at that point. Remember that the smallest 1/β implies the largest β and since $\beta = V_{FB}/V_{OUT}$, the largest β implies the most voltage fed back to the input of the op amp. An easy analogy to remember is that if two people are talking to you in one ear which person do you hear the easiest – the one talking the loudest! So the op amp will "listen" to the feedback path with the largest β or smallest 1/β. The net 1/β plot the op amp sees is the lower one at any frequency of FB#1 or FB#2.

Dual Feedback and 1/β
How will the two feedbacks combine?

Answer:

The **Largest β** (***Smallest 1/β***) will dominate!



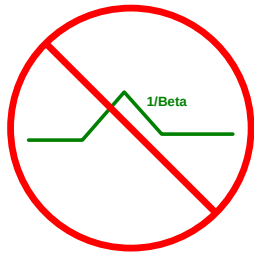
104

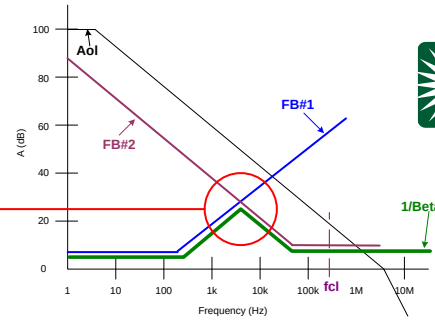
TEXAS INSTRUMENTS

When using dual feedback paths around op amp circuits the largest β path will dominate. An easy analogy to remember is that if two people are talking to you in one ear which person do you hear the easiest – the one talking the loudest! So the op amp will “listen” to the feedback path with the largest β or smallest 1/β. The net 1/β plot the op amp sees is the lower one at any frequency of FB#1 or FB#2.

Dual Feedback and the *BIG NOT*

WARNING: This can be hazardous to your circuit!





Dual Feedback and the *BIG NOT*:

1/β Slope changes from +20db/decade to -20dB/decade

- Implies a "complex conjugate pole " in the 1/β Plot with small damping ratio, ζ.
- Implies a "complex conjugate zero" in the Aolβ (Loop Gain Plot) with small damping ratio, ζ.
- +/-90° phase shift at frequency of complex zero/complex pole.
- Phase slope from +/-90°/decade slope to +/-180° in narrow band near frequency of complex zero/complex pole depending upon damping ratio, ζ.
- Complex zero/complex pole can cause *severe* gain peaking in closed loop response.

105

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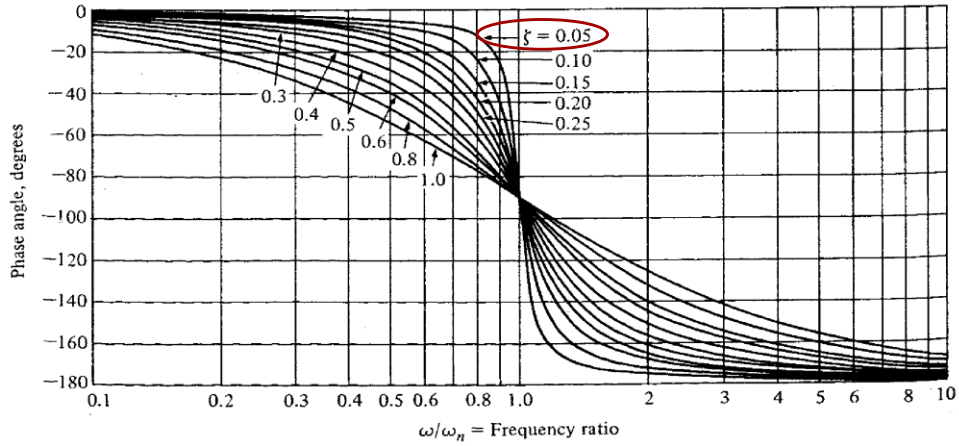
When using dual feedback paths around an op amp there is one extremely important case to avoid – the "BIG NOT". As demonstrated in this slide there op amp circuits which can result in feedback paths that create the BIG NOT, which is seen in the net 1/β plot that contains a net 1/β slope which changes from +20db/decade to -20dB/decade abruptly. This rapid change implies a complex conjugate pole in the 1/β plot with a small damping ratio, ζ , which is therefore a complex conjugate zero in the Loop Gain plot. Complex zeros and poles create a +/-90 degree phase shift at the frequency of the complex zero/complex pole. In addition the phase slope around a complex zero/complex pole can range from +/-90 degrees to +/-180 degrees in a narrow frequency band around the frequency location of the occurrence. Complex zero/complex pole occurrences can cause severe gain peaking in the closed loop op amp response. This can be very undesirable especially in power op amp circuits.

Complex Conjugate Pole Phase Example



From: Dorf, Richard C. Modern Control Systems. Addison-Wesley Publishing Company. Reading, Massachusetts. Third Edition, 1981.

106

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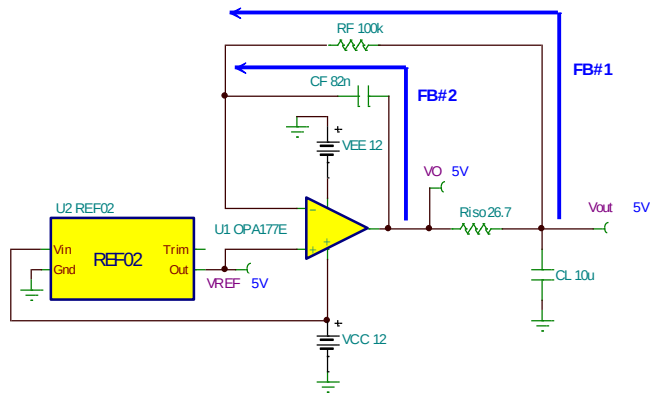
The phase plot for a complex conjugate pole is shown in this slide. It is clear that, depending upon the damping factor, the phase shift can be dramatically different than one for a simple double pole which we would expect to be -90 degree shift at the frequency and a -90 degree/decade slope (damping factor=1).

Dual Feedback and 1/β Example



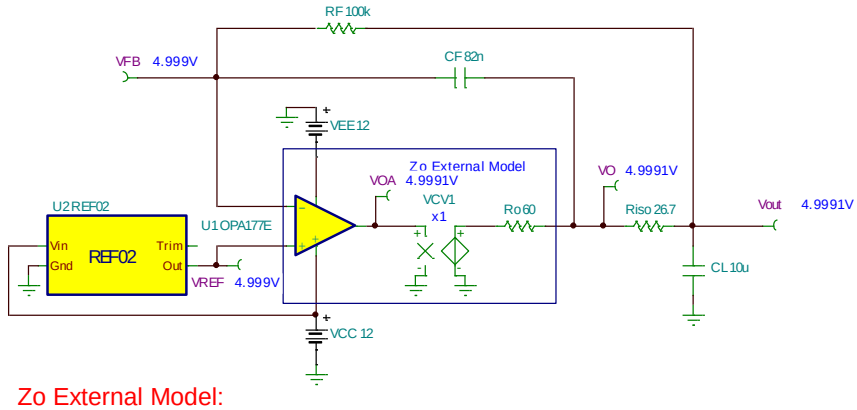
Dual Feedback:
FB#1 through RF forces accurate Vout across CL
FB#2 through CF dominates at high frequency for stability
Riso provides isolation between FB#1 and FB#2

107

TEXAS INSTRUMENTS

This Dual Feedback and 1/β example demonstrates the Riso w/Dual Feedback circuit. FB#1, through RF, provides direct feedback across the load, CL, and thereby forces Vout to equal VREF. FB#2, through CF, provides a second feedback path, which dominates at high frequency, to guarantee stable operation. Riso creates the isolation between FB#1 and FB#2.

Zo External Model for Dual Feedback Analysis



Zo External Model:

VCV1 ideally isolates U1 so U1 only provides data sheet AoI

Set Ro to match measured Ro

Analyze with unloaded Ro (largest Ro) which creates worst instability

Use 1/β on AoI stability analysis

1/β, taken from VOA will include the effects of Zo, Riso and CL

108

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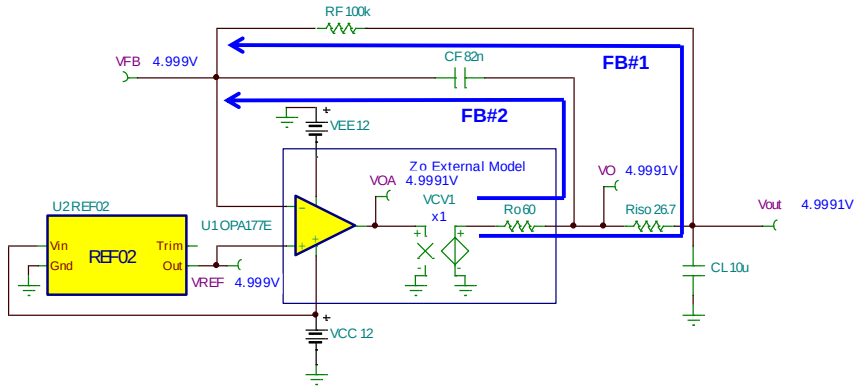
The Zo External Model shown above allows for us to measure the effects of Zo interacting with Riso, CL, RF, and CF on 1/Beta. In our Zo External Model set Ro = Ro for OPA177, measured to be 60 ohms. The voltage-controlled–voltage-source, VCV1 isolated our op amp macromodel, U1, from Ro, Riso, CL, CF, and RF. VCV1 is set to x1 to keep the data sheet AoI gain the same. Remove any large DC load since we want to analyze this circuit under worst case stability conditions which will be with CL only and our calculated unloaded Zo (Ro=60 ohms for this case). VOA is an internal node to the op amp which in the real world cannot be measured. It is also not easy to access this internal node on many SPICE macromodels. 1/Beta is analyzed relative to VOA to include the effects of Ro, Riso, CL, CF, and RF. Final stability simulation in SPICE, without using the Zo External Model cannot plot 1/Beta but can plot Loop Gain to confirm our analysis using the ZO External Model.

Dual Feedback, FB#1 And FB#2



FB#1 and FB#2 1/ β Analysis:

There is only one net voltage fed back as β to the -input of the op amp

β_net = β_FB#1 + β_FB#2

This implies that the largest β will dominate → smallest 1/ β will dominate

Analyze FB#1 with CF = open since it will only dominate at high frequencies

Analyze FB#2 with CL = short since it is at least 10x CF

109

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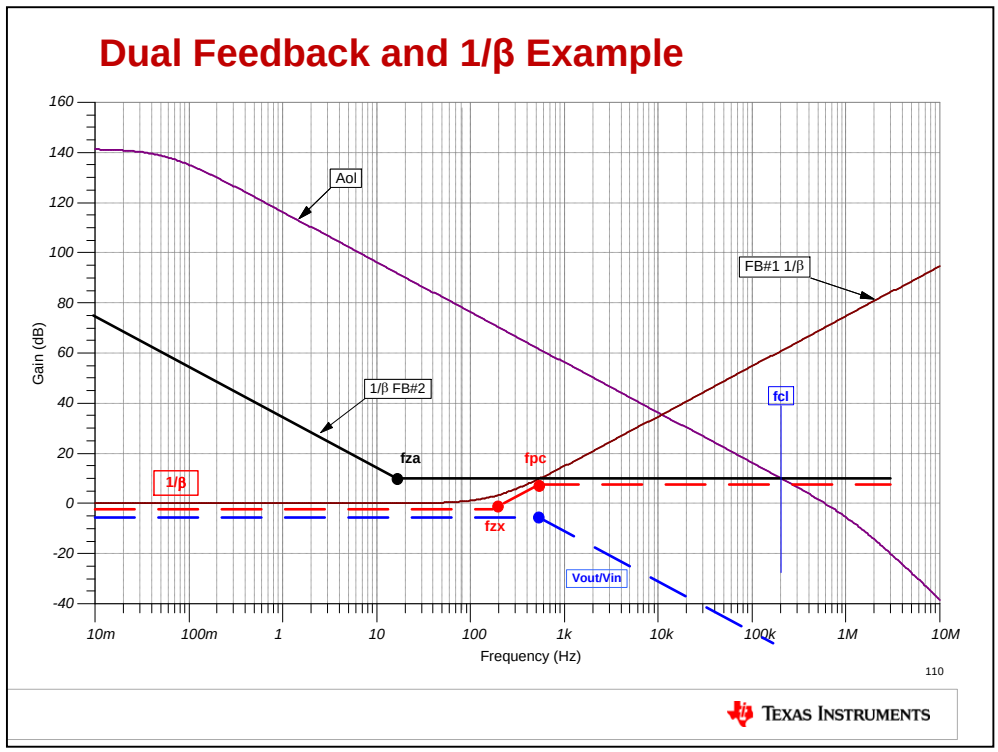
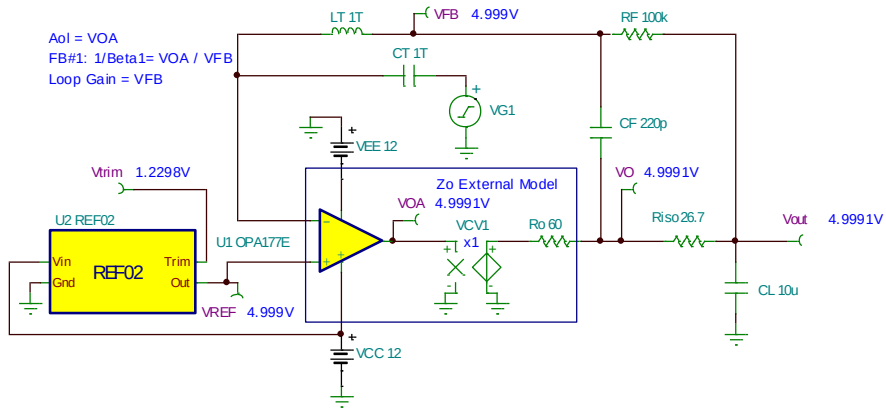
For this Riso with Dual Feedback topology can analyze each feedback path, FB#1 and FB#2 independently and plot their resulting 1/β plots on the Aol curve of the op amp. The net 1/β the op amp will respond to will be the lowest 1/β of either FB#1 or FB#2 at any point in frequency.



For our Dual Feedback example we see the 1/β plotted for each feedback path, FB#1 and FB#2, independently with the net 1/β being the lower of the two that any point in frequency.

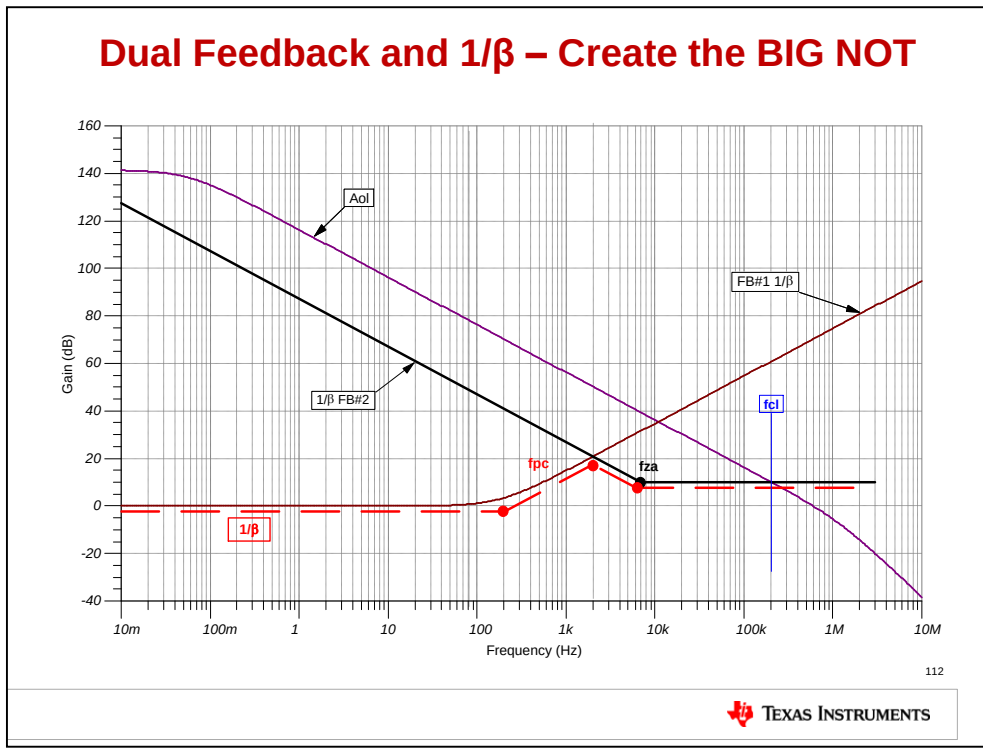
Dual Feedback and 1/β – Create the BIG NOT



111

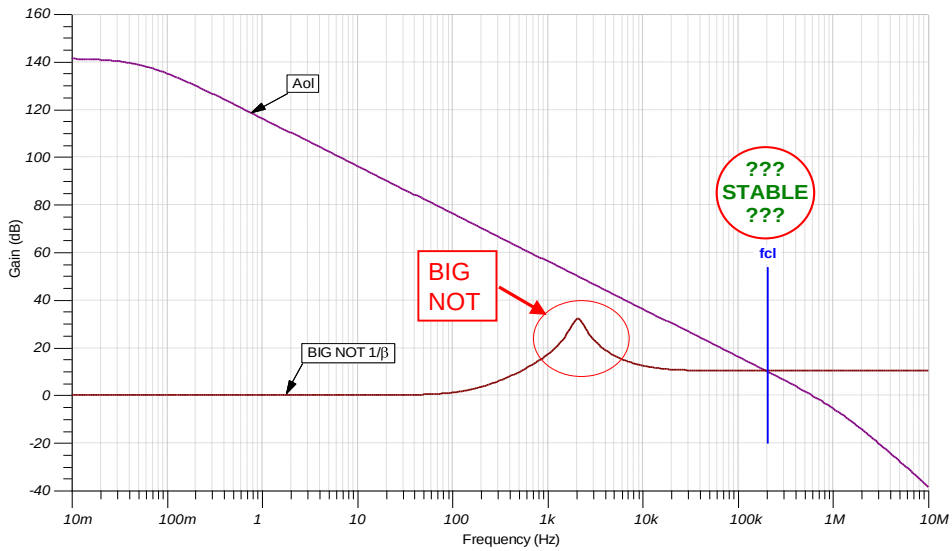
TEXAS INSTRUMENTS

We will use the circuit above to purposely create the BIG NOT.



By adjusting FB#2 improperly we are able to create the BIG NOT in the net 1/β plot.

Dual Feedback and 1/β – Create the BIG NOT



BIG NOT 1/β: At fcl rate-of-closure rule-of-thumb says circuit is stable but is it?

113

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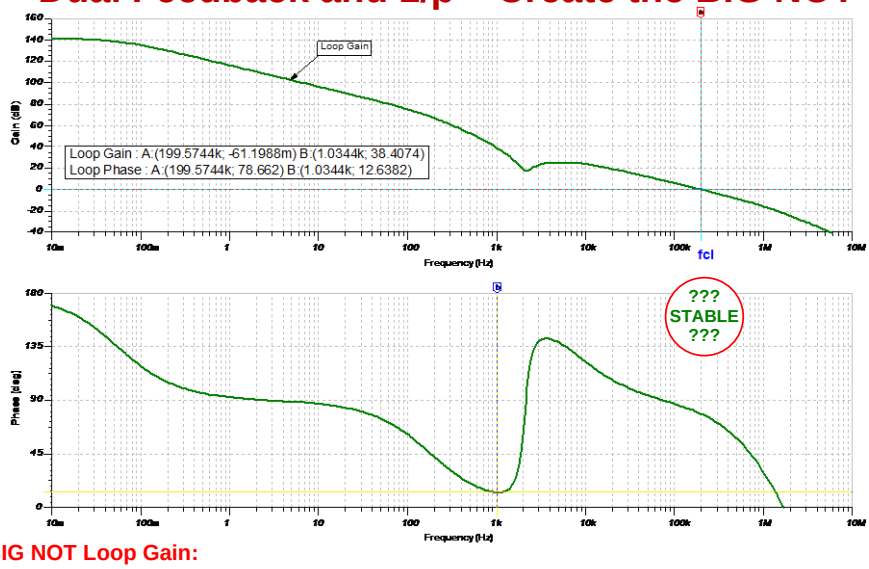
SPICE analysis of our BIG NOT circuit confirms we have created the BIG NOT in the 1/β plot.

Dual Feedback and 1/β – Create the BIG NOT



BIG NOT Loop Gain:

Loop Gain phase shift >135 degrees (<45 degrees from 180 degree phase shift) for frequencies <fcl which violates the loop gain phase buffer rule-of-thumb. But is it stable? 114

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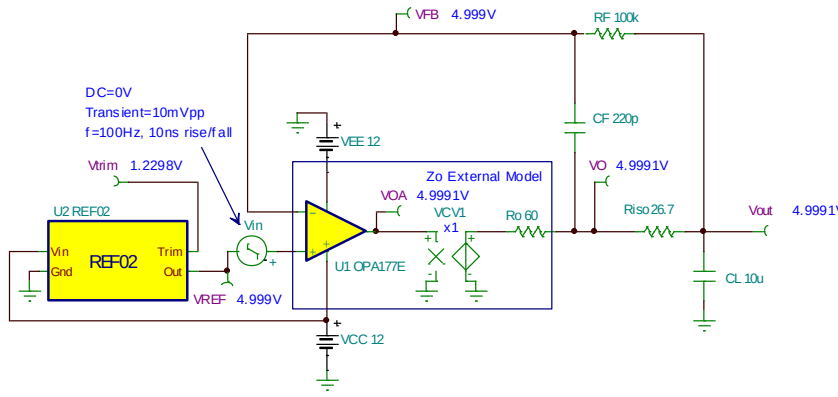
Loop gain confirms that our BIG NOT circuit has a very abrupt phase shift around 2kHz.

Dual Feedback and 1/β – Create the BIG NOT

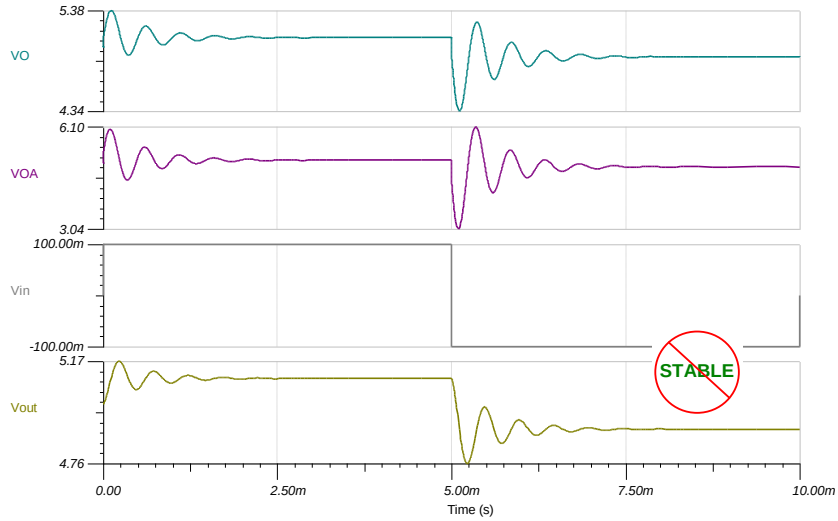


115

TEXAS INSTRUMENTS

We will use this circuit to run a transient closed loop analysis to see how our BIG NOT circuit would perform in the real world.

Dual Feedback and 1/β – Create the BIG NOT



BIG NOT Transient Stability Test:

Excessive ringing and marginal stability are apparent. Real world implementation and use may cause even more severe oscillations. We do not want this in production!

116

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A closed loop transient test of our BIG NOT circuit shows we do not end up with desirable results for a disturbance in the op amp circuit.

4) Non-Loop Stability Problems

Non-Loop Stability

- **Loop Frequencies**
- **RB+**
- **PCB Traces**
- **Supply Bypass**
- **Ground Loops**
- **Output Stage Oscillations**

Non-Loop Stability

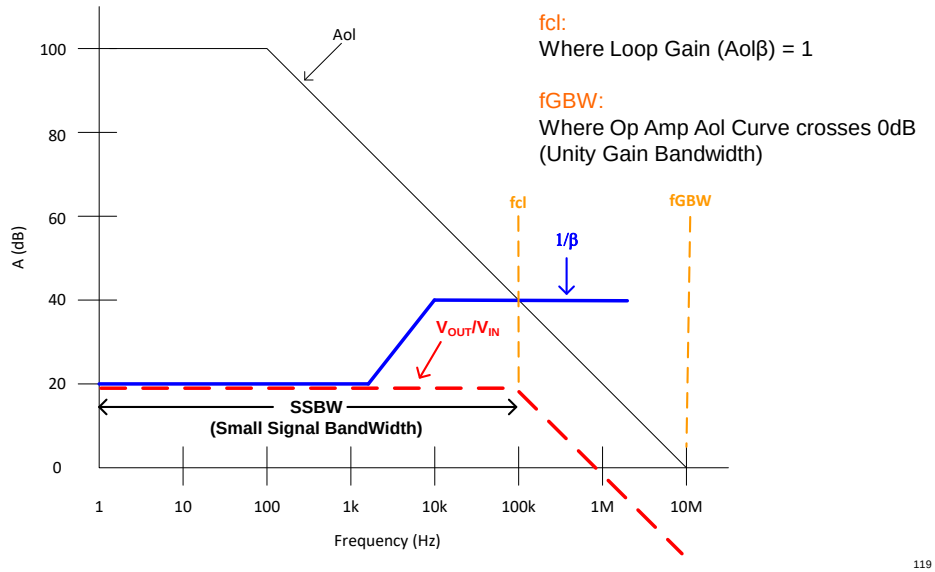
Oscillations NOT predicted by Loop Gain (Aolβ) Analysis

or

SPICE Simulations

There are common Non-Loop Stability issues we need to be aware of.

Non-Loop Stability: Loop Frequency Definitions



119

TEXAS INSTRUMENTS

To clarify Non-Loop Stability issues we see above that oscillations at any frequency beyond fcl ARE NOT Loop Stability issues that are predictable by Loop Gain Analysis or SPICE simulations.

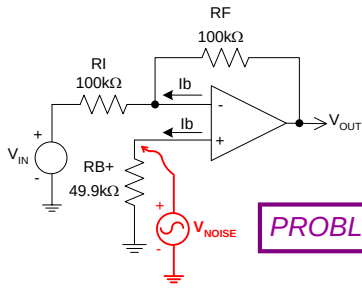
Non-Loop Stability: ? Diagnostic Questions ?

- **Frequency of oscillation (fosc)?**
- **When does the oscillation occur?**
  - **Oscillates Unloaded?**
  - **Oscillates with V_{IN}=0?**

To help easily diagnose what the cause of instability is we need to know the answers to a few simple questions as shown above.

Non-Loop Stability: RB+ Resistor

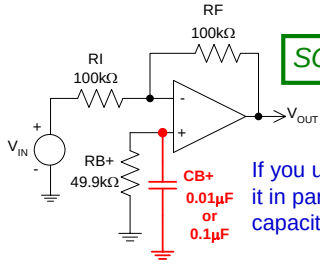
- ✓ fosc < fGBW
- ✓ oscillates unloaded? -- may or may not
- ✓ oscillates with V_{IN}=0? -- may or may not



PROBLEM

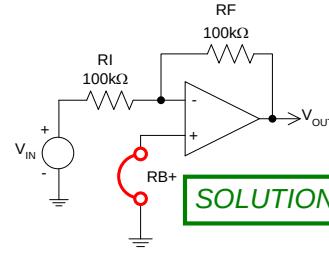
RB+ is Ib current match resistor to reduce Vos errors due to Ib.

RB+ can create high impedance node acting as antenna pickup for unwanted positive feedback.



SOLUTION

If you use RB+ bypass it in parallel with 0.1µF capacitor.



SOLUTION

Many Op Amps have low Ib so error is small. Evaluate DC errors w/o RB+.

121

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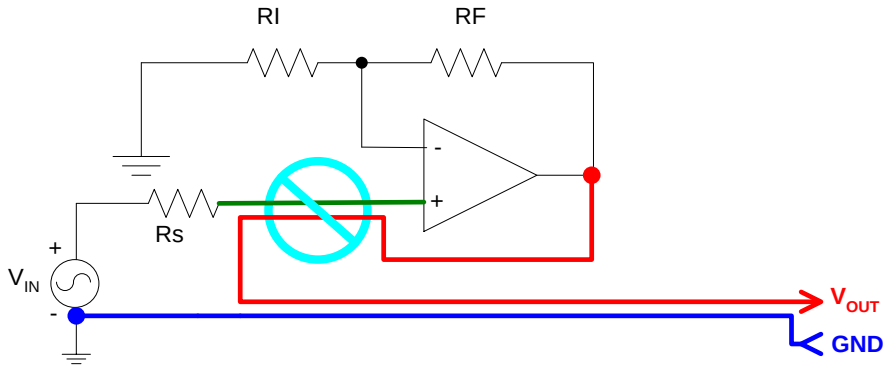
The infamous input bias impedance matching resistor can become a problem for AC frequencies if proper design considerations are not used.

Non-Loop Stability: PCB Traces

- ✓ fosc ≤ fGBW
- ✓ oscillates unloaded? -- may or may not
- ✓ oscillates with V_{IN}=0? -- may or may not



DO NOT route high current, low impedance output traces near high impedance input traces. Unwanted positive feedback path.

DO route high current output traces adjacent to each other (on top of each other in a multi-layer PCB) to form a twisted pair for EMI cancellation.

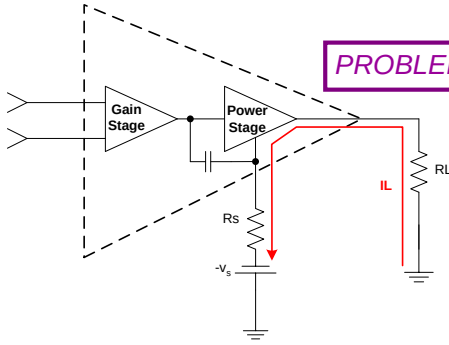
122

Texas Instruments

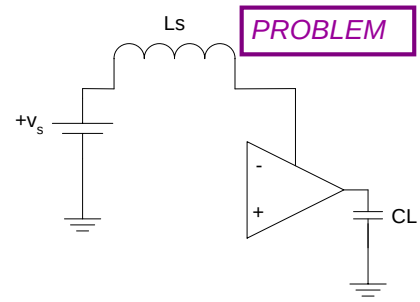
When dealing with high current output traces we need to take the necessary precautions to keep low impedance output traces away from high impedances input traces.

Non-Loop Stability: Supply Lines

- ✓ fosc ≤ fGBW
- ✓ oscillates unloaded? -- no
- ✓ oscillates with V_{IN}=0? -- may or may not



Load current, IL, flows through power supply resistance, Rs, due to PCB trace or wiring. Modulated supply voltages appear at Op Amp Power pins. Modulated signal couples into amplifier which relies on supply pins as AC Ground.



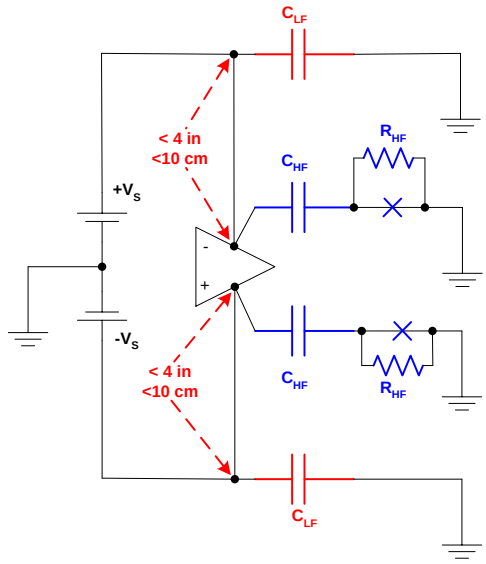
Power supply lead inductance, Ls, interacts with a capacitive load, CL, to form an oscillatory LC, high Q, tank circuit.

123

TEXAS INSTRUMENTS

Supply lines can present Non-Loop Stability problems as shown above.

Non-Loop Stability: Proper Supply Line Decouple



SOLUTION

C_{LF}: Low Frequency Bypass

10µF / Amp Out (peak)

Aluminum Electrolytic or Tantalum

< 4 in (10cm) from Op Amp

C_{HF}: High Frequency Bypass

0.1µF Ceramic

Directly at Op Amp Power Supply Pins

R_{HF}: *Provisional* Series C_{HF} Resistance

$1\Omega \leq R_{HF} \leq 10\Omega$

Highly Inductive Supply Lines

124

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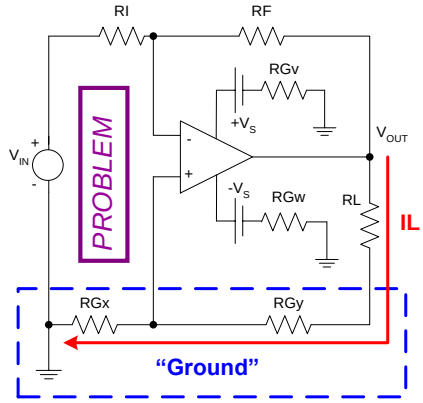
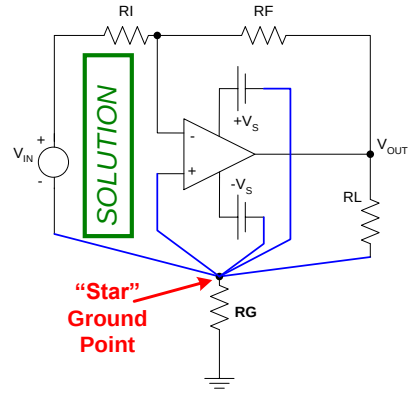
Solutions to power supply line problems are easy and good design practice in general as shown above.

Non-Loop Stability: Ground Loops

- ✓ fosc < fGBW
- ✓ oscillates unloaded? -- no
- ✓ oscillates with V_{IN}=0? -- yes





Ground loops are created from load current flowing through parasitic resistances. If part of V_{OUT} is fed back to Op Amp +input, positive feedback and oscillations can occur.

Parasitic resistances can be made to look like a common mode input by using a "Single-Point" or "Star" ground connection.

125

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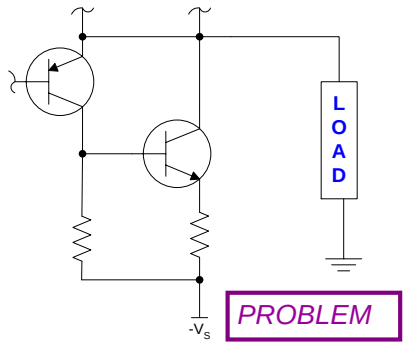
Grounding can also present Non-Loop Stability problems much like power supply line problems as we see here. Again the solution is good design practice.

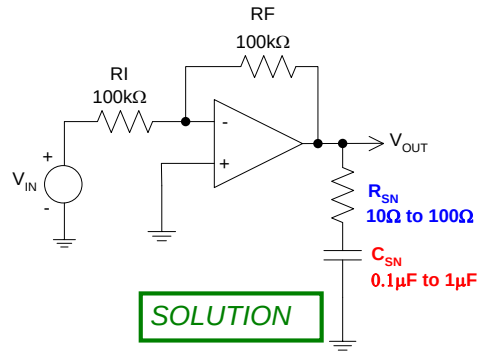
Non-Loop Stability: Output Stages

- ✓ fosc > fGBW
- ✓ oscillates unloaded? -- no
- ✓ oscillates with V_{IN}=0? -- no



PROBLEM

Some Op Amps use composite output stages, usually on the negative output, that contain local feedback paths. Under reactive loads these output stages can oscillate.



SOLUTION

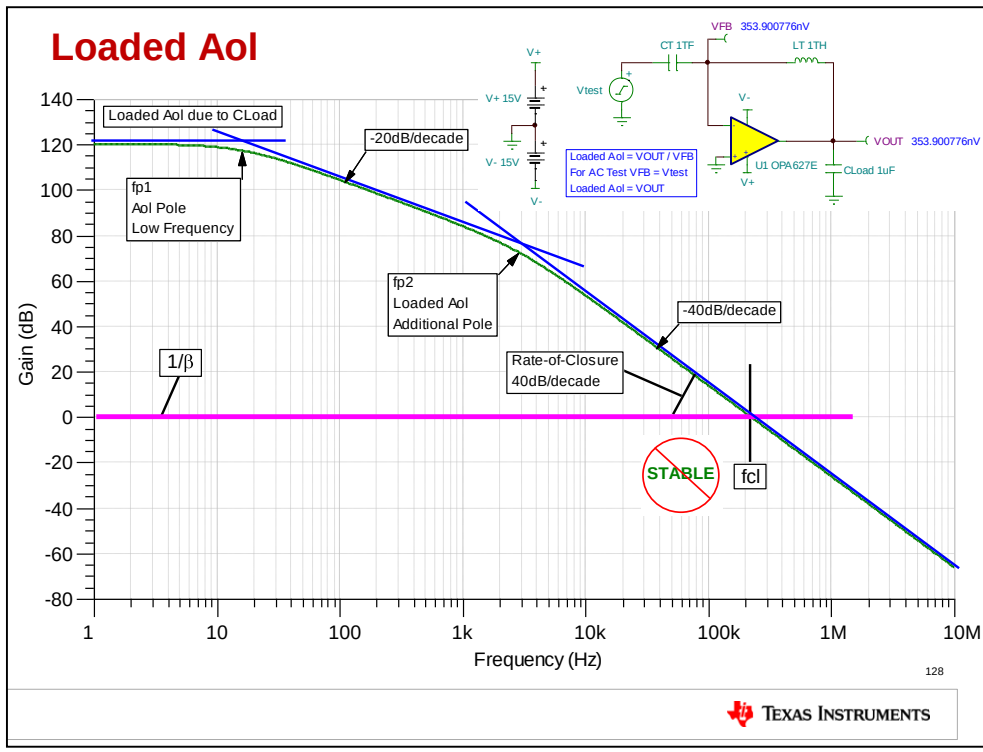
The Output R-C Snubber Network lowers the high frequency gain of the output stage preventing unwanted oscillations under reactive loads.

126

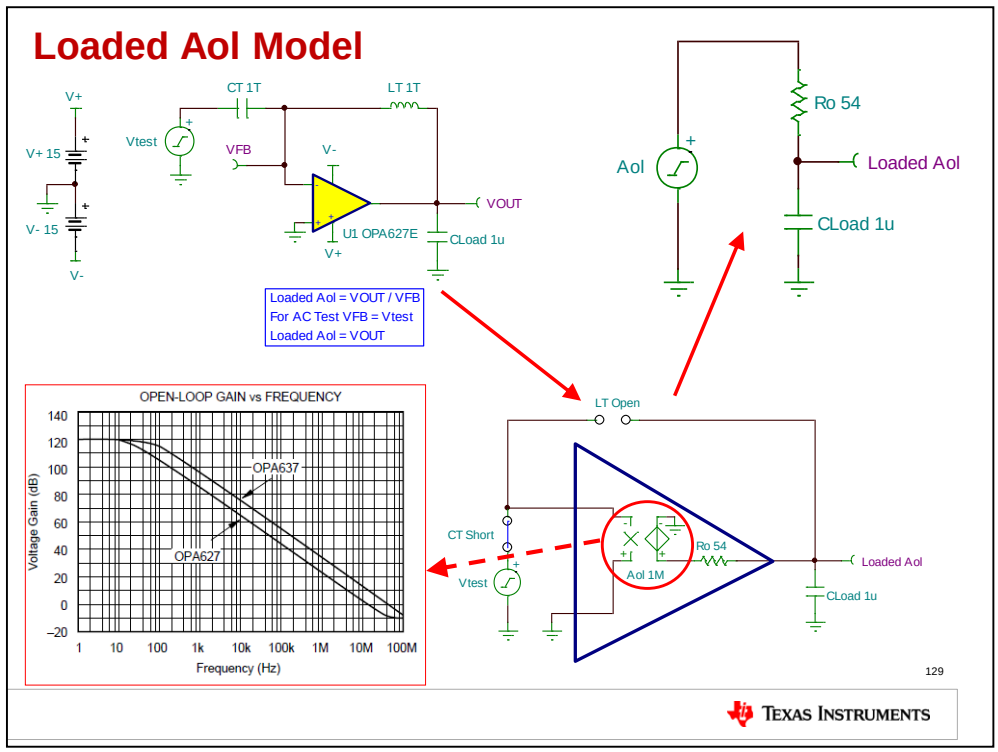
TEXAS INSTRUMENTS

The last common Non-Loop stability problem has to do with Semiconductor IC output stage topologies in Op Amps as shown. Again the solution is fairly simple if it is designed in up front.

5) Riso (Output Cload)

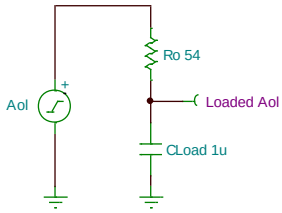


A loop gain analysis circuit can be used to analyze the “Loaded Aol” due to CLoad. As shown here the “Loaded Aol” curve due to CLoad, 1uF, has an additional pole in it around 3kHz, fp2. fp1 is the original pole in the Aol curve of the op amp before CLoad is applied. Since the circuit is running as a unity gain follower 1/β is 0dB and at fcl, where 1/β intersects the Loaded Aol curve we see a 40dB/decade rate-of-closure which is UNSTABLE by our rate-of-closure criteria.



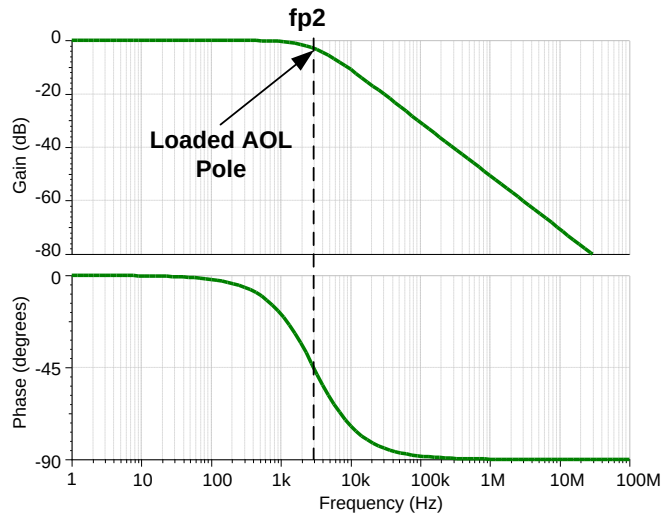
Our stability analysis of the effects of capacitive loading on an op amp will be simplified by the introduction of the “Loaded Aol Model”. As shown in this slide the data sheet Aol curve is followed by the op amp output resistance, Ro. The capacitive load, CLoad, in conjunction with Ro will form an additional pole in the Aol plot and may be represented by a new “Loaded Aol” plot. The Ro-CLoad network form the “Aol Load” on the original op amp “Aol”.

Loaded Aol Model



Loaded Aol Pole Equation

$$fp2 = \frac{1}{2 * \pi * Ro * CLoad}$$



130

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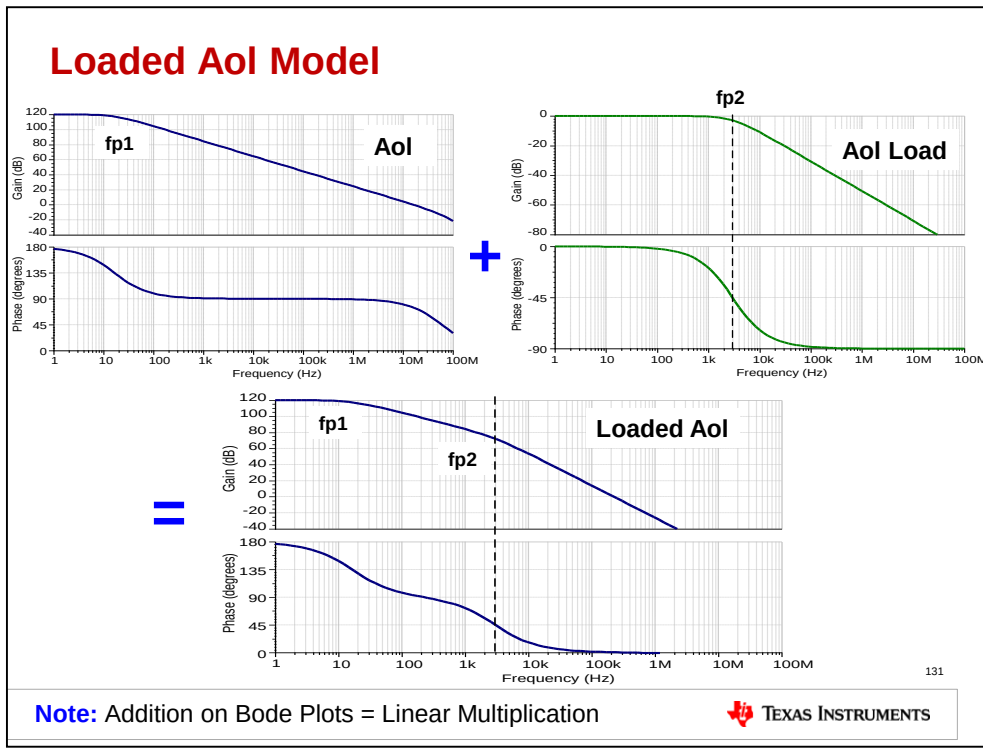
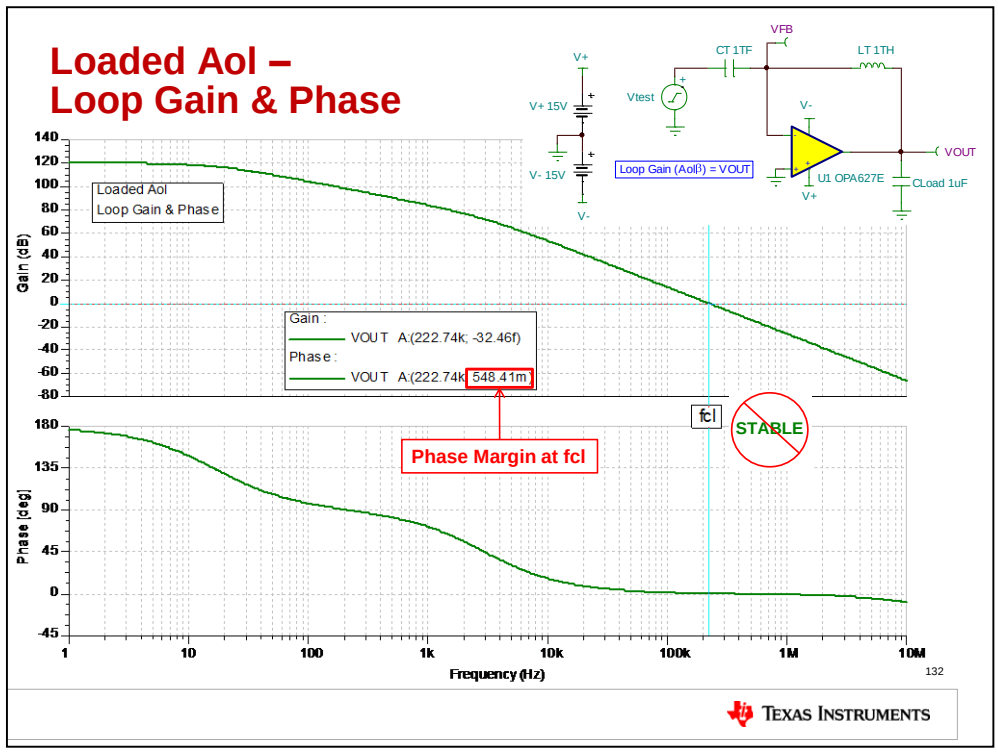
The data sheet Aol is loaded by the Ro-CLoad load network as shown here. The additional pole, fp2, due to Ro and CLoad is computed here.



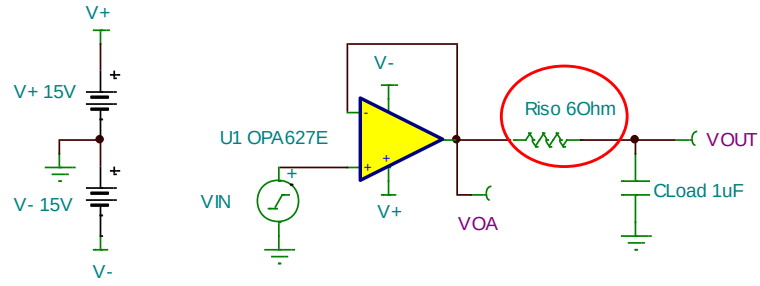
The op amp original “Aol” is “multiplied” by the “Aol Load” to yield the resultant “Loaded Aol” curve. On dB plots linear multiplication is performed by adding the curves in dB. As shown above it becomes easy to see the resultant “Loaded Aol” by adding the op amp original “Aol” plus the “Aol Load” formed by Ro-CLoad.



The Loaded Aol caused by CLoad, 1uF, will result in Loop Gain phase margin at fcl of only 0.548 degrees. This is definitely and UNSTABLE circuit as it stands here.

Riso Compensation

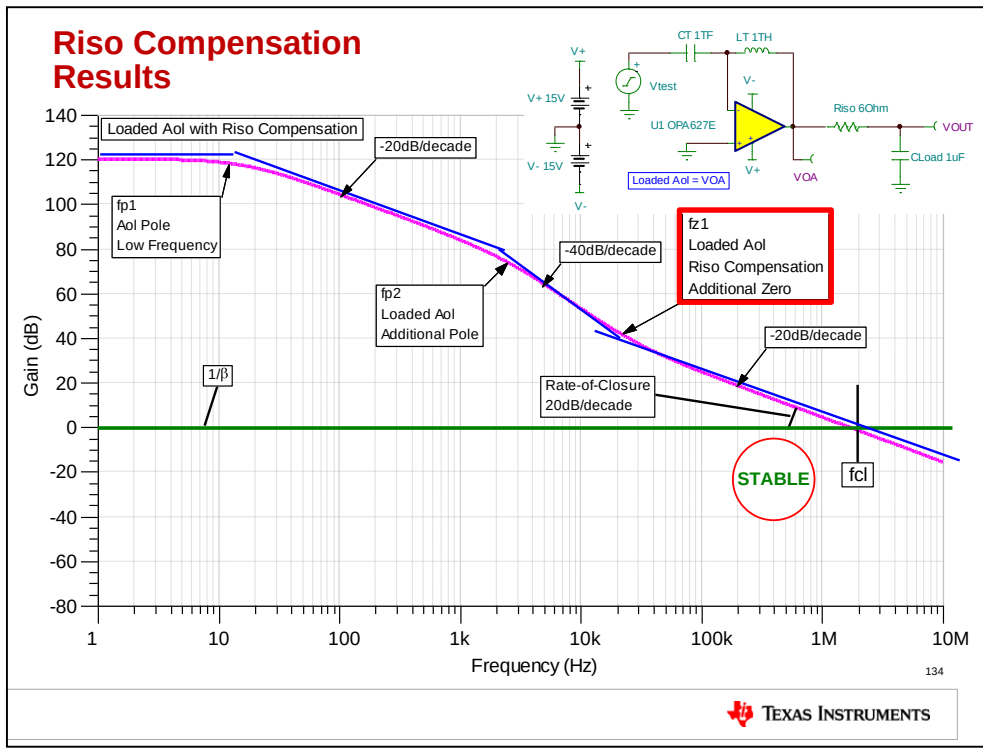
Riso will add a zero in the Loaded Aol Curve



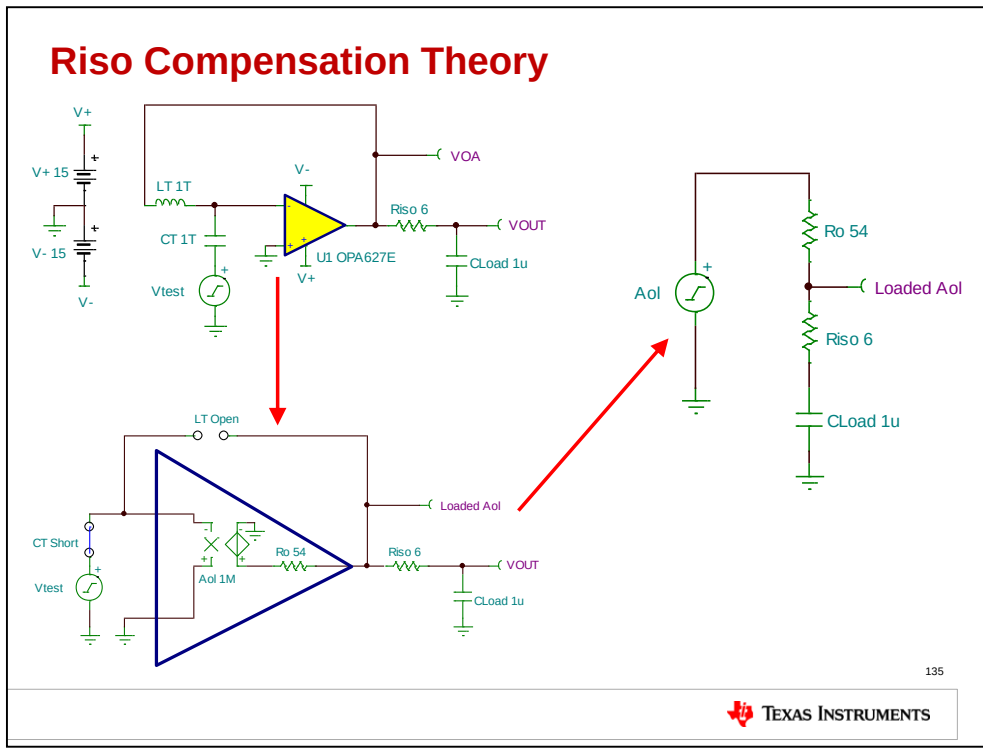
133

TEXAS INSTRUMENTS

One way to compensate the op amp circuit for CLoad is to add Riso Compensation. Note the point of feedback for the circuit is still taken directly at the output of the op amp. The addition of Riso will add a zero into the “Loaded Aol” curve and stabilize the circuit.

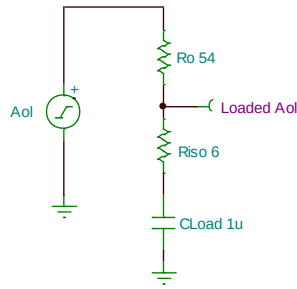


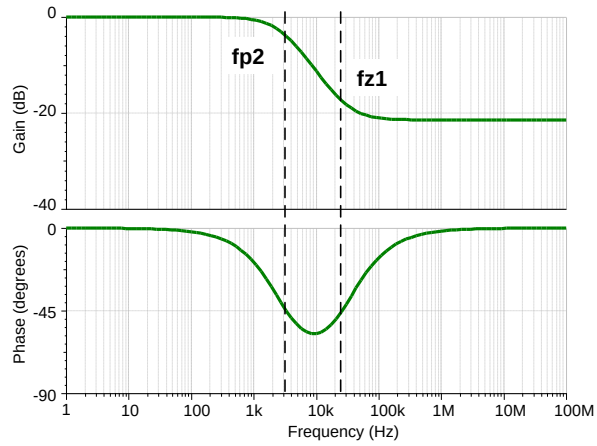
The Riso Compensation will add fz1 into the “Loaded Aol” which will result in a -20dB/decade slope crossing 0db at fcl. This will result in a stable circuit by our rate-of-closure criteria of 20dB/decade indicating stability.



Our stability analysis using the “Loaded Aol Model” will be analyzed for the addition of the Riso Compensation. The data sheet Aol curve is followed by the op amp output resistance, Ro, Riso Compensation, Riso and load capacitance, CLoad. Note the point of feedback is between Ro and Riso. The capacitive load, CLoad, in conjunction with Ro and Riso will form an additional pole in the Loaded Aol plot. The capacitive load, CLoad, in conjunction with Riso will add a zero in the Loaded Aol plot.

Riso Compensation Theory





Transfer Function

$$\text{Loaded Aol}(s) = \frac{1 + \text{CLoad} * \text{Riso} * s}{1 + (\text{Ro} + \text{Riso}) * \text{CLoad} * s}$$

Pole :

$$fp2 = \frac{1}{2\pi(\text{Ro} + \text{Riso}) * \text{CLoad}}$$

Zero :

$$fz1 = \frac{1}{2\pi * \text{Riso} * \text{CLoad}}$$

136

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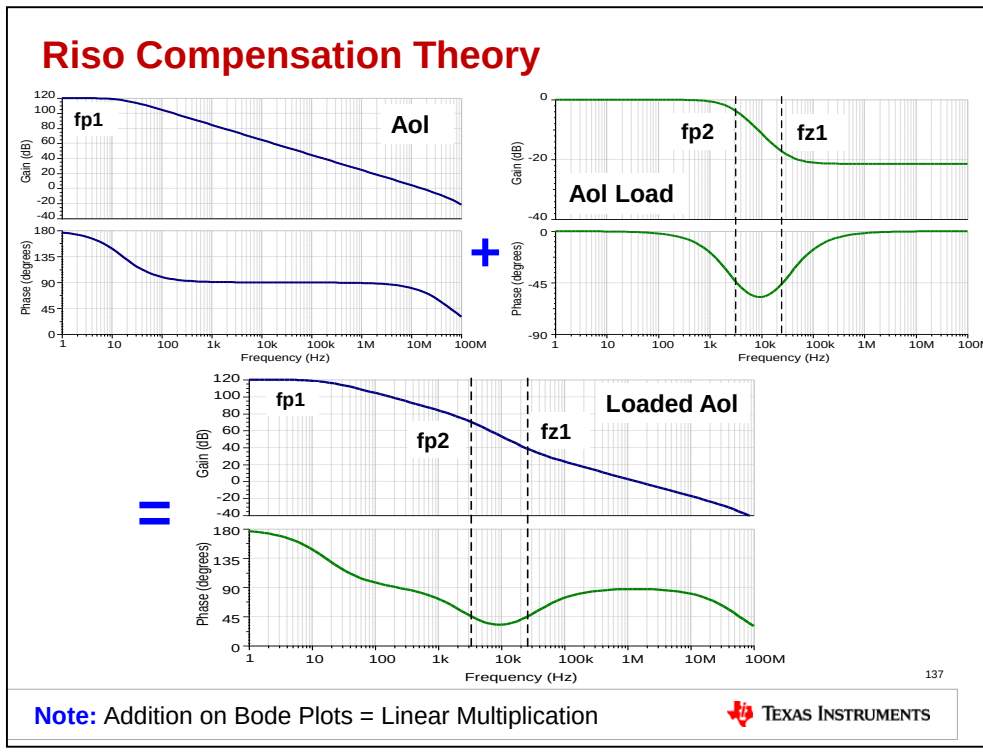
The data sheet Aol is loaded by the Ro-Riso-CLoad load network as shown here. The additional pole, fp2, due to Ro + Riso and CLoad is computed here. Also we see a zero, fz1, formed by Riso and Cload.



The op amp original “Aol” is “multiplied” by the “Aol Load” with Riso Compensation to yield the resultant “Loaded Aol” curve. On dB plots linear multiplication is performed by adding the curves in dB. As shown above it becomes easy to see the resultant “Loaded Aol” by adding the op amp original “Aol” plus the “Aol Load” formed by the Ro-Riso-CLoad combination.

Riso Compensation Design Steps

1) Determine fp2 in Loaded Aol due to CLoad
   A) Measure in SPICE with CLoad on Op Amp Output
2) Plot fp2 on original Aol to create new Loaded Aol
3) Add Desired fz2 on to Loaded Aol Plot for Riso Compensation
   A) Keep fz1 $\leq$ 10*fp2 *(Case A)*
   B) Or keep the Loaded Aol Magnitude at fz1 $\geq$ 0dB *(Case B)*
   (fz1$\geq$10dB will allow for Aol variation of ½ Decade in Unity Gain Bandwidth)
4) Compute value for Riso based on plotted fz1
5) SPICE simulation with Riso for Loop Gain (Aolβ) Magnitude and Phase
6) Adjust Riso Compensation if greater Loop Gain (Aolβ) phase margin desired
7) Check closed loop AC response for VOUT/VIN
   A) Look for peaking which indicates marginal stability
   B) Check if closed AC response is acceptable for end application
8) Check Transient response for VOUT/VIN
   A) Overshoot and ringing in the time domain indicates marginal stability
   B) Determine if settling time is acceptable for end application

138

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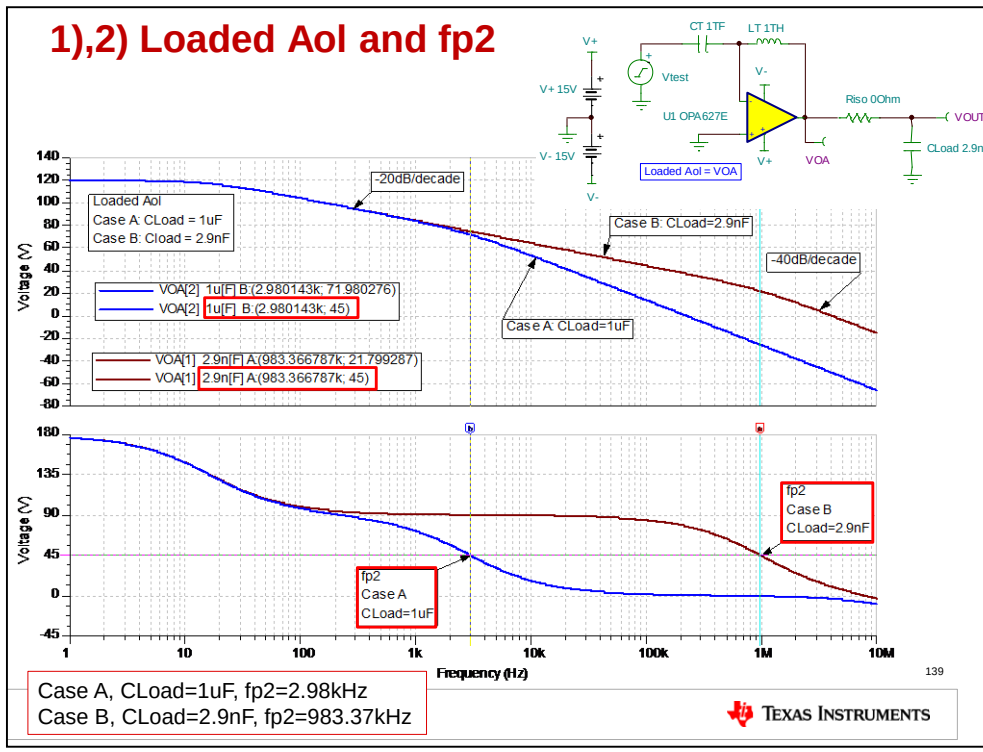
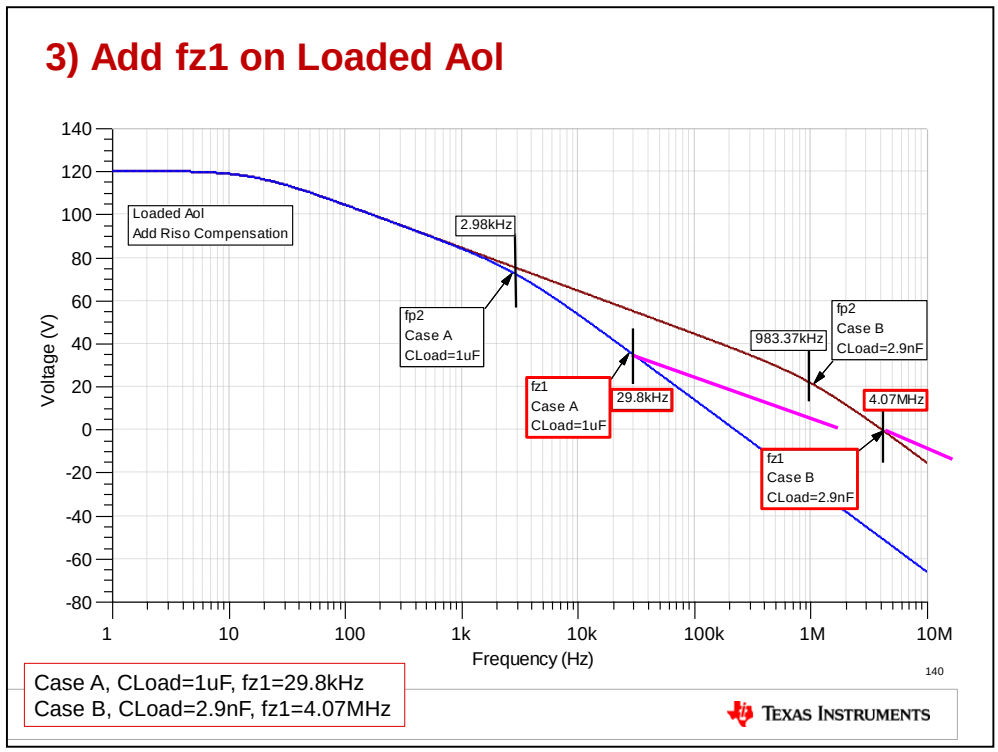
The Riso Compensation design steps are outlined here. Two cases, Case A and Case B, will be presented. Rules-of-thumb will be presented to yield best stability on first pass analysis.



Two different CLoads will be analyzed to show rules-of-thumb to get the best stability using Riso Compensation. Case A will use CLoad = 1uF and Case B will used CLoad = 2.9nF. By setting Riso = 0 ohms we can easily analyze the Loaded Aol for each case without Riso Compensation. From above Loaded Aol plots we can use the phase plots to determine the pole locations of fp2 for each of Case A, CLoad=1uF and Case B, CLoad=2.9nF.

From above we have completed Steps 1 and 2 for the Riso Compensation Design:

1) Determine fp2 in Loaded Aol due to CLoad
    A) Measure in SPICE with CLoad on Op Amp Output
2) Plot fp2 on original Aol to create new Loaded Aol



Our Loaded Aol curves for Case A, CLoad=1uF and Case B, CLoad=2.9nF, found using Step 1 and Step 2, are shown above. We can add straight line approximations to the magnitude plot (-20dB/decade slope) to indicate how and where we want to modify the Loaded Aol curve so the unity gain buffer ($1/\beta = 0dB$) will be stable with each respective capacitive load. These lines are added per the recommended rules-of-thumb below in Step 3.

From above we have completed Step 3 for the Riso Compensation Design:

3) Add Desired fz2 on to Loaded Aol Plot for Riso Compensation

A) Keep fz1 $\leq$ 10*fp2 *(Case A)*

B) Or keep the Loaded Aol Magnitude at fz1 $\geq$ 0dB *(Case B)*

(fz1$\geq$10dB will allow for Aol variation of ½ Decade in Unity Gain Bandwidth)

4) Compute Value for Riso

Case A, CLoad=1uF, fz1=29.8kHz
Case B, CLoad=2.9nF, fz1=4.07MHz

Zero :

$$fz1 = \frac{1}{2\pi * Riso * CLoad}$$

$$Riso = \frac{1}{2\pi * fz1 * CLoad}$$

Zero, Case A, CLoad = 1μF, fz1 = 29.8kHz :

$$fz1 = \frac{1}{2\pi * Riso * CLoad}$$

$$Riso = \frac{1}{2\pi * 29.8kHz * 1\mu F} = 5.34\Omega \rightarrow \textbf{use 5.36Ω}$$

Zero, Case B, CLoad = 2.9nF, fz1 = 4.07MHz :

$$fz1 = \frac{1}{2\pi * Riso * CLoad}$$

$$Riso = \frac{1}{2\pi * 4.07MHz * 2.9nF} = 13.48\Omega \rightarrow \textbf{use 13.7Ω}$$

141

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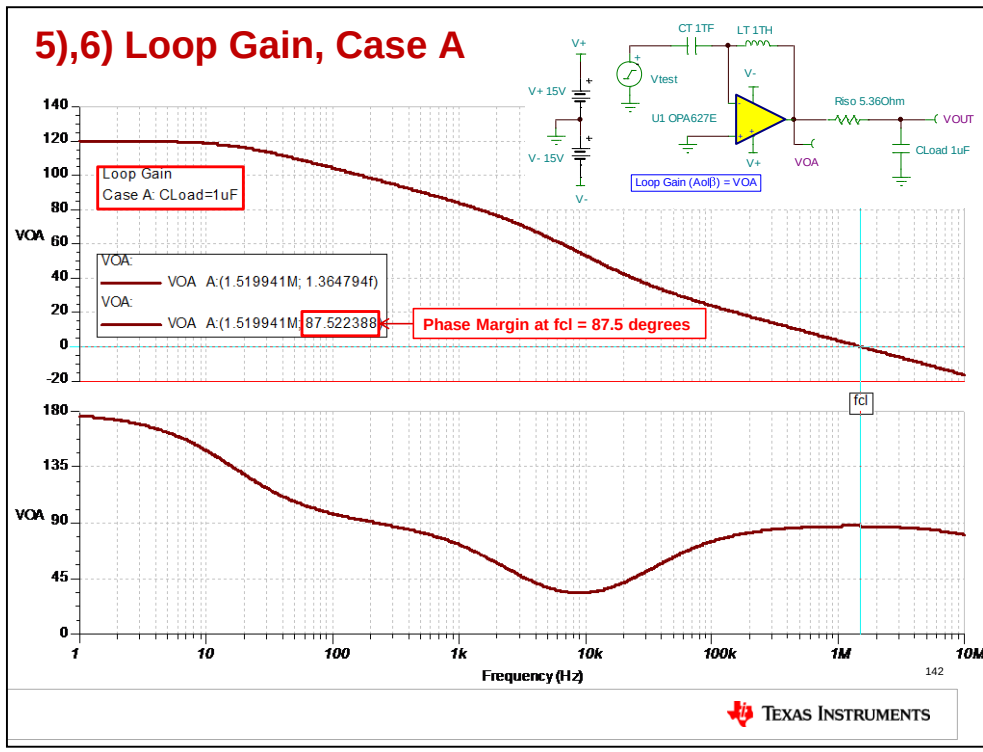
From Riso Compensation Design Step 3 we know the respective locations we want for fz1. From that we can compute Riso and choose a standard resistor value.

From above we have completed Step 4 for the Riso Compensation Design:

4) Compute value for Riso based on plotted fz1

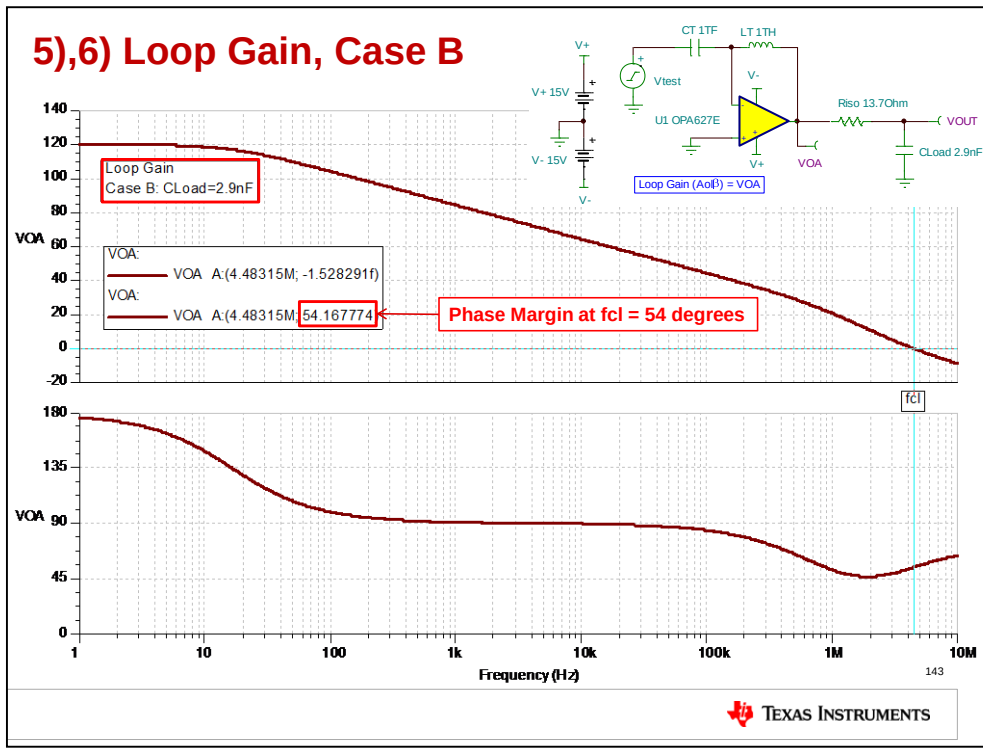


Design Step 5 for Riso Compensation is to check the final Riso value chosen by a loop gain plot on the complete op amp circuit. We see from above that for Case A, CLoad=1uF, at fcl, where Loop Gain (Aolβ) goes to zero, the phase margin is 87.5 degrees. Step 6 is to adjust Riso for more phase margin if we are not satisfied with our first analysis and re-run the loop gain and phase plot to check the final design. Here we are happy with 87.5 degrees of Loop Gain (Aolβ) phase margin.

From above we have completed Steps 5 & 6 for the Riso Compensation Design:

5) SPICE simulation with Riso for Loop Gain (Aolβ) Magnitude and Phase

6) Adjust Riso Compensation if greater Loop Gain (Aolβ) phase margin desired

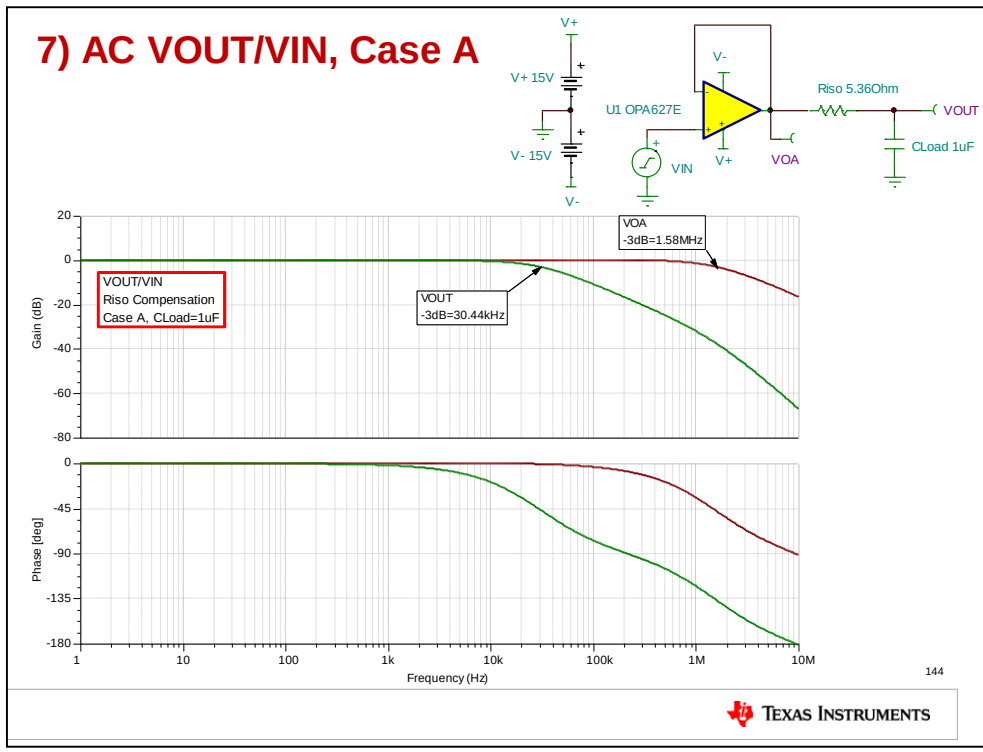


Design Step 5 for Riso Compensation is to check the final Riso value chosen by a loop gain plot on the complete op amp circuit. We see from above that for Case B, CLoad=2.9nF, at fcl, where Loop Gain (Aolβ) goes to zero, the phase margin is 54.2 degrees. Step 6 is to adjust Riso for more phase margin if we are not satisfied with our first analysis and re-run the loop gain and phase plot to check the final design. Here we are happy with 54.2 degrees of Loop Gain (Aolβ) phase margin.

From above we have completed Steps 5 & 6 for the Riso Compensation Design:

5) SPICE simulation with Riso for Loop Gain (Aolβ) Magnitude and Phase

6) Adjust Riso Compensation if greater Loop Gain (Aolβ) phase margin desired



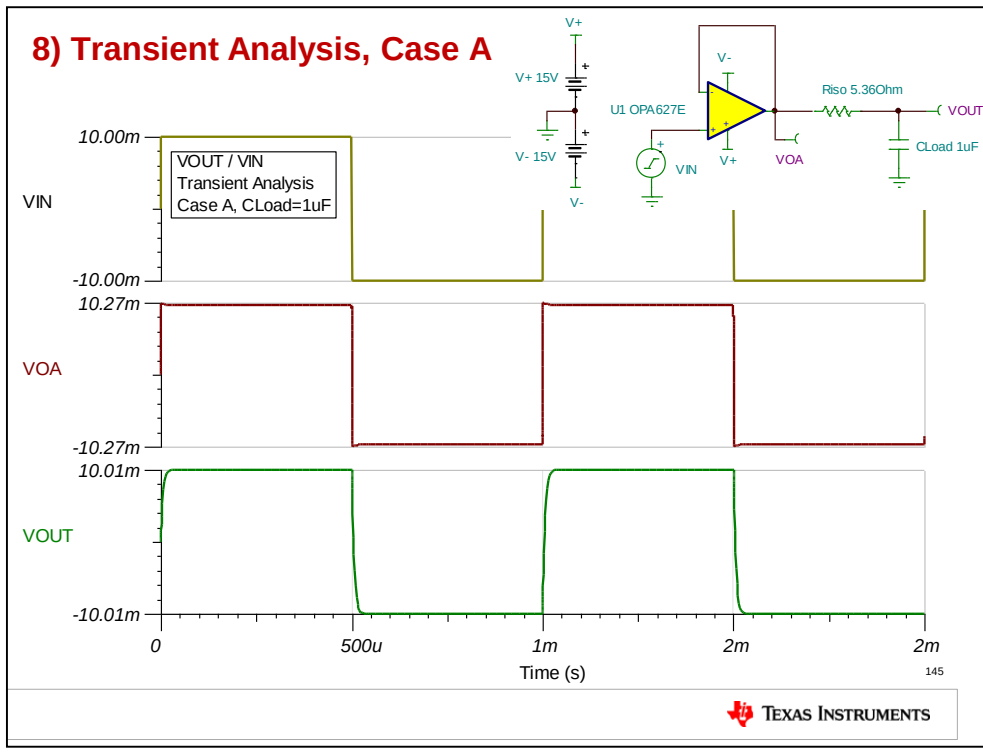
Design Step 7 for Riso Compensation is to check the closed loop AC response over frequency. From above, for Case A, CLoad=1uF, we see the closed loop AC response for both the output of the op amp, VOA, and the output after Riso, VOUT. If this closed loop bandwidth is not acceptable for the final application we will need to consider other capacitive stability techniques (see Appendix) or a different op amp or different load capacitance value.

From above we have completed Step 7 for the Riso Compensation Design:

7) Check closed loop AC response for VOUT/VIN

   A) Look for peaking which indicates marginal stability

   B) Check if closed AC response is acceptable for end application

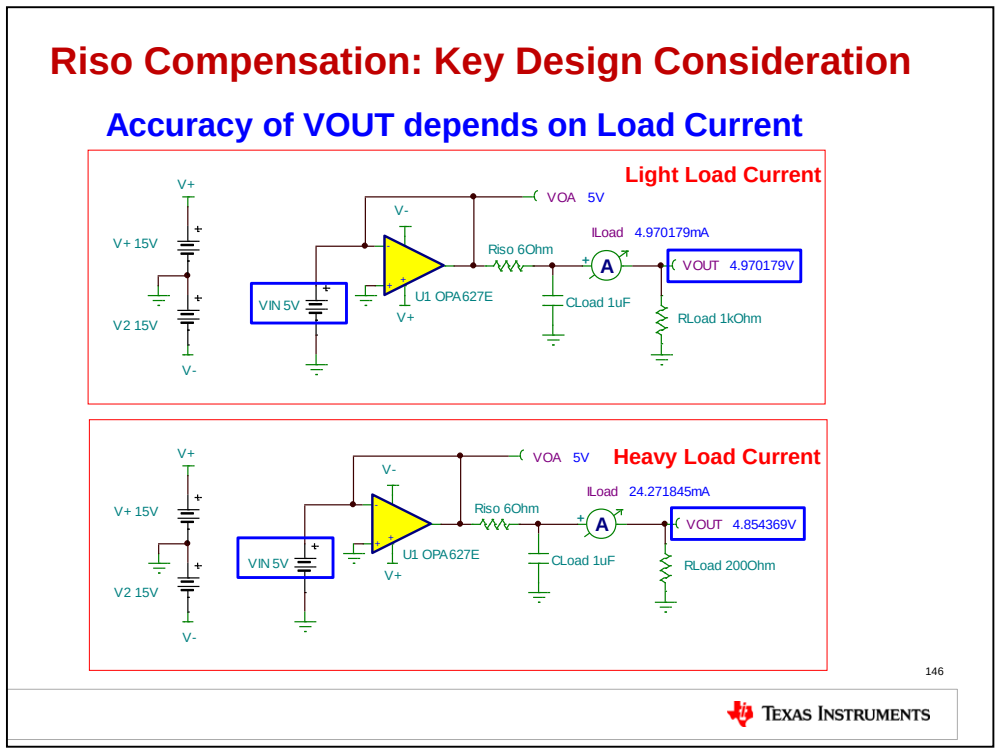


Design Step 8 for Riso Compensation is to check the closed loop transient response. From above, for Case A, CLoad=1uF, we see the closed loop Transient response for both the output of the op amp, VOA, and the output after Riso, VOUT show no signs of excessive overshoot or ringing before settling.

From above we have completed Step 7 for the Riso Compensation Design:

8) Check Transient response for VOUT/VIN

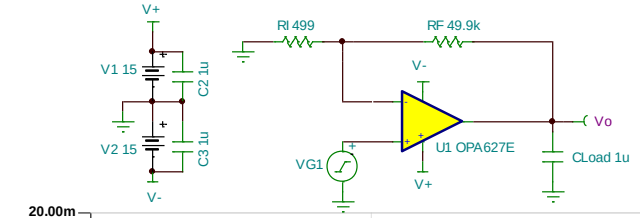
A) Overshoot and ringing in the time domain indicates marginal stability

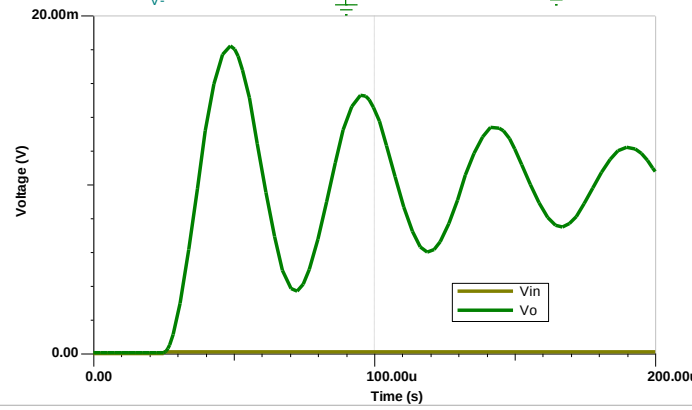


The Riso Compensation has one key design consideration with regards to accuracy at VOUT for heavy loads. The feedback for voltage accuracy is directly at the output of the op amp and the VOUT at the load is isolated by Riso. If output currents are large and depending upon the value of Riso the voltage at VOUT will not be the voltage at VIN for the unity gain follower shown above. If this is a problem in the end application a different compensation technique for the CLoad will need to be used (see Appendix for alternative compensation methods for output capacitive loads).

6) High Gain and CF (Output Cload)

Original Circuit: Transient Response





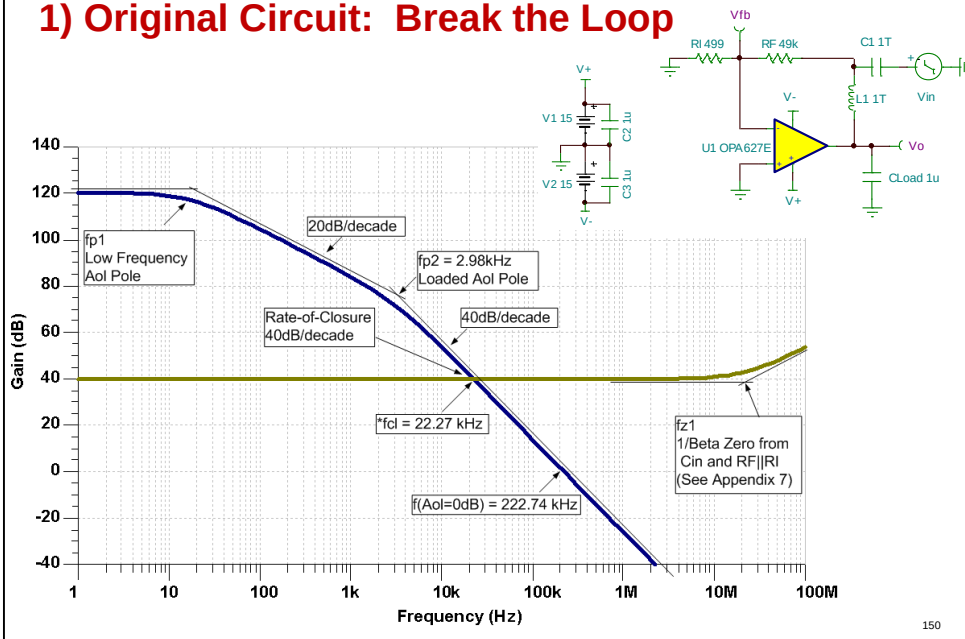
148

TEXAS INSTRUMENTS

High-Gain and CF Compensation Design Steps

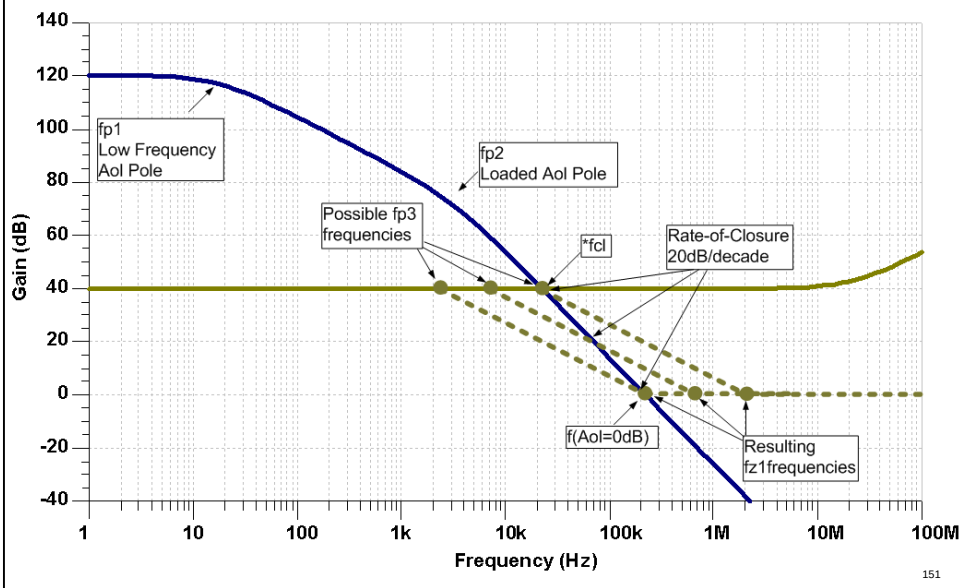
1) Break the loop and plot Aol and 1/Beta
   A. Determine fp2 in Loaded Aol due to Cload
   B. Determine fcl of original Aol and 1/Beta
   C. Determine f(Aol=0dB)
      f(Aol=0dB): the frequency where the Loaded Aol Magnitude = 0dB
2) Add Desired fp3 to 1/Beta for CF compensation
   (fz1 will occur when 1/Beta = 0dB)
   A) Keep fp3 $\leq$ *fcl and fz1 $\leq$ f(Aol=0dB)
   B) To prevent AolB phase dip, Keep fp3 $\leq$ 10*fp2
3) Select value for CF based fp3, fcl, and f(Aol=0dB)
4) SPICE simulation with Riso for Loop Gain (Aolβ) Magnitude and Phase
5) Adjust CF if greater Loop Gain (Aolβ) phase margin desired
6) Check closed loop AC response for VOUT/VIN
   A) Look for peaking which indicates marginal stability
   B) Check if closed AC response is acceptable for end application
7) Check Transient response for VOUT/VIN
   A) Overshoot and ringing in the time domain indicates marginal stability

1) Original Circuit: Break the Loop



150

2) Compensate with 1/Beta Pole (CF)



151

TEXAS INSTRUMENTS

3) 1/Beta Pole/Zero Equations

1/Beta Transfer Function:

$$\frac{V_{out}(s)}{V_{fb}(s)} = \frac{R_F+R_I+(C_I+C_F)\cdot R_I\cdot R_F\cdot s}{R_I+C_F\cdot R_I\cdot R_F\cdot s}$$

DC 1/Beta:

$$s=0,\ \frac{V_{out}(s)}{V_{fb}(s)} = 1+\frac{R_F}{R_I}$$

1/Beta Pole Frequency:

$$fp3 = \frac{1}{2\cdot pi\cdot R_F\cdot C_F}$$

=> Solve for CF

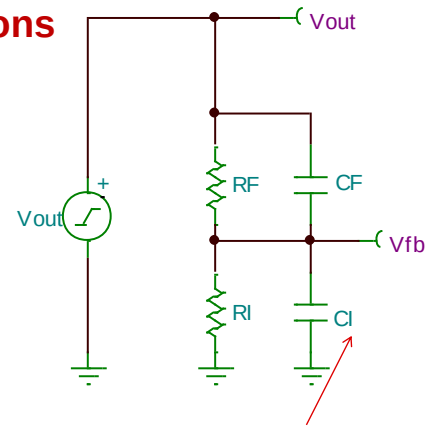
$$C_F=\frac{1}{2\cdot pi\cdot R_F\cdot fp3}$$

1/Beta Zero Frequency:

$$fz1=\frac{1}{2\cdot pi\cdot (R_I \parallel R_F)\cdot (C_F+C_I)}$$

=> Solve for CF

$$C_F=\frac{1}{2\cdot \pi\cdot (R_I \parallel R_F)\cdot fz1}-C_I$$

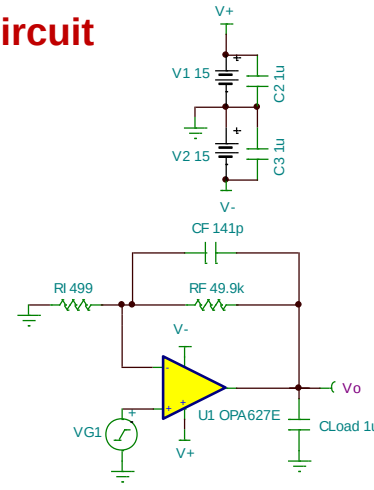


CI is the equivalent input capacitance of the op amp. (See Appendix #7)

3) Select CF to Compensate Circuit

From Step 1:

fp2 = 2.98 kHz
fcl = 22.67 kHz
f(Aol=0dB) = 222.7 kHz



For stability:

A) Keep fp3 ≤ *fcl and fz1 ≤ f(Aol=0dB)

Calculate CF(min) from fp3 < *fcl :

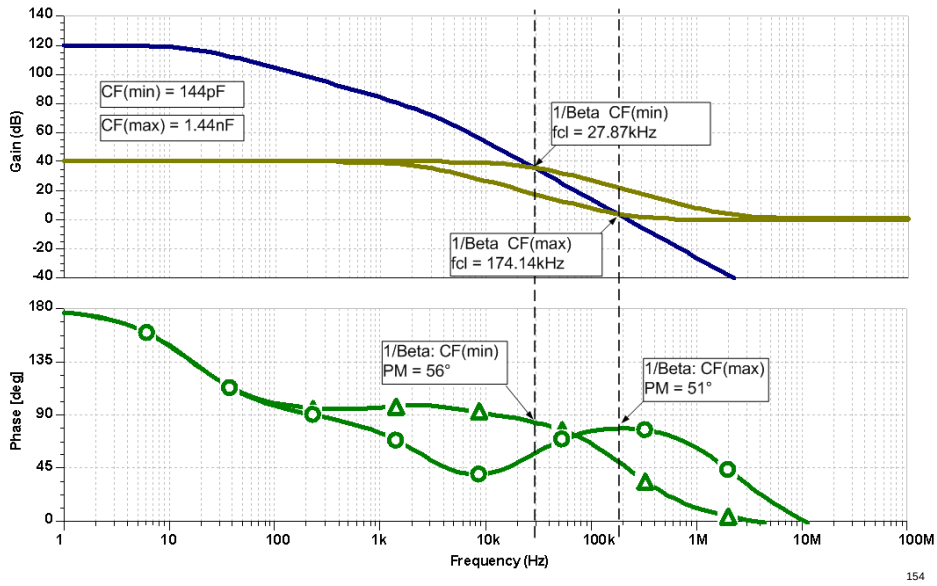
$$C_F min = \frac{1}{2\cdot\pi\cdot R_F\cdot fp3} = \frac{1}{2\cdot\pi\cdot 49.9k\Omega\cdot 22.67kHz} = 141pF$$

Calculate CF(max) from fz1 < f(Aol=0dB) :

$$C_F max = \frac{1}{2\cdot\pi\cdot(R_I \parallel R_F)\cdot fz1} - C_I = = \frac{1}{2\cdot\pi\cdot(49.9k\Omega \parallel 499\Omega)\cdot 222.7kHz} - 10pF = 1.44nF$$

B) To prevent AolB phase dip, Keep fp3 ≤ 10*fp2

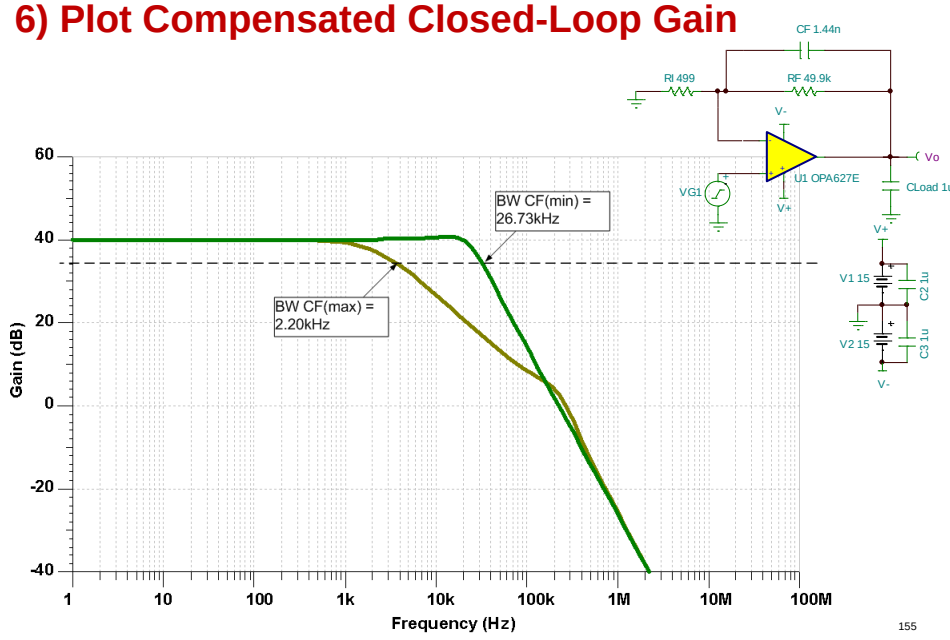
4),5) Plot Aol and 1/Beta for Compensated Circuit



154

TEXAS INSTRUMENTS

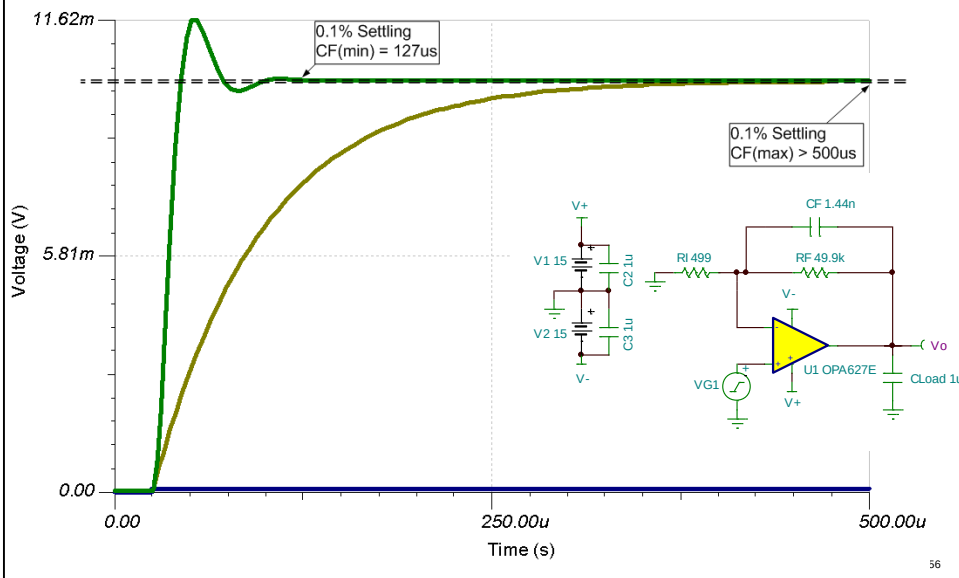
6) Plot Compensated Closed-Loop Gain



155

TEXAS INSTRUMENTS

7) Plot Compensated Transient Response



56

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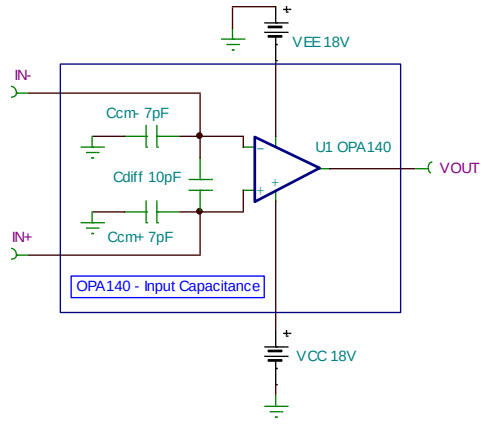
High Gain and CF Summary

1) Select CF between CF(min) and CF(max) for stability
2) CF(min) and CF(max) produce similar phase-margins
3) CF(min) will have the largest closed-loop bandwidth and fastest transient response
4) CF(max) will produce the smallest closed-loop BW and the slowest transient response
5) Selecting a value between CF(min) and CF(max) will produce the most robust design

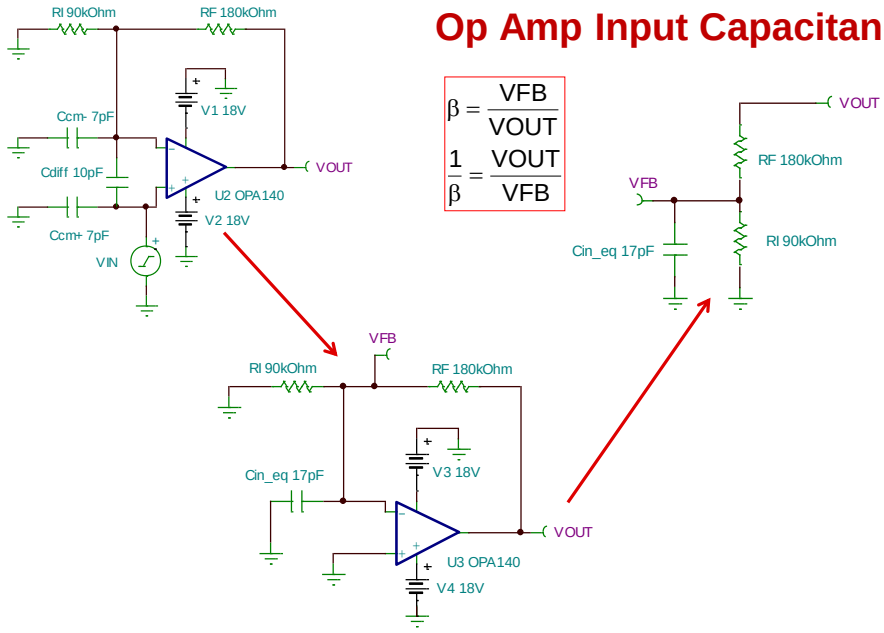
7) CF Non-Inverting (Input Cload)

Op Amp Input Capacitance

PARAMETER	CONDITIONS	OPA140, OPA2140, OPA4140			UNIT
		MIN	TYP	MAX	
INPUT IMPEDANCE					
Differential			10^{13} || 10		Ω || pF
Common-Mode	V_{CM} = (V–) –0.1V to (V+) –3.5V		10^{13} || 7		Ω || pF



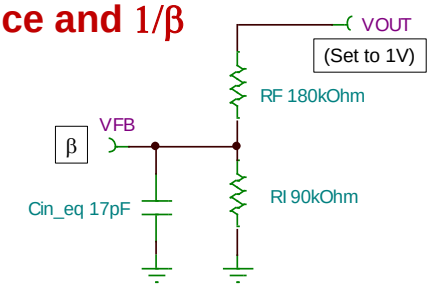
Op Amp Input Capacitance



$$\beta = \frac{VFB}{VOUT}$$

$$\frac{1}{\beta} = \frac{VOUT}{VFB}$$

Equivalent Input Capacitance and 1/β



1/β Computation :

$$\frac{1}{\beta} = \frac{RF + (RI \,//\, X_{Cin\_eq})}{RI \,//\, X_{Cin\_eq}}$$

$$\frac{1}{\beta} = \frac{\left[s + \frac{1}{Cin\_eq * \left(\frac{RF * RI}{RF + RI}\right)}\right] * [Cin\_eq * (RF * RI)]}{RI}$$ ← **(after simplification)**

$$\frac{1}{\beta}\ DC = \frac{RF + RI}{RI} = 1 + \frac{RF}{RI} = 1 + \frac{180k}{90k} = 3 \rightarrow 9.54dB$$

$$\frac{1}{\beta}\ \text{zero: } fz1 = \frac{1}{2\pi * Cin\_eq * (RF \,//\, RI)} = \frac{1}{2\pi * 17pF * (180k \,//\, 90k)} = 156kHz$$

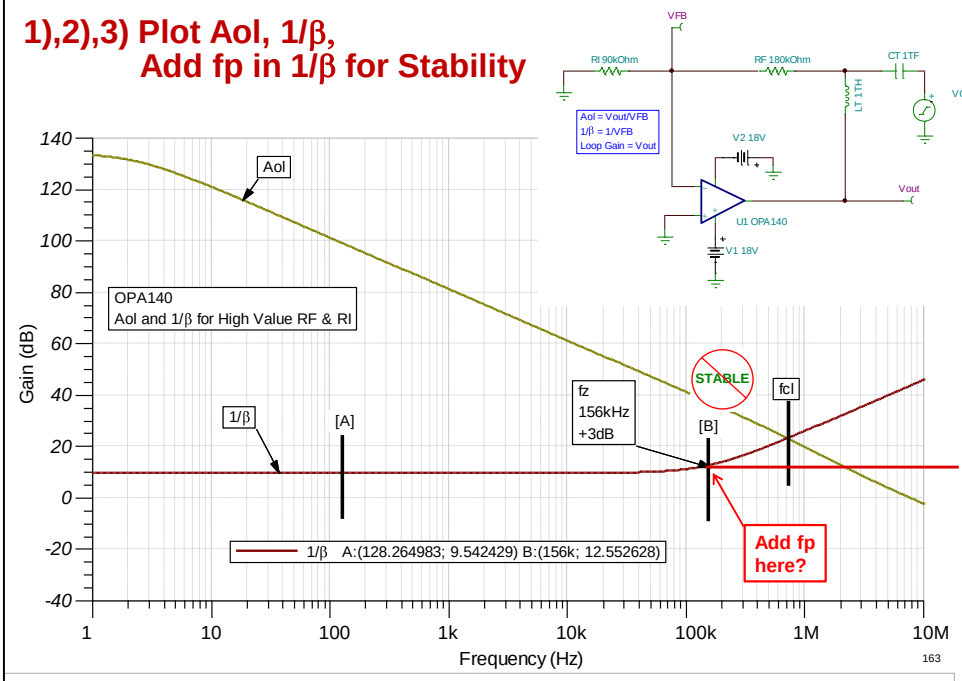
161

CF Compensation Design Steps

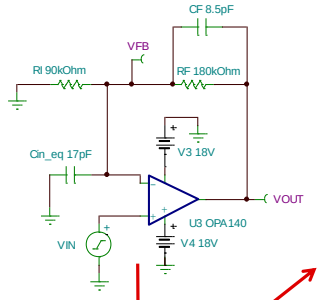
1) Determine fz1 in 1/β due to Cin_eq
   A) Measure in SPICE
   OR
   B) Compute by Datasheet C_{DIFF} and C_{CM} and Circuit RF and RI
2) Plot 1/β with fz1 on original Aol
3) Add Desired fp1 on 1/β for CF Compensation
   A) Keep fp $\leq$ 10*fz
   B) Keep fp $\leq$ 1/10 * fcl
4) Compute value for CF based on plotted fp
5) Check CF Compensation by 1/β plot on Aol
6) SPICE simulation with CF for Loop Gain (Aolβ) Magnitude and Phase
7) Adjust CF Compensation if greater Loop Gain (Aolβ) phase margin desired
8) Check closed loop AC response for VOUT/VIN
   A) Look for peaking which indicates marginal stability
   B) Check if closed AC response is acceptable for end application
9) Check Transient response for VOUT/VIN
   A) Overshoot and ringing in the time domain indicates marginal stability

The CF Compensation design steps are outlined here. Rules-of-thumb are presented to yield best stability on first pass analysis.

1),2),3) Plot Aol, 1/β, Add fp in 1/β for Stability



4) Compute Value for CF based on location of fp

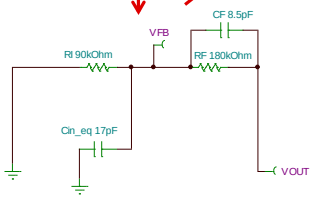


1/β Computation :

$$\frac{1}{\beta} = \frac{(RF \,//\, X_{CF}) + (RI \,//\, X_{Cin\_eq})}{RI \,//\, X_{Cin\_eq}}$$

Note: Location of fz changes when CF is added

$$\frac{1}{\beta} = \frac{(Cin\_eq + CF)\left(s + \frac{1}{\left(\frac{RI * RF}{RF + RI}\right)(Cin\_eq + CF)}\right)}{(CF)\left(s + \frac{1}{RF * CF}\right)} \leftarrow \textbf{after simplification}$$



$$\frac{1}{\beta}\ DC = \frac{RF + RI}{RI} = 1 + \frac{RF}{RI} = 1 + \frac{180k}{90k} = 3 \rightarrow 9.54dB$$

$$\frac{1}{\beta}\ \text{zero: fz} = \frac{1}{2\pi * (Cin\_eq \,//\, CF)(RF \,//\, RI)}$$

$$\frac{1}{\beta}\ \text{zero:fz} = \frac{1}{2\pi * (25.5pF)(180k \,//\, 90k)} = 104kHz$$

$$\frac{1}{\beta}\ \text{pole: fp} = \frac{1}{2\pi * CF * RF}$$

$$\frac{1}{\beta}\ \text{pole: fp} = \frac{1}{2\pi * 8.5pF * 180k} = 104kHz$$

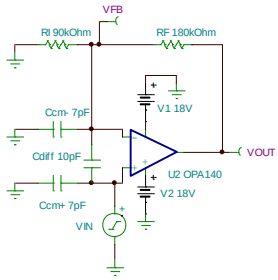
4) Compute Value for CF based on location of fp

Maximum Bandwidth CF Compensation for Cin

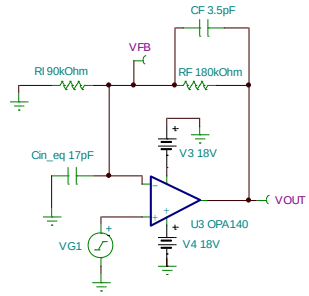
For maximum Closed Loop Bandwidth for VOUT / VIN:

1) CF needs to compensate input capacitance of Ccm- only since gain effects of Cdiff are nulled out (Similar to Non-Inverting Noise Gain op amp configuration)
2) Stability and phase margin are still determined by Cin_eq (Cdiff // Ccm-)

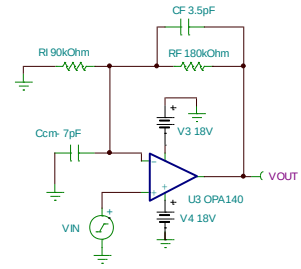
Complete Circuit



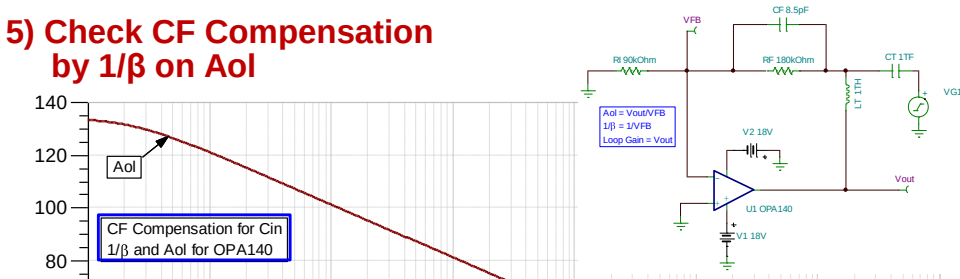
Loop Gain Model



Closed Loop VOUT / VIN Model



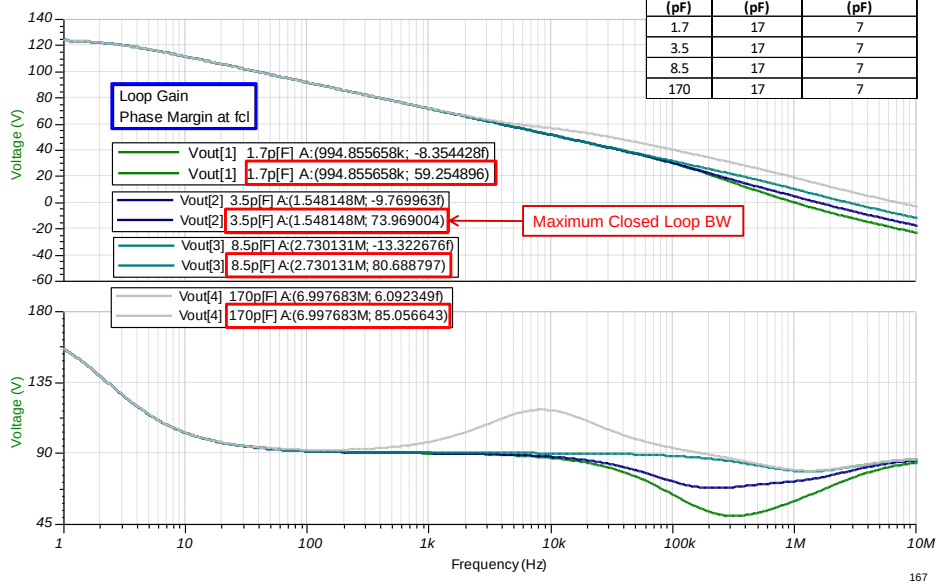
5) Check CF Compensation by 1/β on Aol



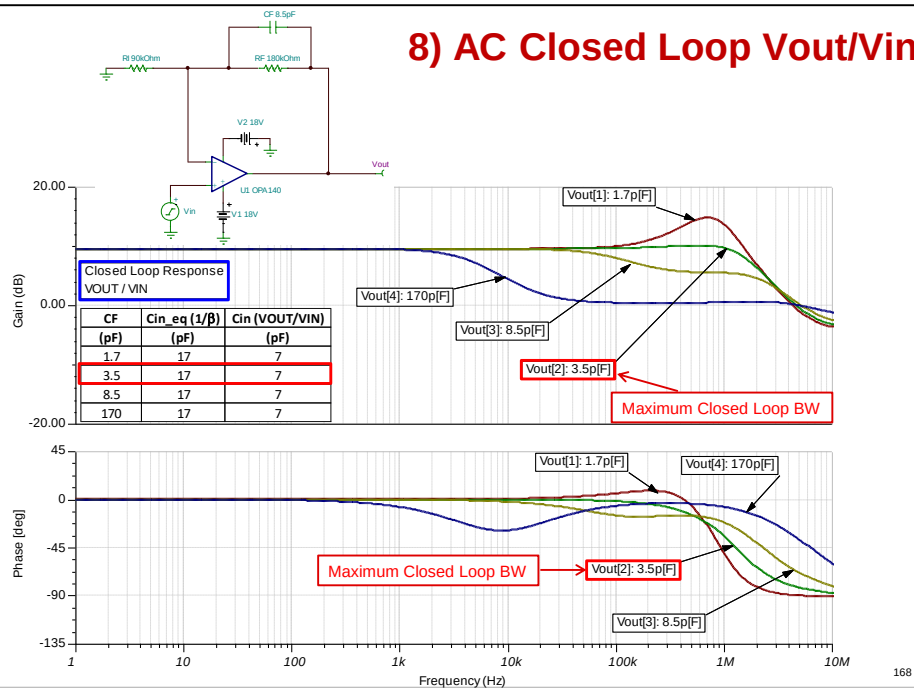
CF (pF)	Cin_eq (1/β) (pF)	Cin (VOUT/VIN) (pF)
1.7	17	7
3.5	17	7
8.5	17	7
170	17	7

6),7) Loop Gain Check

CF (pF)	Cin_eq (1/β) (pF)	Cin (VOUT/VIN) (pF)
1.7	17	7
3.5	17	7
8.5	17	7
170	17	7

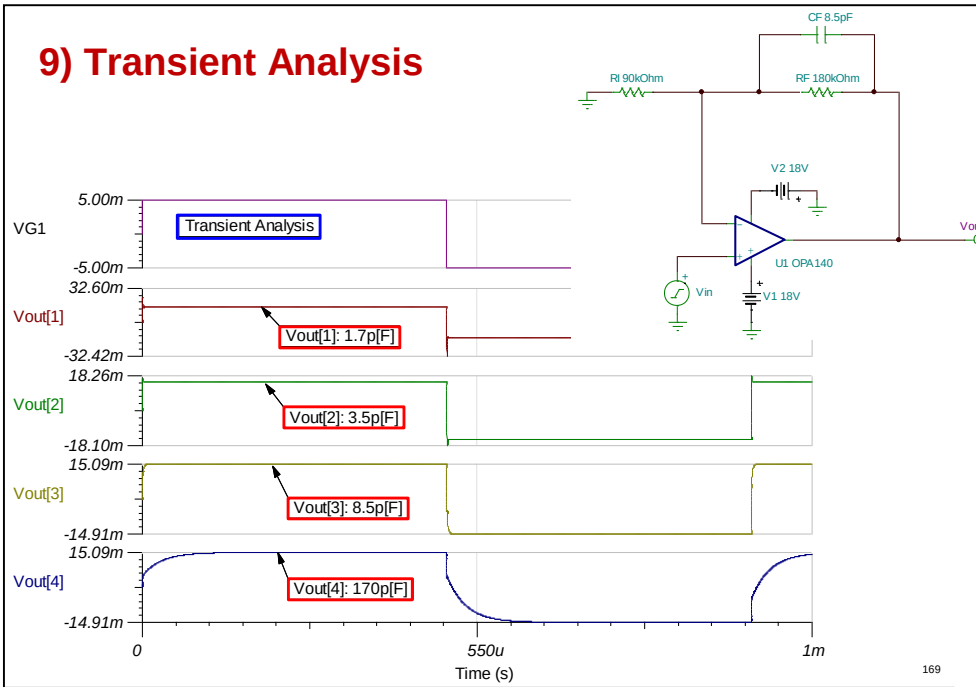


8) AC Closed Loop Vout/Vin

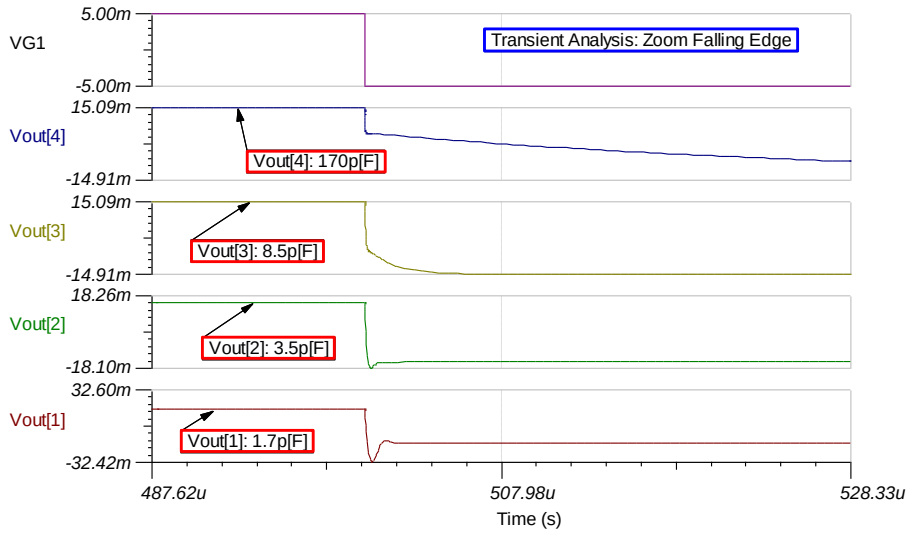


CF (pF)	Cin_eq (1/β) (pF)	Cin (VOUT/VIN) (pF)
1.7	17	7
3.5	17	7
8.5	17	7
170	17	7

9) Transient Analysis

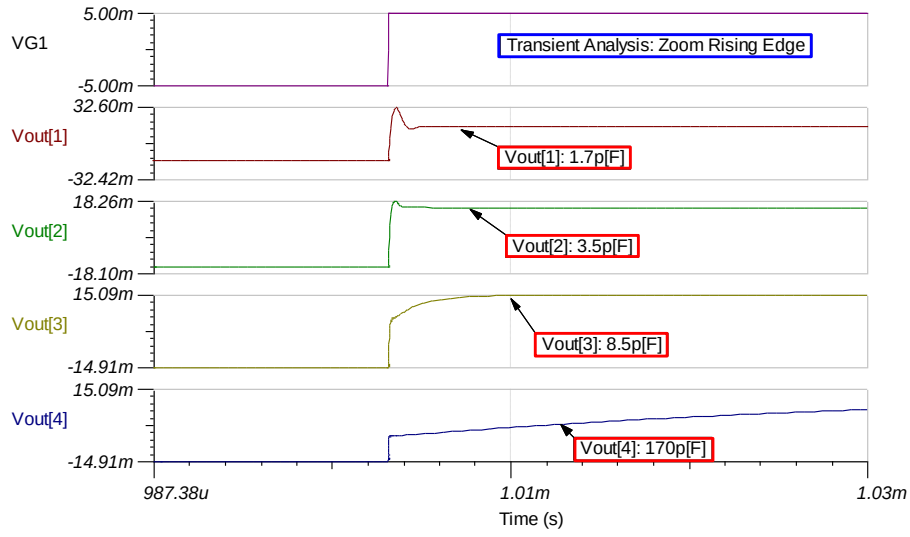


9) Transient Analysis



170

9) Transient Analysis



171

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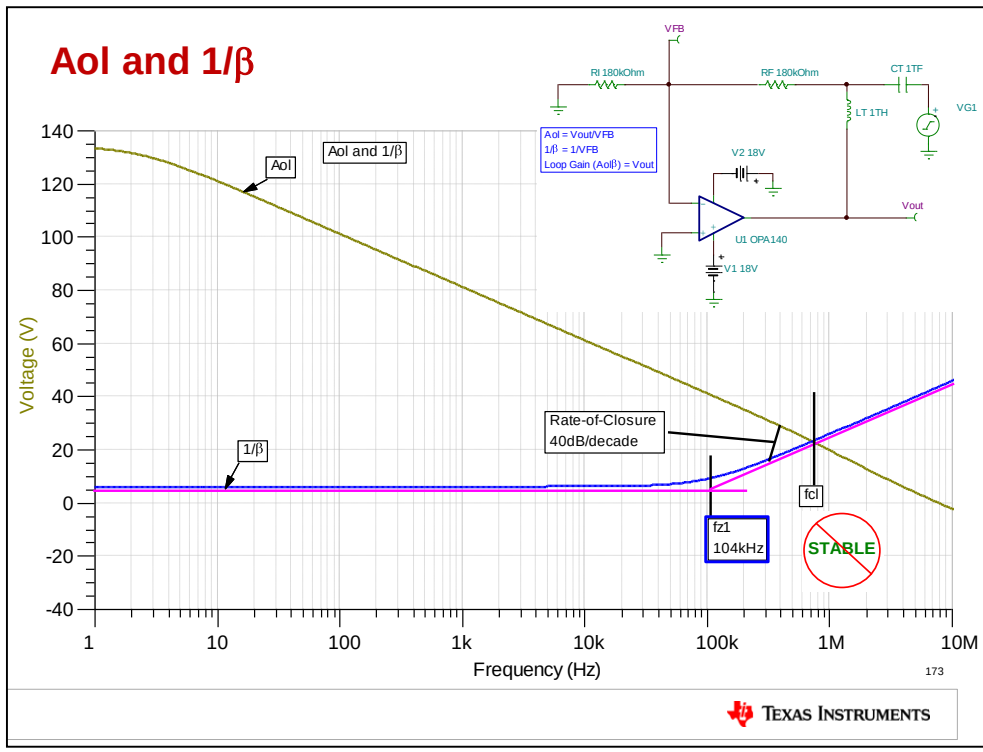
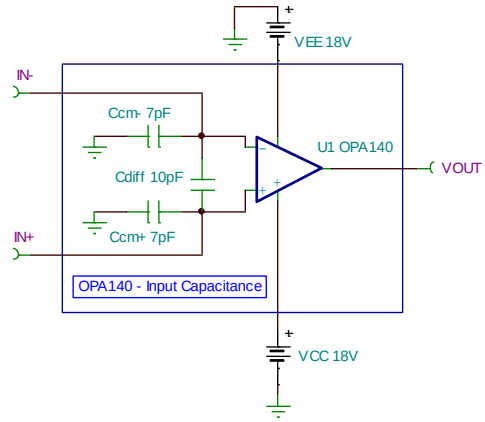
8) CF Inverting (Input Cload)



We can use our SPICE Loop Gain Test circuit above to plot Aol and 1/β for this Gain = -1 circuit. Note that the 1/β curve has a zero in it at 104kHz. At fcl, where Loop Gain (Aolβ) goes to zero, we see that the 1/β curve intersects the Aol at a rate-of-closure that is 40dB/decade which by our criteria implies an UNSTABLE circuit.

Op Amp Input Capacitance

PARAMETER	CONDITIONS	OPA140, OPA2140, OPA4140 MIN	TYP	MAX	UNIT
INPUT IMPEDANCE					
Differential			10^{13} || 10		Ω || pF
Common-Mode	V_{CM} = (V–) –0.1V to (V+) –3.5V		10^{13} || 7		Ω || pF



174

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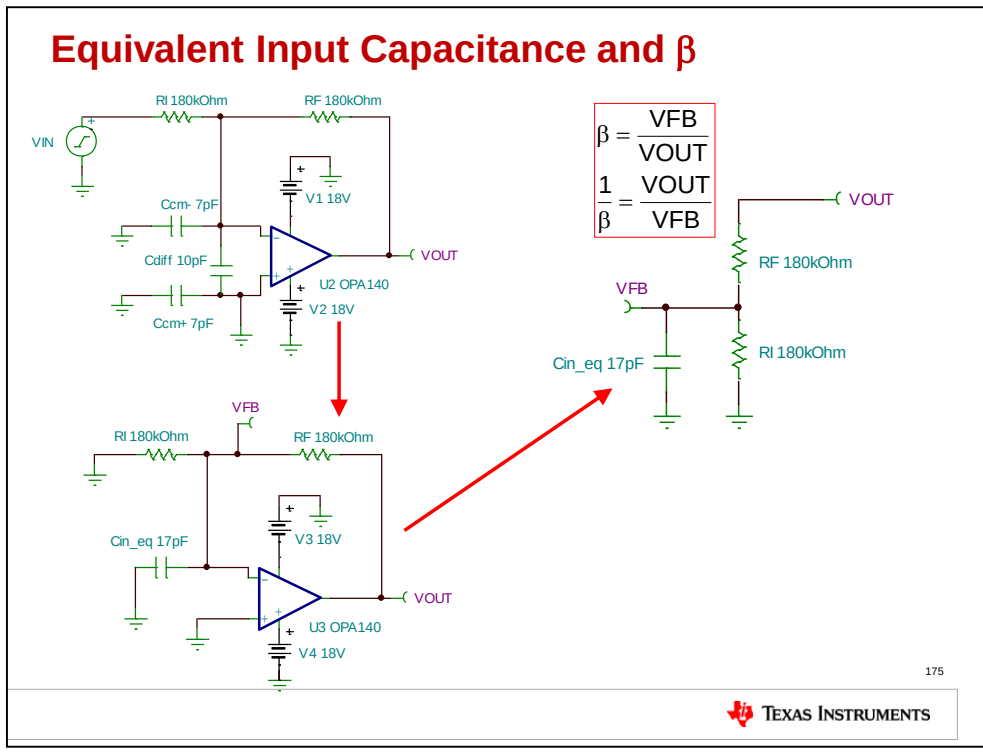
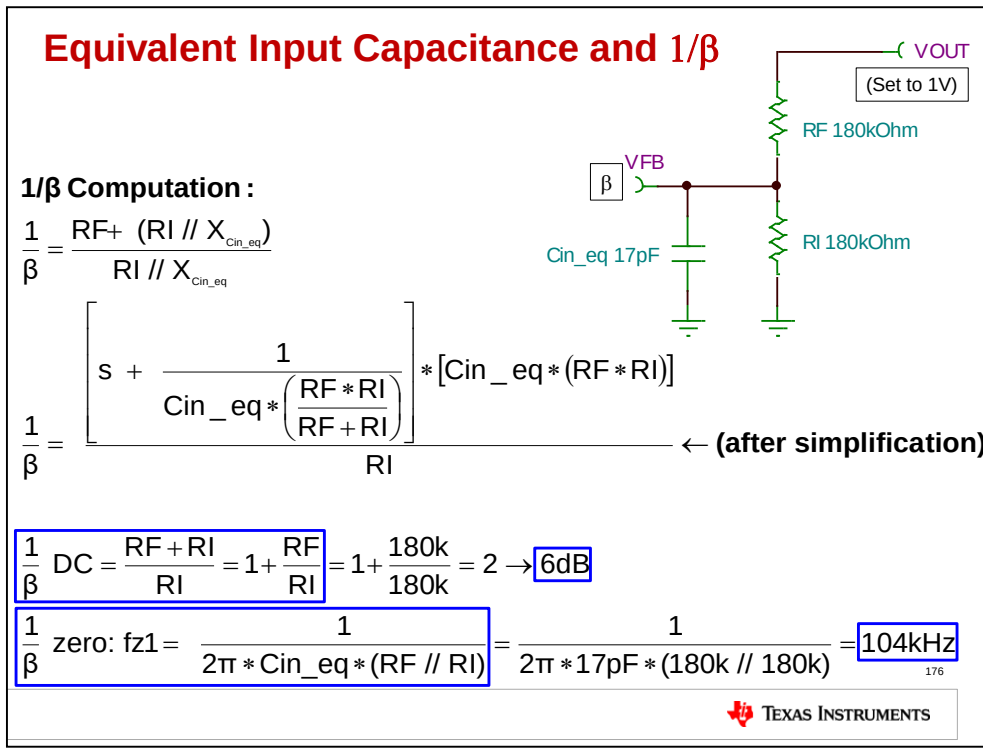
To properly analyze this circuit and thus properly compensate it for stability we first must analyze the OPA140 op amp input capacitance. The datasheet excerpt for the OPA140 is shown here with Input Impedance parameters for Differential and Common-Mode. The input capacitance model for the OPA140 is also shown. From the data sheet we can assign values for the capacitances shown, Ccm+, Ccm-, and Cdiff.



From our input capacitance model for the OPA140 and the circuit topology it is configured in we see there is a net input capacitance, Cin_eq which will affect our feedback factor, β, over frequency. Since the Cin_eq capacitor is buffered by RF, 180k ohm resistor, there are no loading effects on Aol with this circuit topology and so the Aol remains unchanged.



Our β network is shown above. β is easy to compute if one sets VOUT = 1. β=(input impedance)/(feedback impedance + input impedance). Recall that 1/β is just the reciprocal of β. From our derived and simplified equations above we see a zero, fz1, in the 1/β plot due to RF, RI and Cin_eq. Note that although our closed loop gain is -1 our 1/β is at 6dB or x2. Remember our earlier discussion of noise gain and to view the op amp, from a loop gain view, to always be running in a noise gain equivalent to putting a noise source on the +input of the op amp and running in the non-inverting gain based on feedback and input impedances from output to –input.

CF Compensation Design Steps

1) Determine fz1 in 1/β due to Cin_eq
   A) Measure in SPICE
      OR
   B) Compute by Datasheet C_{DIFF} and C_{CM} and Circuit RF and RI
2) Plot 1/β with fz1 on original Aol
3) Add Desired fp1 on 1/β for CF Compensation
   A) Keep fp1 ≤ 10*fz1
   B) Keep fp1 ≤ 1/10 * fcl
4) Compute value for CF based on plotted fp1
5) SPICE simulation with CF for Loop Gain (Aolβ) Magnitude and Phase
6) Adjust CF Compensation if greater Loop Gain (Aolβ) phase margin desired
7) Check closed loop AC response for VOUT/VIN
   A) Look for peaking which indicates marginal stability
   B) Check if closed AC response is acceptable for end application
8) Check Transient response for VOUT/VIN
   A) Overshoot and ringing in the time domain indicates marginal stability

177

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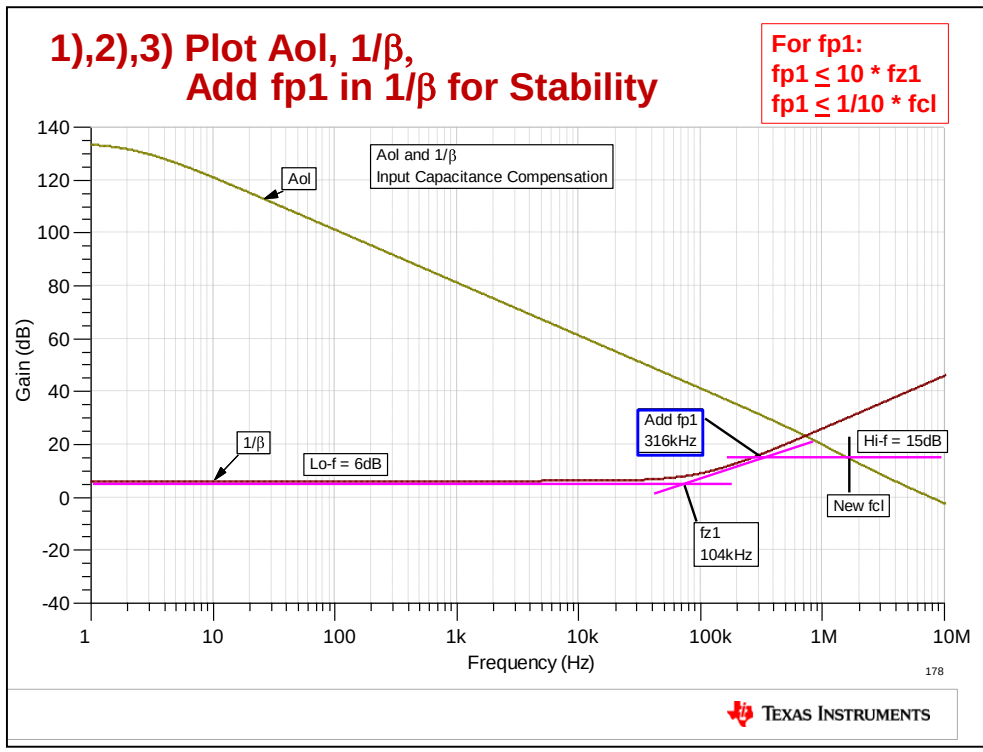
The CF Compensation design steps are outlined here. Rules-of-thumb are presented to yield best stability on first pass analysis.



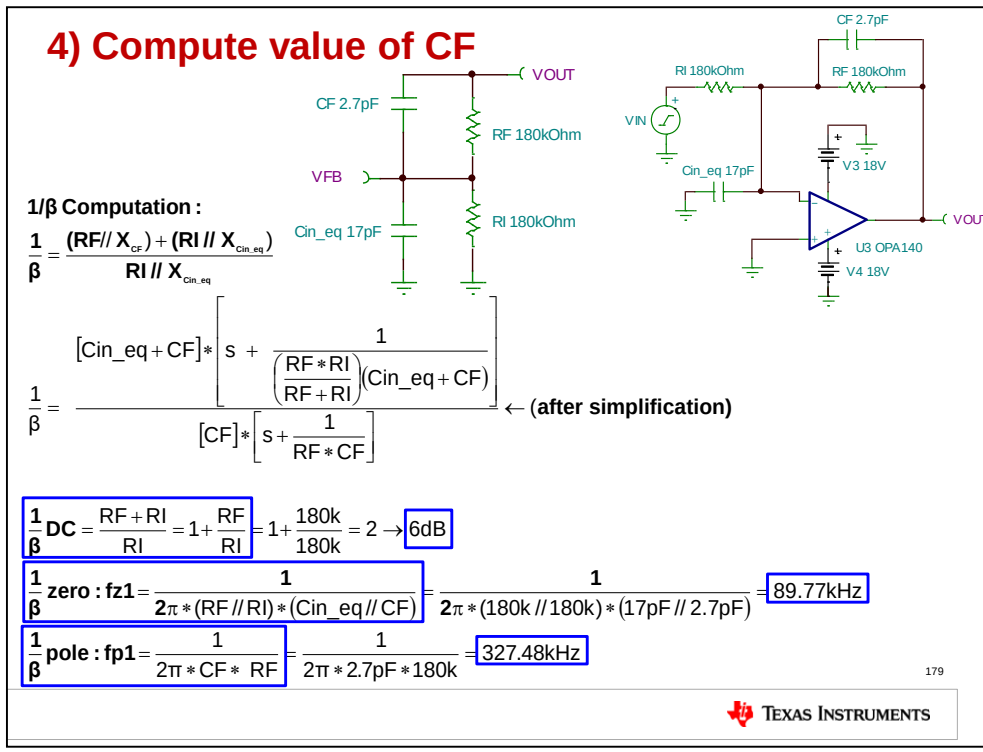
Using our Loop Gain Test circuit in SPICE we can plot the Aol and 1/β for the uncompensated circuit as shown above. For best stability results on first pass we use the recommended rules-of-thumb shown and draw in what we want the final 1/β curve to look like. Based on this graphical approach we see we need a pole, fp1, added into the 1/β curve to allow the compensated 1/β to intersect the Aol at a rate-of-closure which is 20db/decade and thus stable by our criteria.

From above we have completed Steps 1, 2, and 3 for the CF Compensation Design:

1) Determine fz1 in 1/β due to Cin_eq
   A) Measure in SPICE
   B) Compute by Datasheet C_{DIFF} and C_{CM} and Circuit RF and RI
2) Plot 1/β with fz1 on original Aol
3) Add Desired fp1 on 1/β for CF Compensation

A) Keep fp1 ≤ 10*fz1

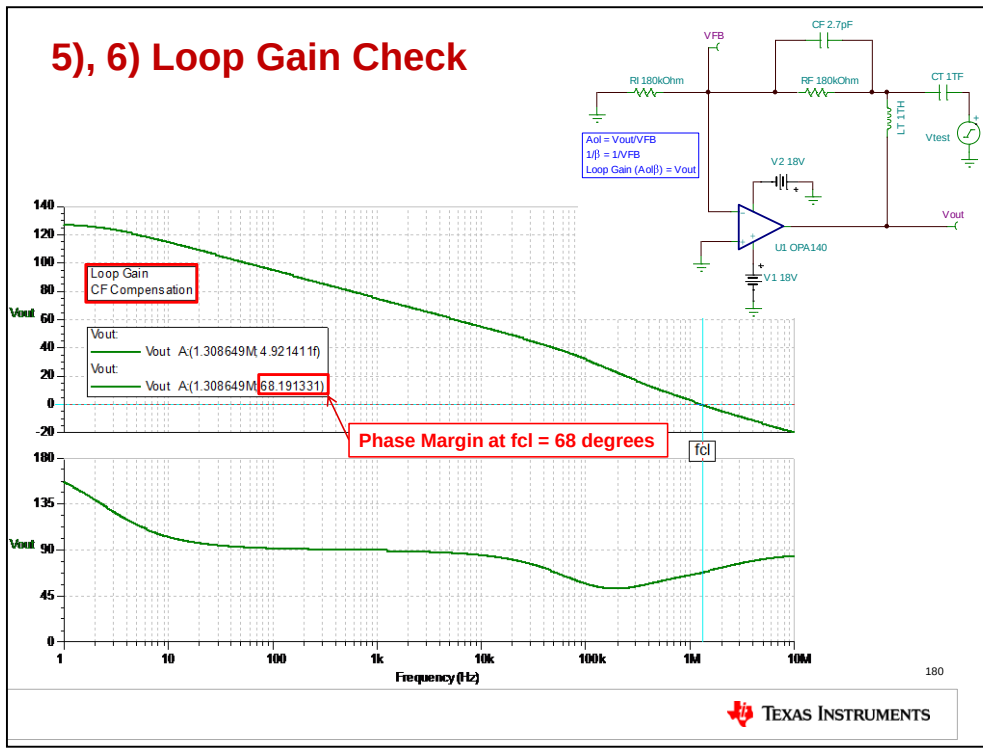
B) Keep fp1 ≤ 1/10 * fcl



Our β network is shown above. β is easy to compute if one sets VOUT = 1. β=(input impedance)/(feedback impedance + input impedance). Recall that 1/β is just the reciprocal of β. From our derived and simplified equations above we see a zero, fz1, in the 1/β plot due to RF, RI, Cin_eq, and CF. Note that although our closed loop gain is -1 our 1/β is at 6dB or x2. Remember our earlier discussion of noise gain and to view the op amp, from a loop gain view, to always be running in a noise gain equivalent to putting a noise source on the +input of the op amp and running in the non-inverting gain based on feedback and input impedances from output to –input. Note that with the addition of CF Compensation the 1/β zero, fz1, is moved to a lower frequency since CF is in parallel with Cin_eq to determine the location of fz1. However, to choose the CF Compensation pole, fp1, it is only dependent upon Rf and CF.

From above we have completed Step 4 for the CF Compensation Design:

4) Compute value for CF based on plotted fp1



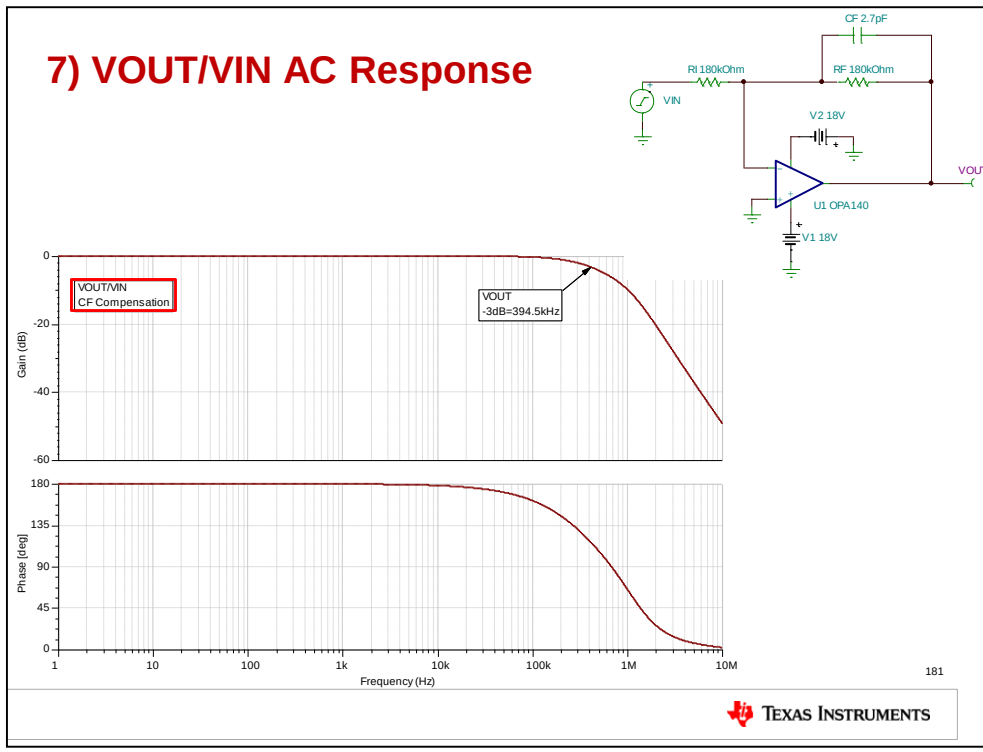
Design Step 5 for CF Compensation is to check the final CF value chosen by a loop gain plot on the complete op amp circuit. We see from above that at fcl, where Loop Gain (Aolβ) goes to zero, the phase margin is 68 degrees. Step 6 is to adjust CF for more phase margin if we are not satisfied with our first analysis and re-run the loop gain and phase plot to check the final design. Here we are happy with 68 degrees of Loop Gain (Aolβ) phase margin.

From above we have completed Steps 5 & 6 for the CF Compensation Design:

5) SPICE simulation with CF for Loop Gain (Aolβ) Magnitude and Phase

6) Adjust CF Compensation if greater Loop Gain (Aolβ) phase margin desired

.



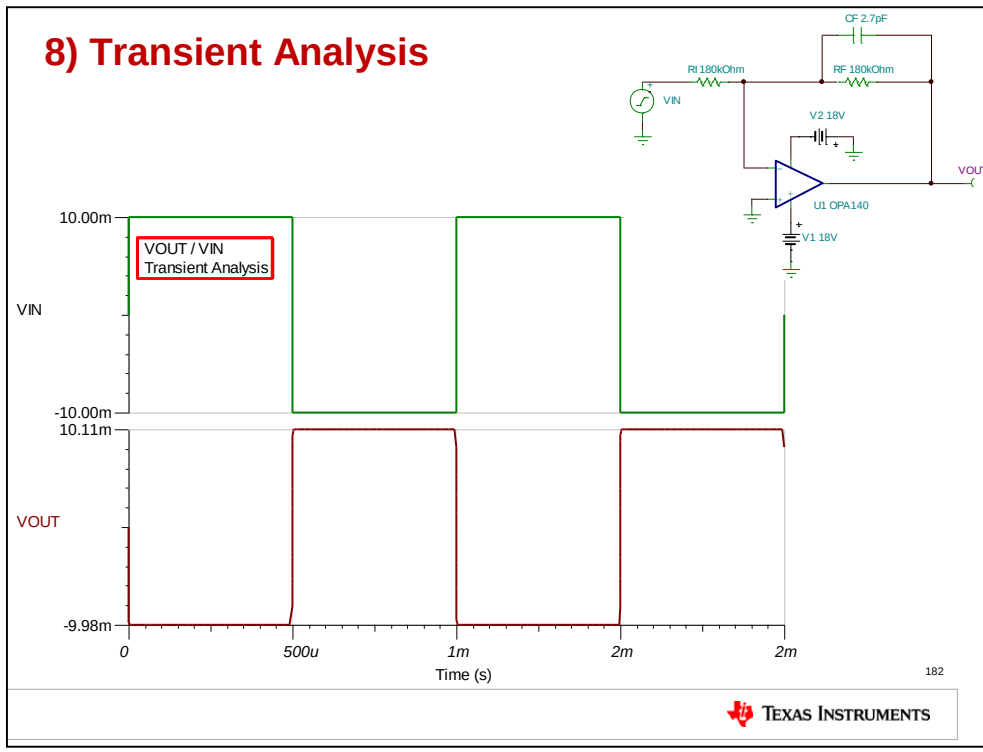
Design Step 7 for CF Compensation is to check the closed loop AC response over frequency. From above, see the closed loop AC response for both the output of the op amp, VOUT. If this closed loop bandwidth is not acceptable for the final application we will need to consider other capacitive stability techniques (see Appendix) or a different op amp or different feedback and input resistor values of lower values.

From above we have completed Step 7 for the CF Compensation Design:

7) Check closed loop AC response for VOUT/VIN

   A) Look for peaking which indicates marginal stability

   B) Check if closed AC response is acceptable for end application



Design Step 8 for CF Compensation is to check the closed loop transient response. From above we see the closed loop Transient response for VOUT shows no signs of excessive overshoot or ringing before settling.

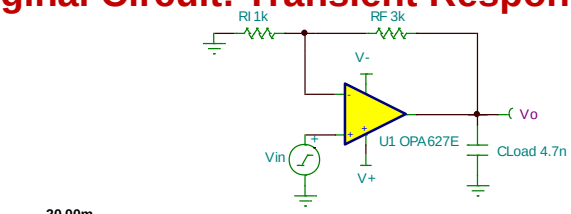
From above we have completed Step 7 for the CF Compensation Design:

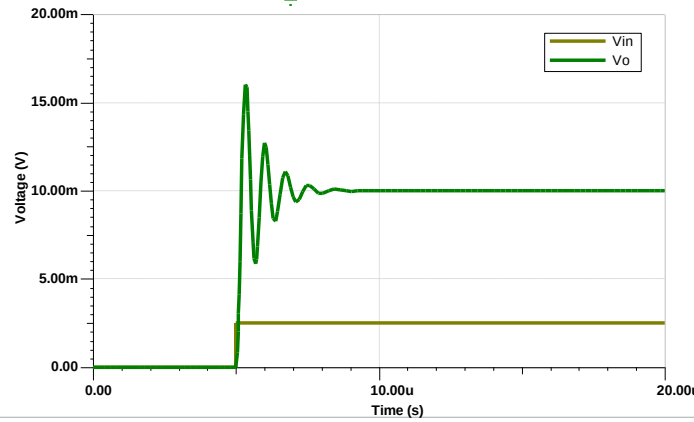
8) Check Transient response for VOUT/VIN

A) Overshoot and ringing in the time domain indicates marginal stability

9) Noise Gain Inverting and Noise Gain Non-Inverting (Output Cload)

Original Circuit: Transient Response



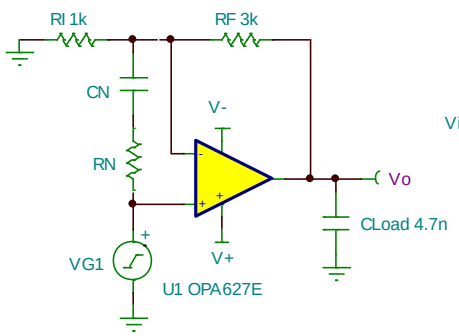


184

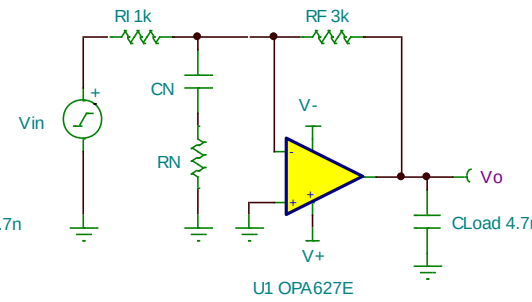
TEXAS INSTRUMENTS

Noise-Gain Compensation Circuit Configurations

Non-Inverting:



Inverting:



Noise-Gain Circuit Equations

1/β Transfer Function:

1/β Transfer function:

$$\frac{V_{out}(s)}{V_{fb}(s)} = \frac{R_F + R_I + (R_I \cdot R_F + R_N \cdot R_F + R_N \cdot R_I) \cdot C_N \cdot s}{R_I + R_N \cdot R_I \cdot C_N \cdot s}$$

DC 1/β Magnitude:

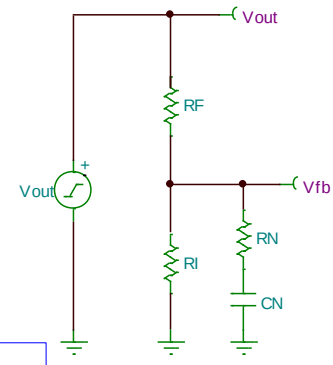
$$s=0,\ \frac{V_{out}(s)}{V_{fb}(s)} = 1+\frac{R_F}{R_I}$$

Hi-Freq 1/β Magnitude:

$$s=\infty,\ \frac{V_{out}(s)}{V_{fb}(s)} = 1/\beta\_Hi\text{-}f = 1+\frac{R_F}{R_I \parallel R_N}$$

=> Solve for RN

$$R_N = -\frac{R_I \cdot R_F}{R_I + R_F - R_I \cdot 1/\beta\_Hi\text{-}f}$$



1/Beta Pole Frequency:

$$fp3 = \frac{1}{2 \cdot \pi \cdot R_N \cdot C_N}$$

=> Solve for CN

$$C_N = \frac{1}{2 \cdot \pi \cdot R_N \cdot fp3}$$

1/Beta Zero Frequency:

$$fz1 = \frac{1}{2 \cdot \pi \cdot (R_N + R_I \parallel R_F) \cdot (C_N)}$$

The op amp equivalent input capacitance, CI, has been left out of these equations to simplify them. If CI and RF||RI are causing a stability issue (Appendix 7), consider a different approach

186

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Noise-Gain Compensation Design Steps

1) Break the loop and plot Aol and 1/ β
   A. Determine fp2 in Loaded Aol due to Cload
   B. Determine Aol Magnitude at fp2, Aol(fp2)
2) Select RN so 1/β_Hi-f ≥ Aol(fp2) +3dB
   1/β_Hi-f: the High-Frequency 1/β magnitude
   A. Plot 1/β_Hi-f and determine new fcl
3) Select value for CN based on required fp3 frequency
   A) Keep fp3 ≤ fcl/10
   B) To prevent AolB phase dip, Keep fp3 ≤ 10*fz1
4) SPICE simulation with Riso for Loop Gain (Aolβ) Magnitude and Phase
5) Adjust CN if greater Loop Gain (Aolβ) phase margin desired
6) Check closed loop AC response for VOUT/VIN
   A) Look for peaking which indicates marginal stability
   B) Check if closed AC response is acceptable for end application
7) Check Transient response for VOUT/VIN
   A) Overshoot and ringing in the time domain indicates marginal stability

187

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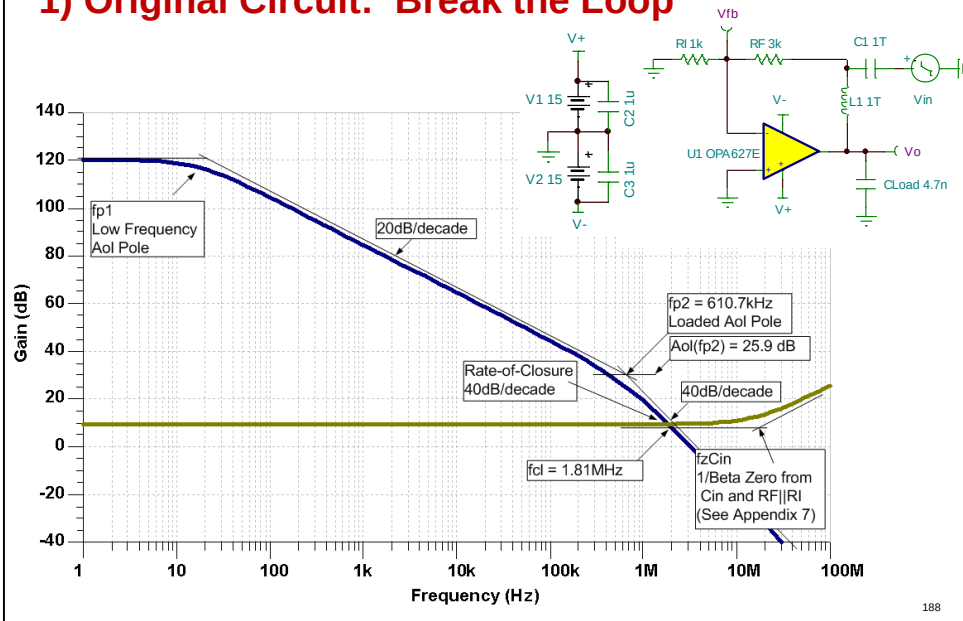
The Riso Compensation design steps are outlined here. Two cases, Case A and Case B, will be presented. Rules-of-thumb will be presented to yield best stability on first pass analysis.

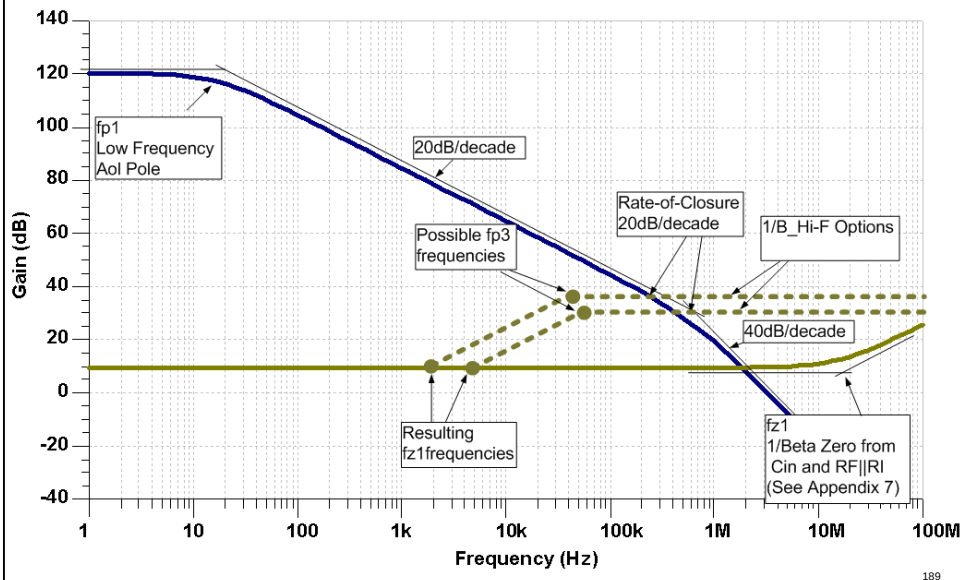
1) Original Circuit: Break the Loop



188

TEXAS INSTRUMENTS

1) Desired Compensation for Original Circuit



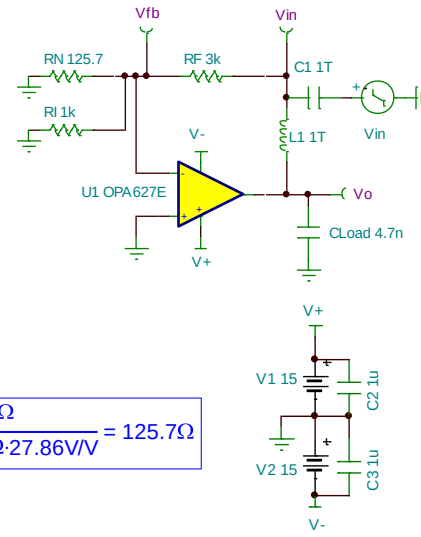
189

TEXAS INSTRUMENTS

2) Calculate RN

From Step 1:

Aol(fp2) = 25.9dB



For stability keep 1/β_Hi-F > Aol(fp2) +3dB:

1/β_Hi-f = Aol(fp2) + 3dB = 28.9dB

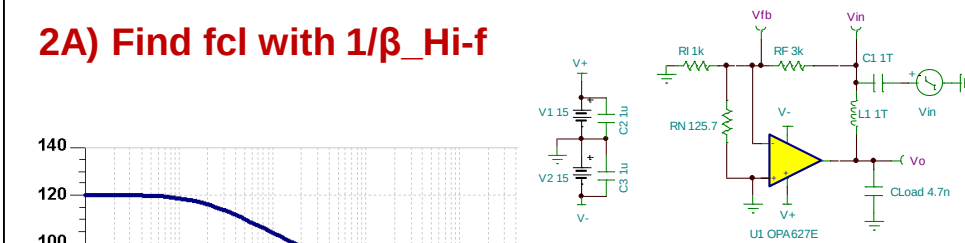
Convert 1/β_Hi-F to V/V:

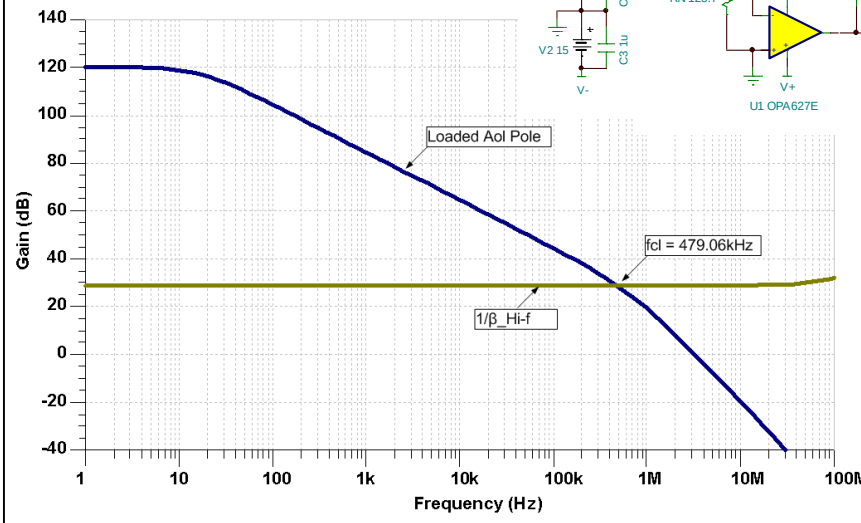
$28.9\text{dB} = 10^{\frac{28.9\text{dB}}{20}}\ \text{V/V} = 27.86\ \text{V/V}$

Calculate RN(min):

$$R_N(\text{min}) = -\frac{R_I \cdot R_F}{R_I + R_F - R_I \cdot 1/\beta\_\text{Hi-f}} = -\frac{1\text{k}\Omega \cdot 2\text{k}\Omega}{1\text{k}\Omega + 2\text{k}\Omega - 1\text{k}\Omega \cdot 27.86\text{V/V}} = 125.7\Omega$$

2A) Find fcl with 1/β_Hi-f





191

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3) Select CN

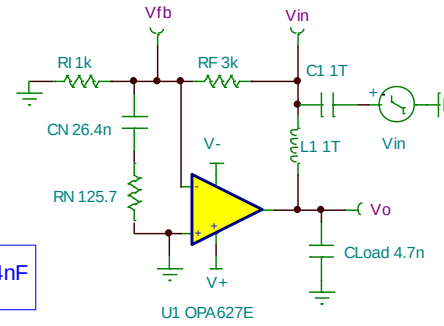
From Steps 1 and 4:

AoI(fp2) = 25.9dB
fcl = 479.06 kHz

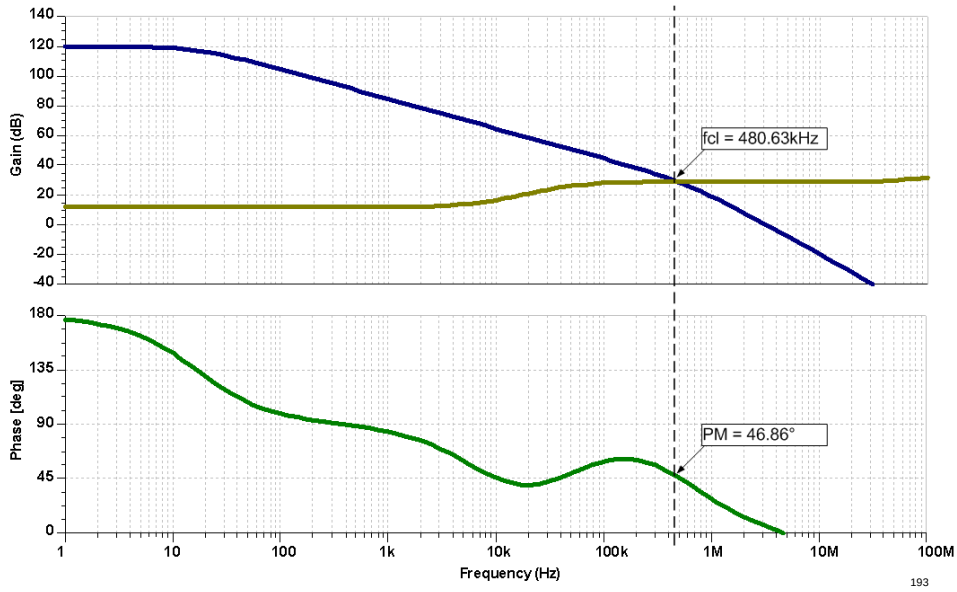
For stability keep fp3 ≤ fcl/10:

fp3 = fcl/10 = 47.906kHz

$$C_N = \frac{1}{2 \cdot \pi \cdot R_N \cdot fp3} = \frac{1}{2 \cdot \pi \cdot 125.7 \cdot 47.906kHz} = 26.4nF$$



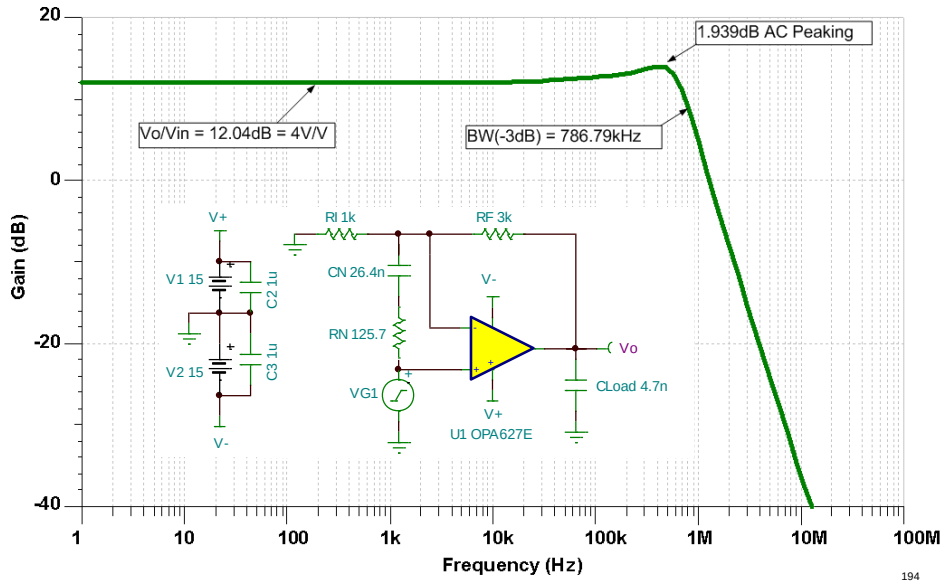
4),5) Plot Aol and 1/Beta for Compensated Circuit



193

TEXAS INSTRUMENTS

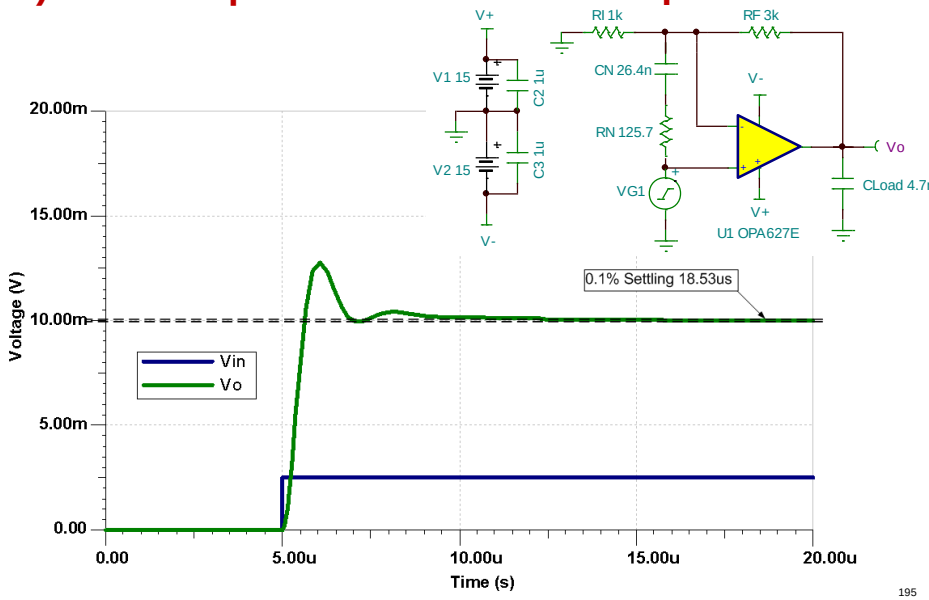
6) Plot Compensated Closed-Loop Gain



194

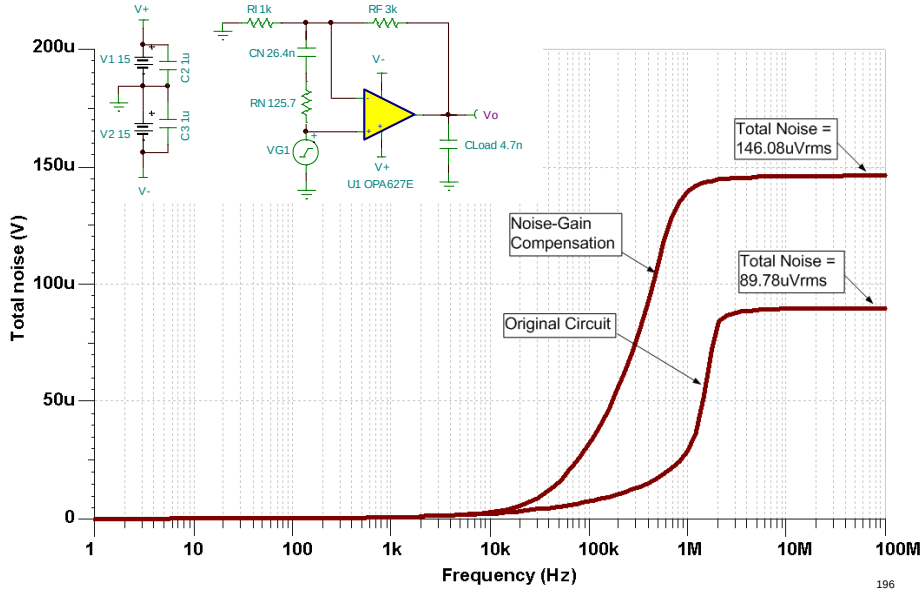
TEXAS INSTRUMENTS

7) Plot Compensated Transient Response



TEXAS INSTRUMENTS

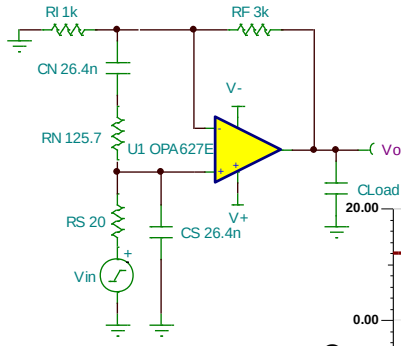
It’s called “Noise-Gain” for a reason



196

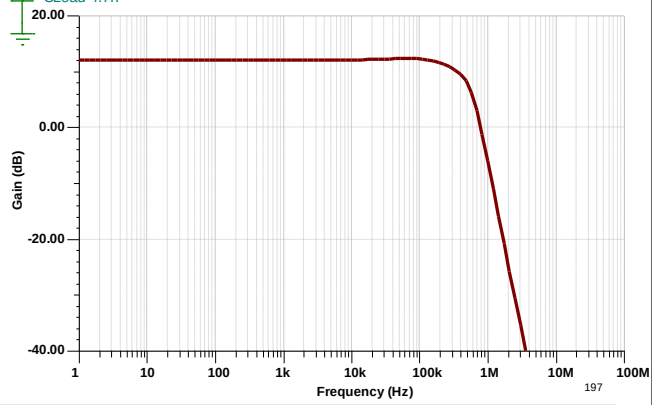
TEXAS INSTRUMENTS

Watch Out for Source Impedance



Note for Non-Inverting Noise Gain Compensation:

1) Keep Rsource (RS) < 1/10*RN
   OR
2) Add capacitor at U1, +input, to ground to lower impedance to < 1/10*RN at fp3 for effective Non-Inverting Noise Gain Compensation



197

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Noise-Gain Compensation Summary

1) Set 1/ β_Hi-f ≥ Aol(fp2)
2) Determine the new fcl
3) Set CN so fp3 ≤ fcl/10
4) Avoid using this circuit in instances where fp3 ≥ fz1*10 or large Loop Gain (Aolβ) phase dipping will occur which minimizes phase buffer for frequencies < fcl

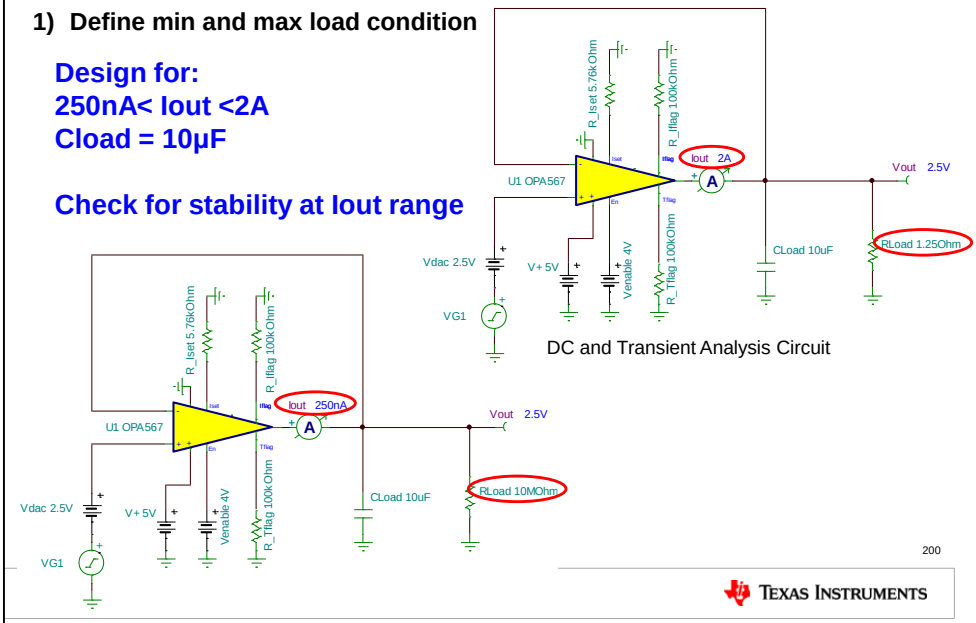
10) Noise Gain and CF (Output Cload)

Noise Gain and CF:
Programmable Power Supply (PPS) Design Example

1) **Define min and max load condition**

Design for:
250nA< Iout <2A
Cload = 10µF

Check for stability at Iout range

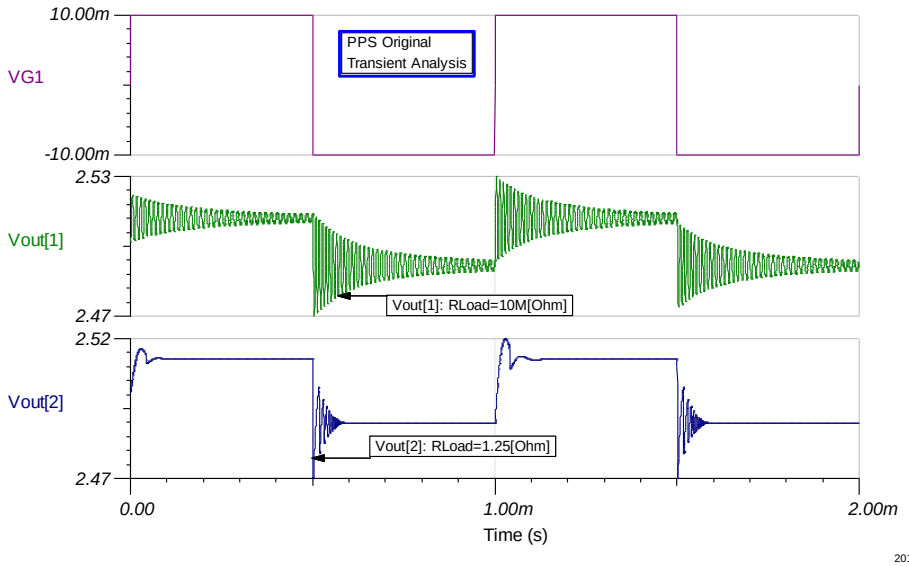


DC and Transient Analysis Circuit

200

TEXAS INSTRUMENTS

Original Transient Analysis



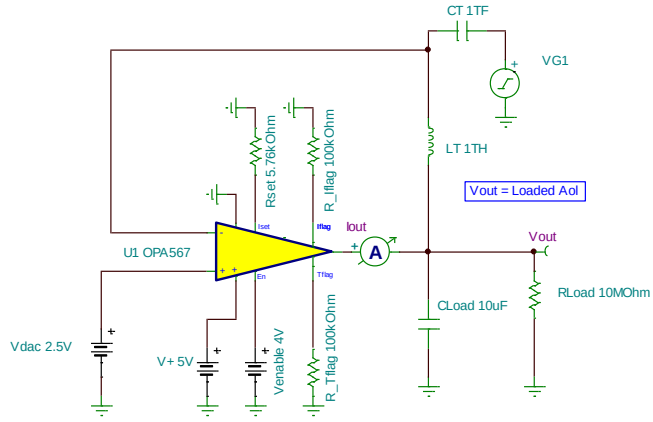
201

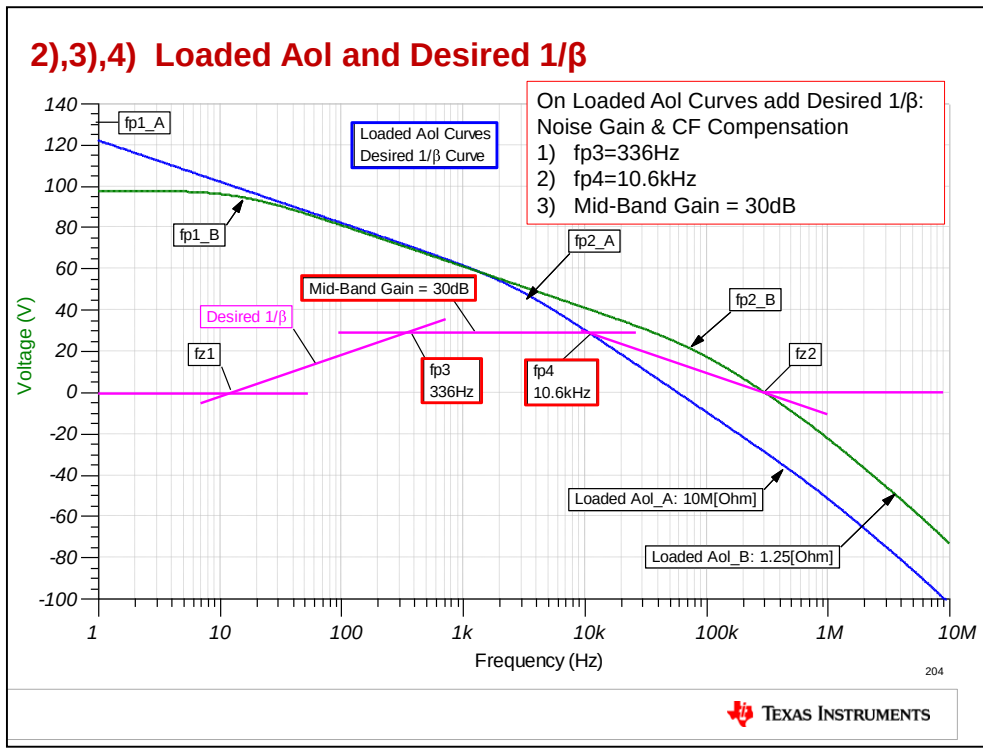
Noise Gain and CF Compensation Design Steps

1) Define min and max load condition
2) SPICE simulation for Loaded Aol curves (min and max load)
3) Plot Desired 1/β on Loaded Aol curves (min and max load)
   A) Use Noise Gain and CF Compensation
4) From Desired 1/β detemine fp3, fp4, and Mid-Band Gain
5) Compute values for RF, CF, Rn, Cn based on plotted fp3, fp4, Mid-Band Gain
6) SPICE simulation w/final compensation for Loop Gain (Aolβ) Magnitude and Phase
7) Adjust Compensation if greater Loop Gain (Aolβ) phase margin desired
8) Check closed loop AC response for VOUT/VIN
   A) Look for peaking which indicates marginal stability
   B) Check if closed AC response is acceptable for end application
9) Check Transient response for VOUT/VIN
   A) Overshoot and ringing in the time domain indicates marginal stability

The CF Compensation design steps are outlined here. Rules-of-thumb will be present to yield best stability on first pass analysis.

2) Loop Gain Check for Loaded Aol





1) Loaded Aol_A Curve:

fp1_A is low frequency pole from op amp unloaded Aol down around 1Hz. fp2_A is second pole in Loaded Aol_A due to Zo and CLoad.

2) Loaded Aol_B Curve:

fp1_B is low frequency pole in Loaded Aol due to lower resistive loading of 1.25 ohms on CMOS output. fp2_B is second pole in Loaded Aol_A due to Zo and CLoad.

3) Desired 1/β Curve:

fz1 and fp3 are a zero and pole due t noise gain set by Rn and Cn. We do not need to know exact location of fz1 since once we set fp3, fz1 can be seen graphically by using a +20dB/decade slope from fp3 down in frequency to the DC gain of 0dB. Noise gain fp3 is easy to find and compute.

fp4 is due to CF.

fz1 is the result of high frequency 1/β going to 0dB due to CF acting as a short at high frequencies.

All we need from our drawn, Desired 1/β curve is fp3, Mid-Band Gain and fp4. The other 1/β zeroes will occur as plotted by the nature of the input and feedback networks containing only one reactive element.

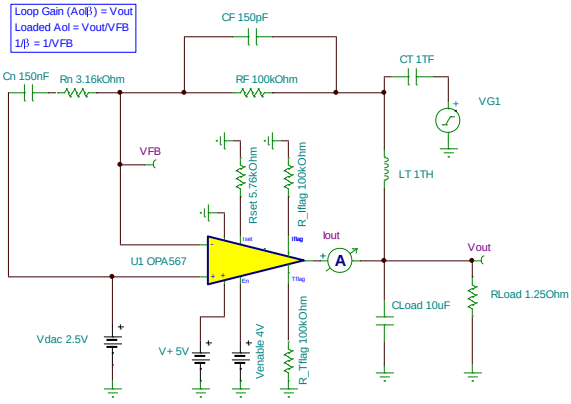
General considerations:

Because of the large difference between the two loaded Aol curves at high frequency it is necessary to plot the Desired 1/β as the best compromise to keep

most phase margin for the two cases. This is shown here. We will strive for better than 45 degrees phase margin for each case to allow for Aol shifts in the real world. A worst case Aol frequency shift at the Unity Gain Bandwidth (UGBW), over process and temperature, can be estimated as ½*UGBW to 1.5*UGBW. For best “Phase Buffer” we prefer to keep fp3 and fz1 one decade apart. We cannot quite do that here so we compromise as shown.

5) Noise Gain and CF Compensation

Noise Gain & CF Compensation
1) fp3=336Hz
2) fp4=10.6kHz
3) Mid-Band Gain = 30dB



Loop Gain (Aolβ), Loaded Aol, 1/ β Circuit

Desired $\frac{1}{\beta}$ Curve :

Set RF = 100kΩ

to use reasonable values for CF & Cn

$$\text{Mid}-\text{band Gain} = \frac{RF}{Rn} = 30dB$$

$$\frac{100k\Omega}{Rn} = 30dB = 31.6 \rightarrow Rn = 3.16k\Omega$$

$$fp3 = \frac{1}{2\pi * Rn * Cn}$$

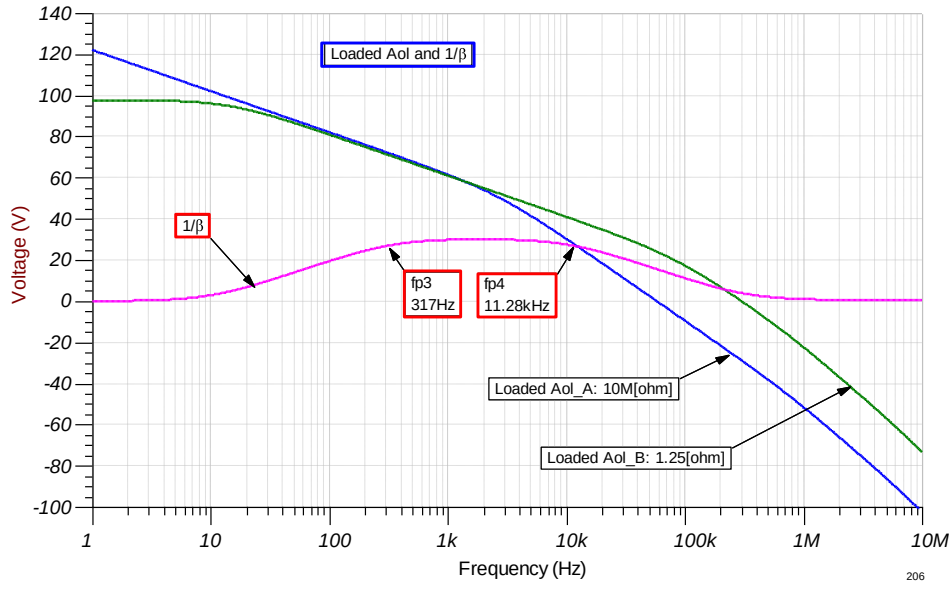
$$336Hz = \frac{1}{2\pi * 3.16k\Omega * Cn} \rightarrow Cn = 150nF$$

$$fp4 = \frac{1}{2\pi * RF * CF}$$

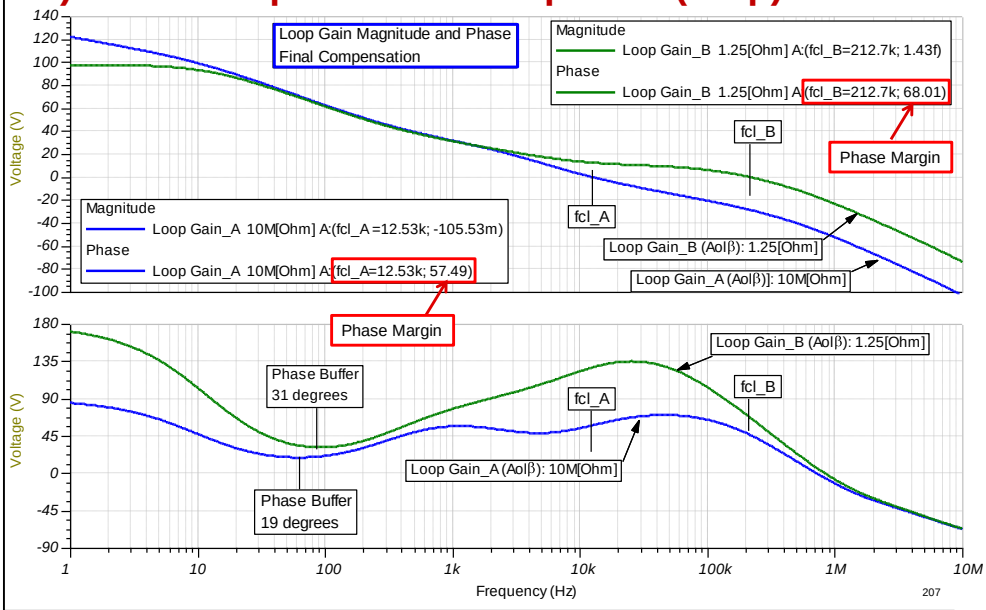
$$10.6kHz = \frac{1}{2\pi * 100k\Omega * CF} \rightarrow CF = 150pF$$

205

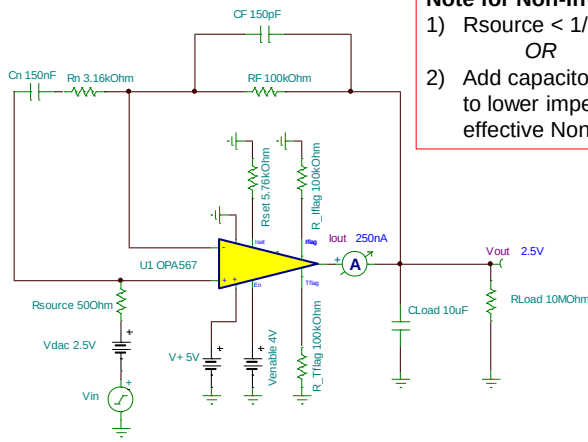
5) Final Compensation: 1/β & Loaded Aol



6) Final Compensation: Loop Gain (Aolβ)



7) Final Compensation: Vout/Vin AC Closed Loop



Note for Non-Inverting Noise Gain Compensation:

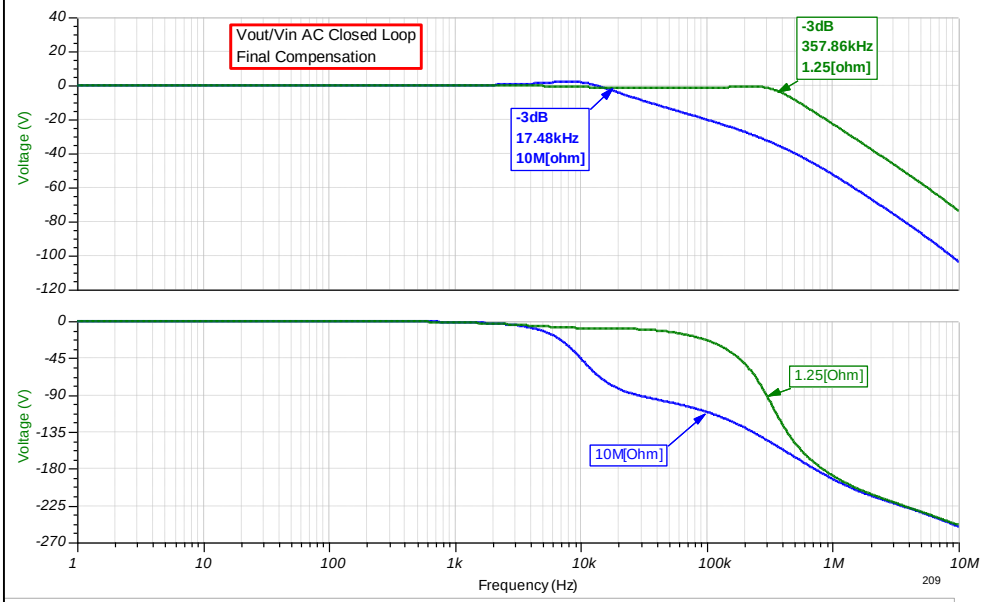
1) Rsource < 1/10*Rn

   OR

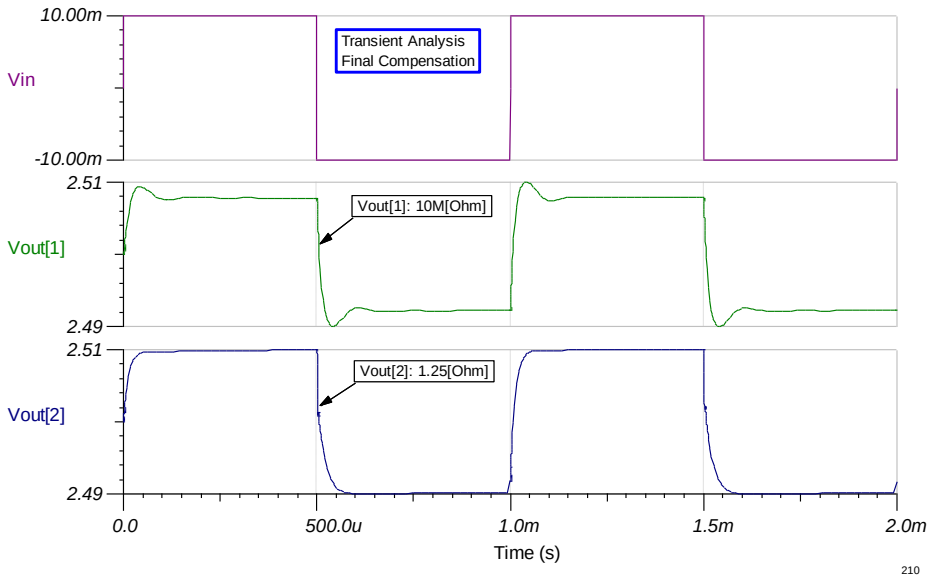
2) Add capacitor (>10*Cn) at U1, +input, to ground to lower impedance to < 1/10*Rn at fp3 for effective Non-Inverting Noise Gain Compensation

Vout/Vin AC Closed Loop and Transient Circuit

8) Final Compensation: Vout/Vin AC Closed Loop



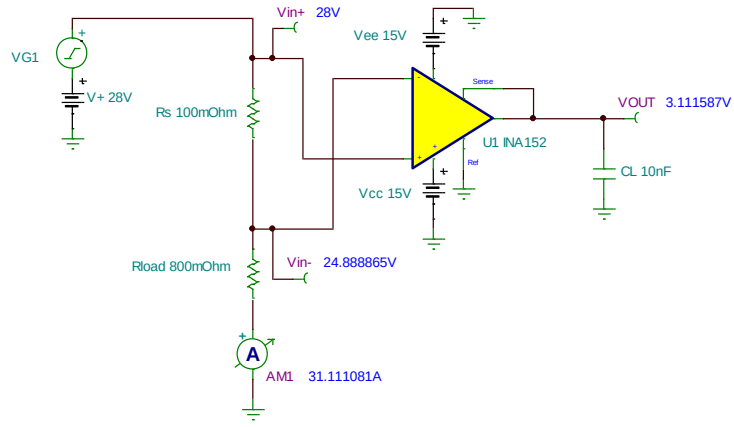
9) Final Compensation: Transient Analysis



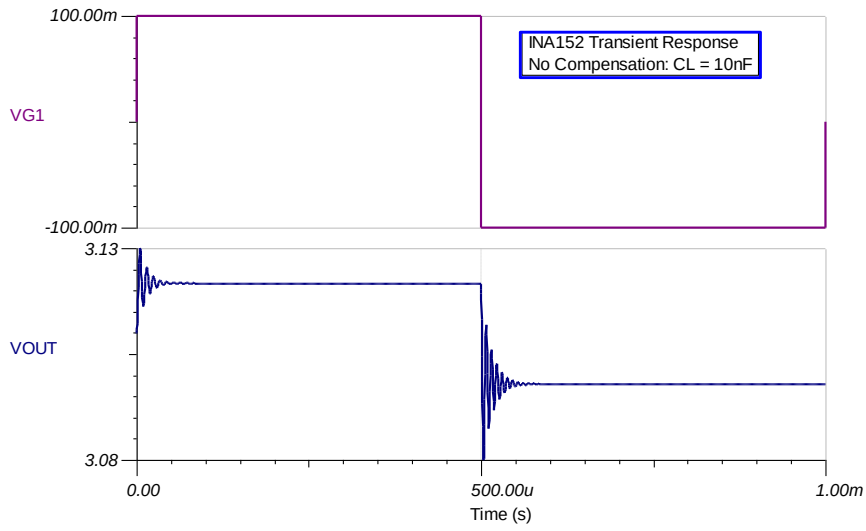
TEXAS INSTRUMENTS

11) Output Pin Compensation (Output Cload)

Output Pin Compensation – Design Example



INA152 Transient Analysis – No Compensation



213

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Aol Test Circuit for Difference Amp

At DC LT = Short

At any frequency of interest LT forces op amp open loop and VM is esentially 0V AC.
VP = VG1 since VIN+ and Ref are connected to VG1

Therefore:
Aol = VOA/VG1

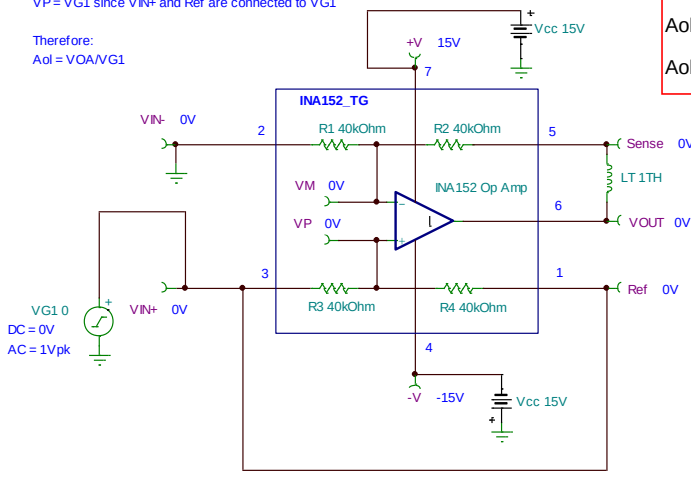
$1/\beta$:

$$\beta = \frac{R1}{R1+R2} = \frac{40k\Omega}{40k\Omega+40k\Omega} = \frac{1}{2}$$

$$\frac{1}{\beta} = 2 = 6dB$$

Aol :

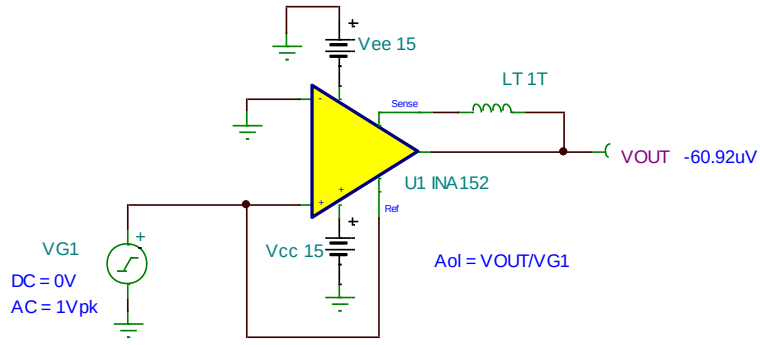
$$Aol = \frac{VOUT}{VG1}$$



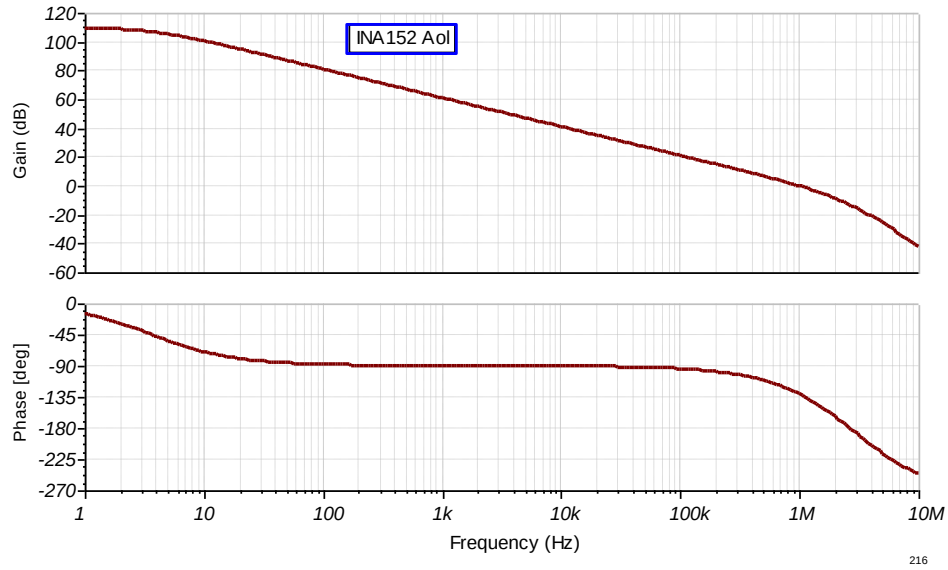
214

TEXAS INSTRUMENTS

INA152 Aol


Vee 15
LT 1T
Sense
VOUT -60.92uV
U1 INA152
Ref
VG1
DC = 0V
AC = 1Vpk
Vcc 15
Aol = VOUT/VG1

INA152 Aol



216

TEXAS INSTRUMENTS

Output Pin Compensation Design Steps

1) SPICE simulation for Loaded Aol curves (min and max load)
2) Measure Zo in SPICE
3) Determine if CLoad is on resistive portion of Zo
4) Plot Loaded Aol Original and Loaded Aol New for Ouptut Pin Compensation
5) Compute Rco and Cco and check Loaded Aol New in SPICE
6) SPICE simulation w/final compensation for Loop Gain (Aolβ) Magnitude and Phase
7) Adjust Compensation if greater Loop Gain (Aolβ) phase margin desired
8) Check closed loop AC response for VOUT/VIN
   A) Look for peaking which indicates marginal stability
   B) Check if closed AC response is acceptable for end application
9) Check Transient response for VOUT/VIN
   A) Overshoot and ringing in the time domain indicates marginal stability

217

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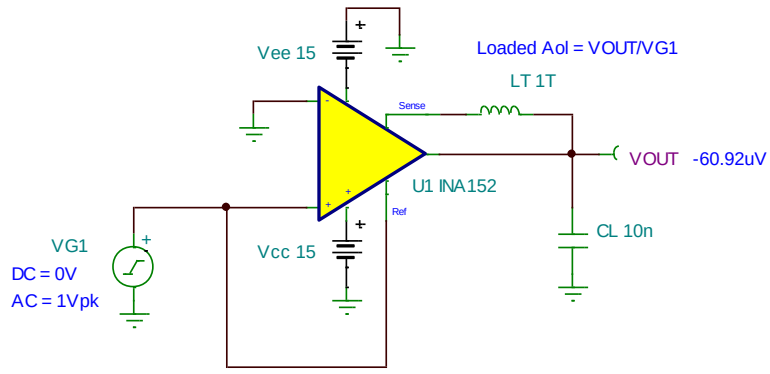
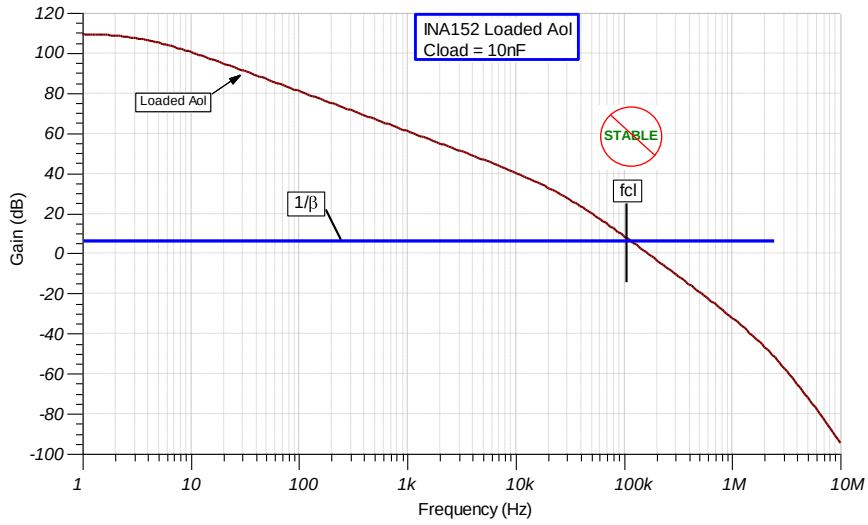
The CF Compensation design steps are outlined here. Rules-of-thumb will be present to yield best stability on first pass analysis.

1) INA152 Loaded Aol



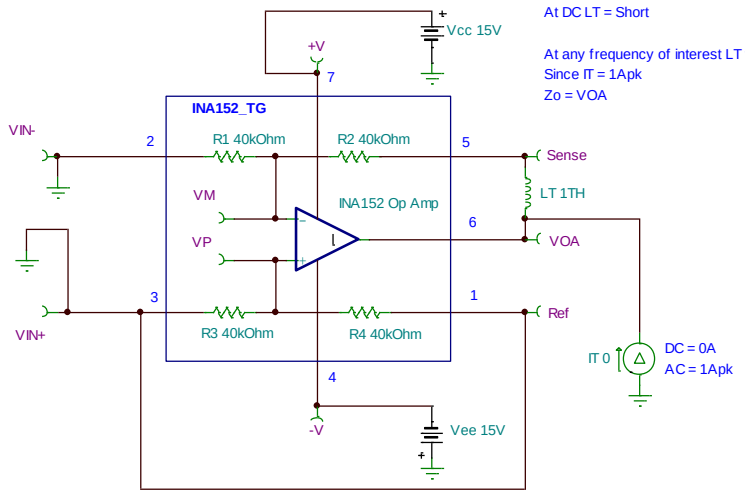
1) INA152 Loaded AoI



219

TEXAS INSTRUMENTS

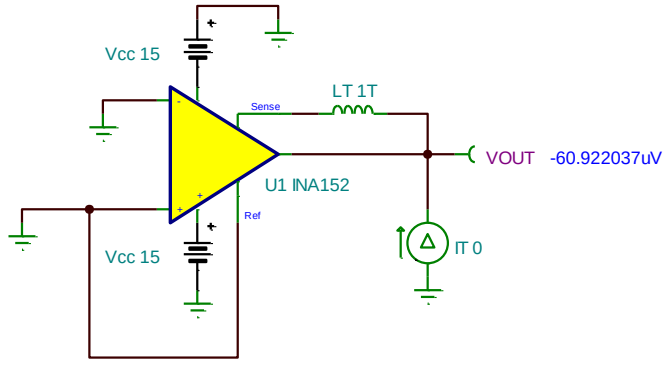
2) INA152 Z_O Test



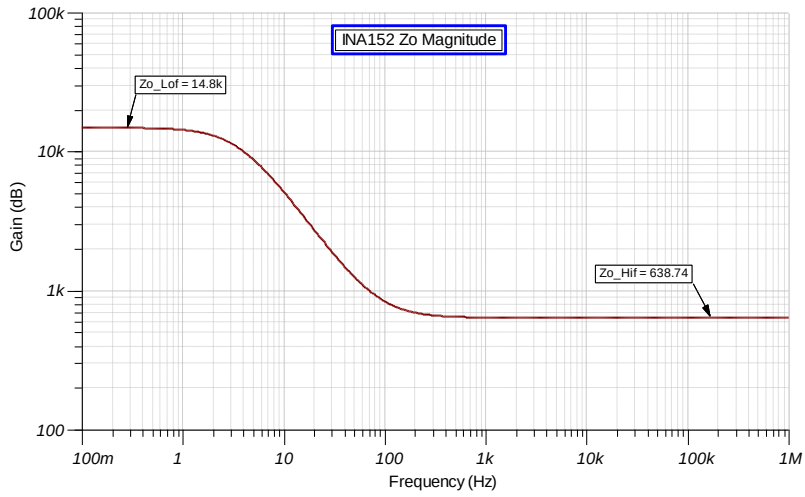
At DC LT = Short

At any frequency of interest LT forces op amp open loop
Since IT = 1Apk
Zo = VOA

2) TINA SPICE Z_O Test Circuit



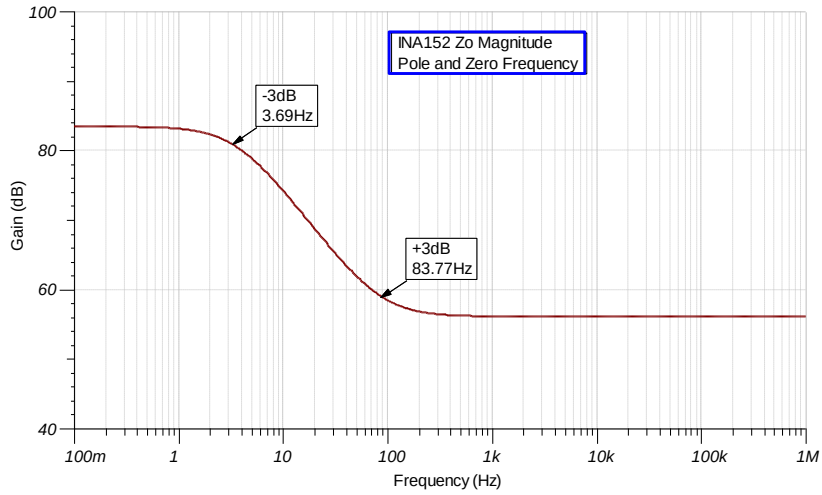
2) INA152 Z_O Magnitude



222

TEXAS INSTRUMENTS

2) INA152 Z_O Pole and Zero

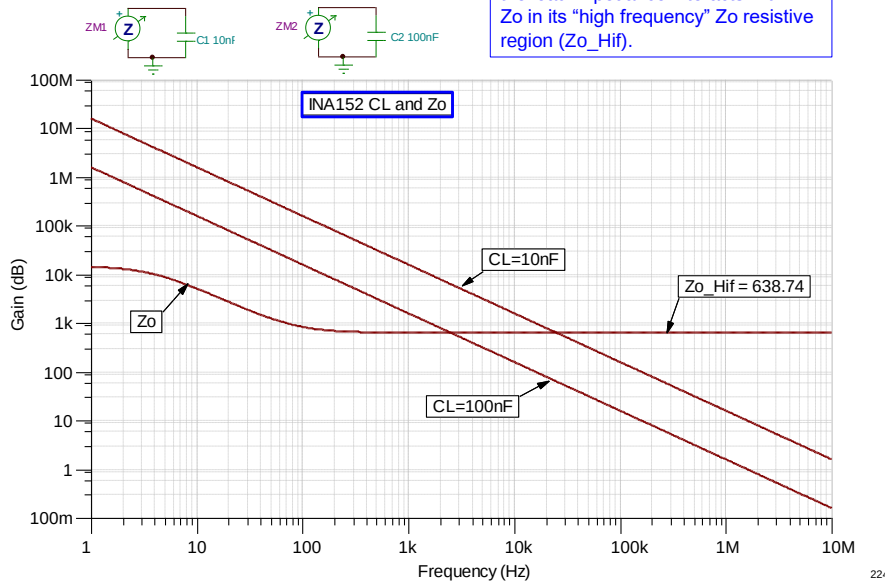


223

TEXAS INSTRUMENTS

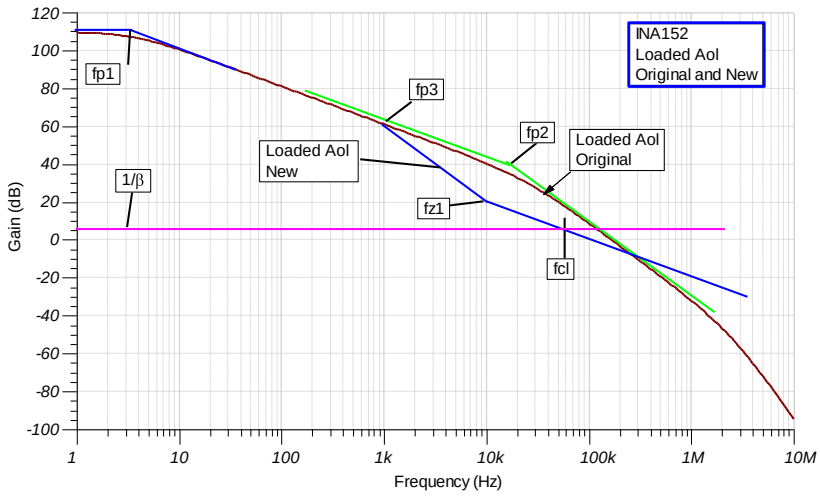
3) INA152 Z_O and CL

Note :
For both capacitive values of CL the load impedance interacts with Zo in its “high frequency” Zo resistive region (Zo_Hif).



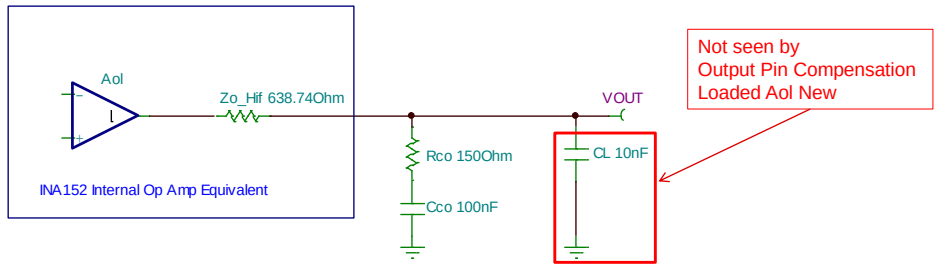
TEXAS INSTRUMENTS

4) INA152 Loaded Aol: Original and New



Add Cco = 10x CL then fp3 will move one decade to the left of fp2
Add Rco to create fz1
Keep fz1 $\leq$ 10*fp3 for overall best loop gain phase margin

5) Compute Rco and Cco



Output Pin Compensation : Loaded Aol New

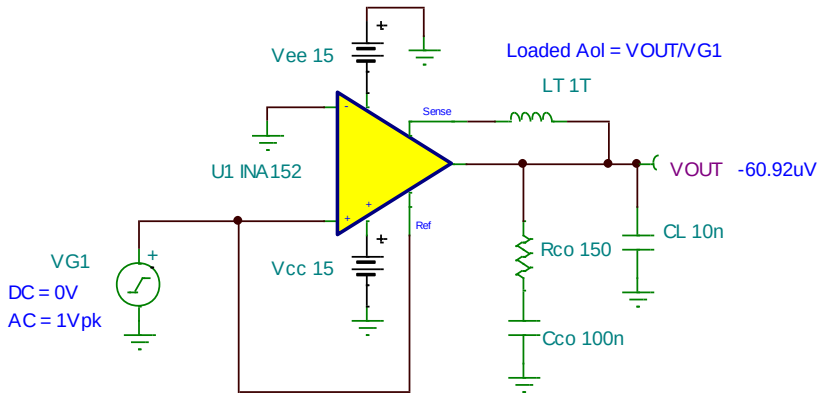
$$fp3 = \frac{1}{2*\pi*(Zo\_Hif + Rco)*Cco}$$

$$fp3 = \frac{1}{2*\pi*(638.74\Omega + 150\Omega)*100nF} = 2.02kHz$$

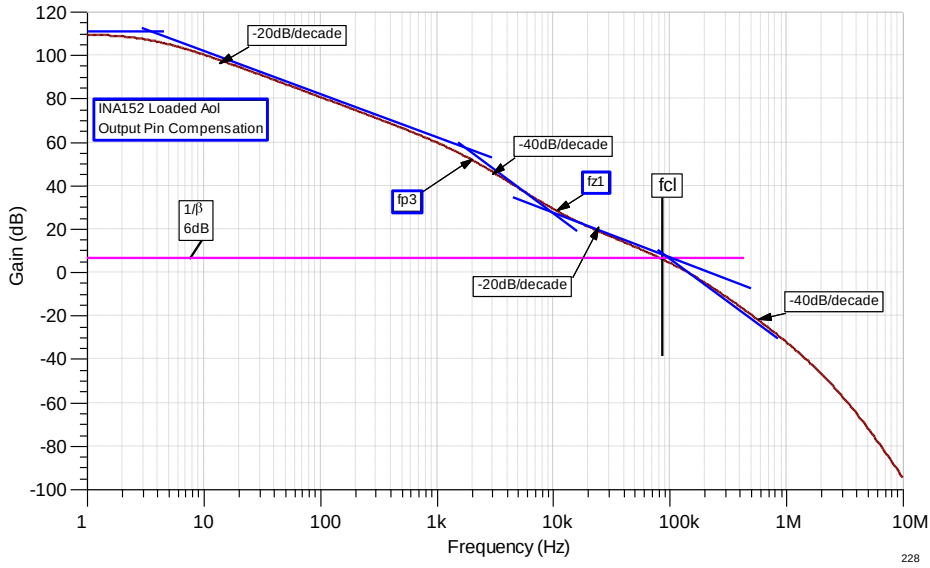
$$fz1 = \frac{1}{2*\pi*Rco*Cco}$$

$$fz1 = \frac{1}{2*\pi*150\Omega*100nF} = 10.6kHz$$

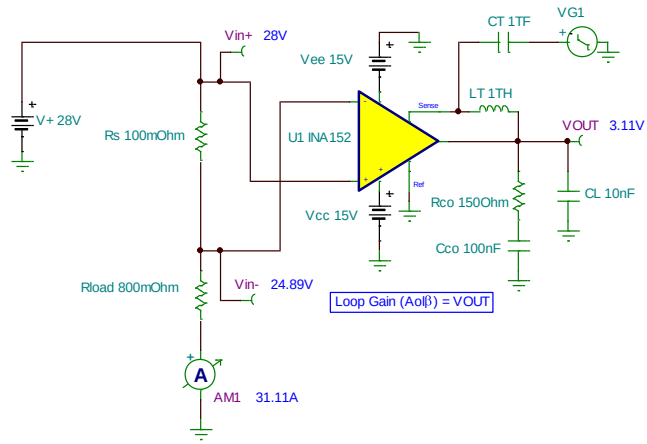
5) Compute Rco and Cco and check in SPICE



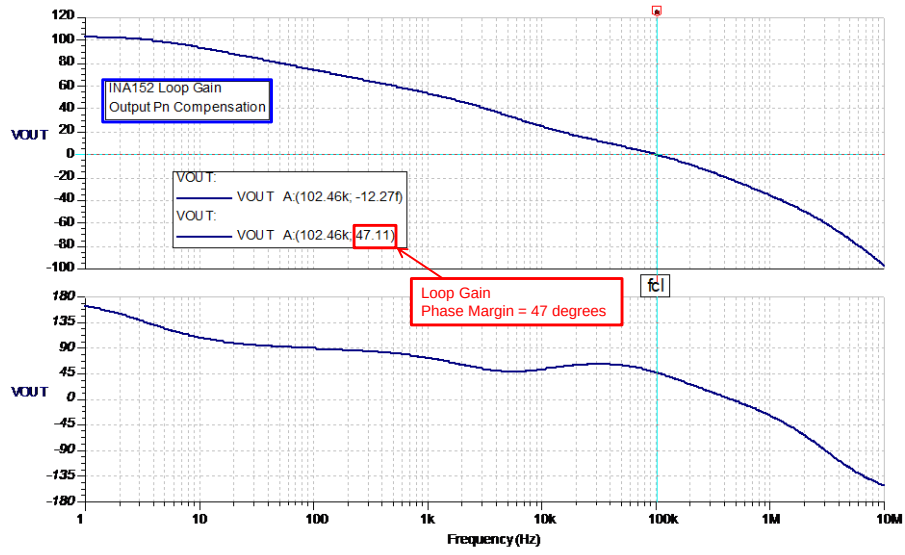
5) Compute Rco and Cco and check in SPICE



6),7) Loop Gain Check



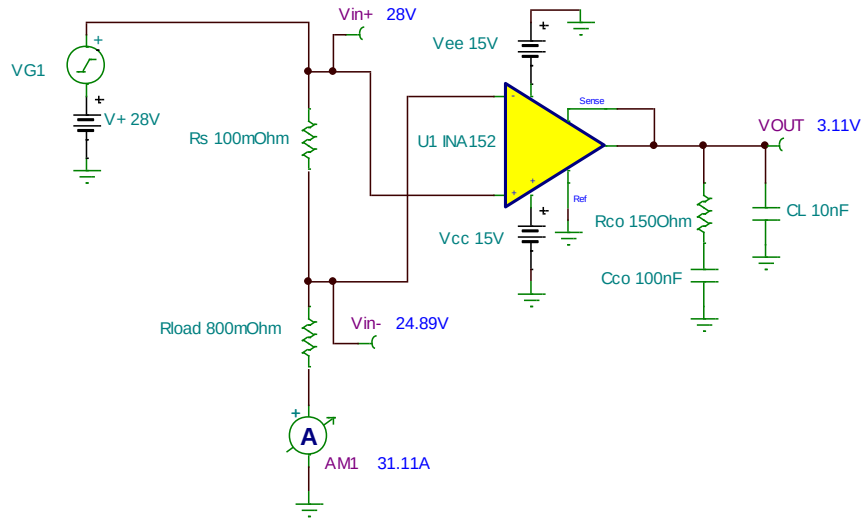
6),7) Loop Gain Check



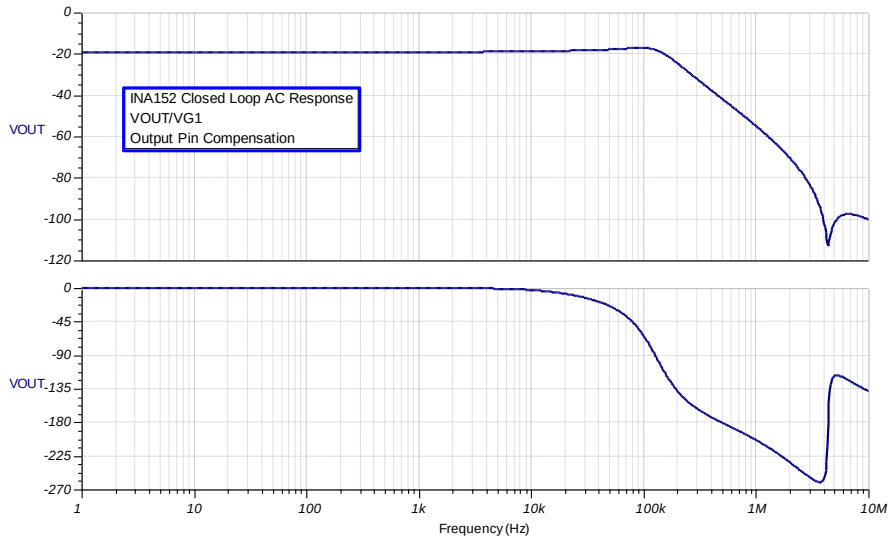
230

TEXAS INSTRUMENTS

8) Closed Loop AC Response

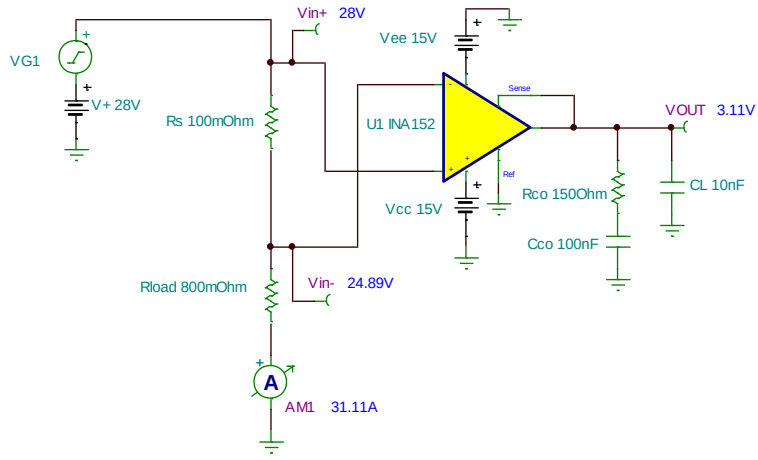


8) Closed Loop AC Response

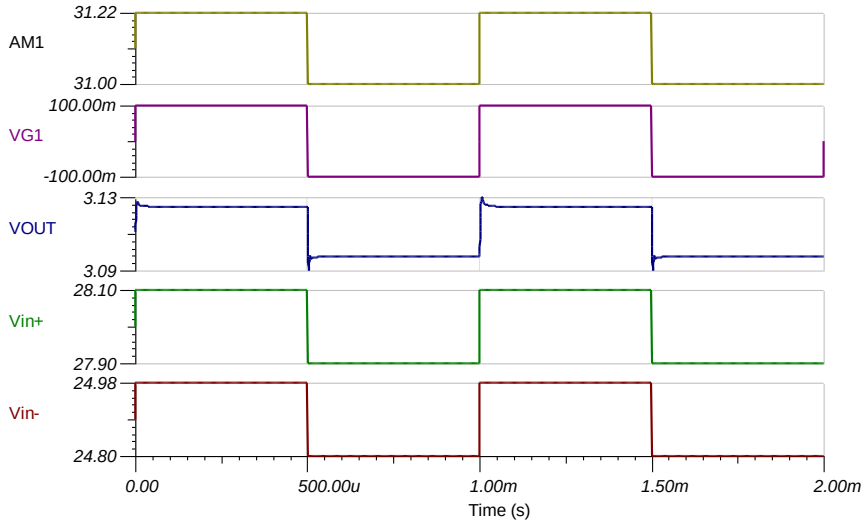


232

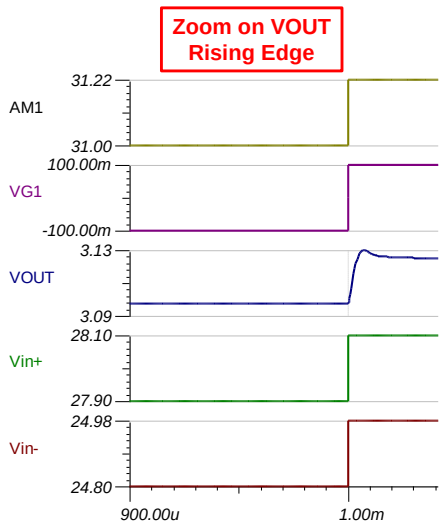
9) Transient Analysis

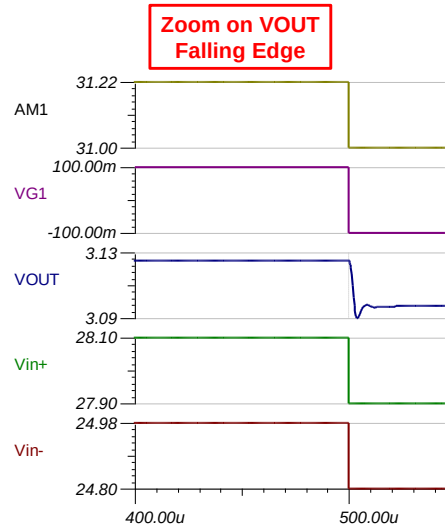


9) Transient Analysis



9) Transient Analysis





12) Riso with Dual Feedback (Output Cload) - Zo, 1/β, Aol Technique

Riso with Dual Feedback- Zo, 1/β, Aol Technique

1) Given: Op Amp and Cload
2) Determine Op Amp Zo
   A) Measure in SPICE *OR* Data Sheet Curve
3) Create External Zo Model for Loop Gain Analysis only
4) If large RF value to be used model Cin_eq
4) Set Riso = 1/10*Ro → 1/β_Hif ≈ 20dB
5) SPICE simulation: Aol, 1/β FB#1
   A) FB#1 gives: 1/β_Lof and fz1
6) Draw 1/β FB#2 (1/β_Hif ≈ 20dB from Step 4)
   A) fp1=10*fz1
   B) fz3=1/10*fp1
   C) fp1≤1/10*fcl
7) Choose RF and CF so standard values yield fz3
8) SPICE simulation: Loop Gain (Aolβ) Magnitude & Phase
   A) Adjust compensation for more Loop Gain (Aolβ) phase margin if needed
9) Check closed loop AC response for VOUT/VIN
   A) Look for peaking which indicates marginal stability
   B) Check if closed AC response is acceptable for end application
10) Check Transient response for VOUT/VIN
   A) Overshoot and ringing in the time domain indicates marginal stability

237

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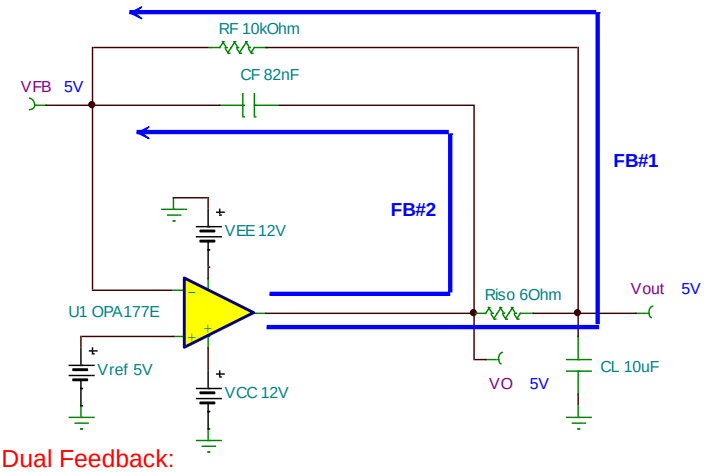
The Riso Compensation design steps are outlined here. Two cases, Case A and Case B, will be presented. Rules-of-thumb will be presented to yield best stability on first pass analysis.

1) Riso w/Dual Feedback

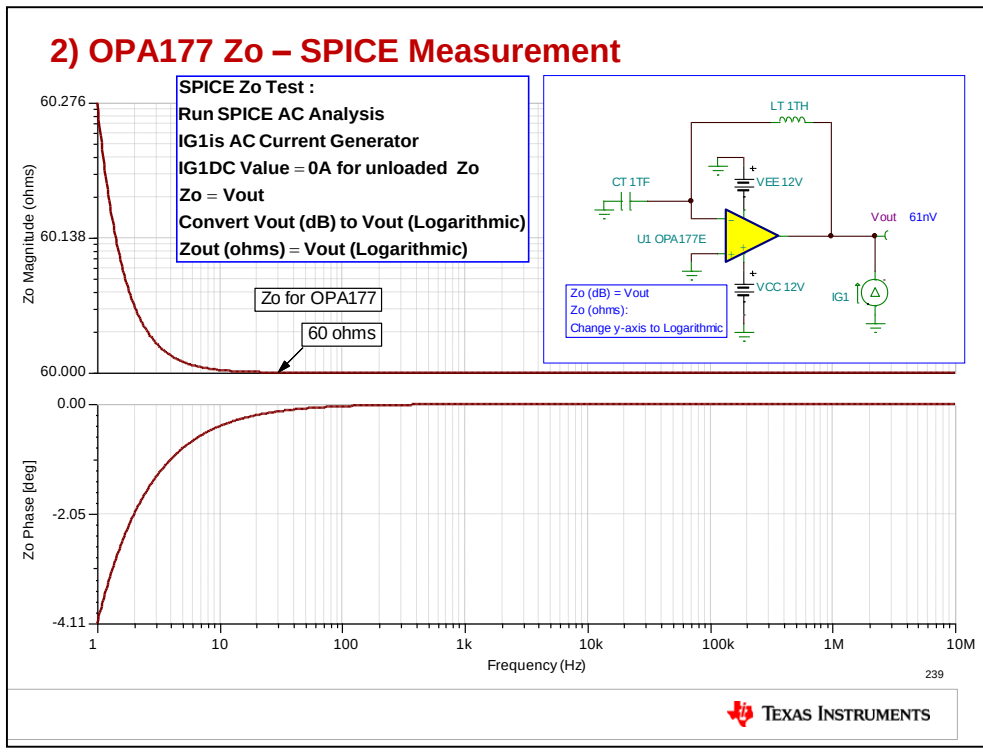


Dual Feedback:

FB#1 through RF forces accurate Vout across CL

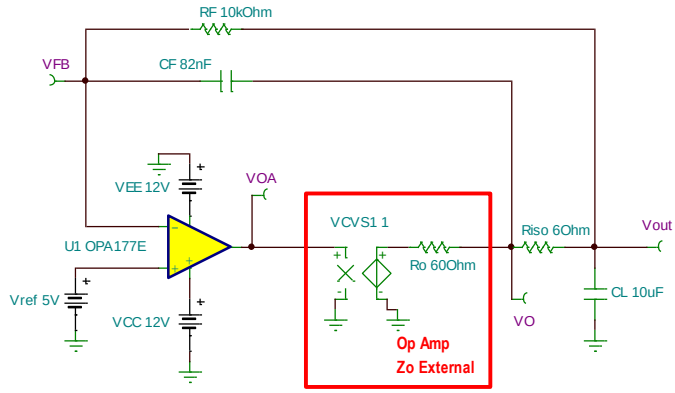
FB#2 through CF dominates at high frequency for stability

Riso provides isolation between FB#1 and FB#2



For many op amp application circuits is will be necessary to know the op amp Open Loop Small Signal AC Output Impedance, Zo. Often this can be obtained from the op amp data sheet. Many op amp SPICE macromodels properly model Zo. If the data sheet contains a Zo curve we can easily check the macromodel for Zo accuracy. The test circuit here uses inductor, LT, in the feedback path to act as a short for the DC Operating Point analysis. The capacitor, CT, on the – input to ground is open for DC Analysis and will be a short for all frequencies of interest during the AC Analysis. Current Generator, IG1, is set to DC Current =0 and selected as AC Current of 1. During the AC Analysis IG1 injects current into the output, Vout, and the op amp is open loop. AC Analysis reports Vout in dB over frequency as a ratio of Vout/IG1 which is Zo, in dB. To convert Zo in dB to Zo in ohms simply change the y-axis scaling from dB-Linear to logarithmic.

3) Riso w/Dual Feedback – Zo External Model



Zo External Model:

VCVS1 ideally isolates U1 so U1 only provides data sheet Aol at VOA

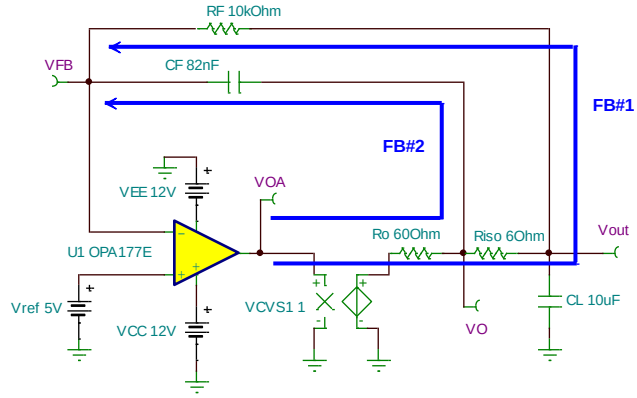
Set Ro to match measured Ro

Analyze with unloaded Ro (largest Ro) which creates worst instability

Use 1/β on Aol stability analysis

1/ β, taken from VOA, will include the effects of Zo, Riso, and CL

3) Zo External Model, FB#1 and FB#2 Analysis



FB#1 and FB#2 1/ β Analysis:

There is only one net voltage fed back as β to the –input of the op amp

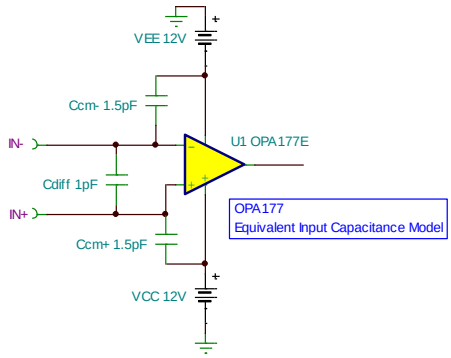
β_net = β_FB#1 + β_FB#2

This implies that the largest β will dominate → smallest 1/ β will dominate

Analyze FB#1 with CF = open since it will only dominate at high frequencies

Analyze FB#2 with CL = short since it is at least 10x CF

4) OPA177 Input Capacitance




```
*******************************
* OPA177 "E" - ENHANCEMENTS
*******************************
* OUTPUT SUPPLY MIRROR
FQ3   0 20 POLY(1) VLIM 0  1
DQ1  20 21 DX
DQ2  22 20 DX
VQ1  21  0 0
VQ2  22  0 0
FQ1   3  0 POLY(1) VQ1  0.976E-3  1
FQ2   0  4 POLY(1) VQ2  0.976E-3 -1
* QUIESCIENT CURRENT
RQ    3  4  3.0E4
* DIFF INPUT CAPACITANCE
CDIF  1  2  1.0E-12
* COMMON MODE INPUT CAPACITANCE
C1CM  1  99 1.5E-12
C2CM  2  99 1.5E-12
```

OPA177 Input Capacitance:

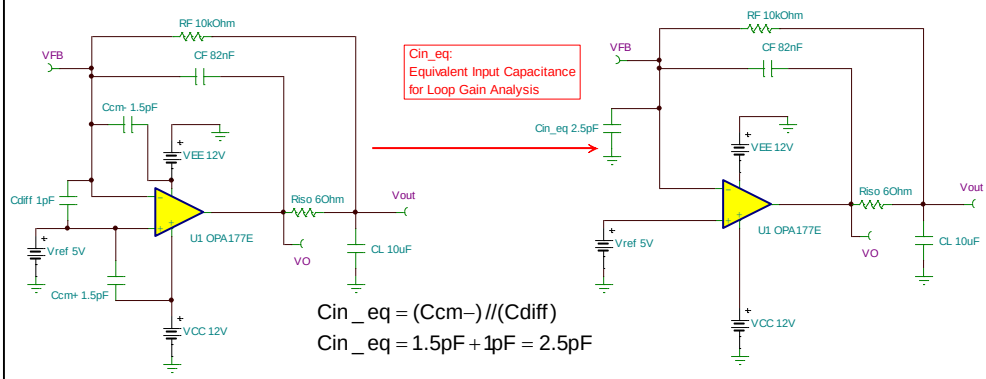
Ccm- and Ccm+ are common mode input capacitance

Cdiff is differential input capacitance

Ccm and Cdiff can usually be found in op amp data sheet

For OPA177 Ccm and Cdiff are found inside the SPICE macromodel

4) Cin_eq → Equivalent Input Capacitance for Loop Gain Analysis



$$Cin\_eq = (Ccm-)\,//\,(Cdiff)$$
$$Cin\_eq = 1.5pF + 1pF = 2.5pF$$

Input Capacitance and Loop Gain Analysis:

Final Loop Gain circuit break needs to break both FB#1 and FB#2

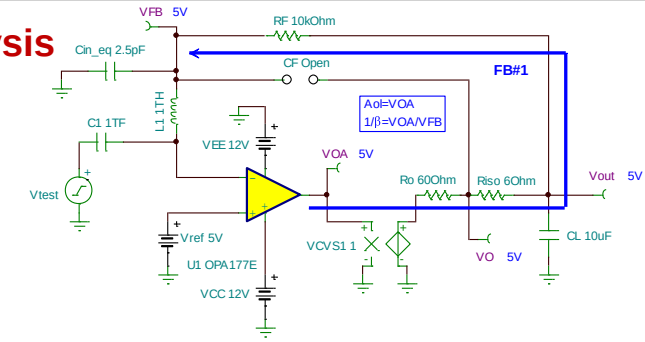
Loop Gain circuit break will need to be made on op amp –input

For some op amps feedback elements can interact with input capacitance and add zero or pole to 1/β

For Loop Gain analysis break loop at –input but add Cin_eq

243

5) 1/β FB#1 Analysis



$\frac{1}{\beta}$ FB#1 Analysis :

For CL > 10 * CF then FB#2 will only dominate at high frequencies

FB#2 can be viewed as an open for analysis of FB#1

$$fpz1 = \frac{1}{2*\pi*CL*(Ro+Riso)} = \frac{1}{2*\pi*10\mu F*(60\Omega+6\Omega)} = 241Hz$$

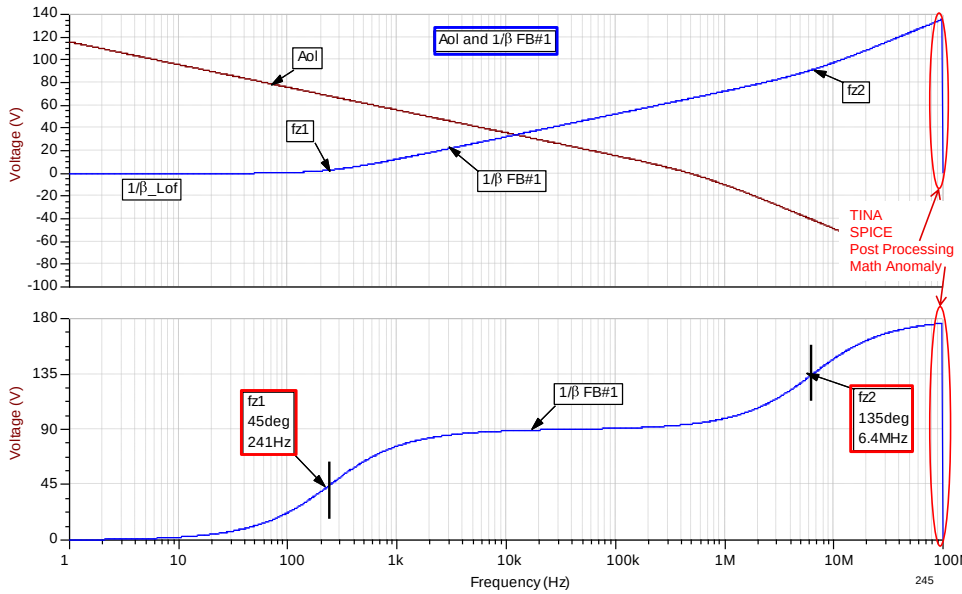
For : RF > 10 * (Ro + Riso)

$$fpz2 = \frac{1}{2*\pi*Cin\_eq*RF} = \frac{1}{2*\pi*2.5pF*10k\Omega} = 6.4MHz$$

$$\frac{1}{\beta}\_Lof = 1 \rightarrow 0dB$$

Set Riso = 1/10*Ro
→ 1/β_Hif ≈ 20dB

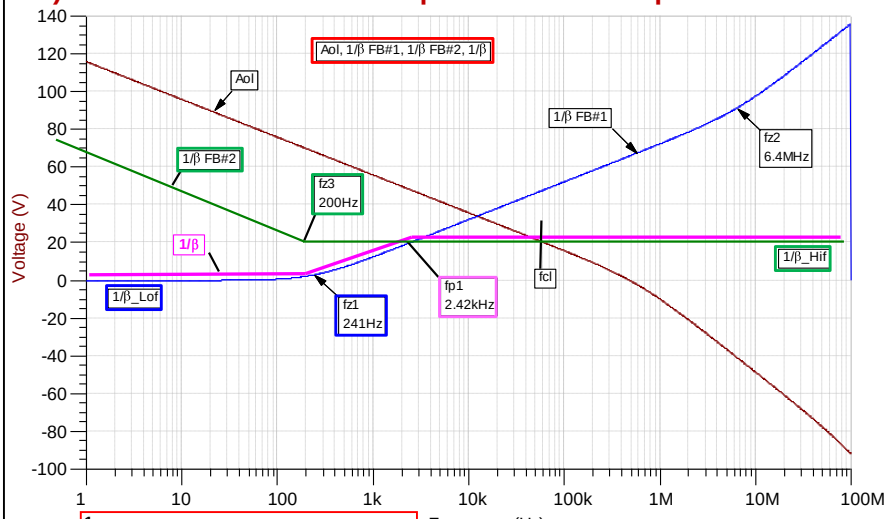
5) 1/β FB#1 SPICE Results



245

TEXAS INSTRUMENTS

6) Add FB#2: Draw Desired 1/β FB#2on Aol & 1/β FB#1 Curves



246

Note :

- $\frac{1}{\beta}$_Lof and fz1 set by FB#1
- $\frac{1}{\beta}$_Hif and fz3 set by FB#2
- $\frac{1}{\beta}$_fp1 set by intersection of $\frac{1}{\beta}$ FB#1 and $\frac{1}{\beta}$ FB#2

Set : $fp1 = 10 * fz1$

Set : $fz3 = \frac{1}{10} * fp1$

Set : $fp1 \leq \frac{1}{10} * fcl$

Set Riso = 1/10*Ro
→ 1/β_Hif ≈ 20dB

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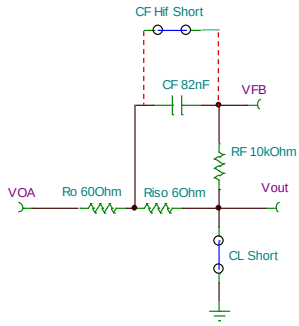
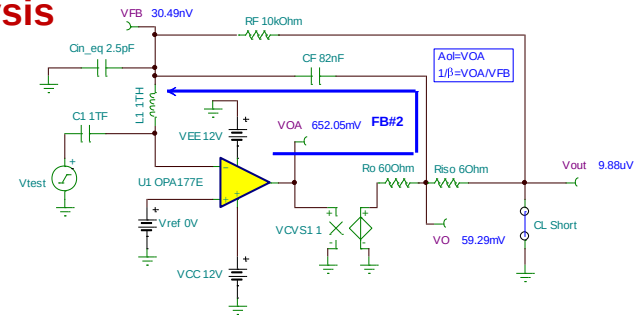
7) 1/β FB#2 Analysis





For 1/β FB#2 SPICE Analysis:
Set Vref = 0V
Else OPA177 VOA will saturate with Vout = 5V into a short

$\frac{1}{\beta}$ FB#2 Analysis :

For CL > 10 * CF then CL will look like low impedance for FB#2

CF can be viewed as short for analysis of FB#2

$$\frac{1}{\beta}\_Hif = \frac{Ro + Riso}{Riso} = \frac{60\Omega + 6\Omega}{6\Omega} = 11 \rightarrow 20.8dB \leftarrow \textbf{CF = short at Hif}$$

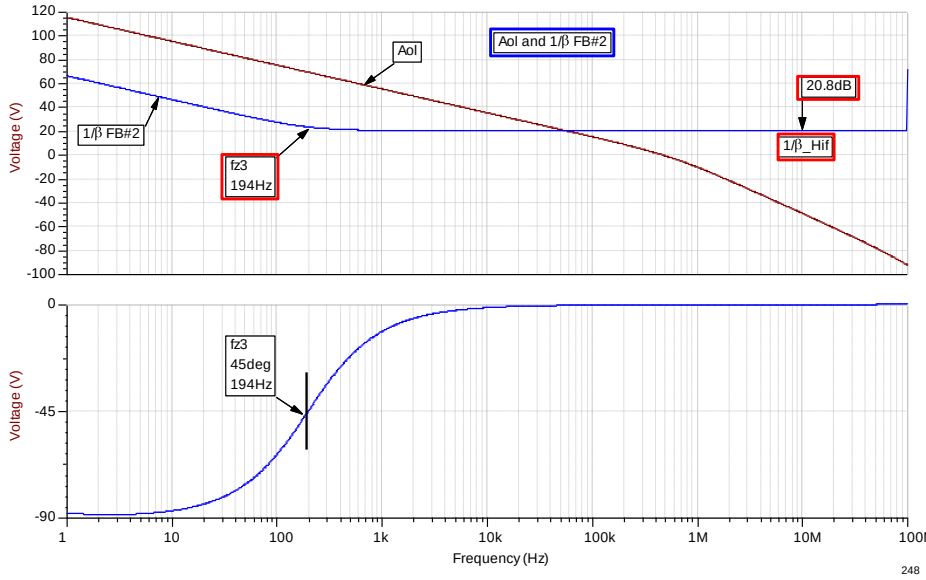
Set Riso = 1/10*Ro
→ 1/β_Hif ≈ 20dB

$$fz3 = \frac{1}{2 * \pi * CF * RF} = \frac{1}{2 * \pi * 82nF * (10k\Omega)} = 194Hz$$

247

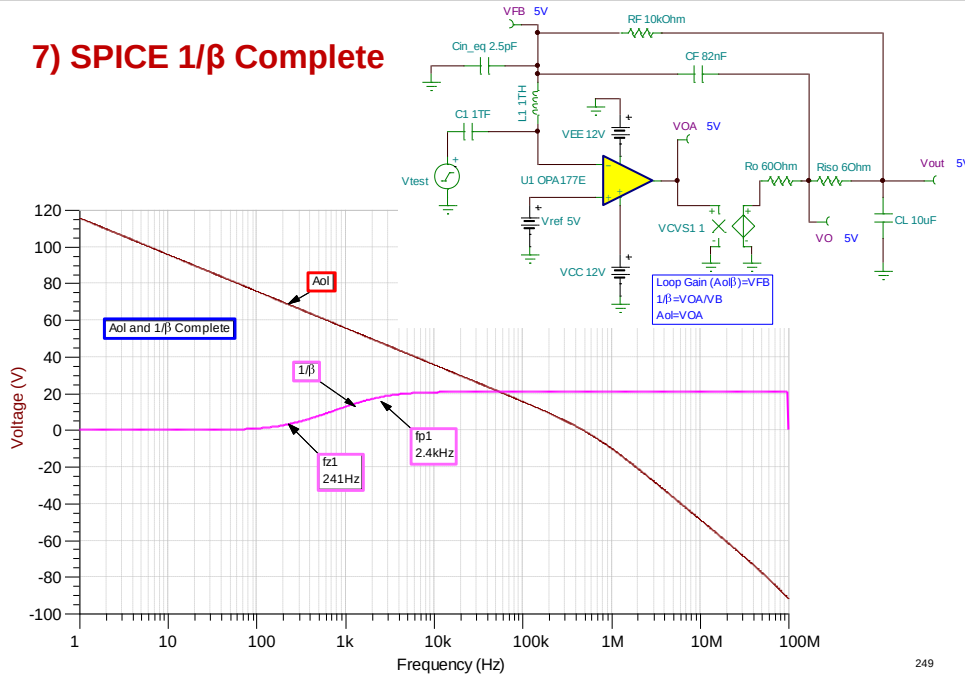
TEXAS INSTRUMENTS

7) 1/β FB#2 SPICE Results



248

7) SPICE 1/β Complete



249

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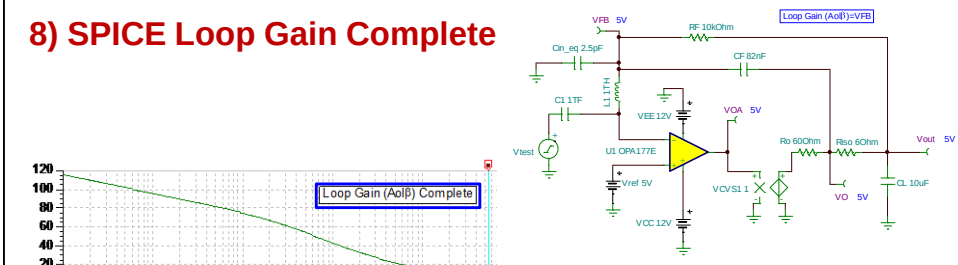
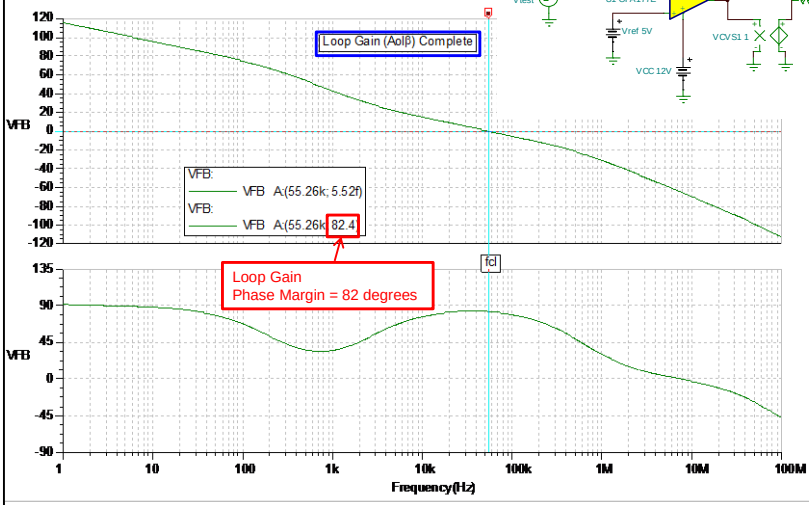
8) SPICE Loop Gain Complete

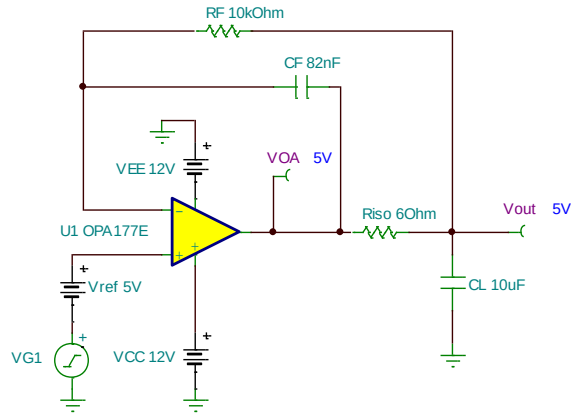




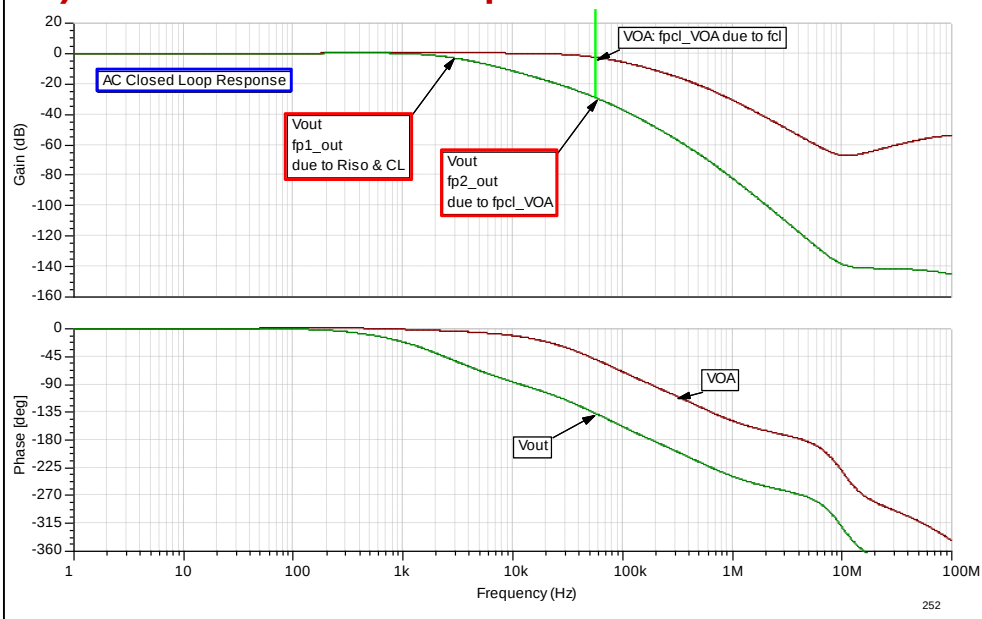
250

TEXAS INSTRUMENTS

9) SPICE AC Closed Loop

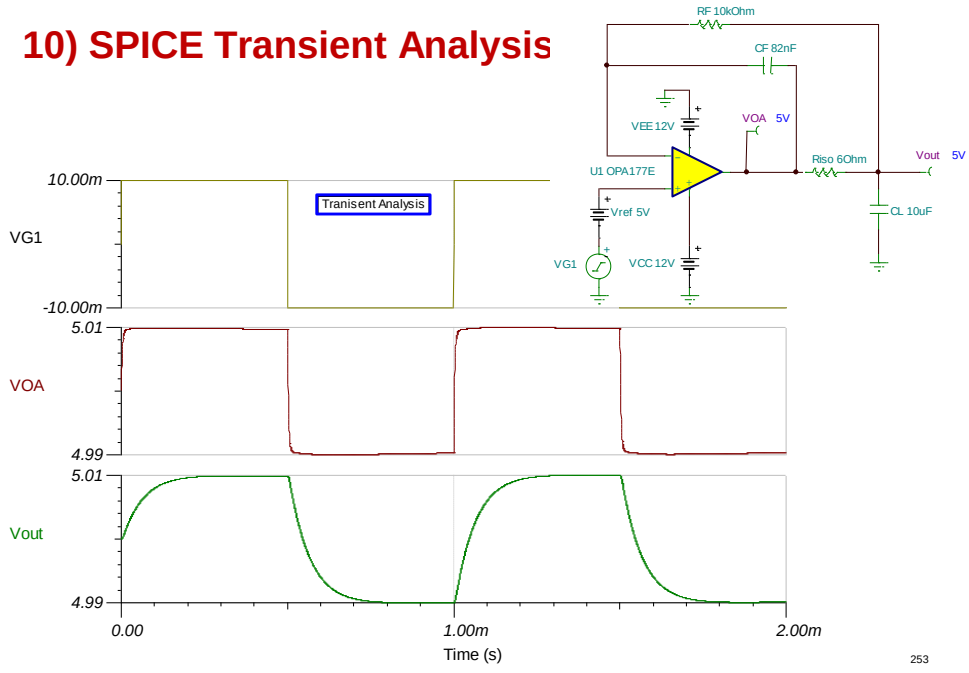


9) SPICE AC Closed Loop



TEXAS INSTRUMENTS

10) SPICE Transient Analysis

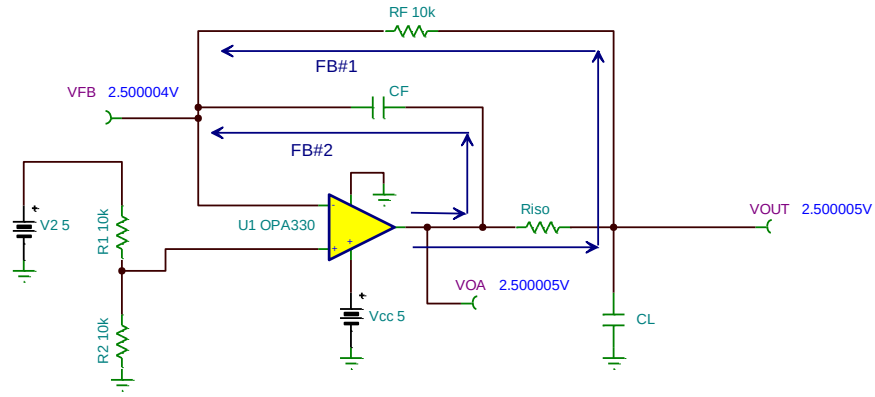


253

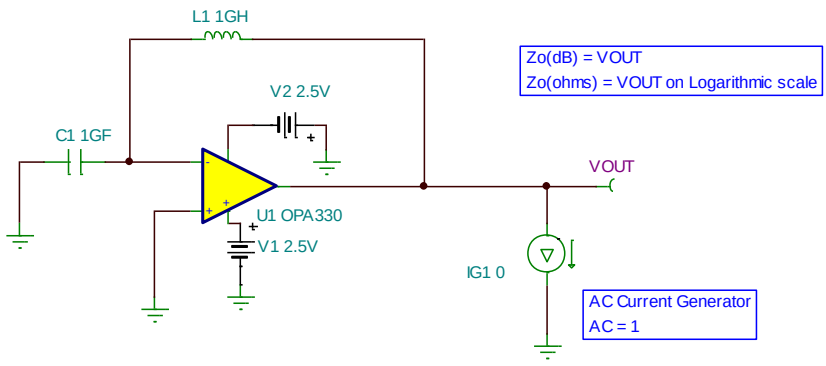
TEXAS INSTRUMENTS

13) Riso with Dual Feedback (Output Cload) - 1/β, Loaded Aol Technique

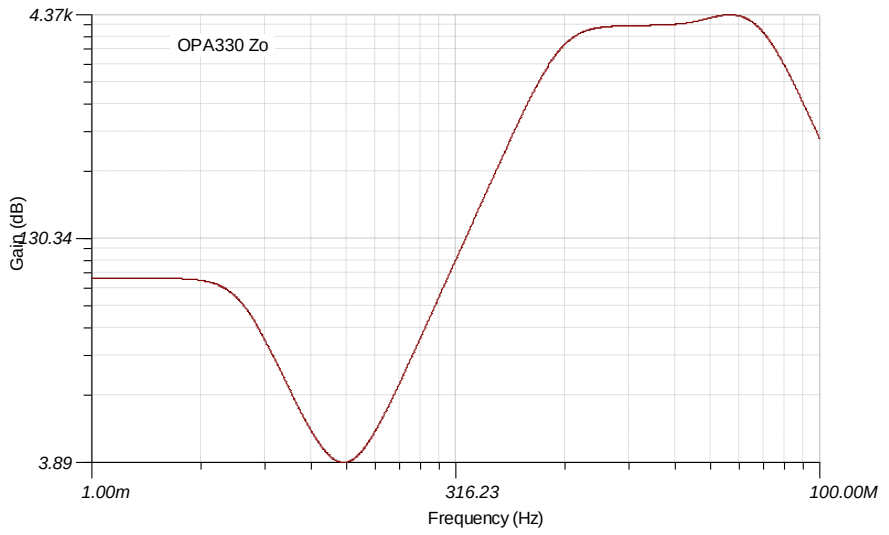
Riso with Dual FB Topology (OPA330 Example)



Zo Test

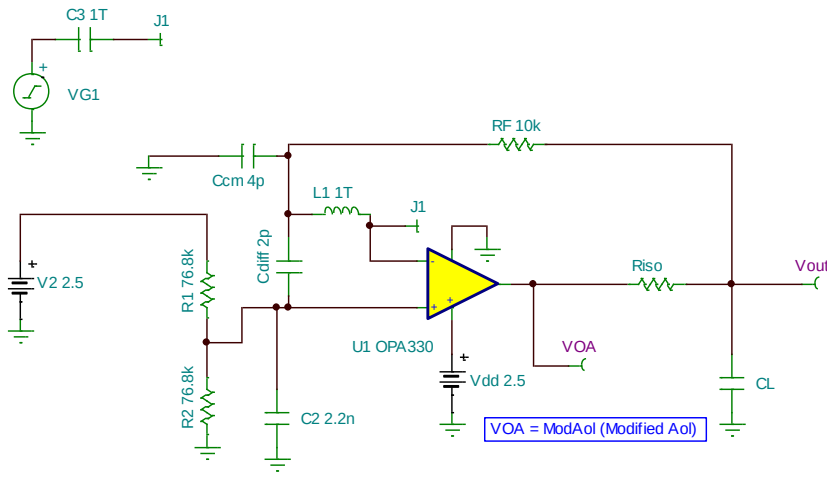

L1 1GH
V2 2.5V
C1 1GF
U1 OPA330
V1 2.5V
VOUT
IG1 0
Zo(dB) = VOUT
Zo(ohms) = VOUT on Logarithmic scale
AC Current Generator
AC = 1

Zo Test

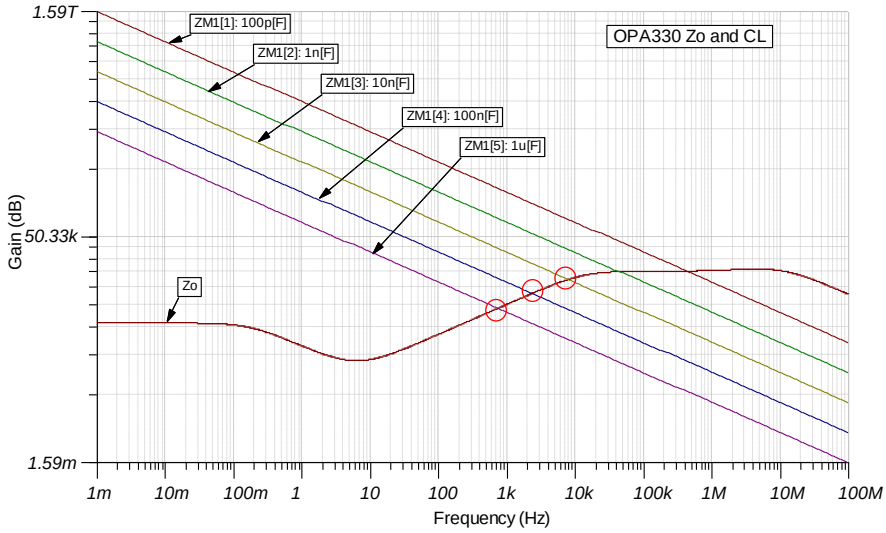

4.37k
OPA330 Zo
Gain (dB)
30.34
3.89
1.00m
316.23
100.00M
Frequency (Hz)

257

Modified Aol



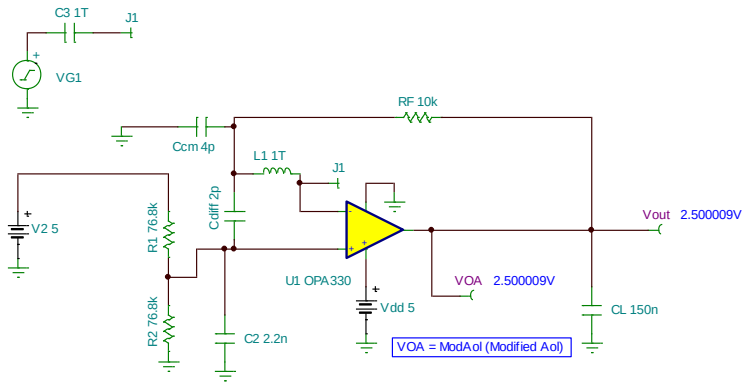
Zo and CL



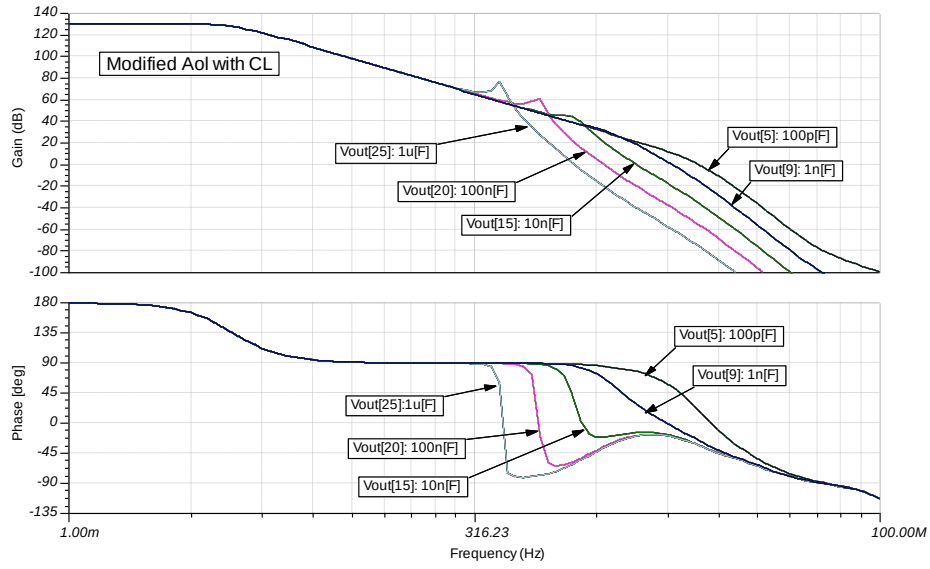
Modified AoI will have Complex Poles with sharp phase shifts anywhere CL Crosses Zo in Zo “Inductive” region.

259

Modified Aol with CL

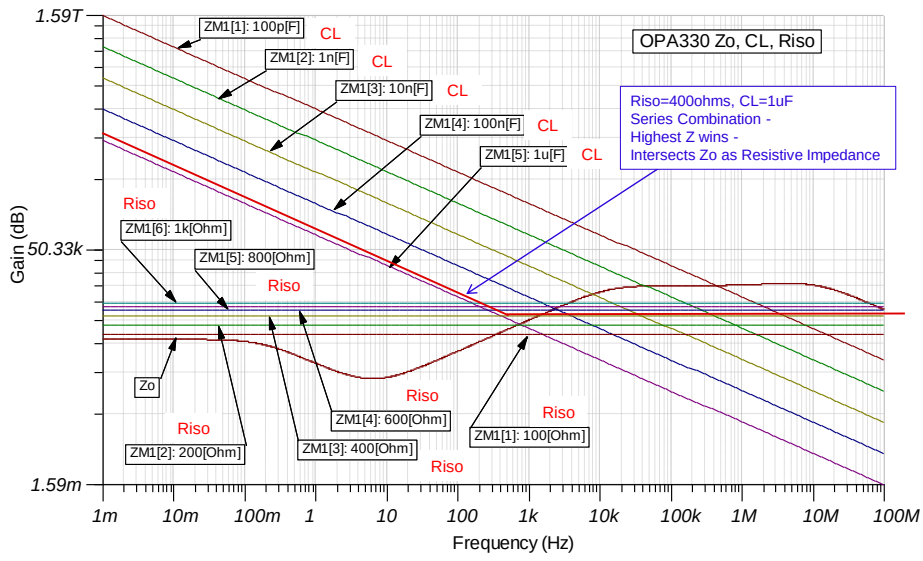


Modified Aol with CL



261

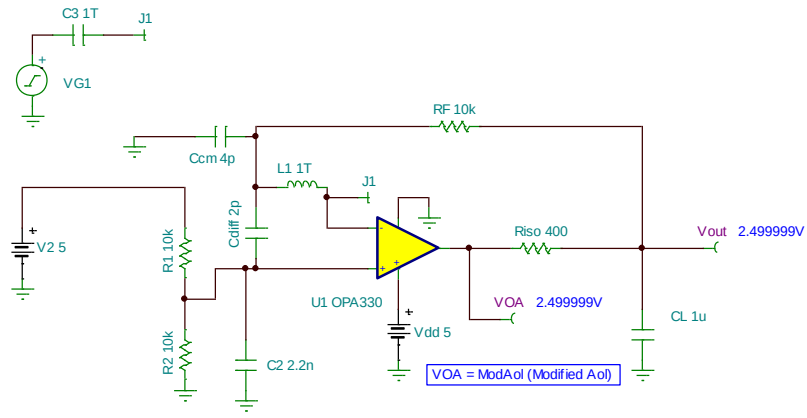
Zo, CL, Riso



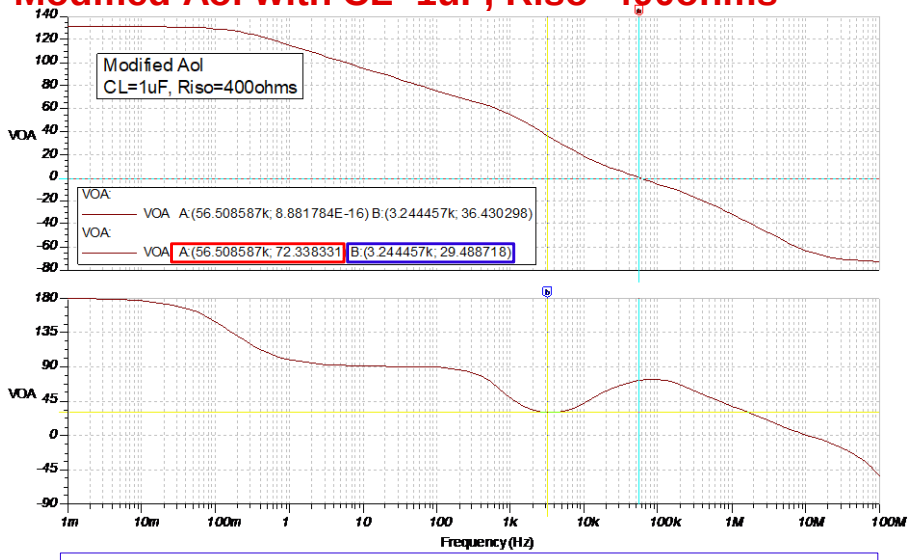
262

TEXAS INSTRUMENTS

Modified Aol with CL=1uF, Riso=400ohms

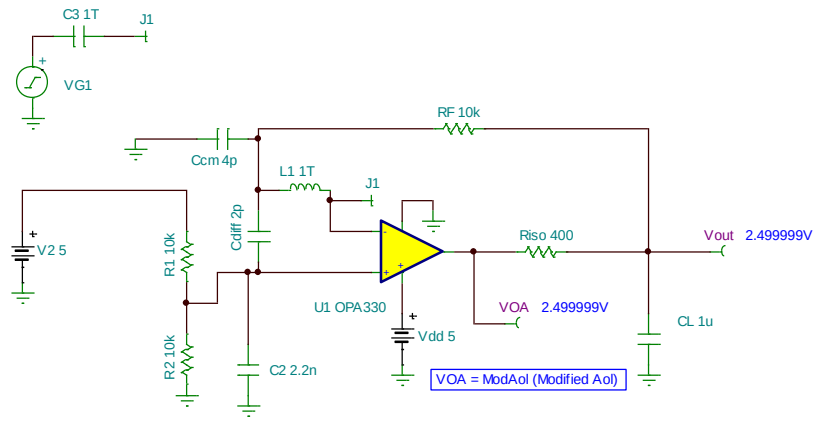


Modified Aol with CL=1uF, Riso=400ohms

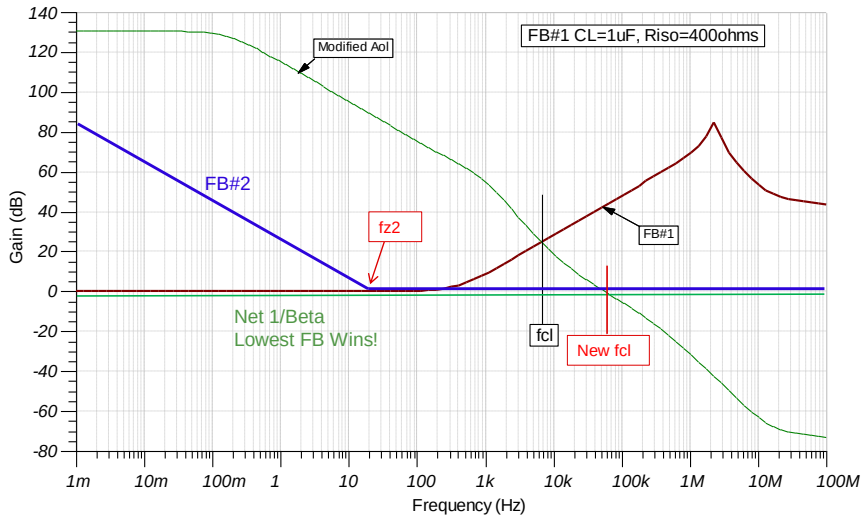


Note:
1) Modified Aol looks like an Aol with a second pole around 1kHz and a zero at about 20kHz
2) No abrupt phase shifts and minimum phase is 29.488 degrees away from 180 degree total phase shift
3) Modified Aol UGBW=56.5kHz with phase margin at 72.33 degrees

FB#1 with CL=1uF, Riso=400ohms



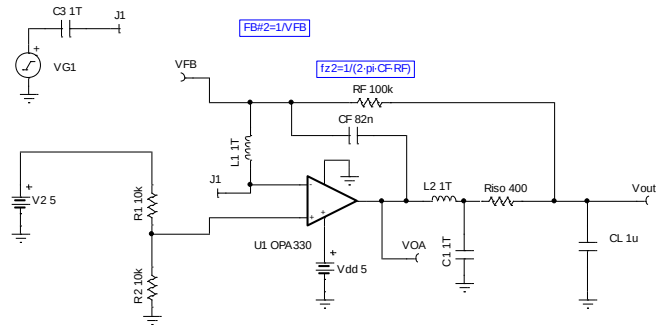
FB#1 with CL=1uF, Riso=400ohms



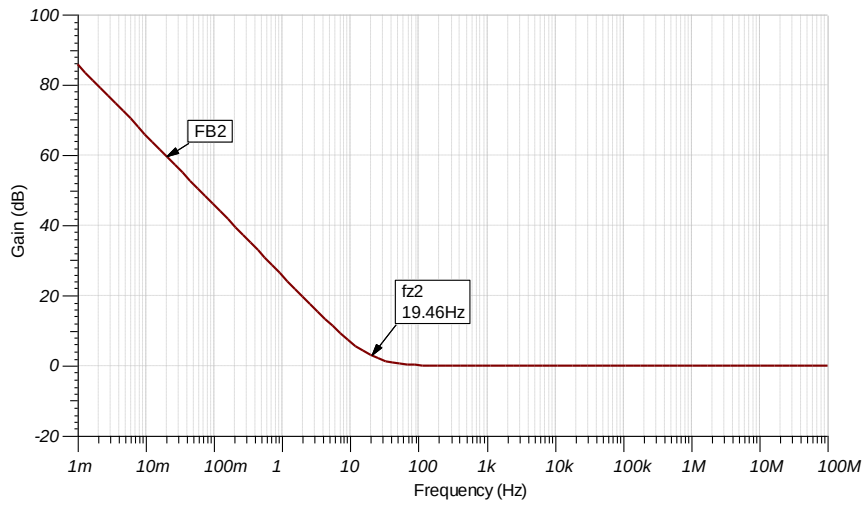
Note:
1) At fcl, where loop gain goes to zero, there is a 40dB/decade rate-of-closure indicating INSTABILITY for FB#1 alone
2) We will add FB#2 s shown for a Net 1/Beta which will be stable at new fcl

266

FB#2 with CL=1uF, Riso=400ohms, RF=100k, CF=82nF



FB#2 with CL=1uF, Riso=400ohms, RF=100k, CF=82nF



268

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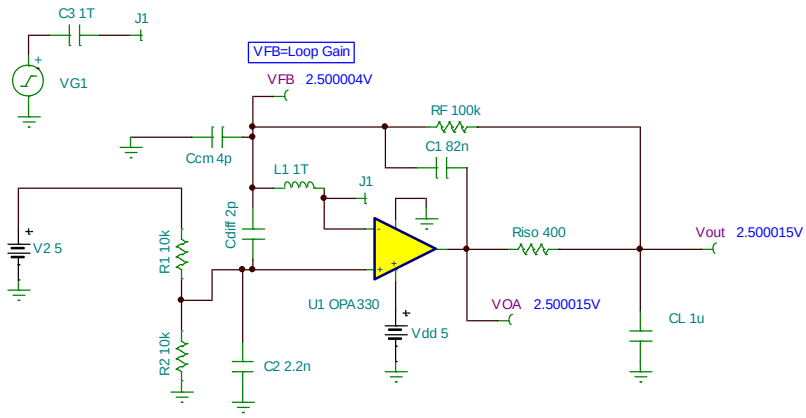
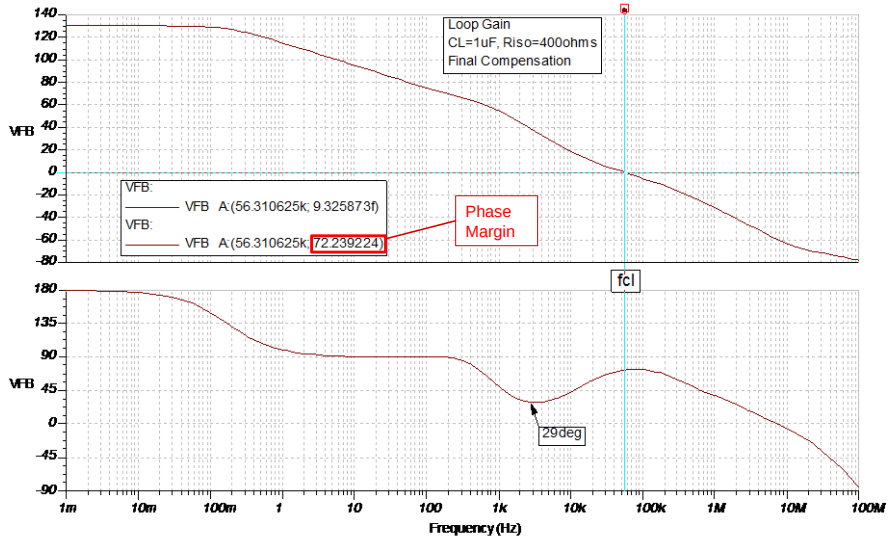
Loop Gain for CL=1uF, Riso=400ohms Final Compensation

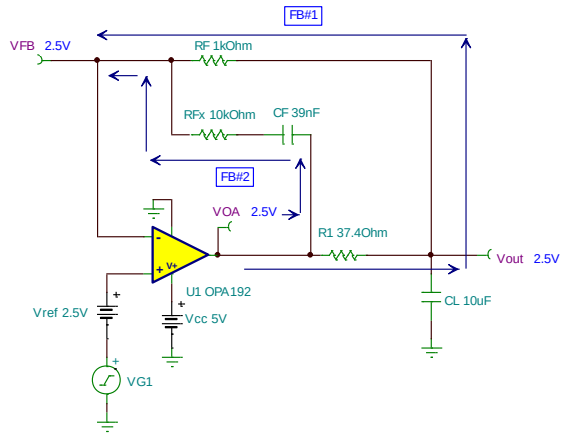


Loop Gain for CL=1uF, Riso=400ohms Final Compensation

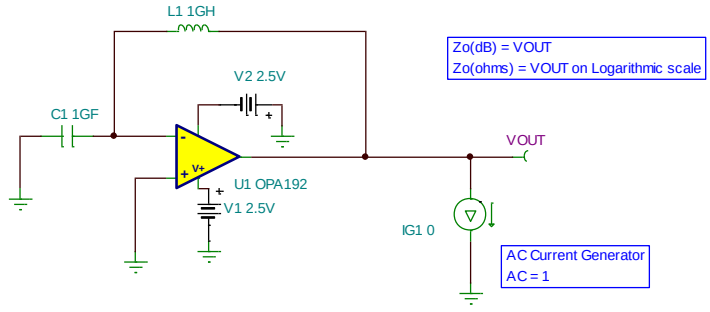


14) Riso with Dual Feedback plus RFx (Output Cload) - 1/β, Loaded Aol Technique

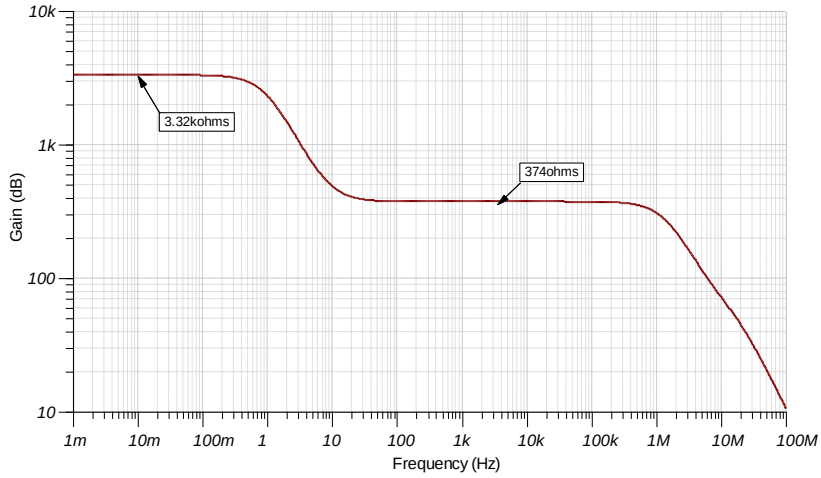
Riso with Dual FB plus RFx Topology



Zo Test

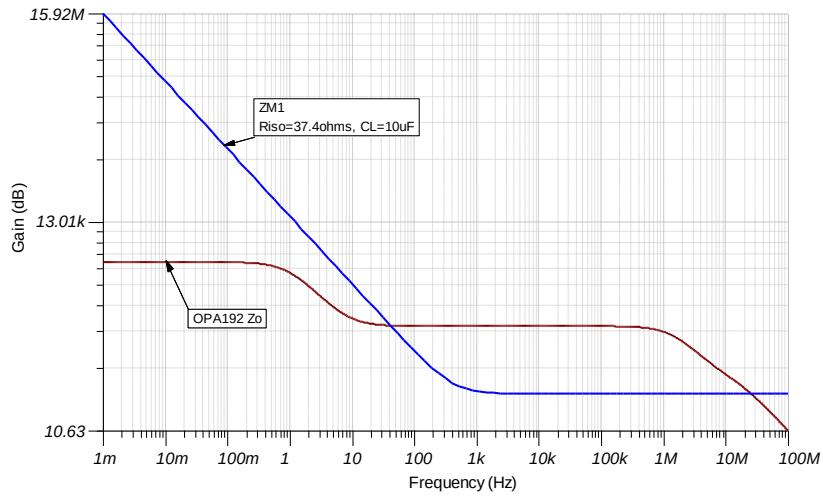

L1 1GH
Zo(dB) = VOUT
Zo(ohms) = VOUT on Logarithmic scale
V2 2.5V
C1 1GF
VOUT
U1 OPA192
V1 2.5V
IG1 0
AC Current Generator
AC = 1

Zo Test

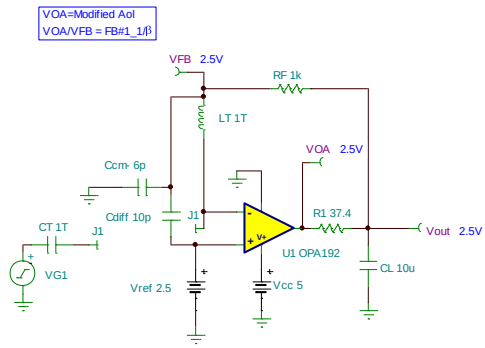

10k
1k
100
10
Gain (dB)
3.32kohms
374ohms
1m
10m
100m
1
10
100
1k
10k
100k
1M
10M
100M
Frequency (Hz)

274

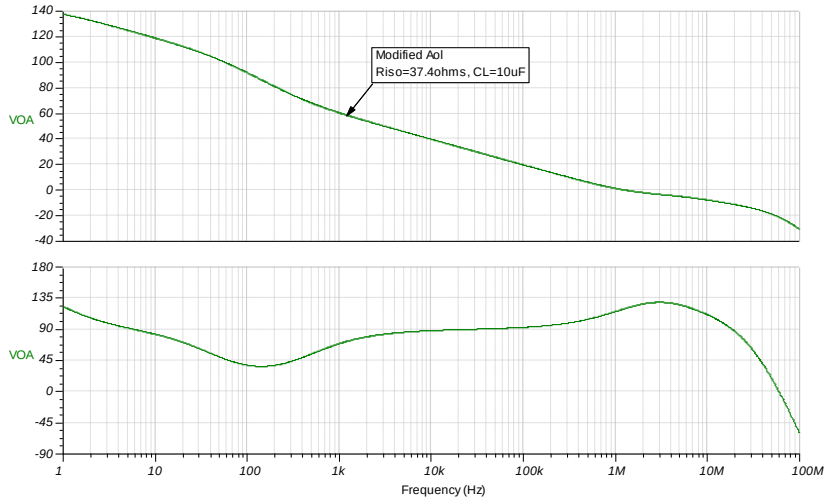
Zload on Aol


15.92M
13.01k
10.63
Gain (dB)
ZM1
Riso=37.4ohms, CL=10uF
OPA192 Zo
1m
10m
100m
1
10
100
1k
10k
100k
1M
10M
100M
Frequency (Hz)

Modified Aol

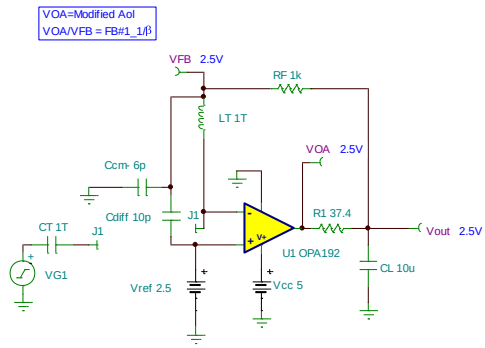


Modified Aol

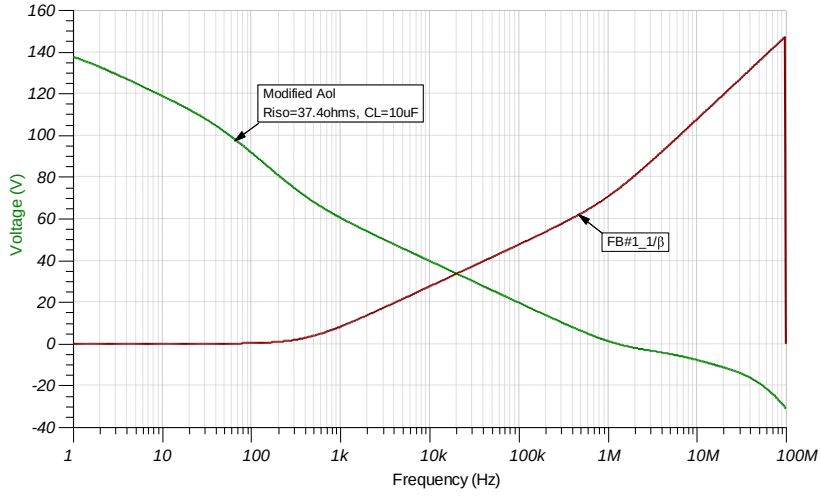


277

FB#1 with CL=10uF, Riso=37.4ohms



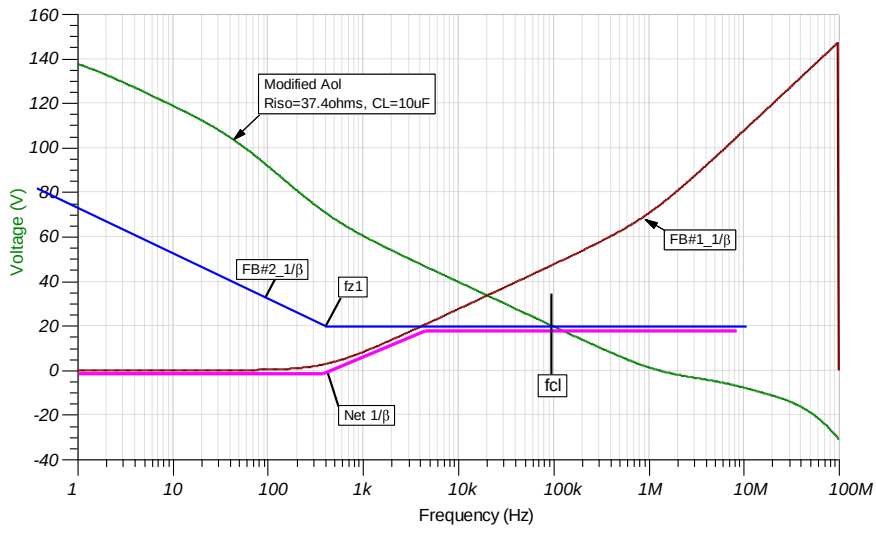
FB#1 with CL=10uF, Riso=37.4ohms



279

TEXAS INSTRUMENTS

FB#1 with CL=10uF, Riso=37.4ohms
Add FB#2 for Stability



280

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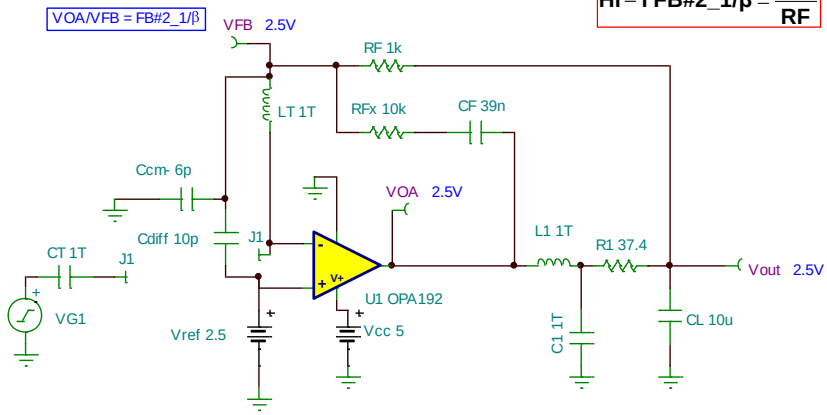
FB#2 with CL=10uF, Riso=37.4ohms, RF=1k, RFx=10k

$$fz1 = \frac{1}{2\pi(RFx + RF)CF}$$

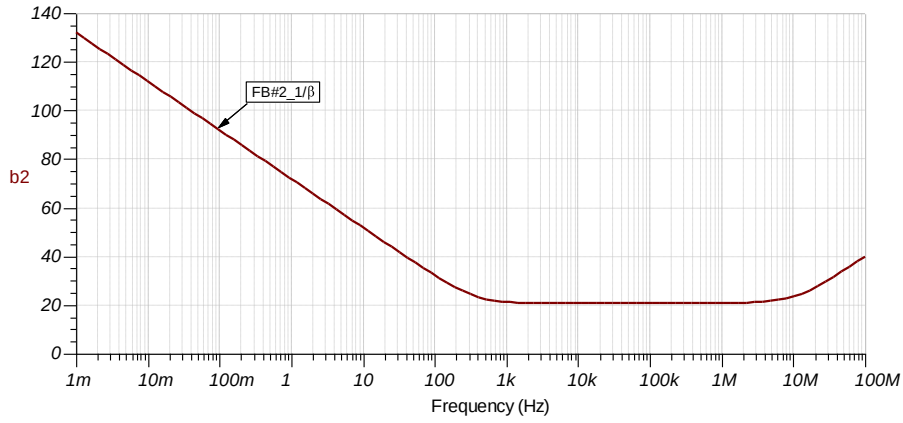
$$\mathbf{Hi - f\ FB\#2\_1/\beta} = \frac{\mathbf{RFx}}{\mathbf{RF}}$$



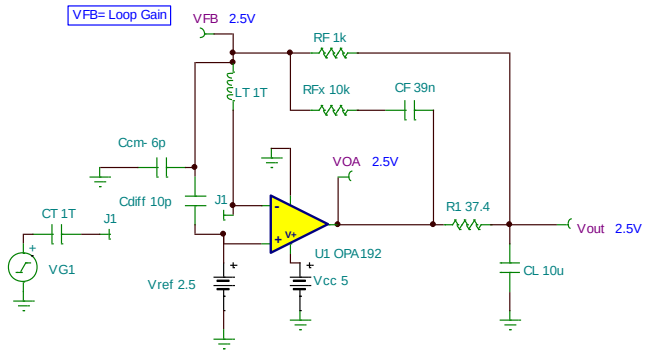
281

TEXAS INSTRUMENTS

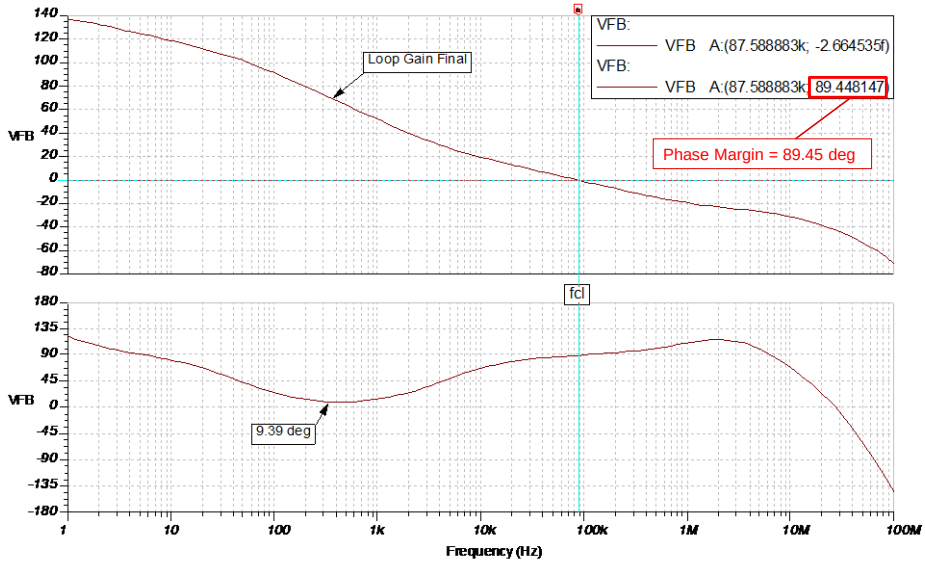
FB#2 with CL=10uF, Riso=37.4ohms, RF=1k, RFx=10k



Loop Gain for CL=10uF, Riso=37.4ohms, RF=1k, RFx=10k



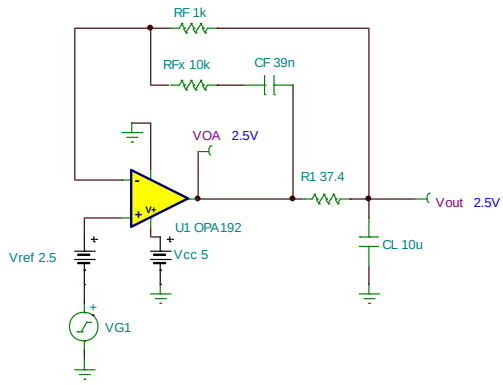
Loop Gain for CL=10uF, Riso=37.4ohms, RF=1k, RFx=10k



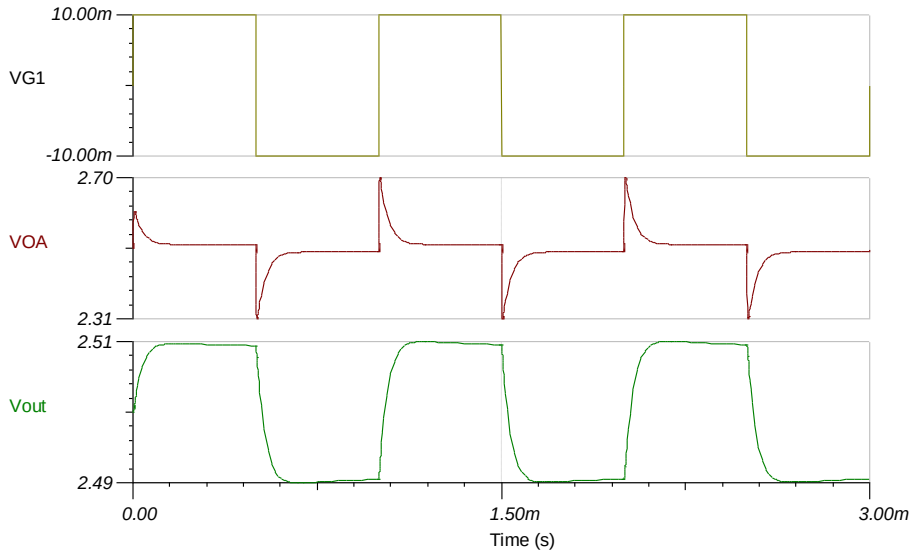
284

TEXAS INSTRUMENTS

Transient for CL=10uF, Riso=37.4ohms, RF=1k, RFx=10k



Transient for CL=10uF, Riso=37.4ohms, RF=1k, RFx=10k



286

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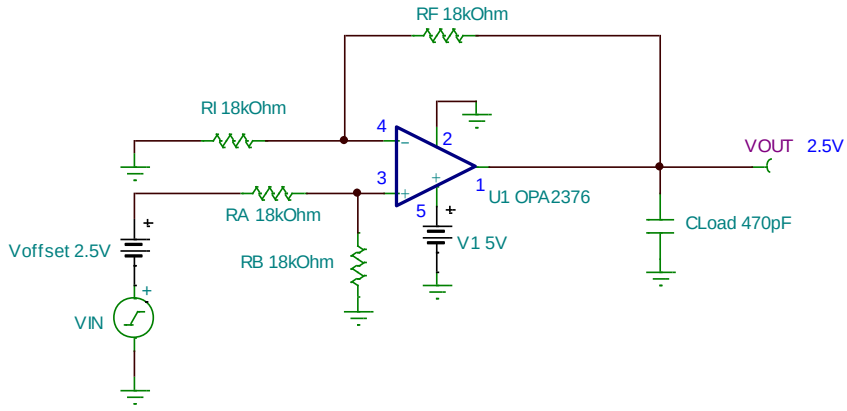
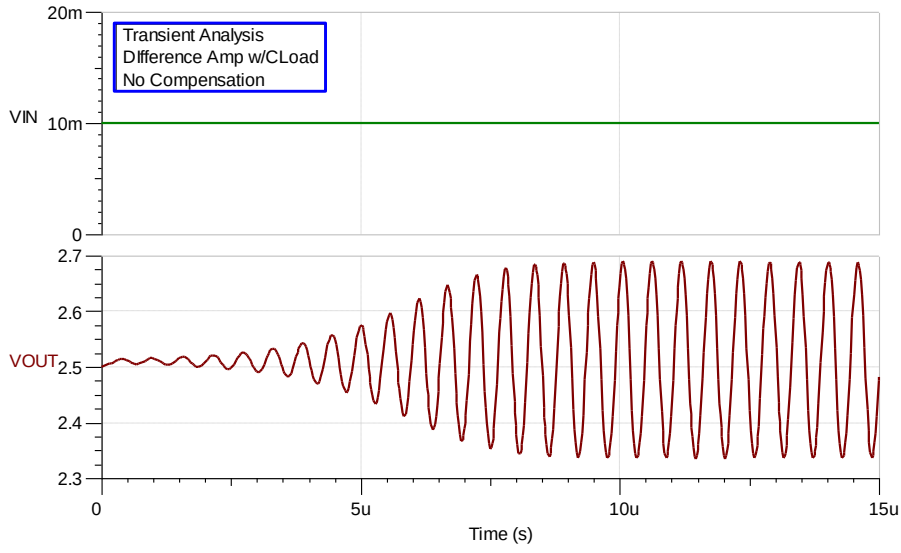
15) Discrete Difference Amplifier (Output Cload)

Difference Amp w/CLoad: No Compensation



Difference Amp w/CLoad: No Compensation



289

Discrete Difference Amplifier Compensation Design Steps

1) SPICE simulation for Loaded Aol curves
2) Plot Desired 1/β on Loaded Aol curves
   A) Use Noise Gain Compensation
3) From Desired 1/β determine fp and 1/β_Hif
4) Compute values for Rn, Cn based on fp and 1/β_Hif
5) SPICE simulation w/final compensation for Loop Gain (Aolβ) Magnitude and Phase
6) Adjust Compensation if greater Loop Gain (Aolβ) phase margin desired
7) Add Rnp-Cnp to +input of Difference Amplifier for flat VOUT/VIN Response
   A) Look for peaking which indicates marginal stability
   B) Check if closed AC response is acceptable for end application
8) Check Transient response for VOUT/VIN
   A) Overshoot and ringing in the time domain indicates marginal stability

290

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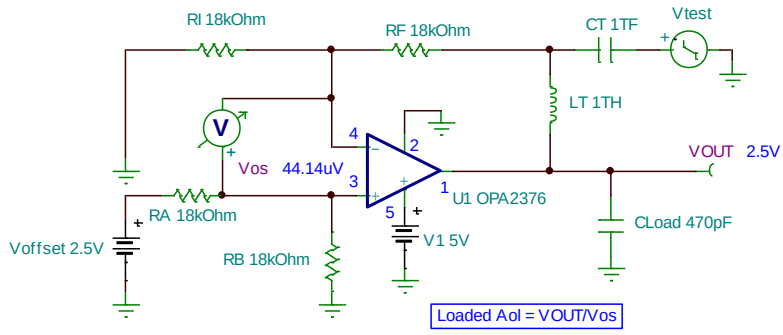
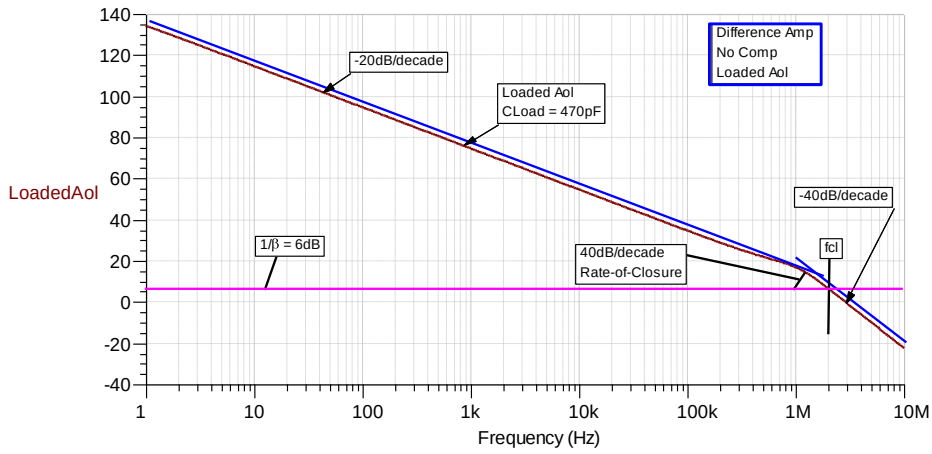
The CF Compensation design steps are outlined here. Rules-of-thumb will be present to yield best stability on first pass analysis.

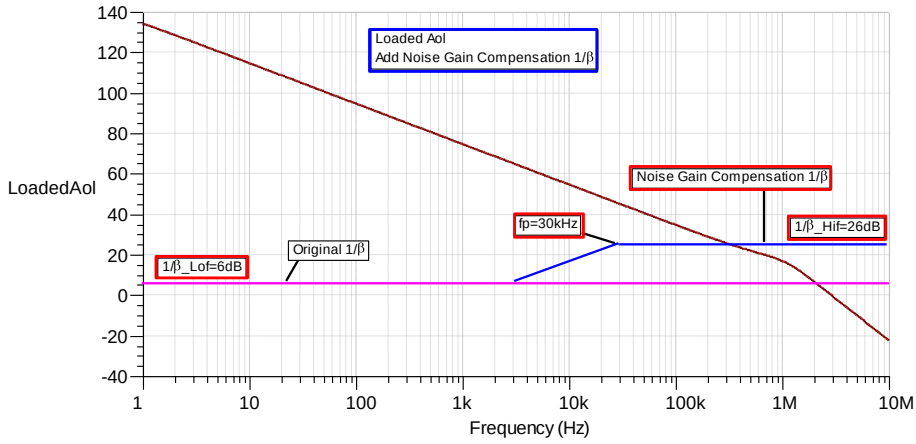
1) Loaded Aol: No Compensation



1) Loaded Aol: No Compensation



2), 3) Plot 1/β on Loaded Aol



293

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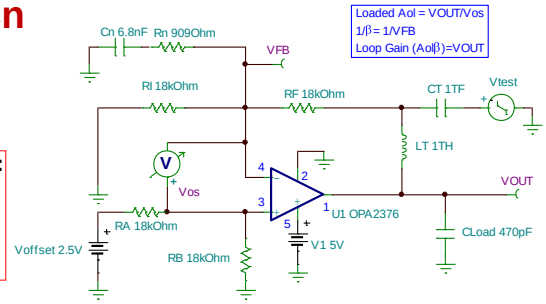
4) Compute Rn and Cn



From Noise Gain Compensation 1/β :

$1/\beta\_Lof = 6dB = 2$

$1/\beta\_Hif = 26dB = 19.95$

$fp = 30kHz$

From Noise Gain Compensation Analysis :

$$1/\beta\_Lof = \frac{RF+RI}{RI} = 1+\frac{RF}{RI} = 1+\frac{18k\Omega}{18k\Omega} = 2$$

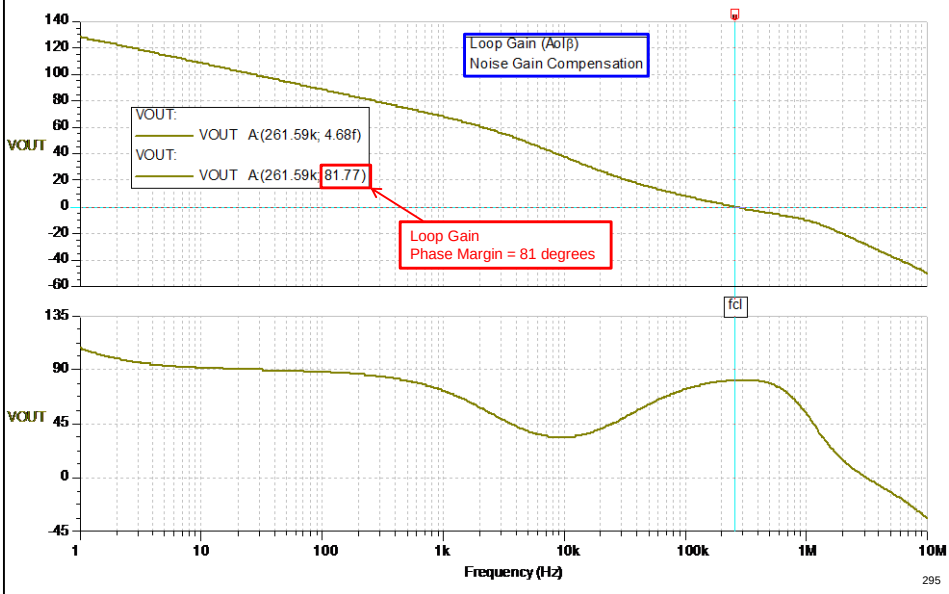
$$1/\beta\_Hif \approx \frac{RF}{Rn} = \frac{18k\Omega}{Rn} = 19.95 \rightarrow Rn = 902.25\Omega$$

Use Rn = 909Ω → standard value resistor

$$fp = \frac{1}{2\pi RnCn} = \frac{1}{2\pi(909\Omega)Cn} = 30kHz \rightarrow Cn = 5.84nF$$

Use Cn = 5.6nF → standard value capacitor

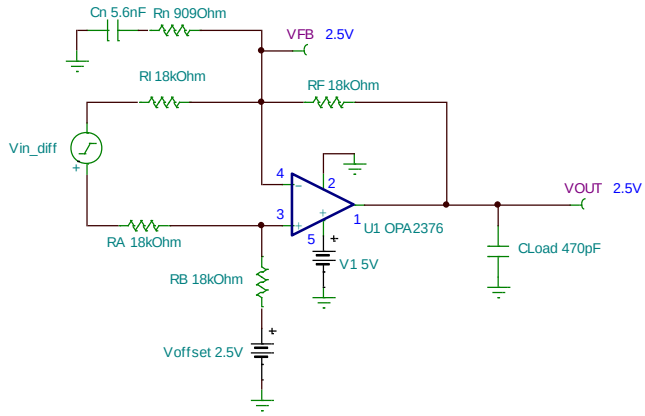
5),6) Loop Gain Check



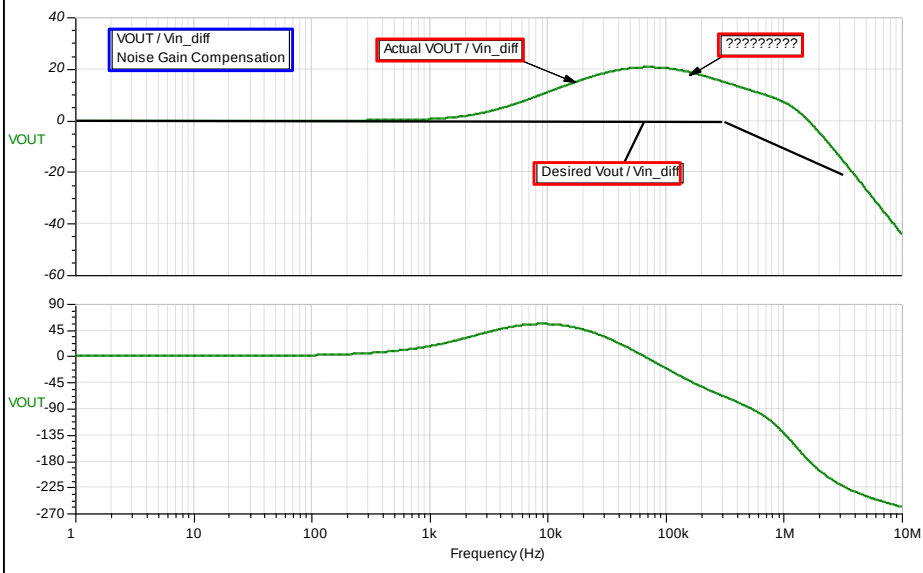
295

TEXAS INSTRUMENTS

7) VOUT/Vin_diff: Noise Gain Compensation



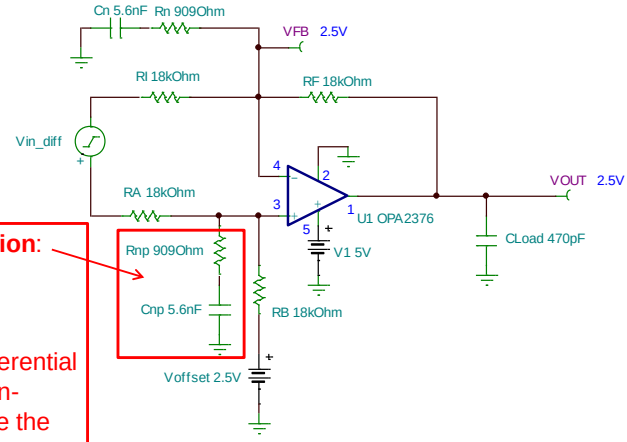
7) VOUT/Vin_diff: Noise Gain Compensation



297

TEXAS INSTRUMENTS

7) Rnp-Cnp Compensation plus Noise Gain Compensation = FLAT VOUT/Vin_diff Response

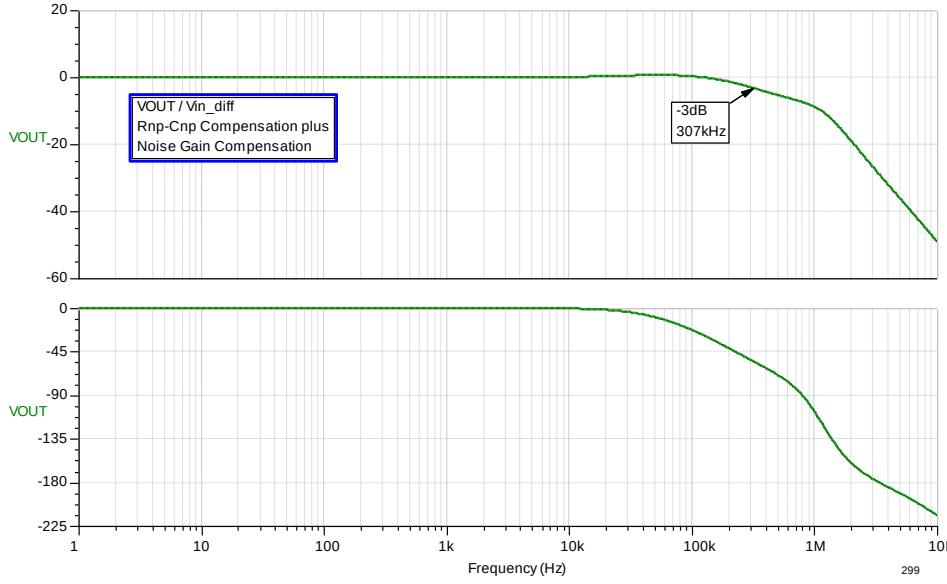


Add Rnp-Cnp Compensation:
Rnp = Rn
Cnp = Cp

1) This will balance the differential gain so inverting and non-inverting gain paths have the same gain over frequency for a flat differential gain of VOUT/Vin_diff.

1) No Effect on Loop Gain (Aolβ)

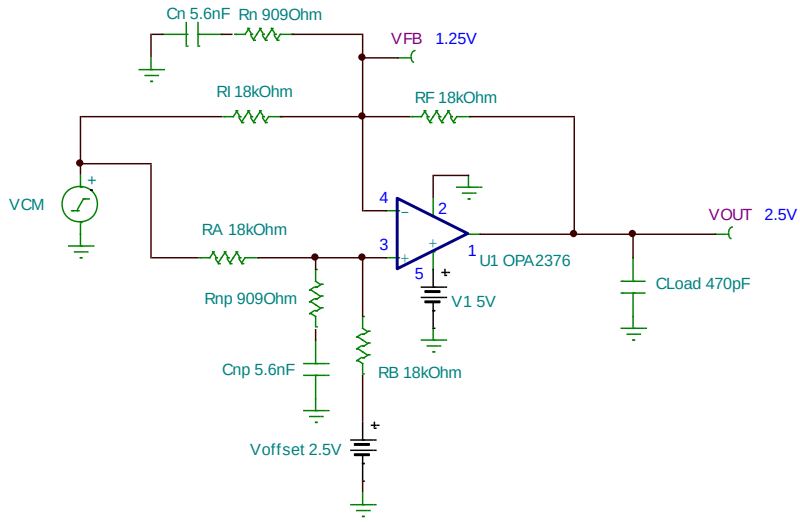
7) Rnp-Cnp Compensation plus Noise Gain Compensation = FLAT VOUT/Vin_diff Response



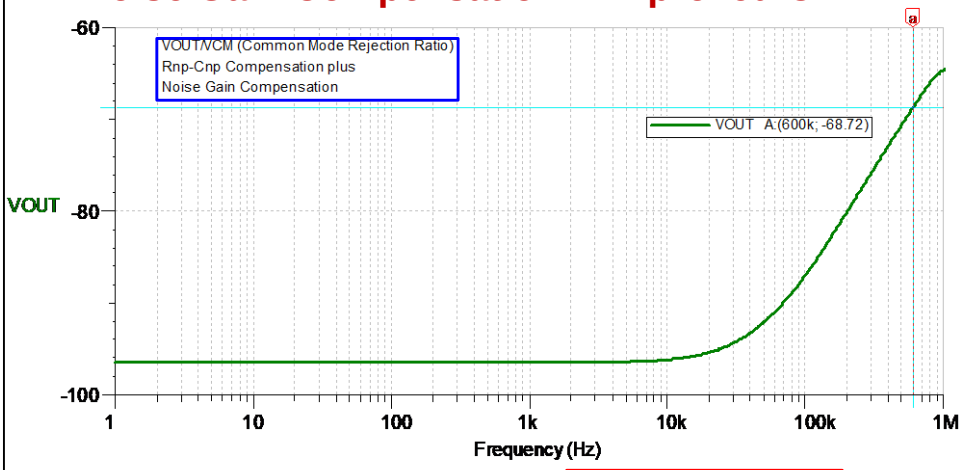
299

TEXAS INSTRUMENTS

7) Rnp-Cnp Compensation plus Noise Gain Compensation = Improved CMRR



7) Rnp-Cnp Compensation plus Noise Gain Compensation = Improved CMRR



OPA2367
CMRR = 40dB @ 600kHz

Difference Amp
Noise Gain Compensation
Rnp-Cnp Compensation
CMRR = 69dB @ 600kHz

301

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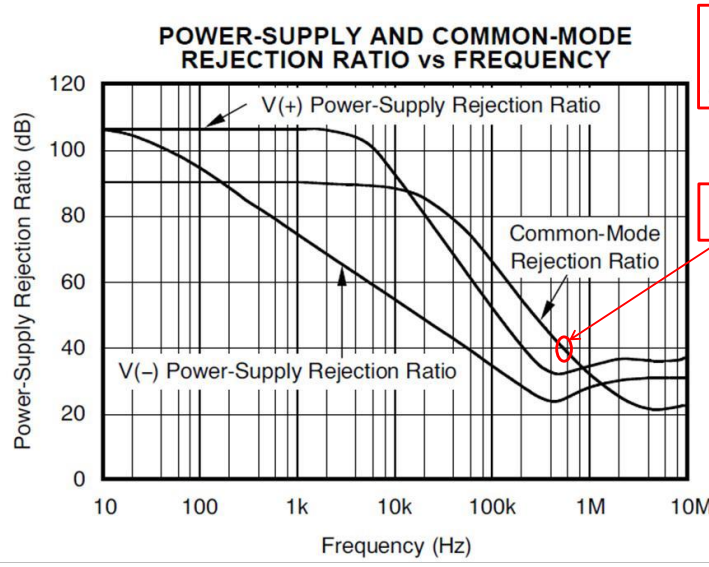
7) Rnp-Cnp Compensation plus Noise Gain Compensation = Improved CMRR



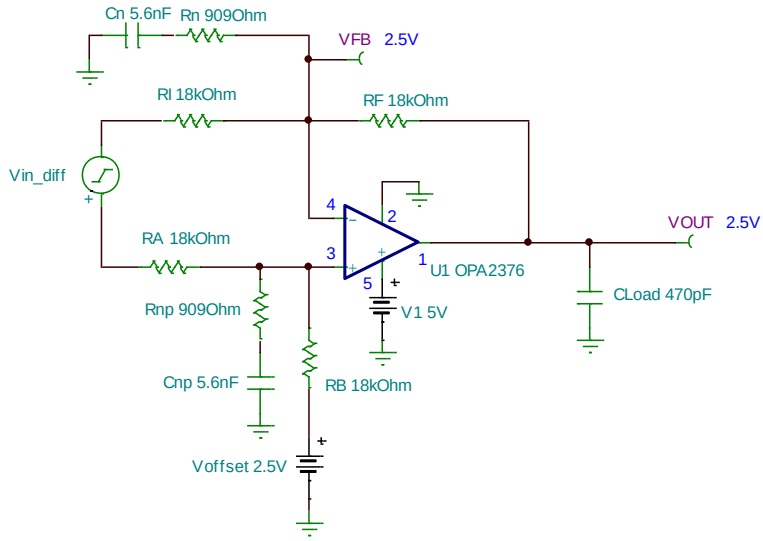
Difference Amp
Noise Gain Compensation
Rnp-Cnp Compensation
CMRR = 69dB @ 600kHz

OPA2367
CMRR = 40dB @ 600kHz

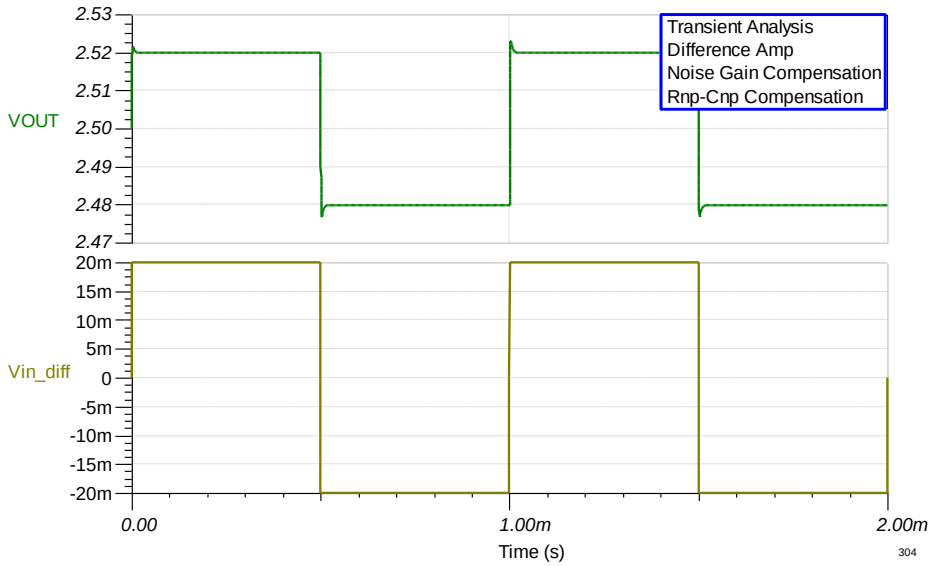
302

TEXAS INSTRUMENTS

8) Transient Analysis:
Rnp-Cnp Compensation plus Noise Gain Compensation



8) Transient Analysis:
Rnp-Cnp Compensation plus Noise Gain Compensation



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