Operational Amplifier Stability

Collin Wells

Texas Instruments

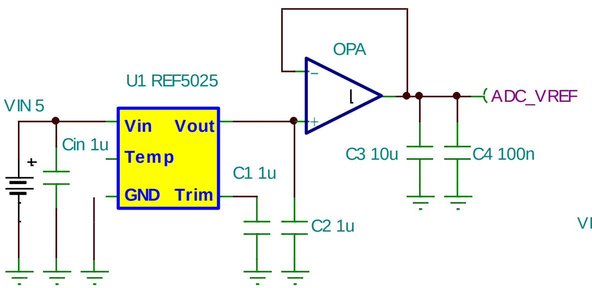
HPA Linear Applications

2/22/2012

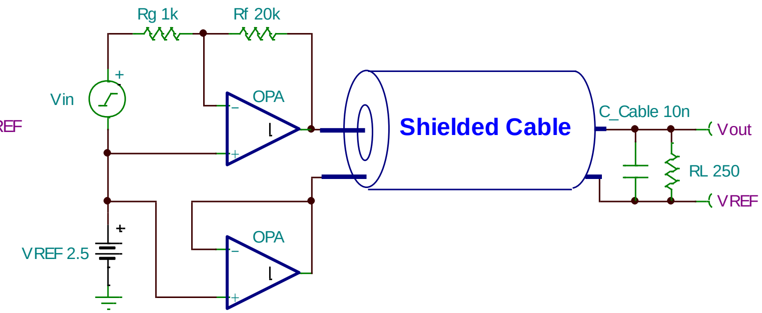
The Culprits

Capacitive Loads!

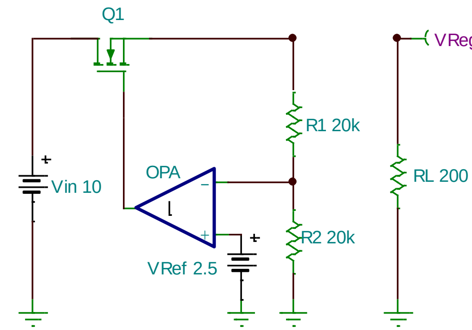
Reference Buffers!



Cable/Shield Drive!

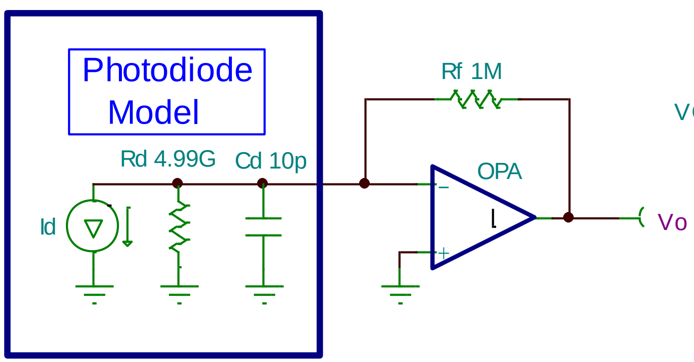


MOSFET Gate Drive!

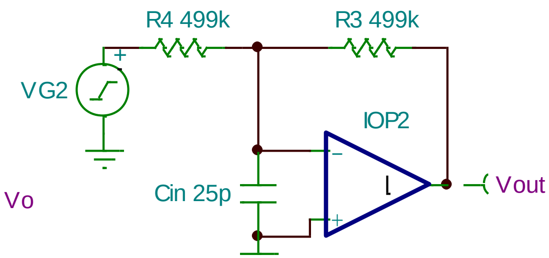


High Feedback Network Impedance!

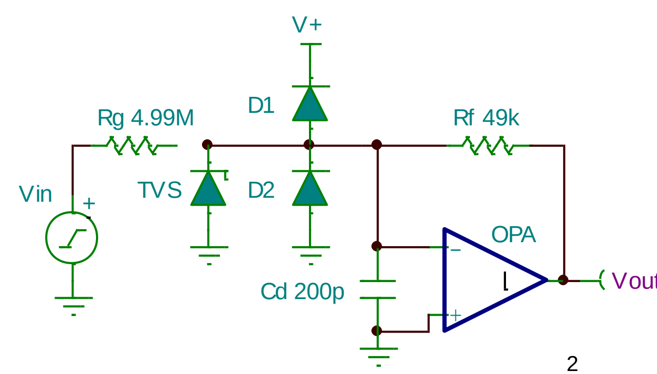
Transimpedance Amplifiers!



High-Source Impedance or Low-Power Circuits!

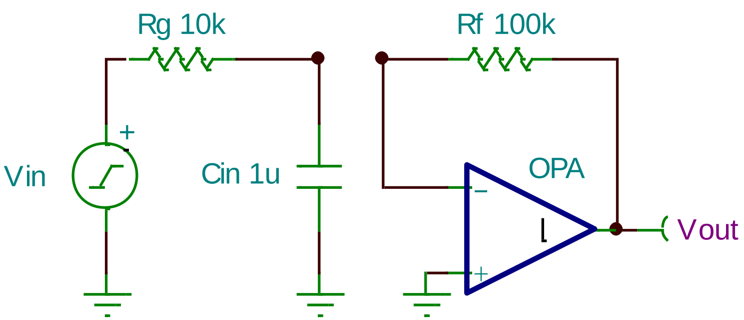


Attenuators!

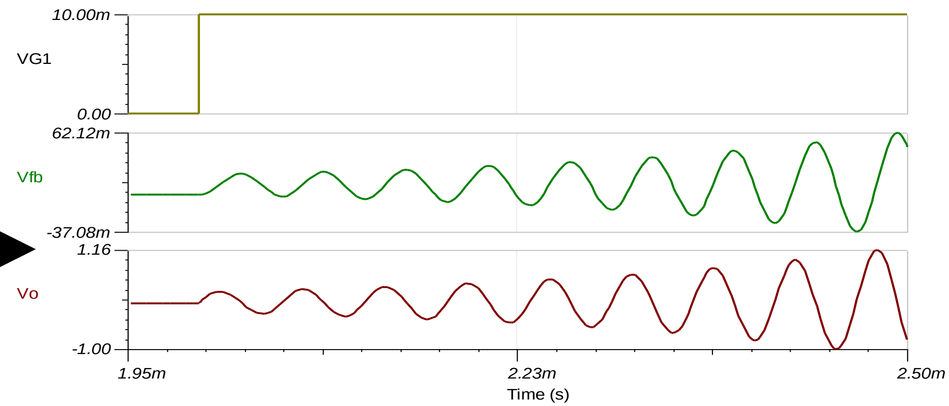


Just Plain Trouble!

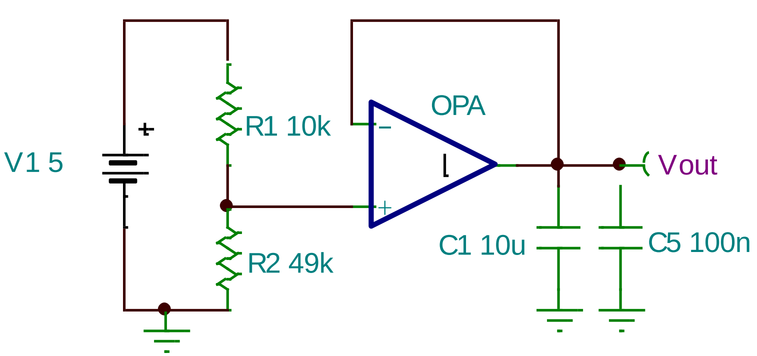
Inverting Input Filter??



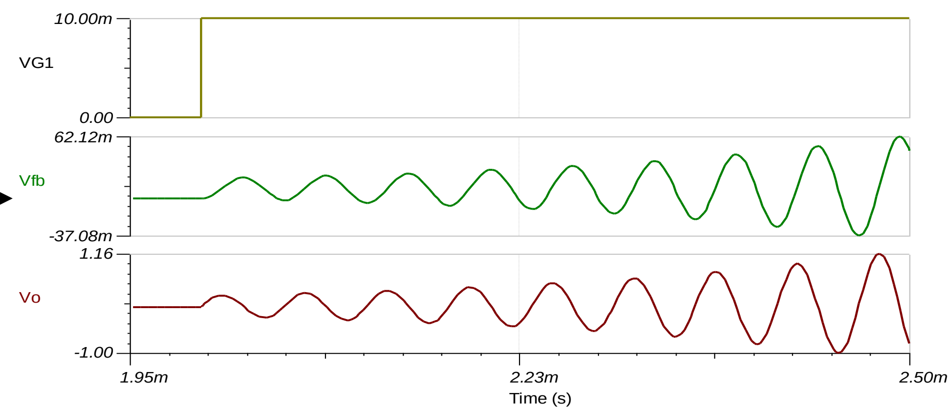
Oscillator



Output Filter??



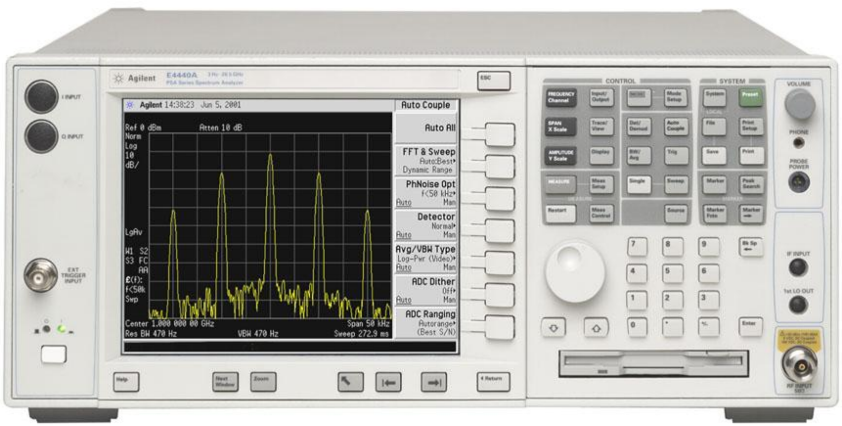
Oscillator



Recognize Amplifier Stability Issues on the Bench

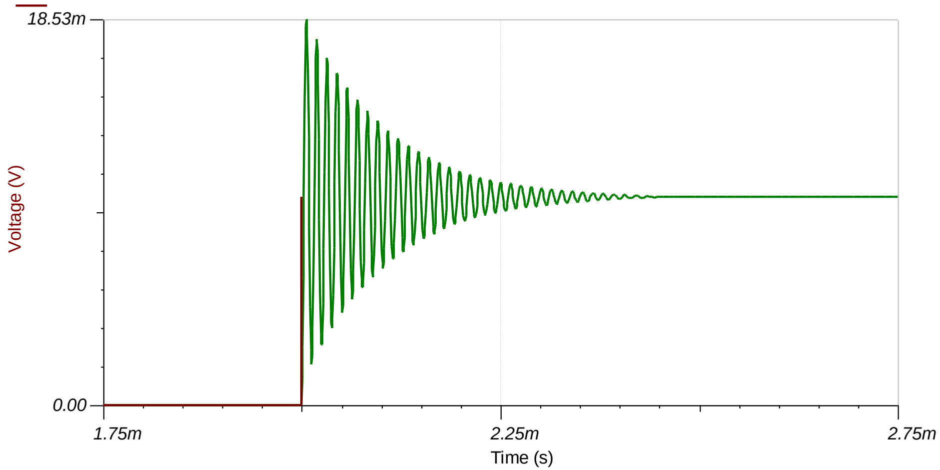
- <u>Required Tools:</u>
  - Oscilloscope
  - Step Generator

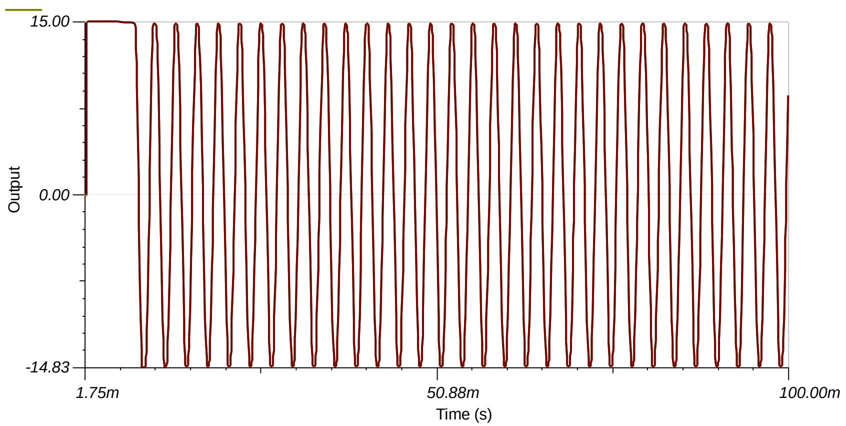
- <u>Other Useful Tools:</u>
  - Gain / Phase Analyzer
  - Network / Spectrum Analyzer

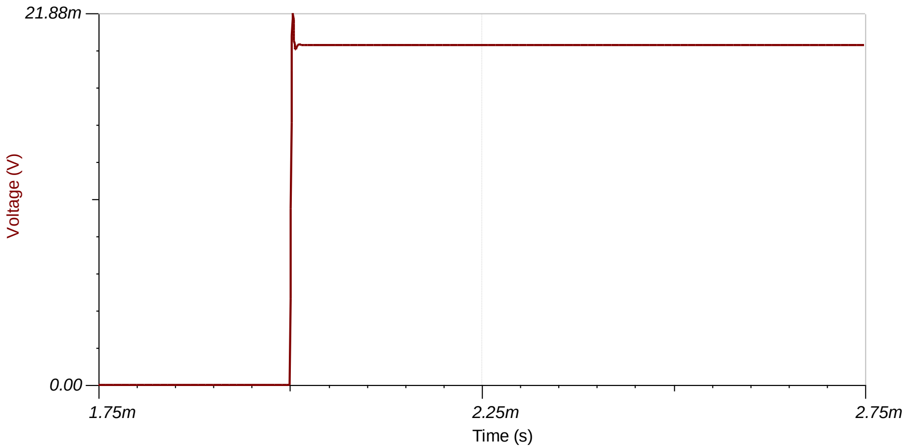


Recognize Amplifier Stability Issues

- <u>Oscilloscope - Transient Domain Analysis:</u>
  - Oscillations or Ringing
  - Overshoots
  - Unstable DC Voltages
  - High Distortion

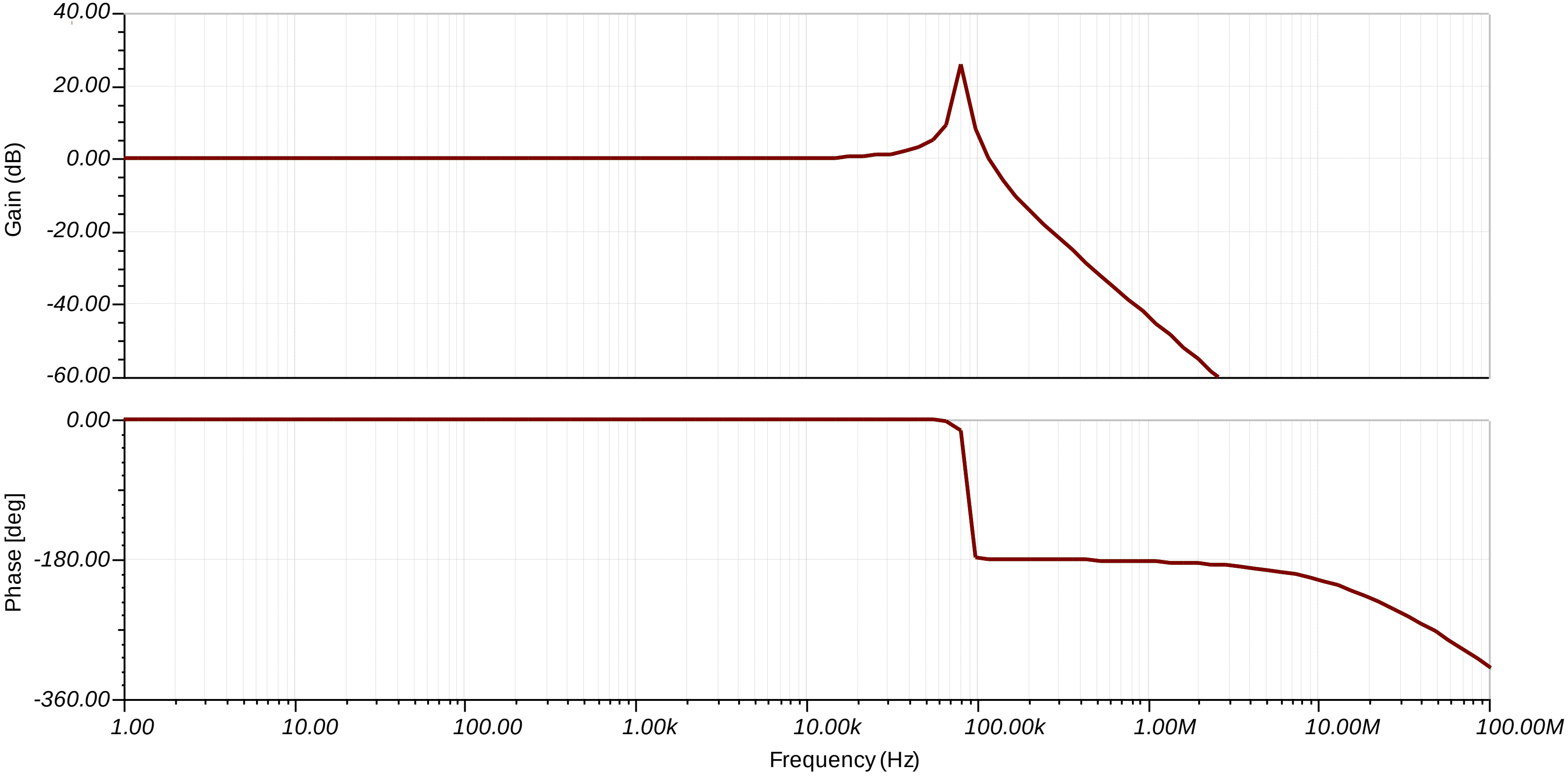






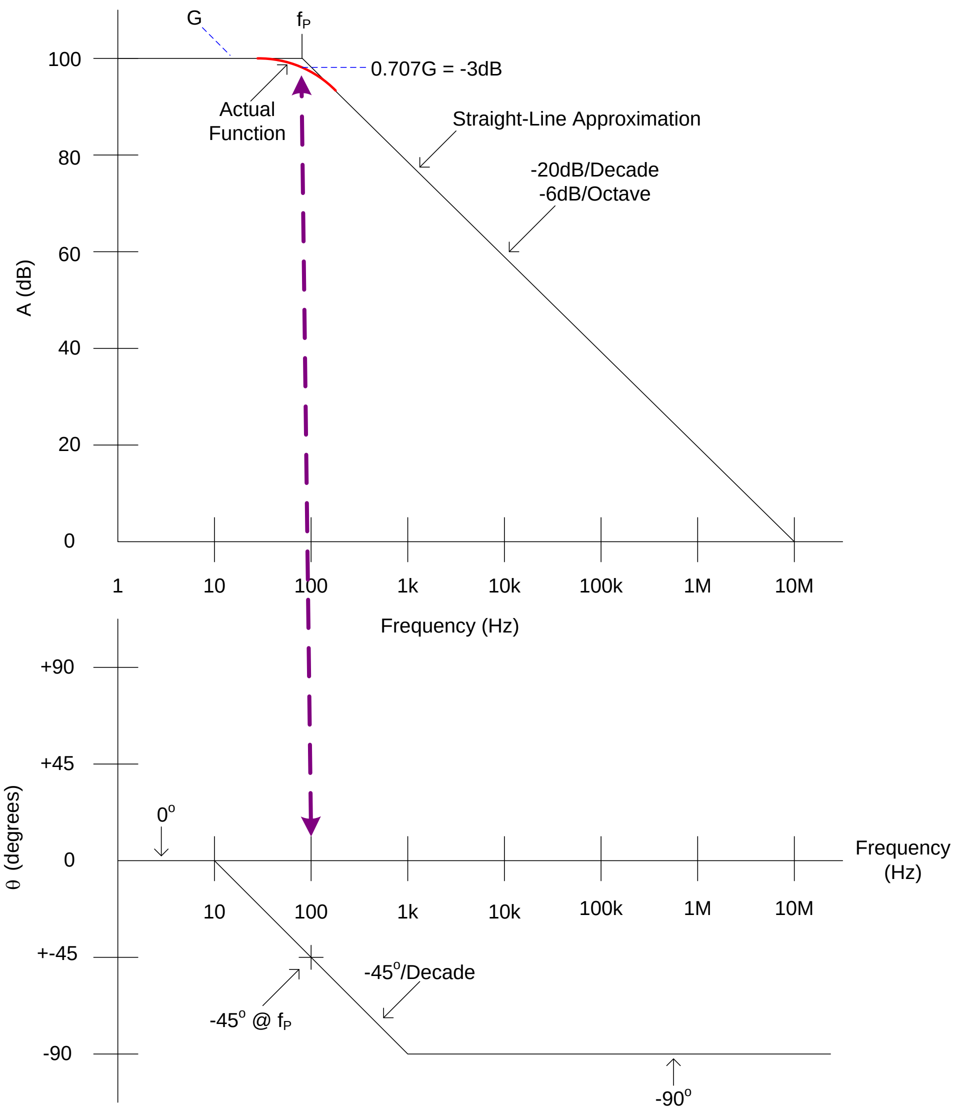
Recognize Amplifier Stability Issues

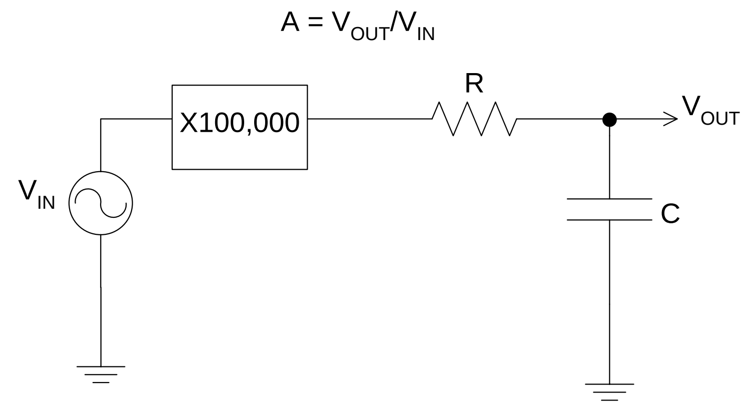
- <u>Gain / Phase Analyzer - Frequency Domain:</u> Peaking, Unexpected Gains, Rapid Phase Shifts



Quick Op-Amp Theory and Bode Plot Review

Poles and Bode Plots

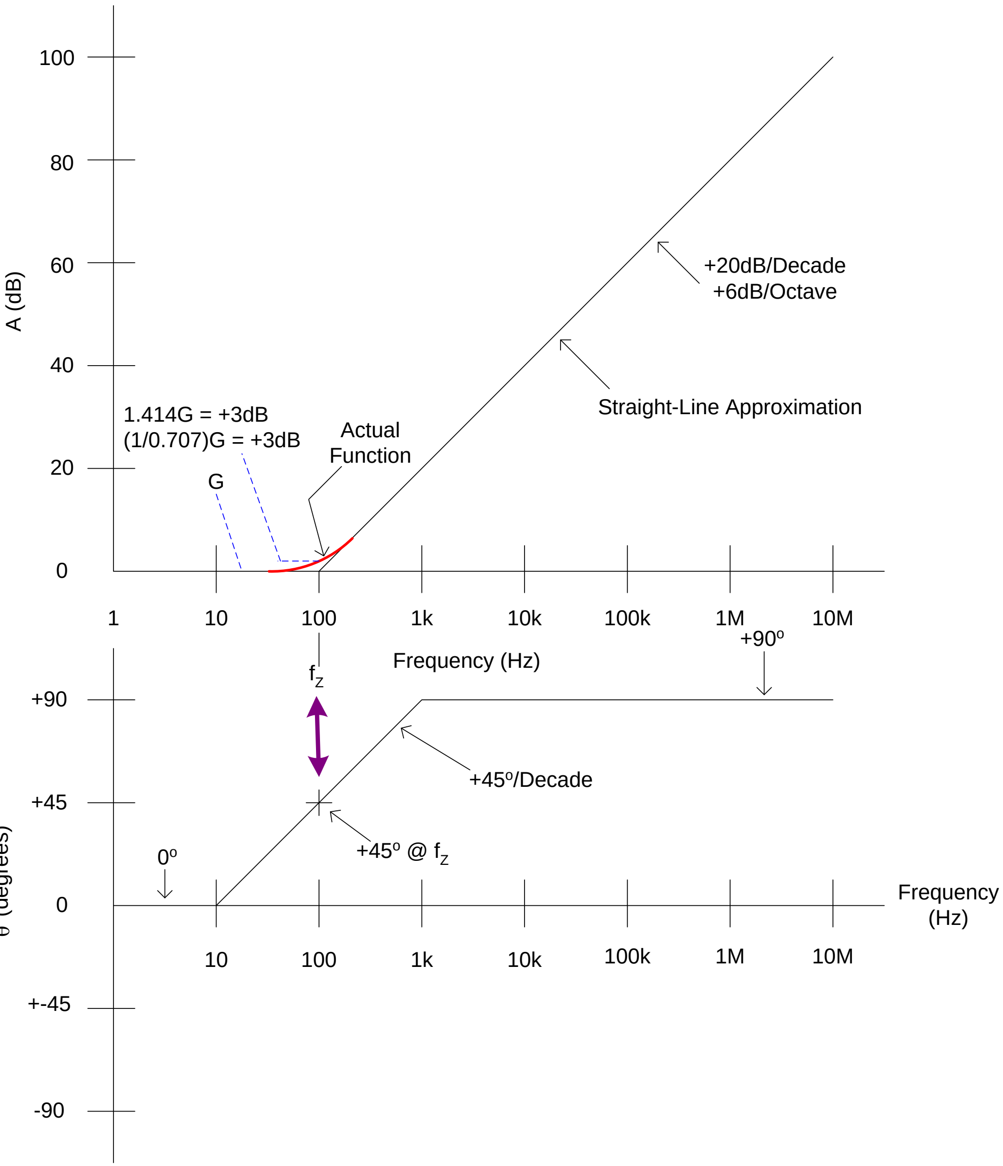


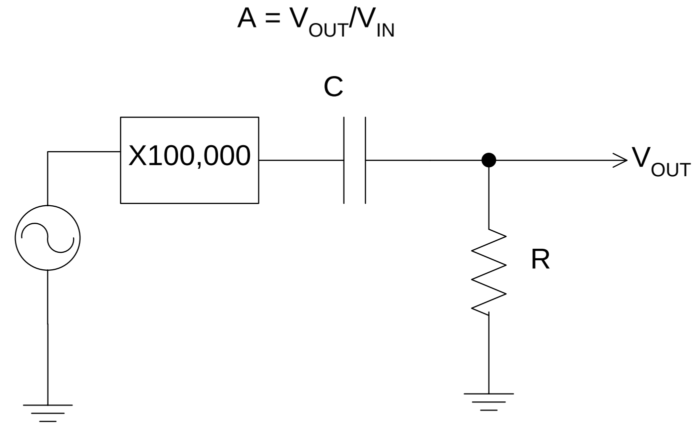


Single Pole Circuit Equivalent

- **Pole Location** = f_P
- **Magnitude** = -20dB/Decade Slope
- Slope begins at f_P and continues down as frequency increases
- Actual Function = -3dB down @ f_P
- **Phase** = -45°/Decade Slope through f_P
- Decade Above f_P Phase = -84.3°
- Decade Below f_P Phase = -5.7°

Zeros and Bode Plots

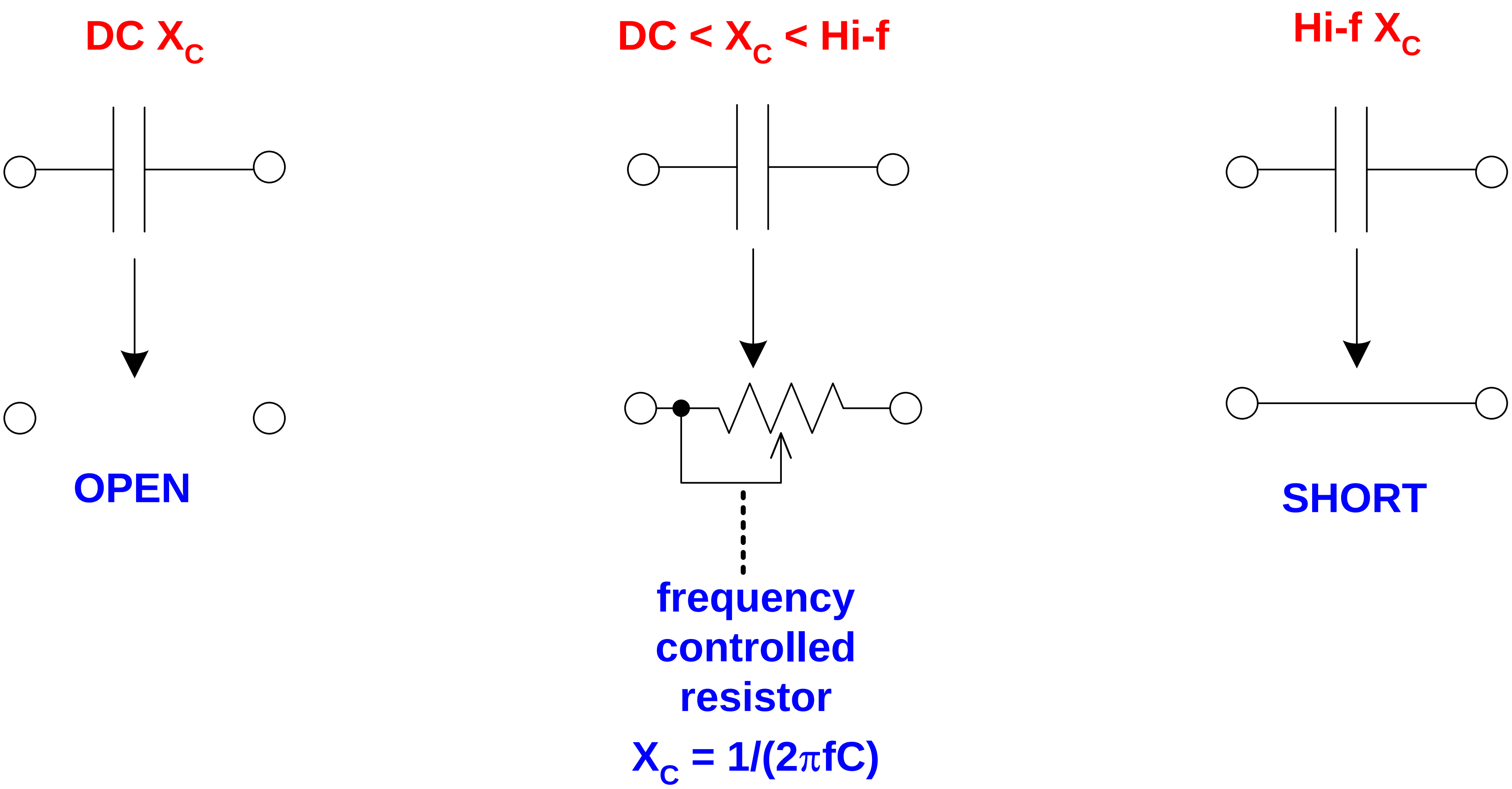




Single Zero Circuit Equivalent

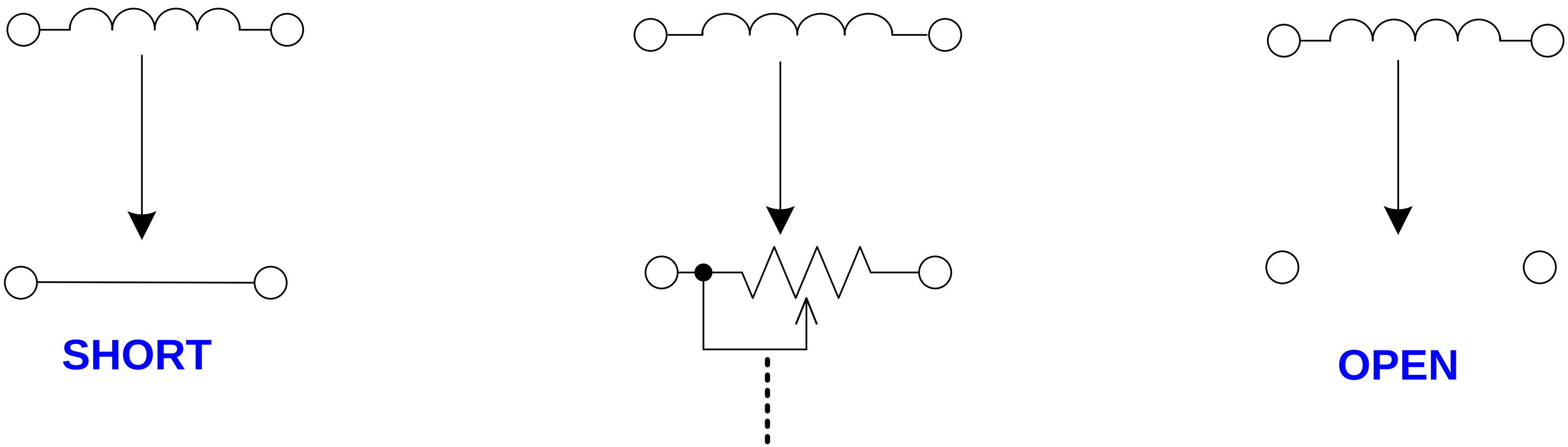
- **Zero Location** = f_Z
- **Magnitude** = +20dB/Decade Slope
  - Slope begins at f_Z and continues up as frequency increases
  - Actual Function = +3dB up @ f_Z
- **Phase** = +45°/Decade Slope through f_Z
  - Decade Above f_Z Phase = +84.3°
  - Decade Below f_Z Phase = 5.7°

Capacitor Intuitive Model



Inductor Intuitive Model

DC X_L | **DC < X_L < Hi-f** | **Hi-f X_L**



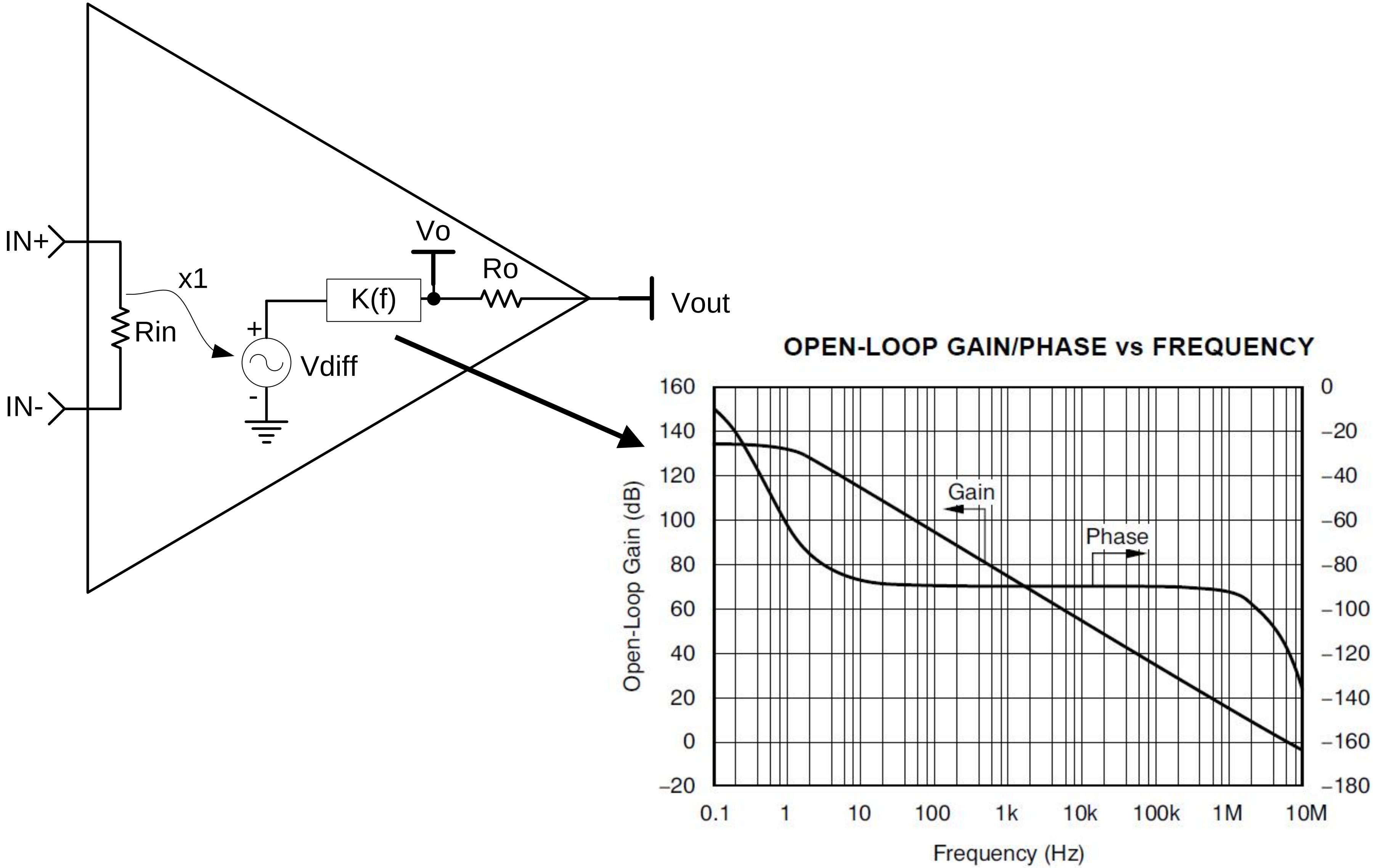
SHORT

frequency controlled resistor

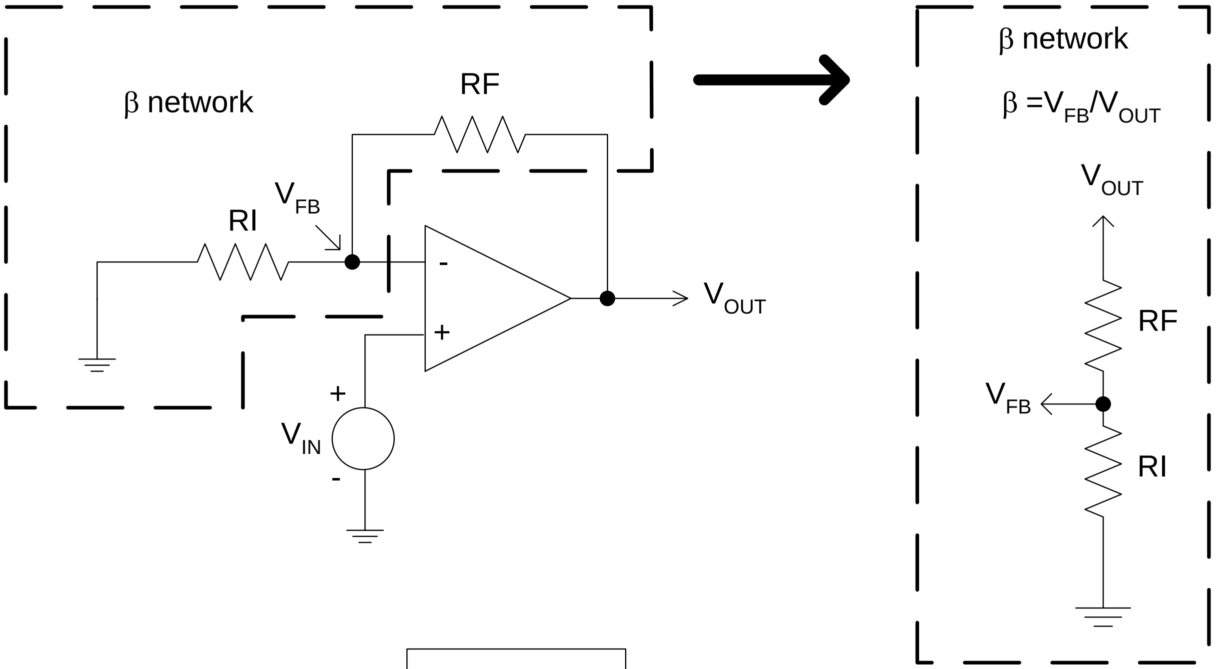
$$X_L = 2\pi fL$$

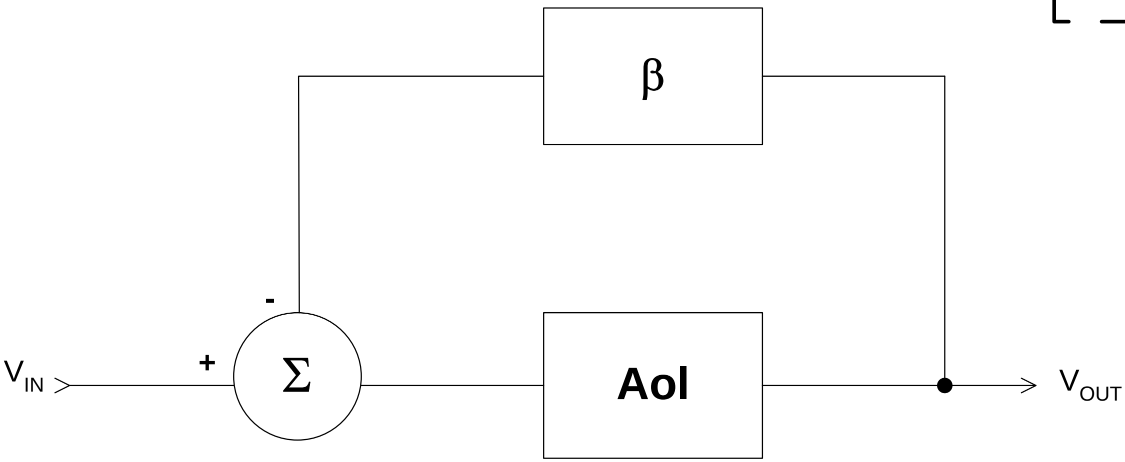
OPEN

Op-Amp Intuitive Model



Op-Amp Loop Gain Model





V_{OUT}/V_{IN} = Acl = Aol/(1+Aolβ)

If Aol >> 1 then Acl ≈ 1/β

Aol: Open Loop Gain

β: Feedback Factor

Acl: Closed Loop Gain

Amplifier Stability Criteria

$V_{OUT}/V_{IN} = Aol / (1+ Aol\beta)$

If: $Aol\beta = -1$

Then: $V_{OUT}/V_{IN} = Aol / 0 \rightarrow \infty$

If $V_{OUT}/V_{IN} = \infty$ → Unbounded Gain

Any small changes in V_{IN} will result in large changes in V_{OUT} which will feed back to V_{IN} and result in even larger changes in V_{OUT} → *OSCILLATIONS* → *INSTABILITY !!*

Aolβ: Loop Gain

Aolβ = -1 → Phase shift of ±180°, Magnitude of 1 (0dB)

fcl: frequency where Aolβ = 1 (0dB)

Stability Criteria:

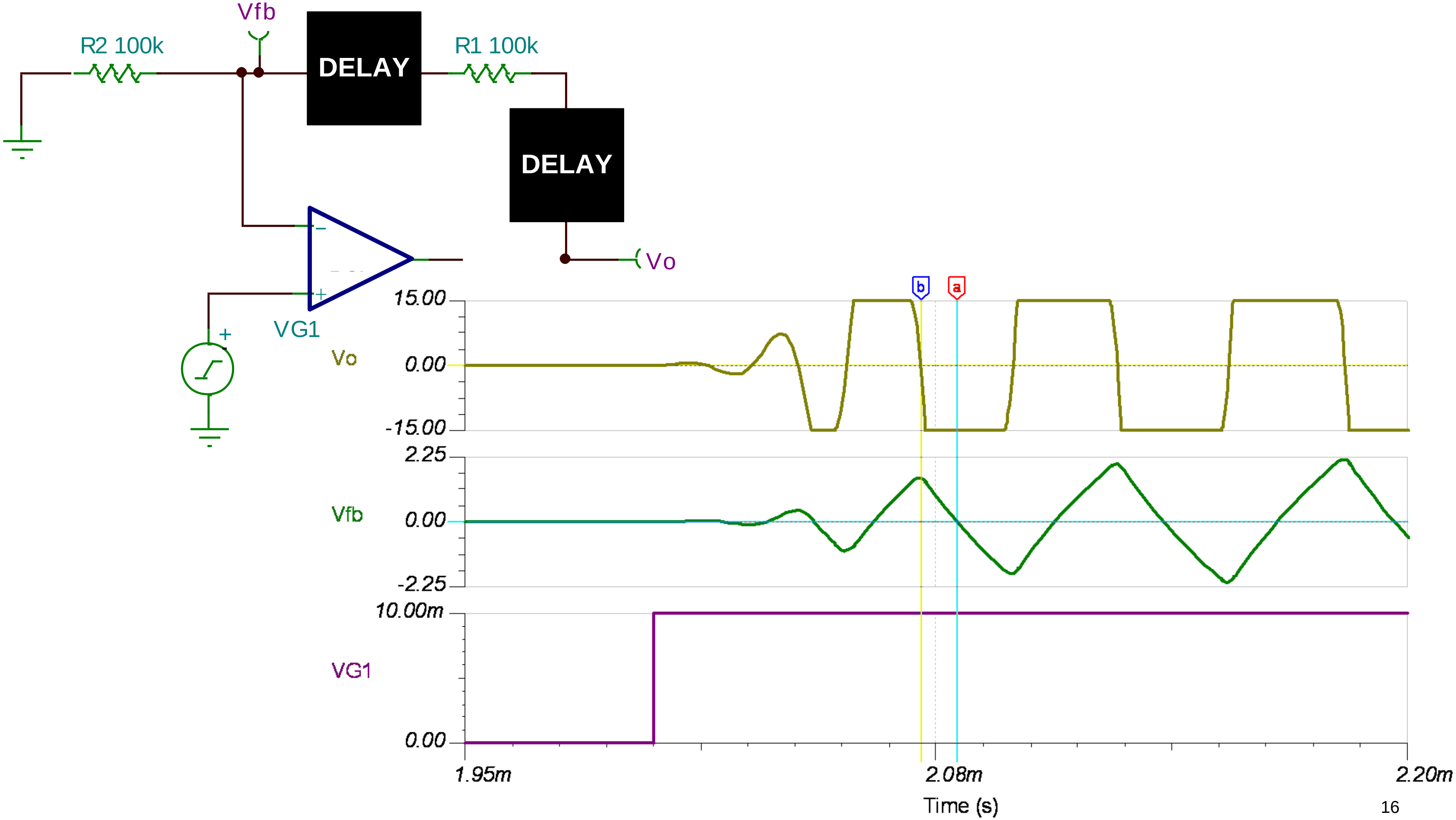
At fcl, where Aolβ = 1 (0dB), Phase Shift < ±180°

Desired Phase Margin (distance from ±180° Phase Shift) ≥ 45°

What causes amplifier stability issues???

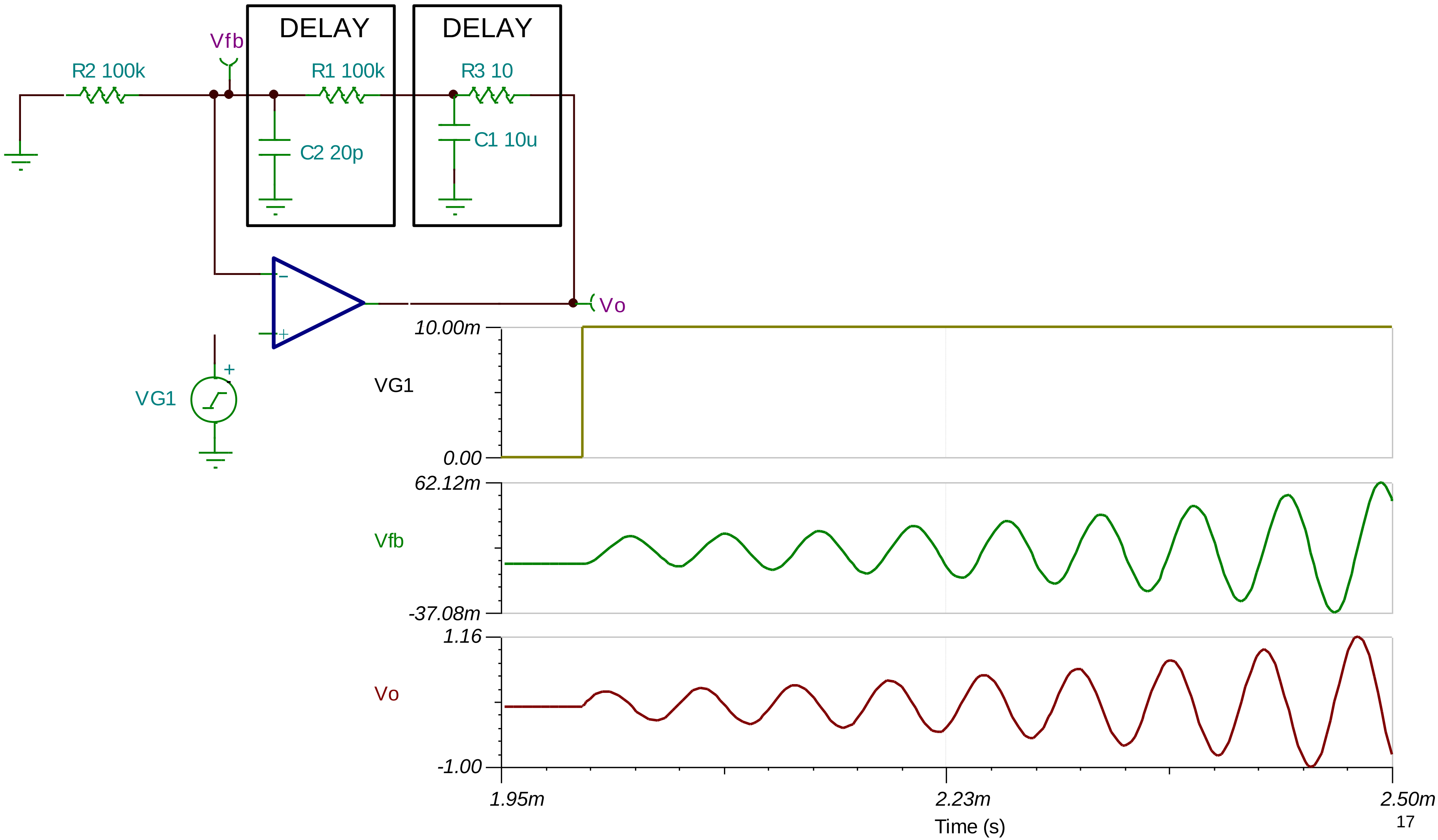
Fundamental Cause of Amplifier Stability Issues

- Too much delay in the feedback network



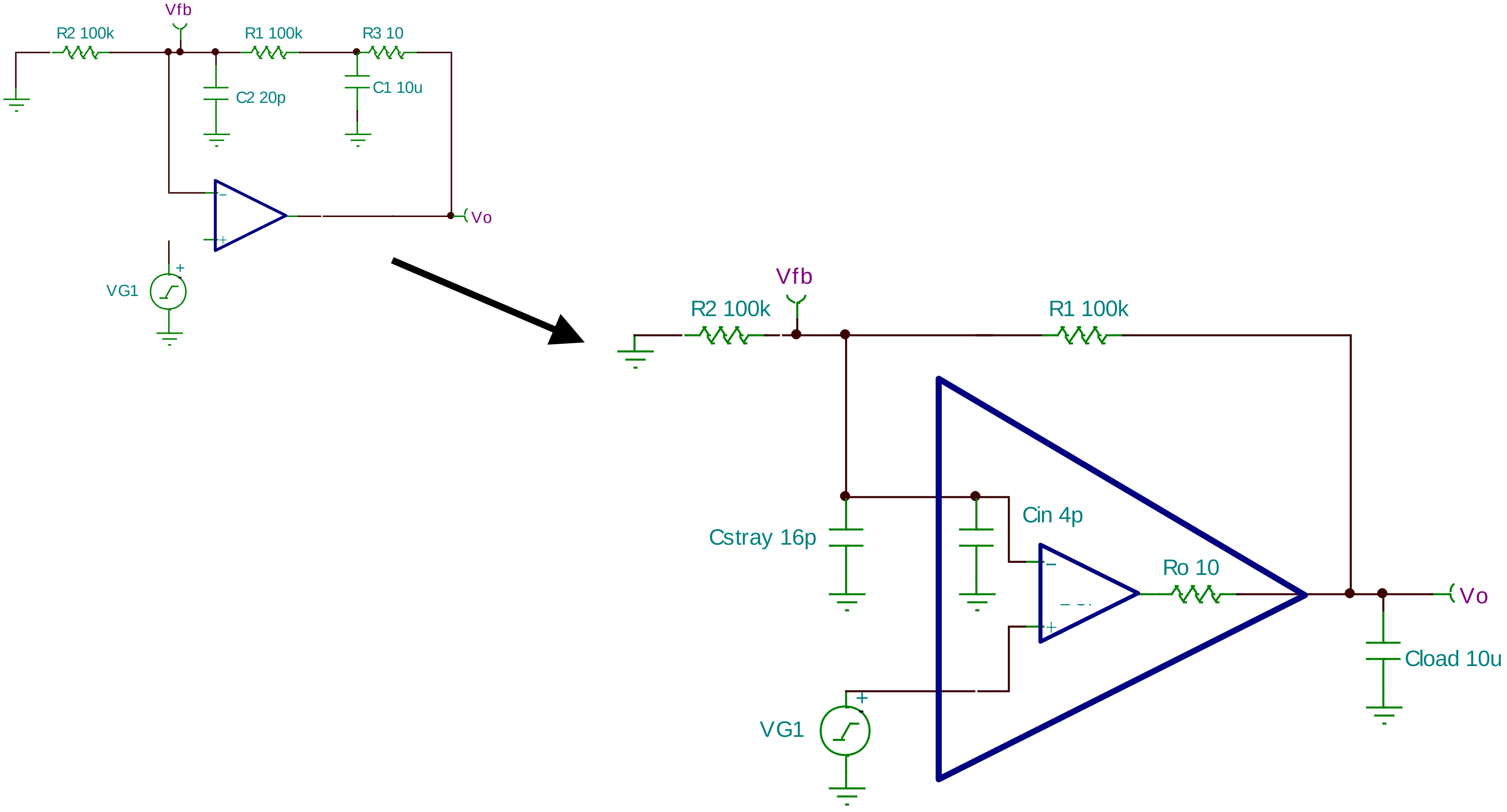
Cause of Amplifier Stability Issues

- Example circuit with too much delay in the feedback network



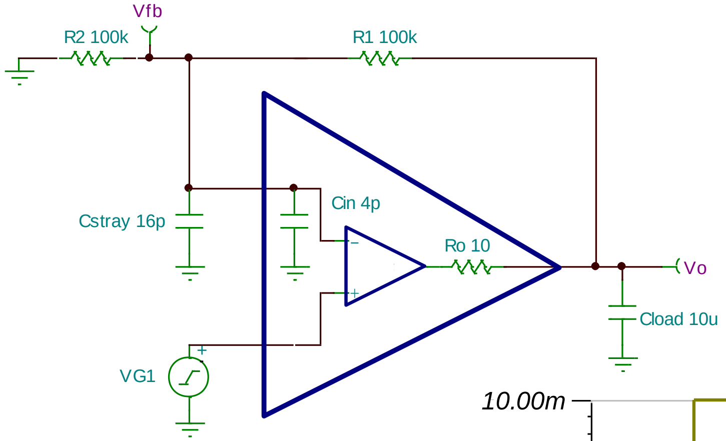
Cause of Amplifier Stability Issues

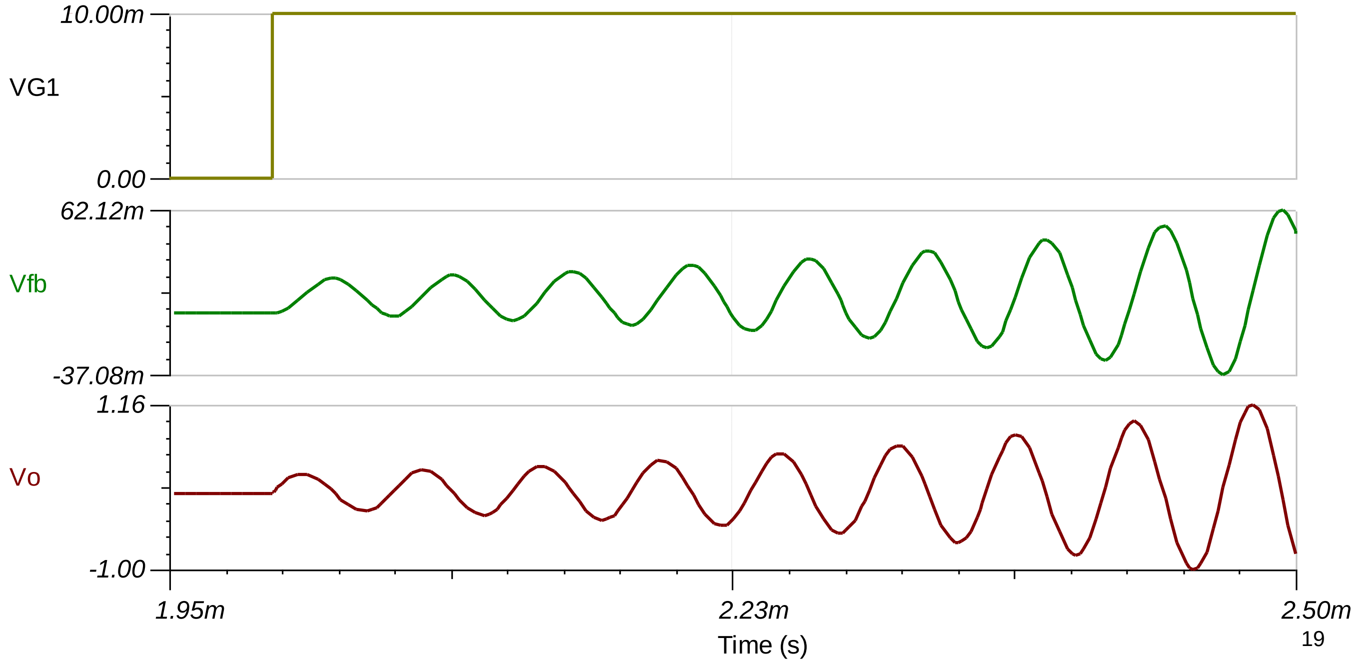
- Real circuit translation of too much delay in the feedback network



Cause of Amplifier Stability Issues

- Same results as the example circuit

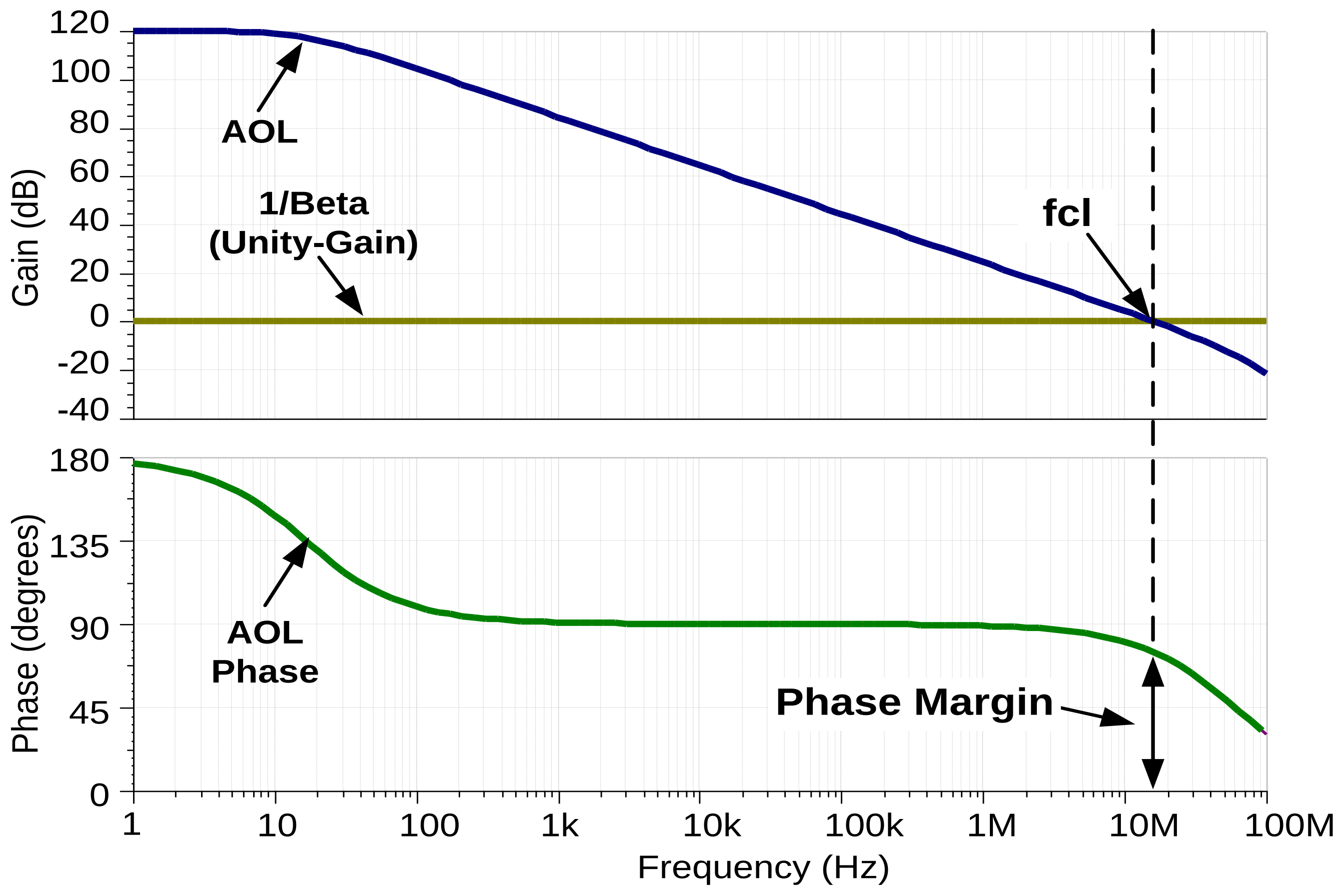


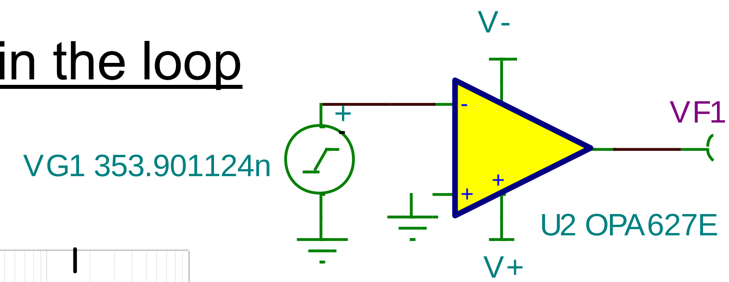


How do we determine if our system has too much delay??

Phase Margin

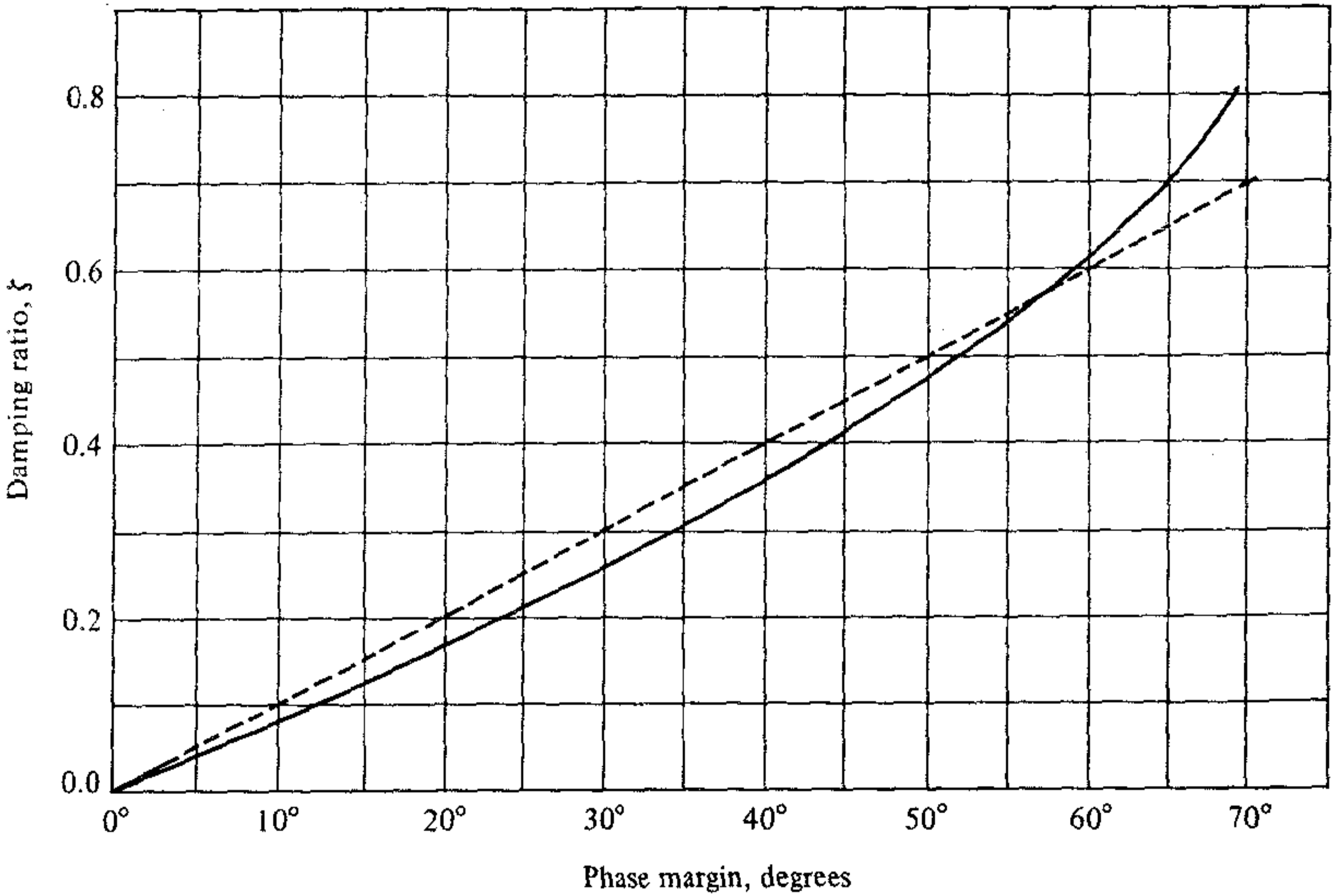
- Phase Margin is a measure of the "delay" in the loop





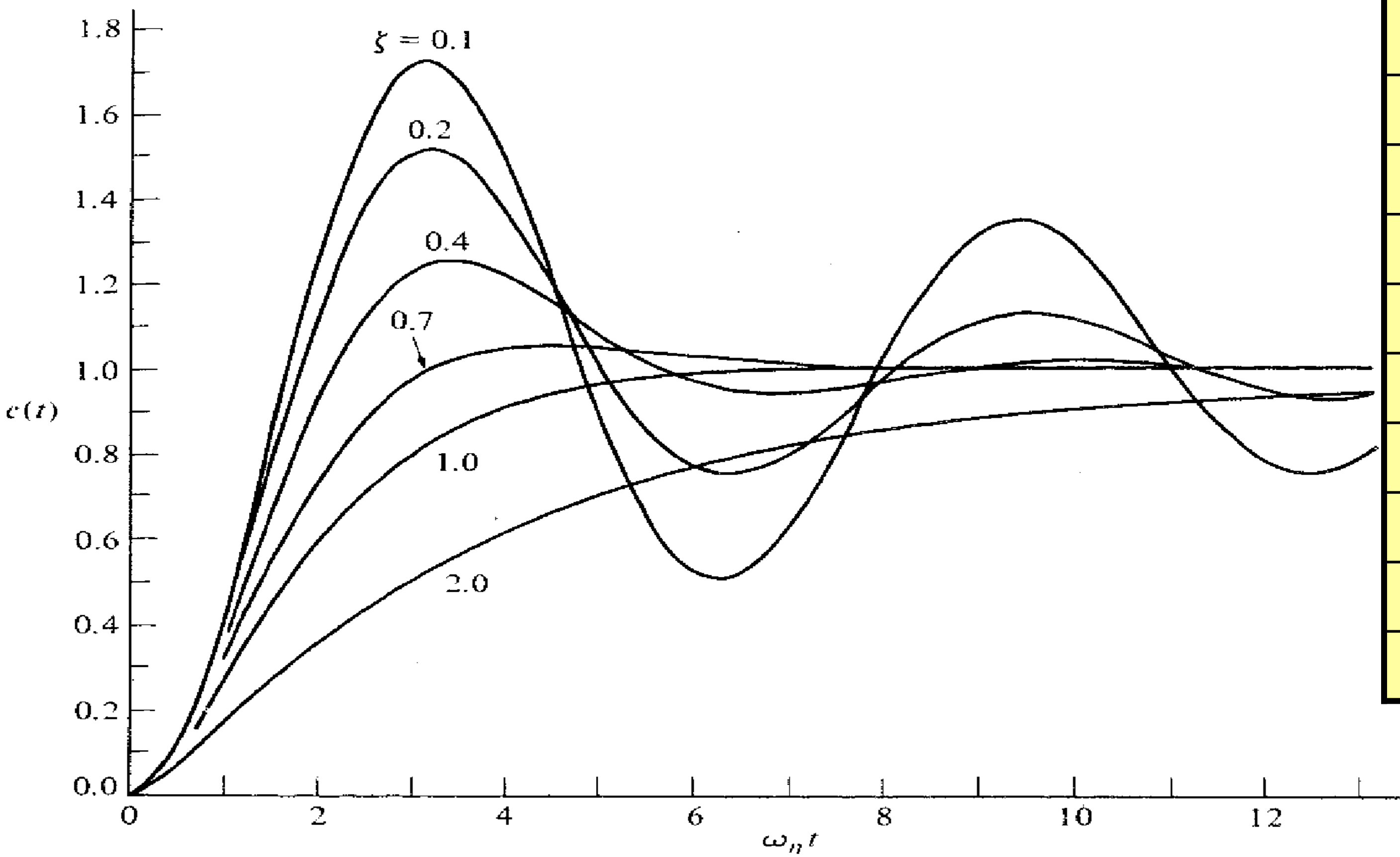
Open-Loop

Damping Ratio vs. Phase Margin



From: Dorf, Richard C. Modern Control Systems. Addison-Wesley Publishing Company. Reading, Massachusetts. Third Edition, 1981.

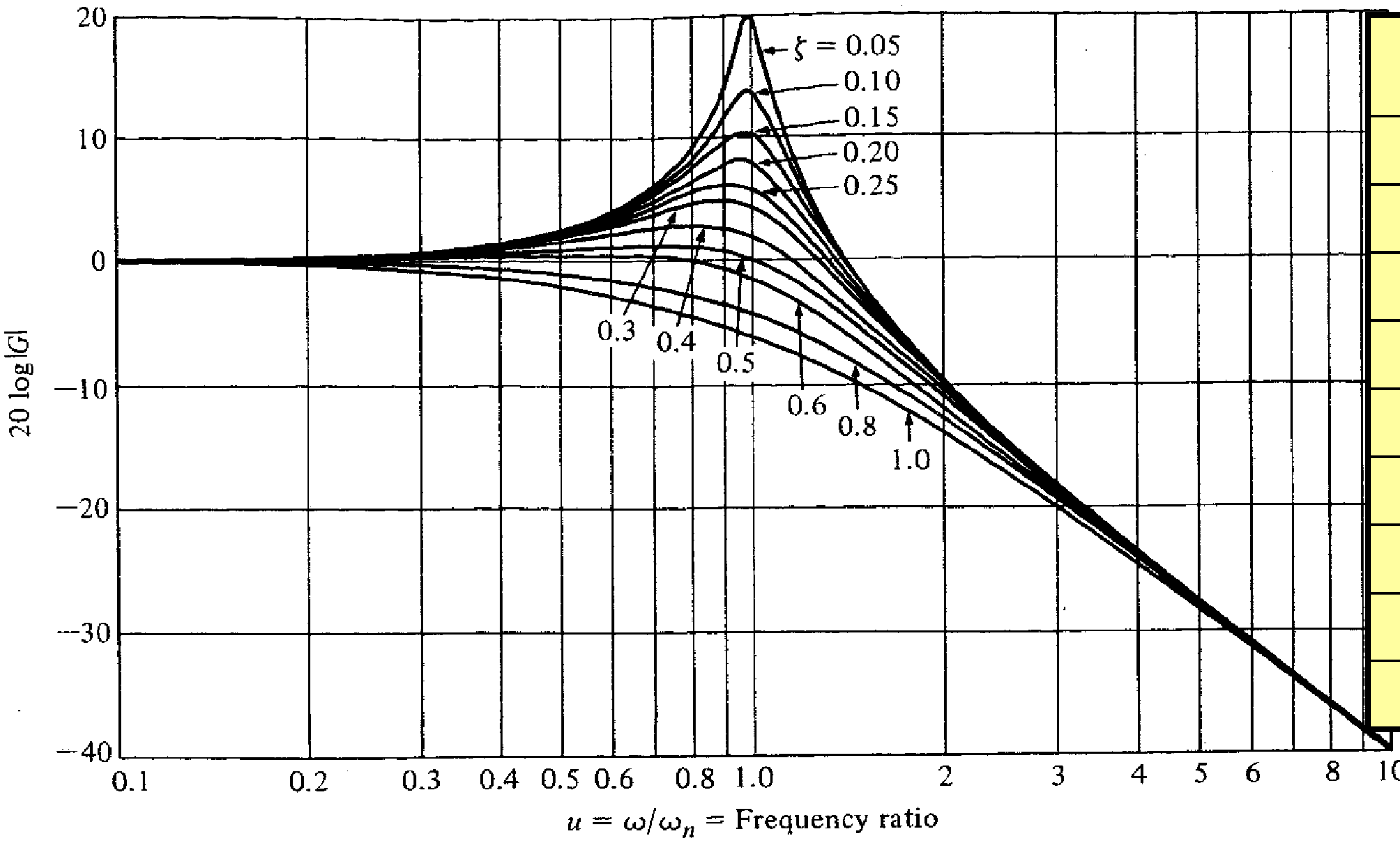
Small-Signal Overshoot vs. Damping Ratio



Phase Margin	Overshoot
90°	0
80°	2%
70°	5%
60°	10%
50°	16%
40°	25%
30°	37%
20°	53%
10°	73%

From: Dorf, Richard C. Modern Control Systems. Addison-Wesley Publishing Company. Reading, Massachusetts. Third Edition, 1981.

AC Peaking vs. Damping Ratio



(a)

Phase Margin	AC Peaking @Wn
90°	-7dB
80°	-5dB
70°	-4dB
60°	-1dB
50°	+1dB
40°	+3dB
30°	+6dB
20°	+9dB
10°	+14dB

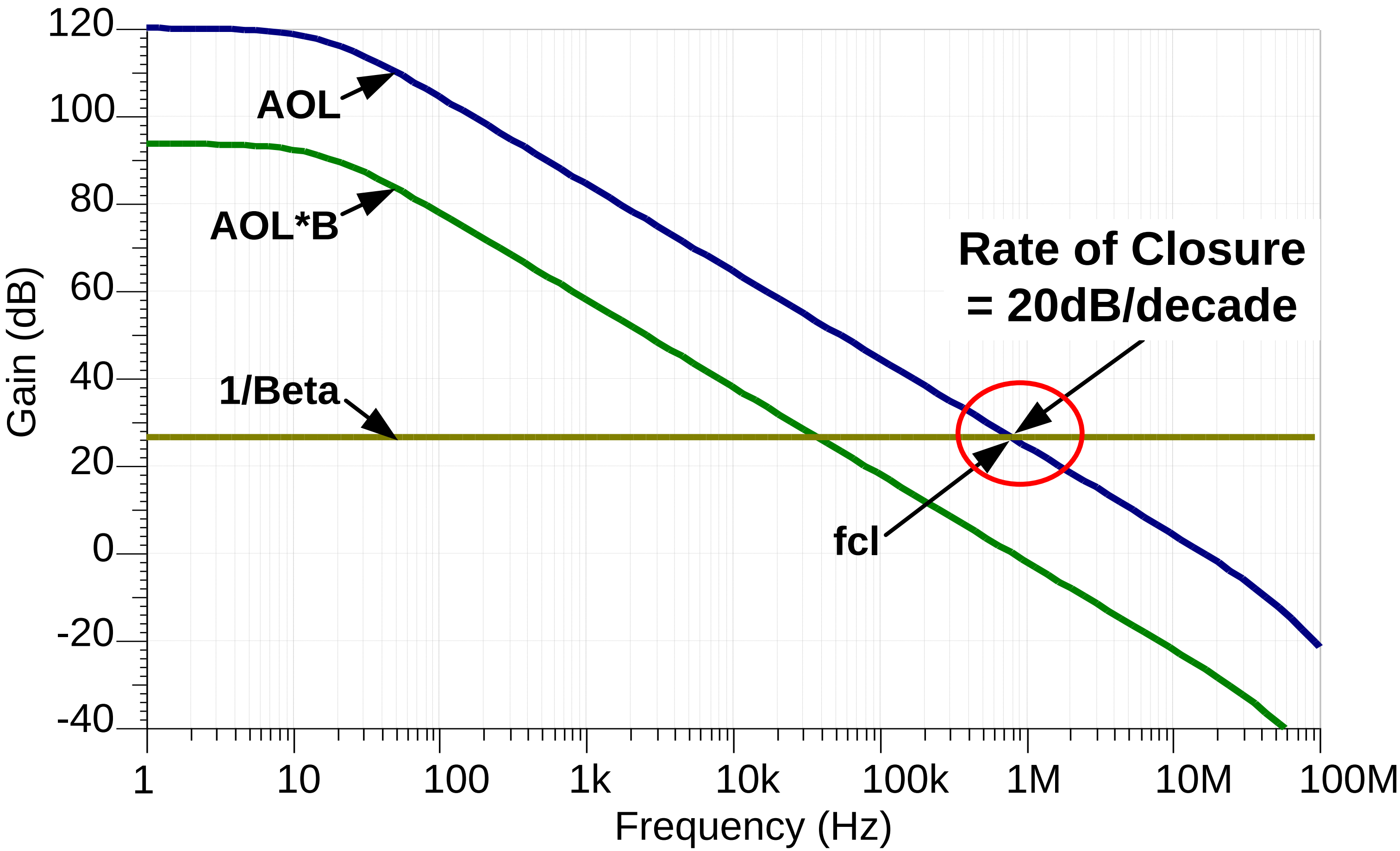
From: Dorf, Richard C. Modern Control Systems. Addison-Wesley Publishing Company. Reading, Massachusetts. Third Edition, 1981.

Rate of Closure

Rate of Closure: **Rate at which 1/Beta and AOL intersect**

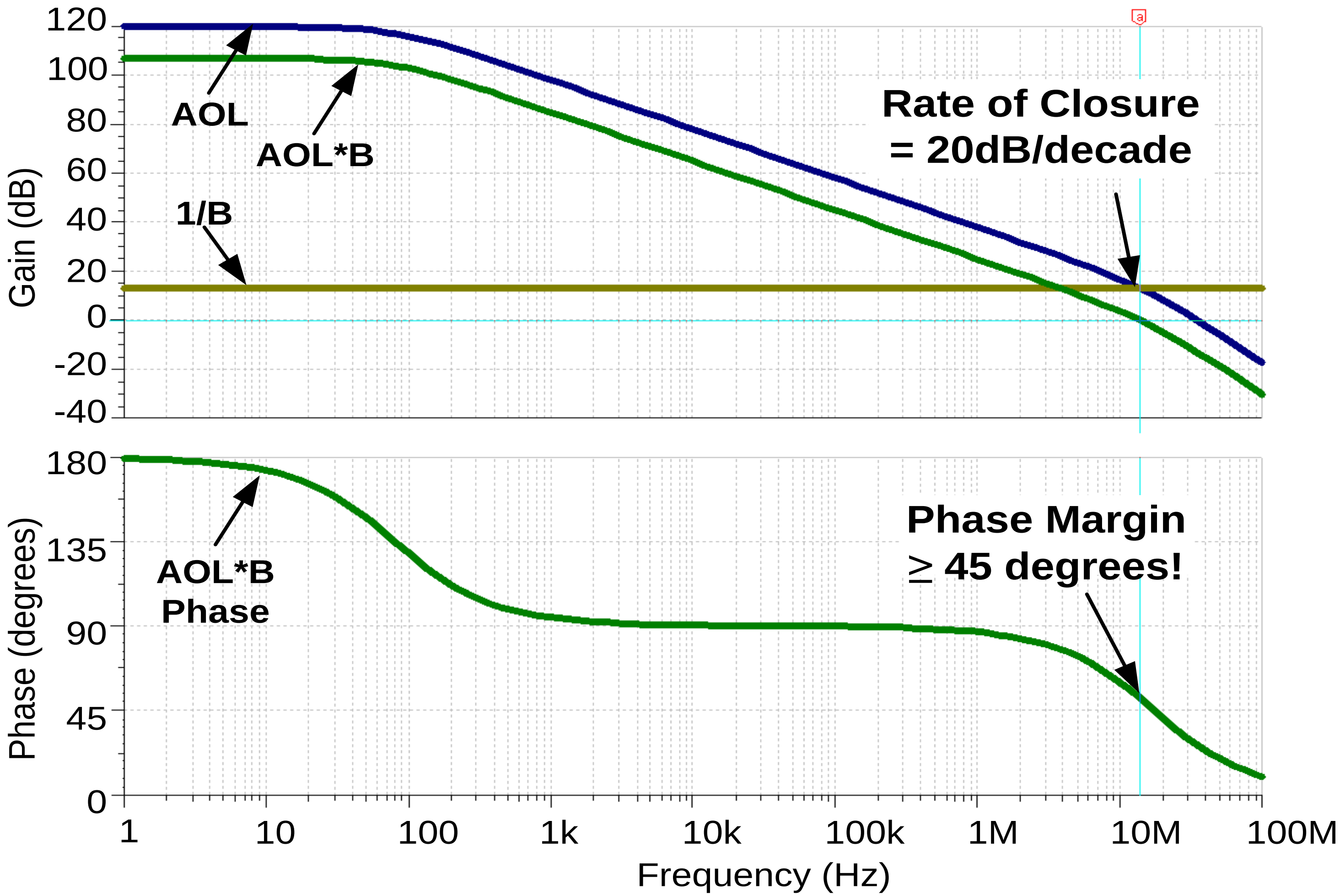
ROC = Slope(1/Beta) – Slope(AOL)

ROC = 0dB/decade – (-20dB/decade) = 20dB/decade



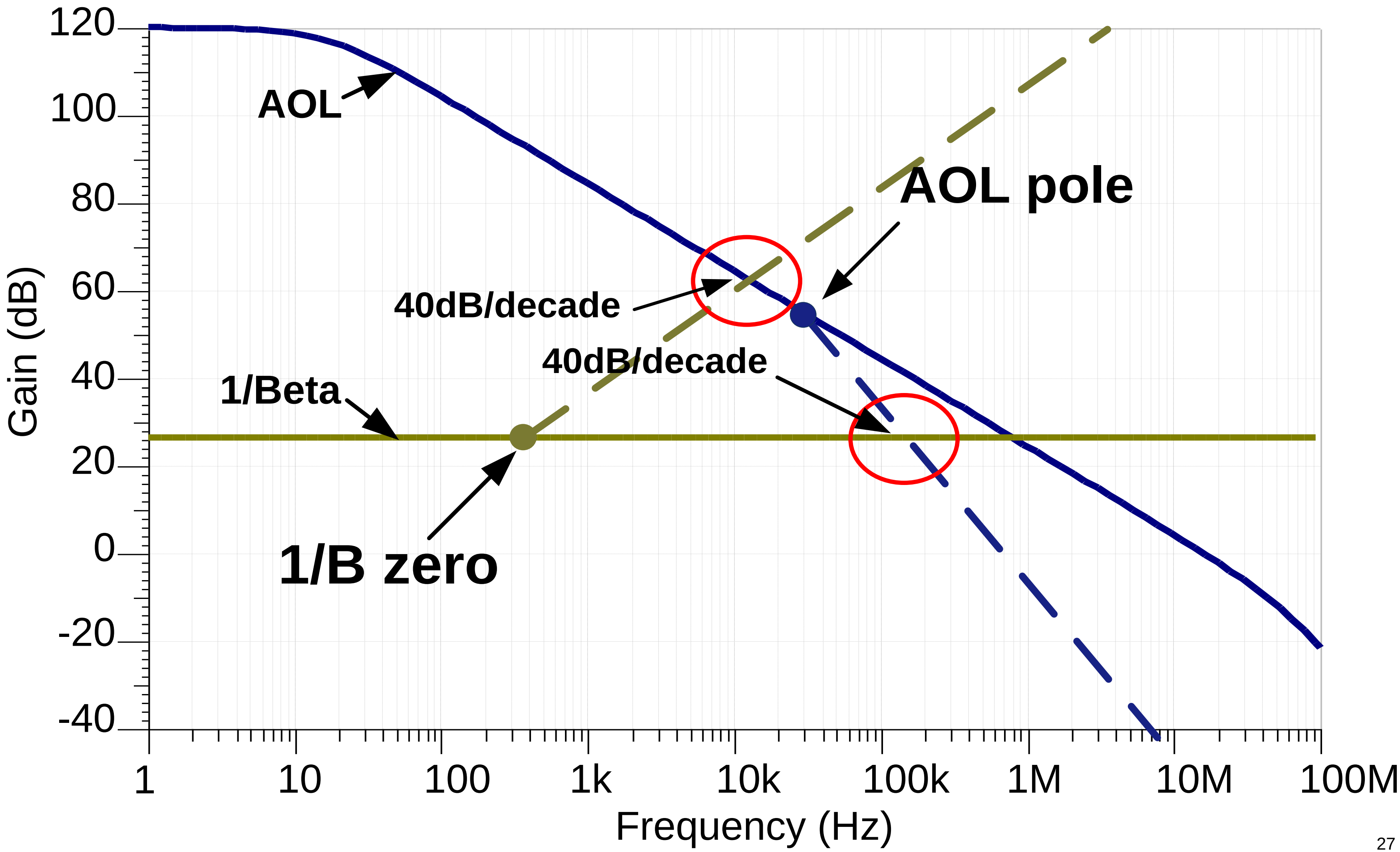
Rate of Closure and Phase Margin

Relationship between the AOL and 1/Beta rate of closure and Loop-Gain (AOL*B) phase margin



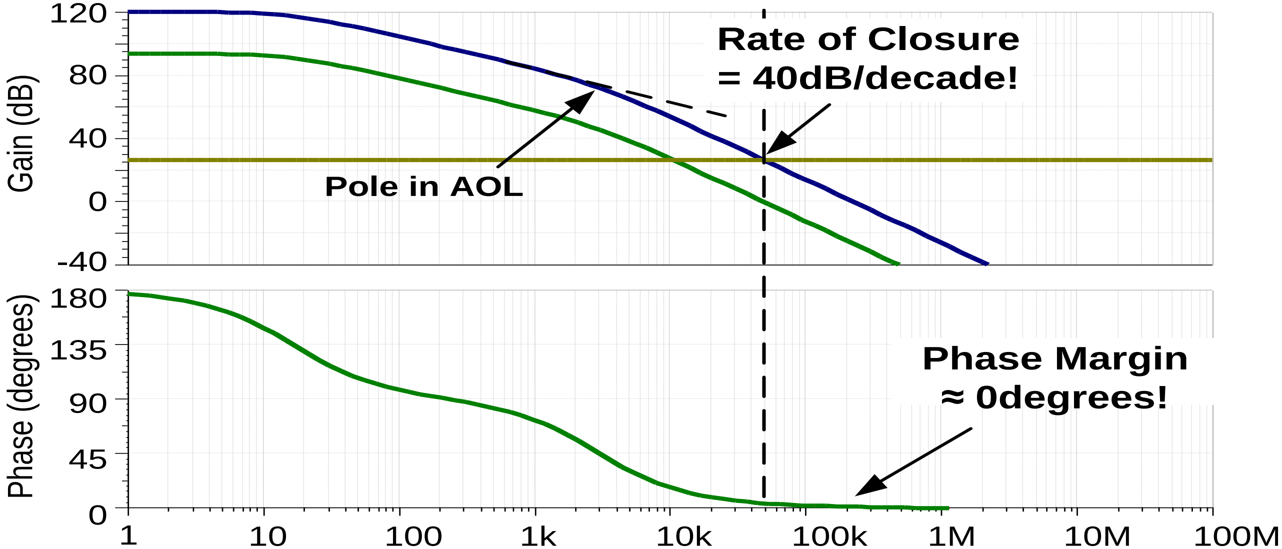
Rate of Closure and Phase Margin

So a pole in AOL or a zero in 1/Beta inside the loop will decrease AOL*B Phase!!

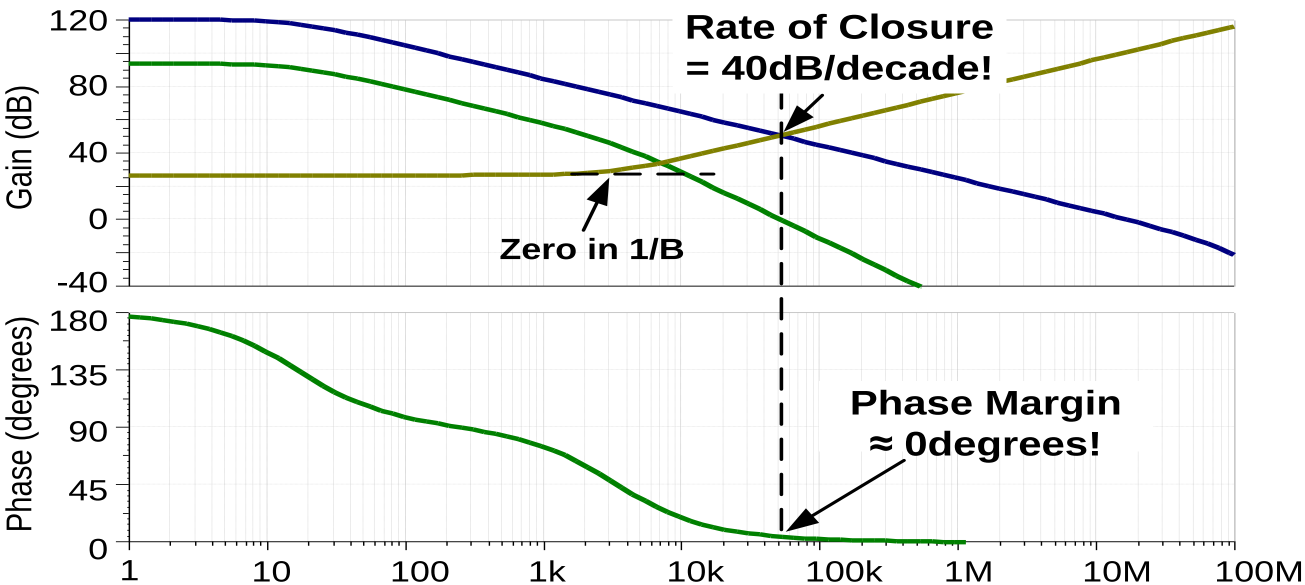


Rate of Closure and Phase Margin

AOL Pole

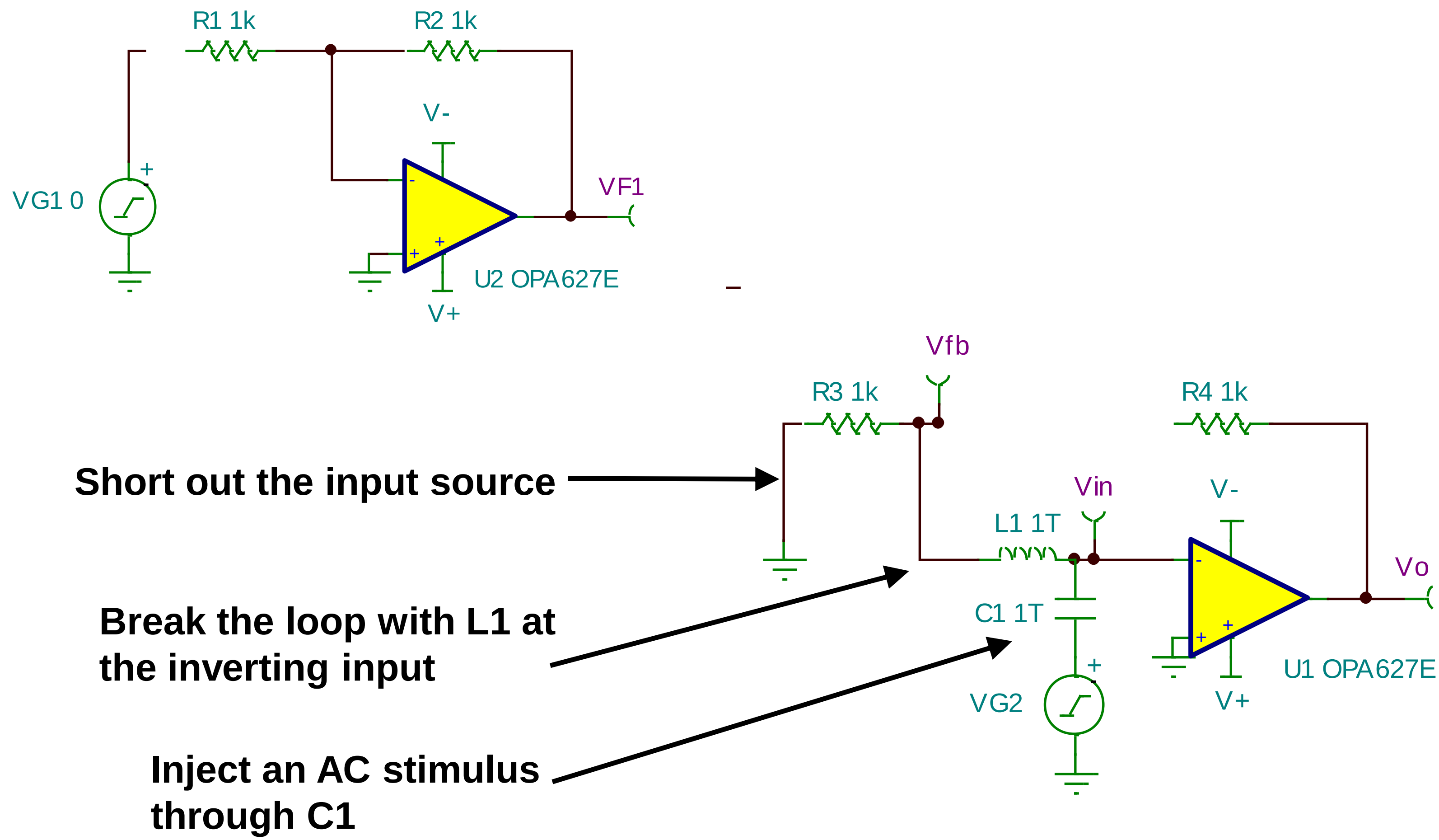


1/Beta Zero

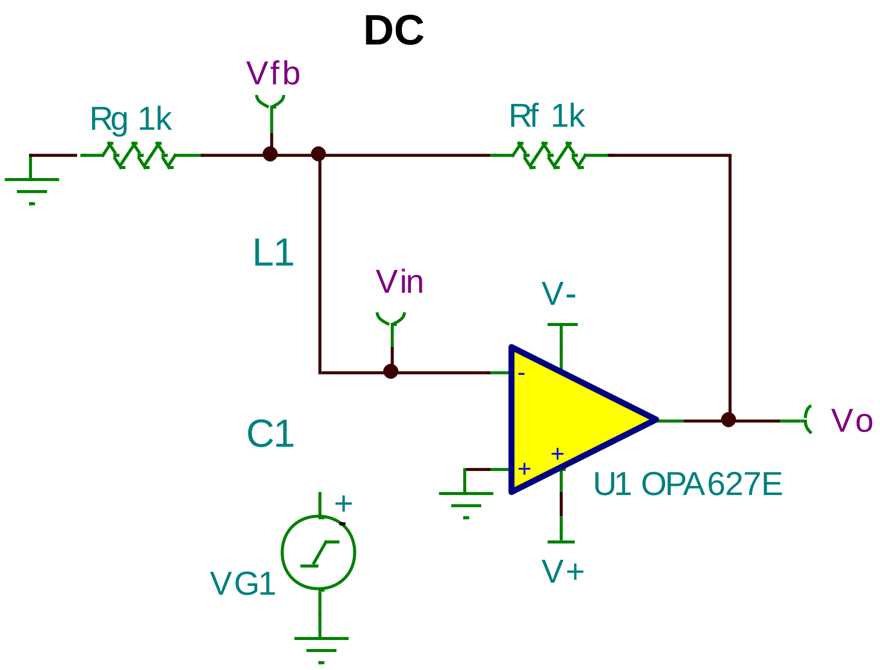


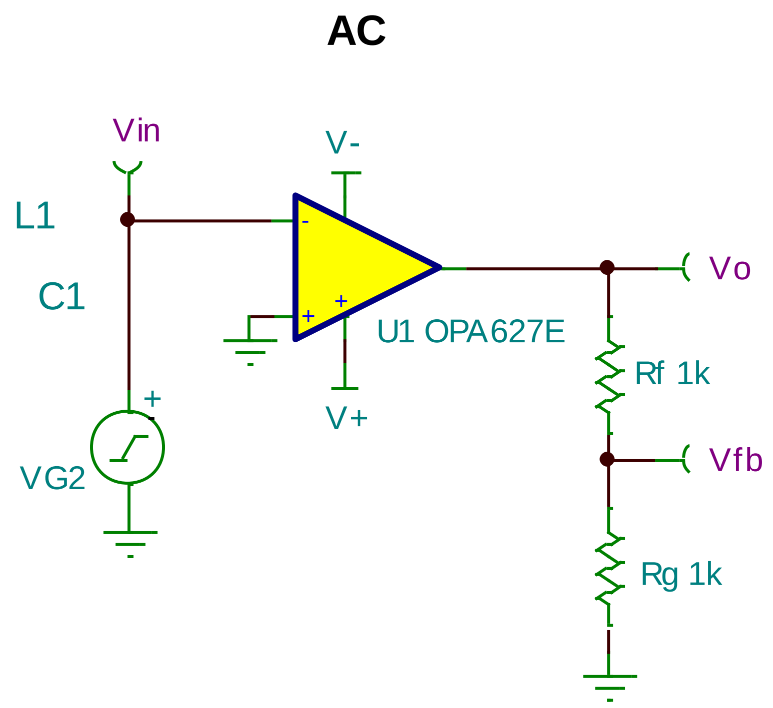
Testing for Rate of Closure in SPICE

- Break the feedback loop and inject a small AC signal



Breaking the Loop



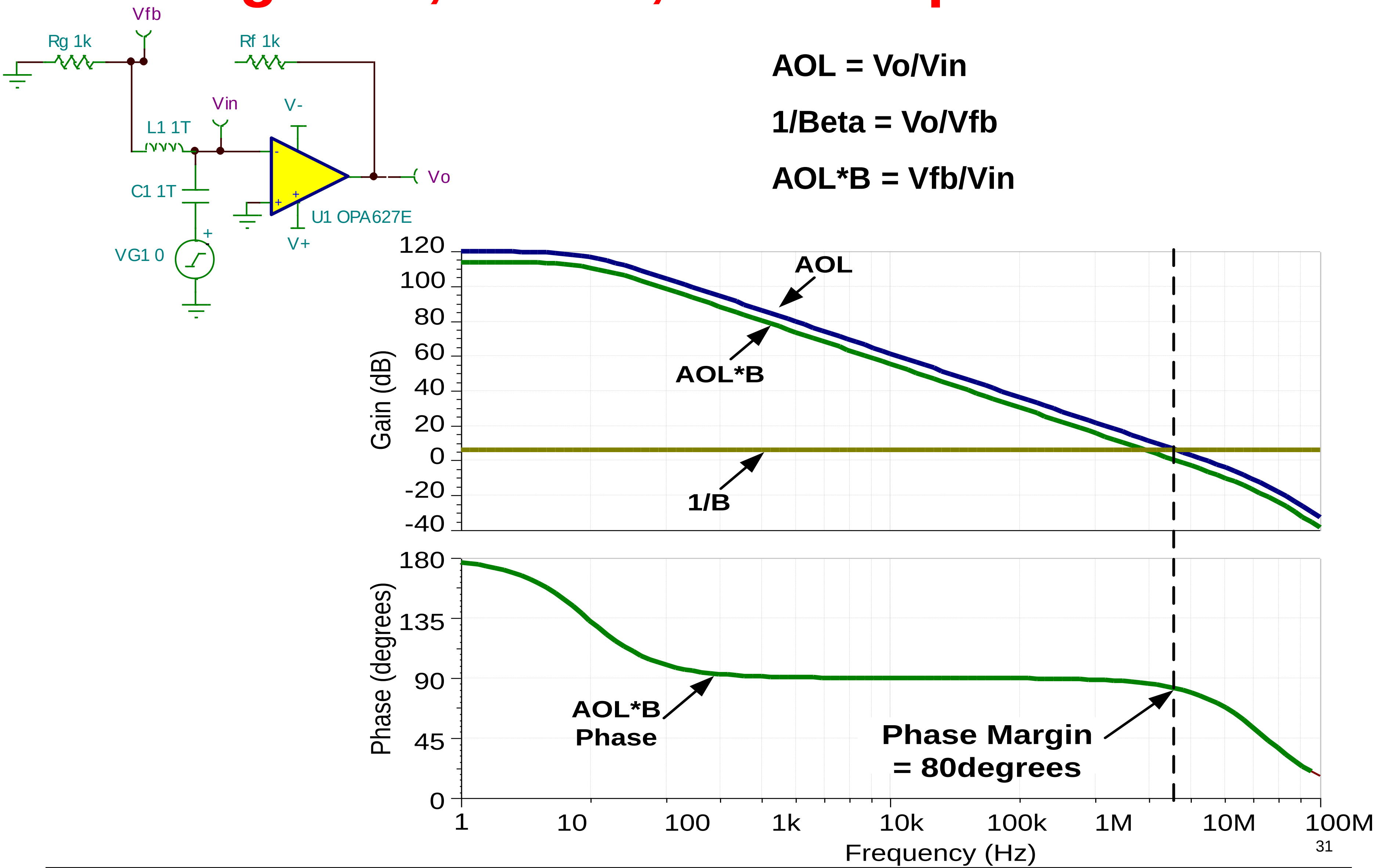


Plotting AOL, 1/Beta, and Loop Gain

AOL = Vo/Vin

1/Beta = Vo/Vfb

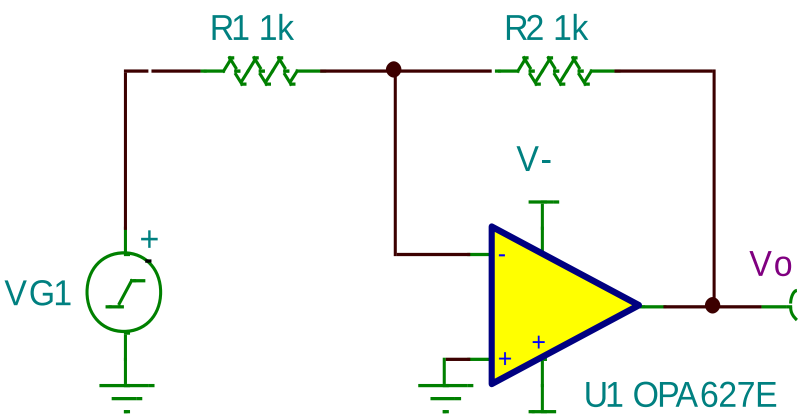
AOL*B = Vfb/Vin



Noise Gain

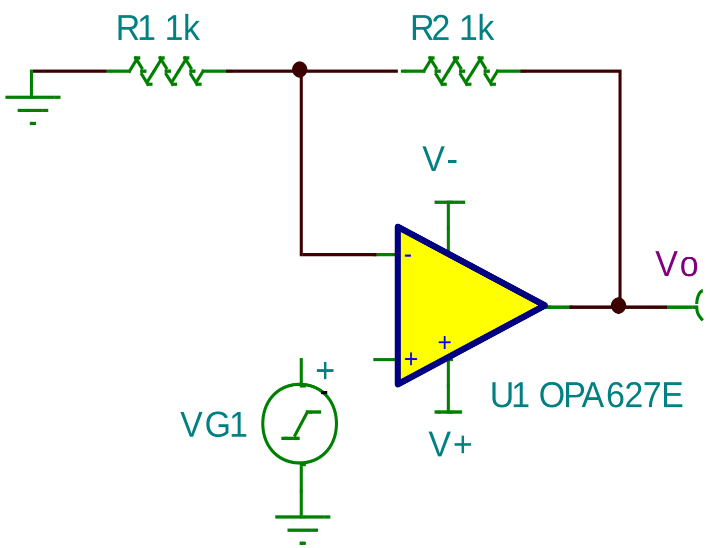
- <u>Understanding Noise Gain vs. Signal Gain</u>

Signal Gain, G = -1



NG = 1 + ISGI = 2

Signal Gain, G = 2



NG = SG = 2

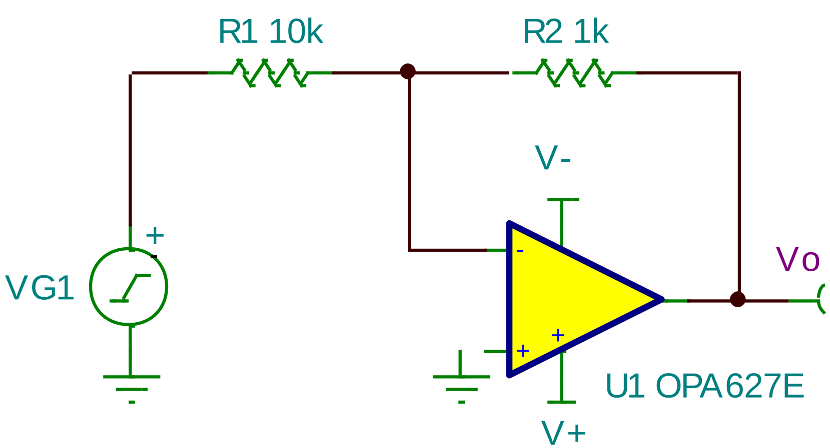
Both circuits have a *<u>NOISE GAIN</u>* (NG) of 2.

Noise Gain

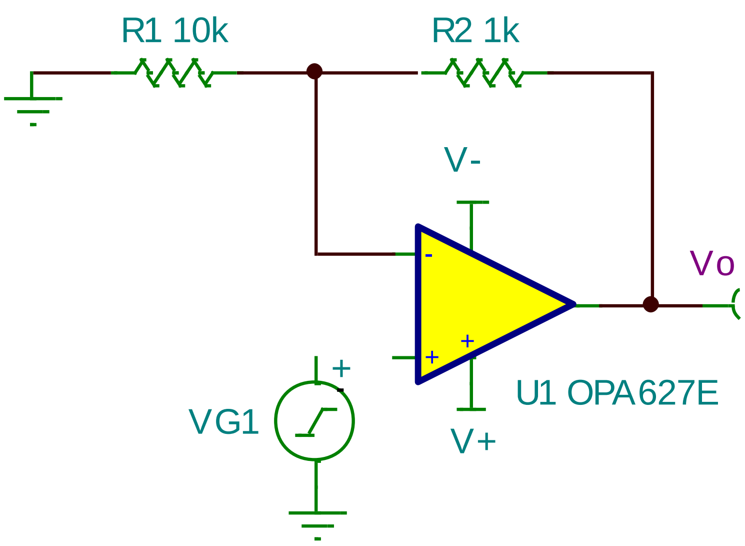
- <u>Noise Gain vs. Signal Gain</u>

  Gain of -0.1V/V, Is it Stable?

Signal Gain, G = -0.1



Noise Gain, NG = 1.1

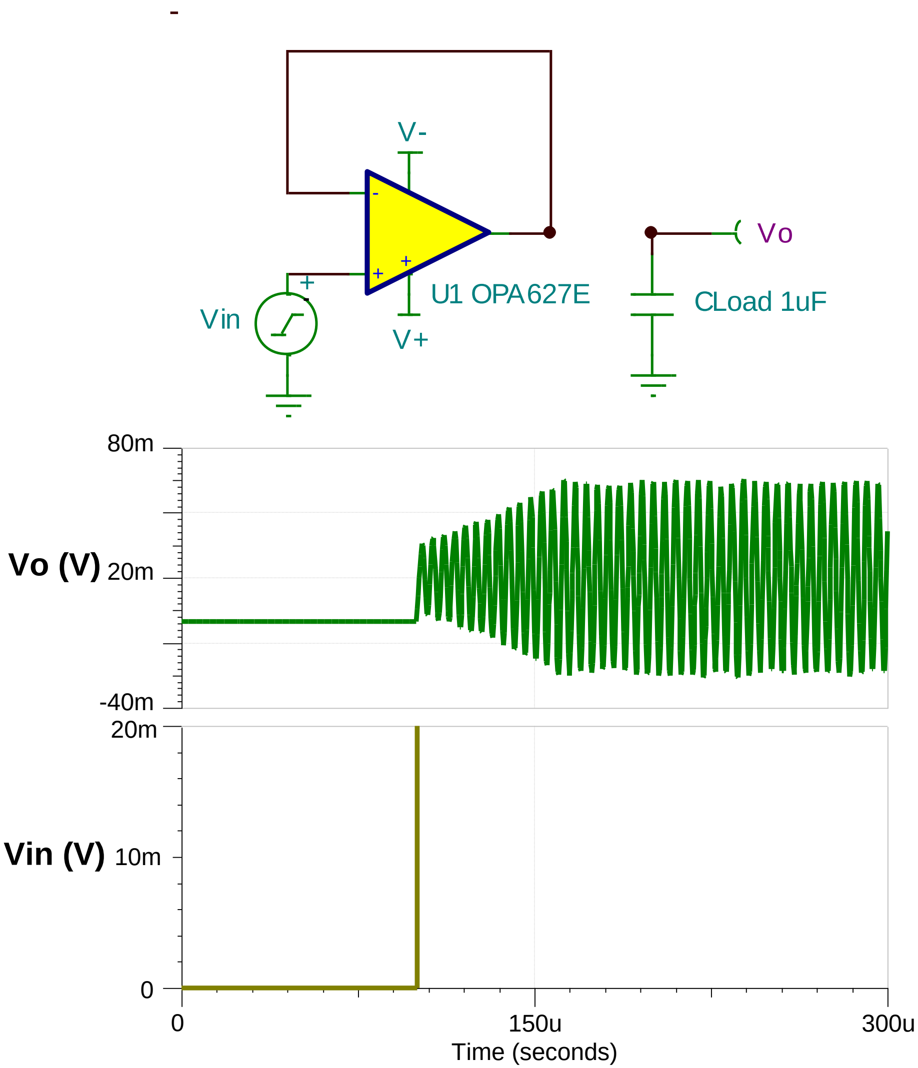


If it's unity-gain stable then it's stable as an inverting attenuator!!!

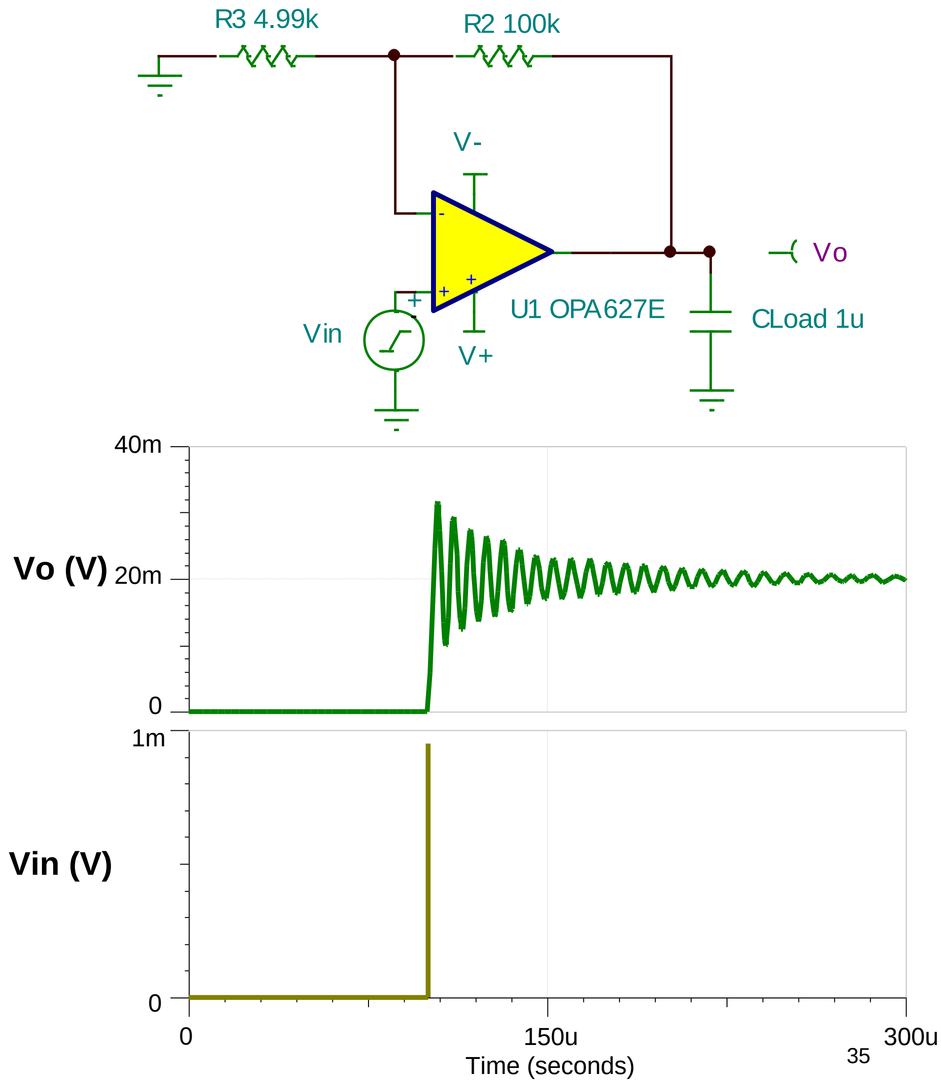
Capacitive Loads

Capacitive Loads

Unity Gain Buffer Circuits



Circuits with Gain



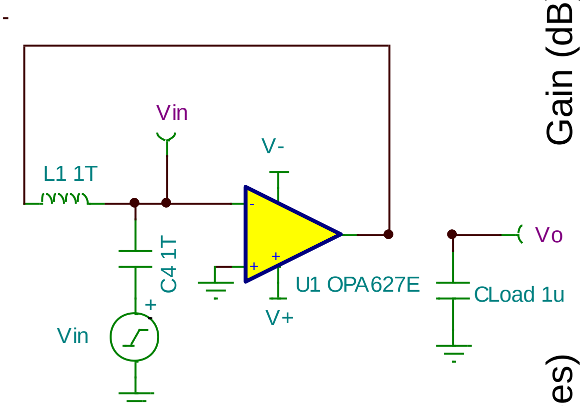
Capacitive Loads – Unity Gain Buffers - Results

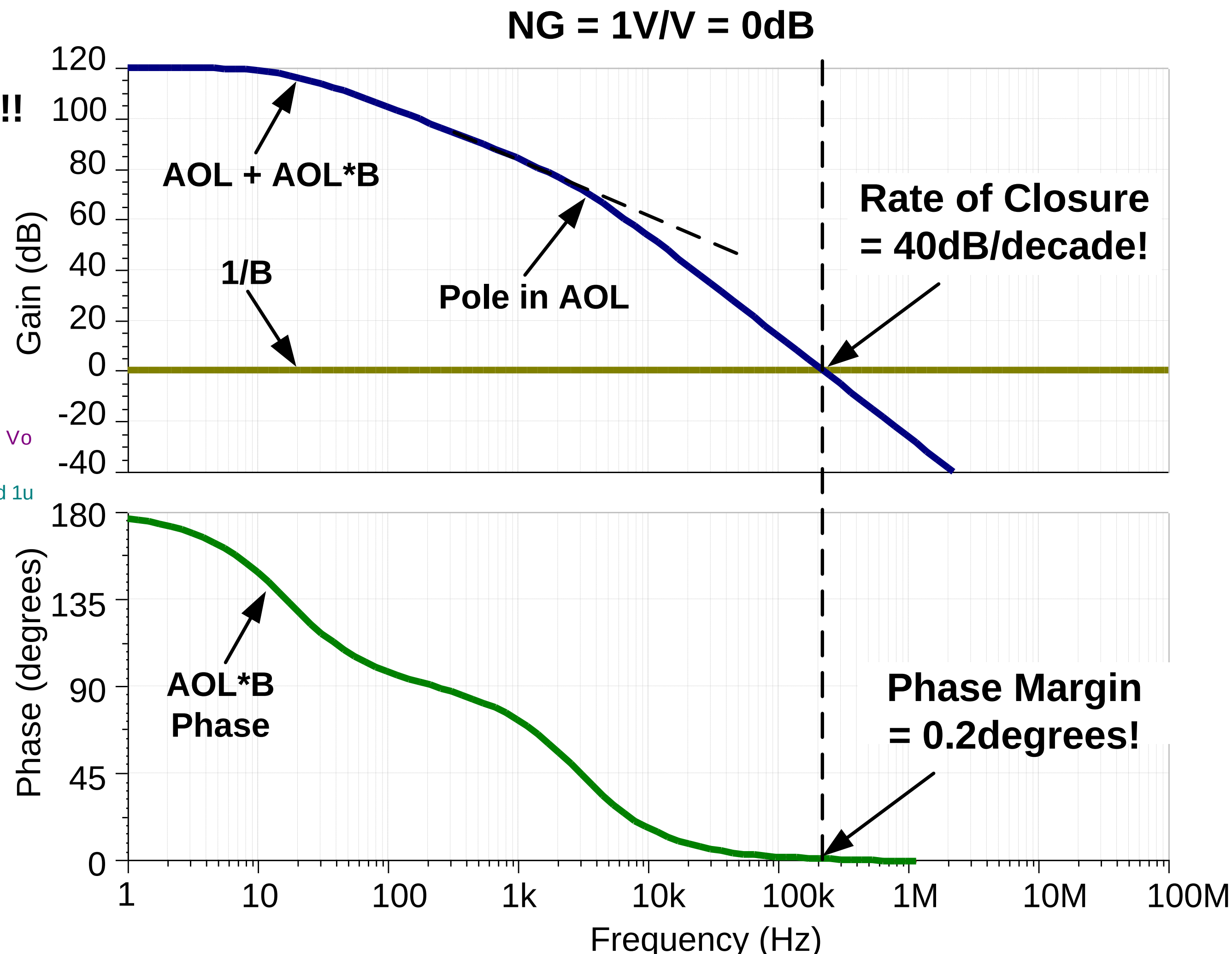
Determine the issue:

Pole in AOL!!

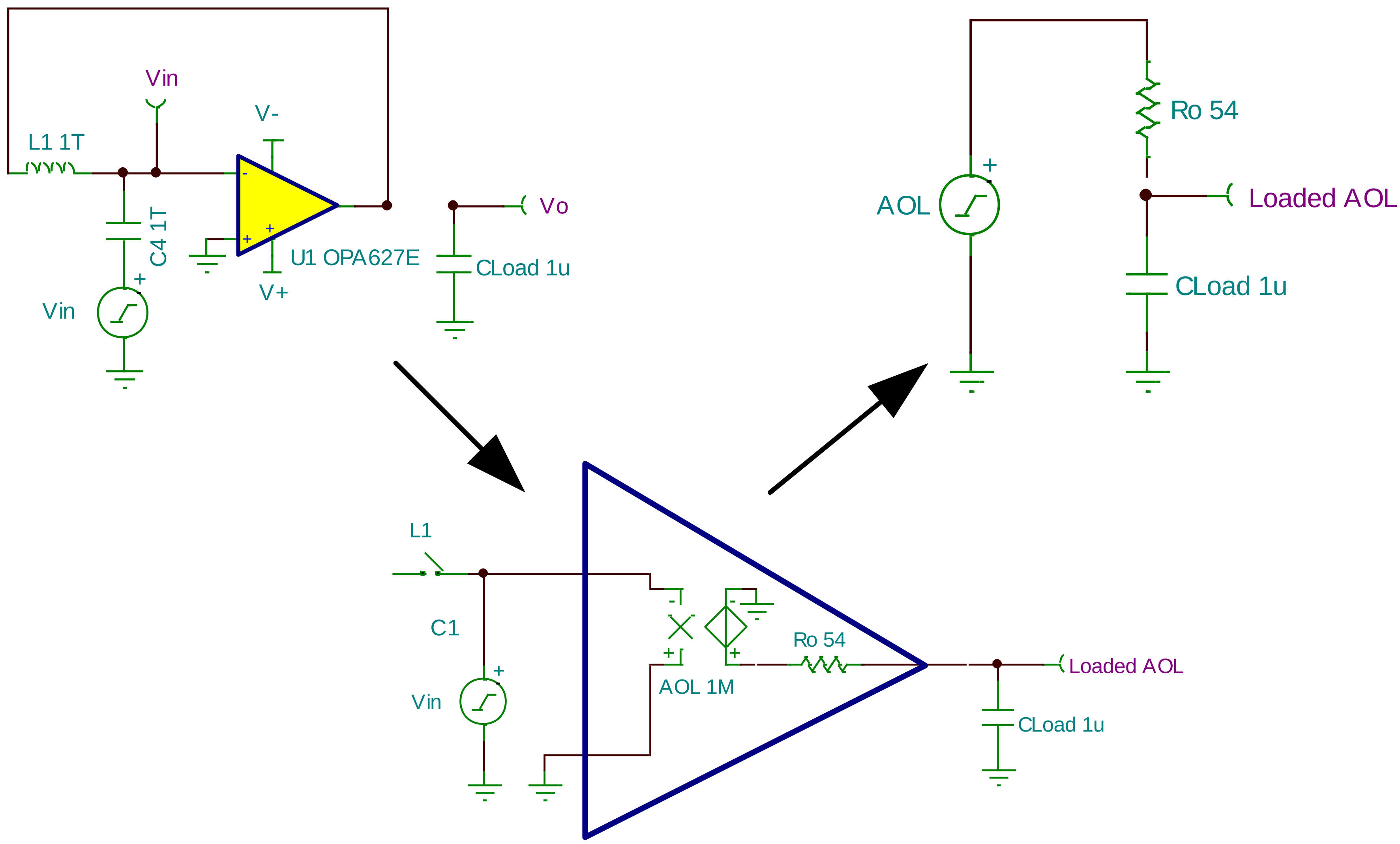
ROC = 40dB/decade!!

Phase Margin 0!!

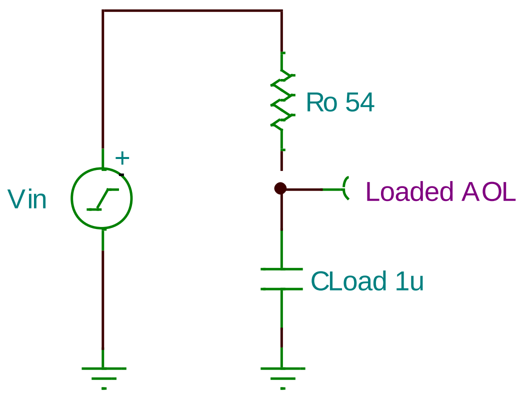




Capacitive Loads – Unity Gain Buffers - Theory



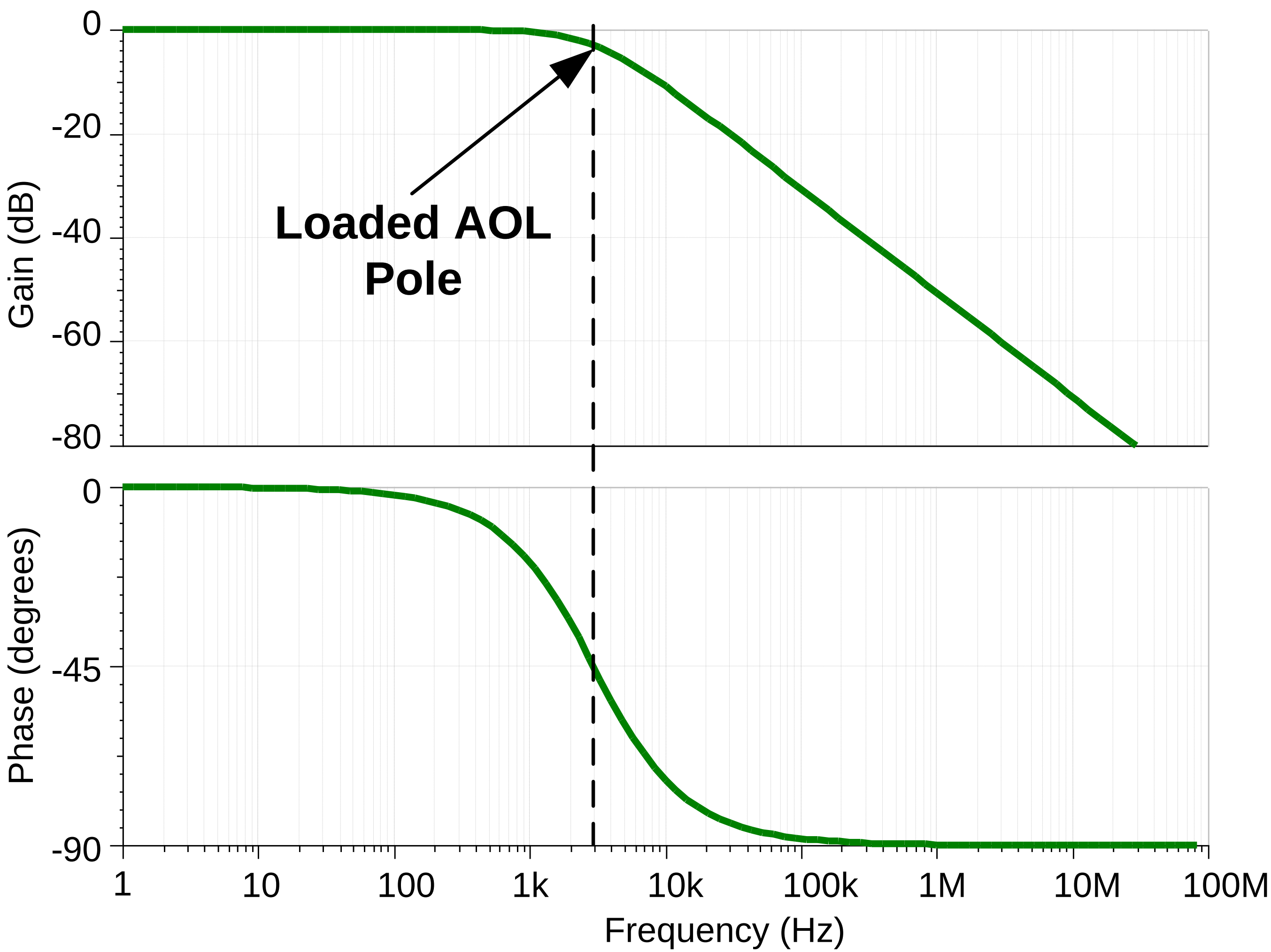
Capacitive Loads – Unity Gain Buffers - Theory



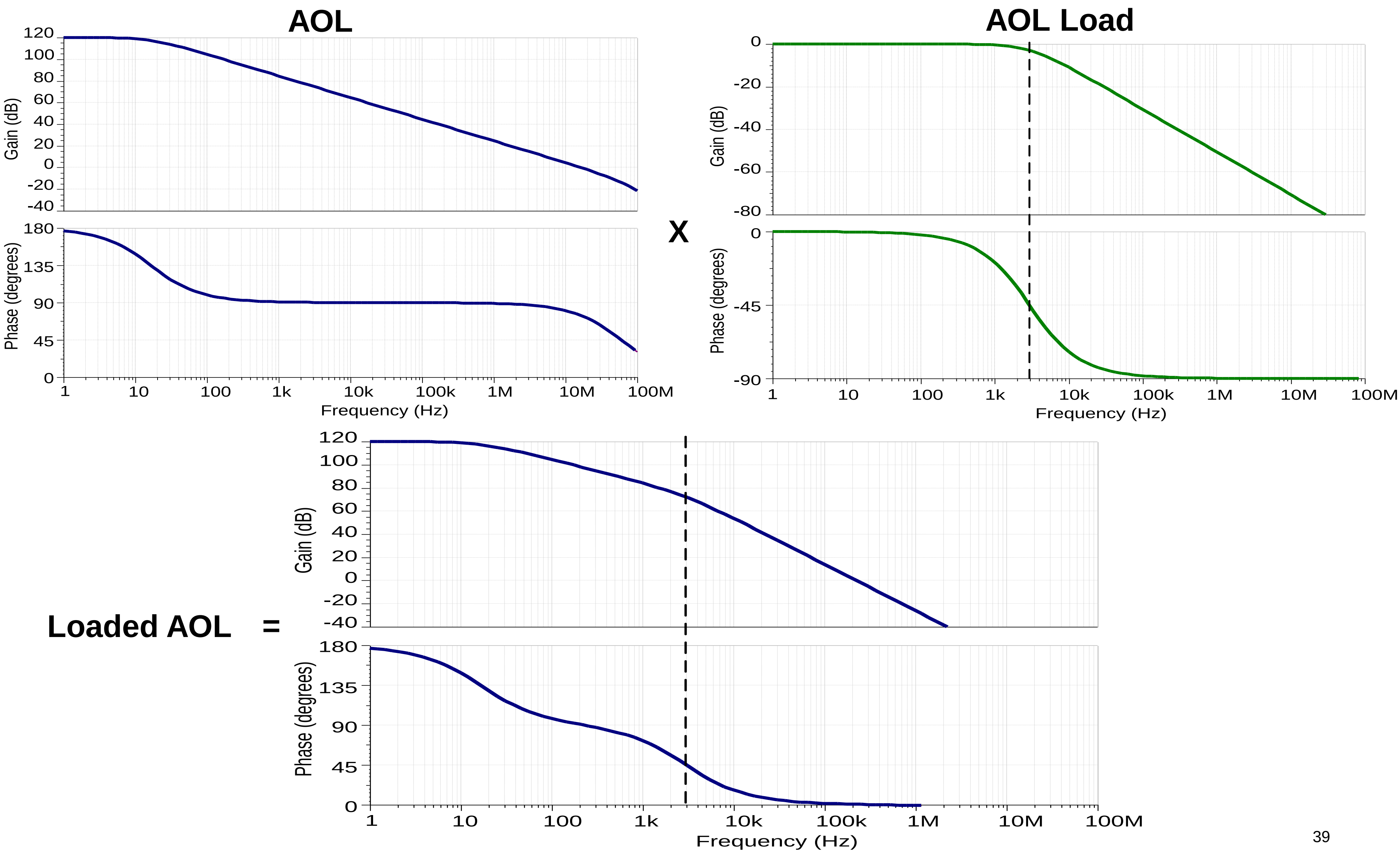
Transfer function:

$$W(s)=\frac{1}{1+R_o\cdot C_{load}\cdot s}$$

$$f(pole)=\frac{1}{2\cdot pi\cdot R_o\cdot C_{Load}\cdot s}$$



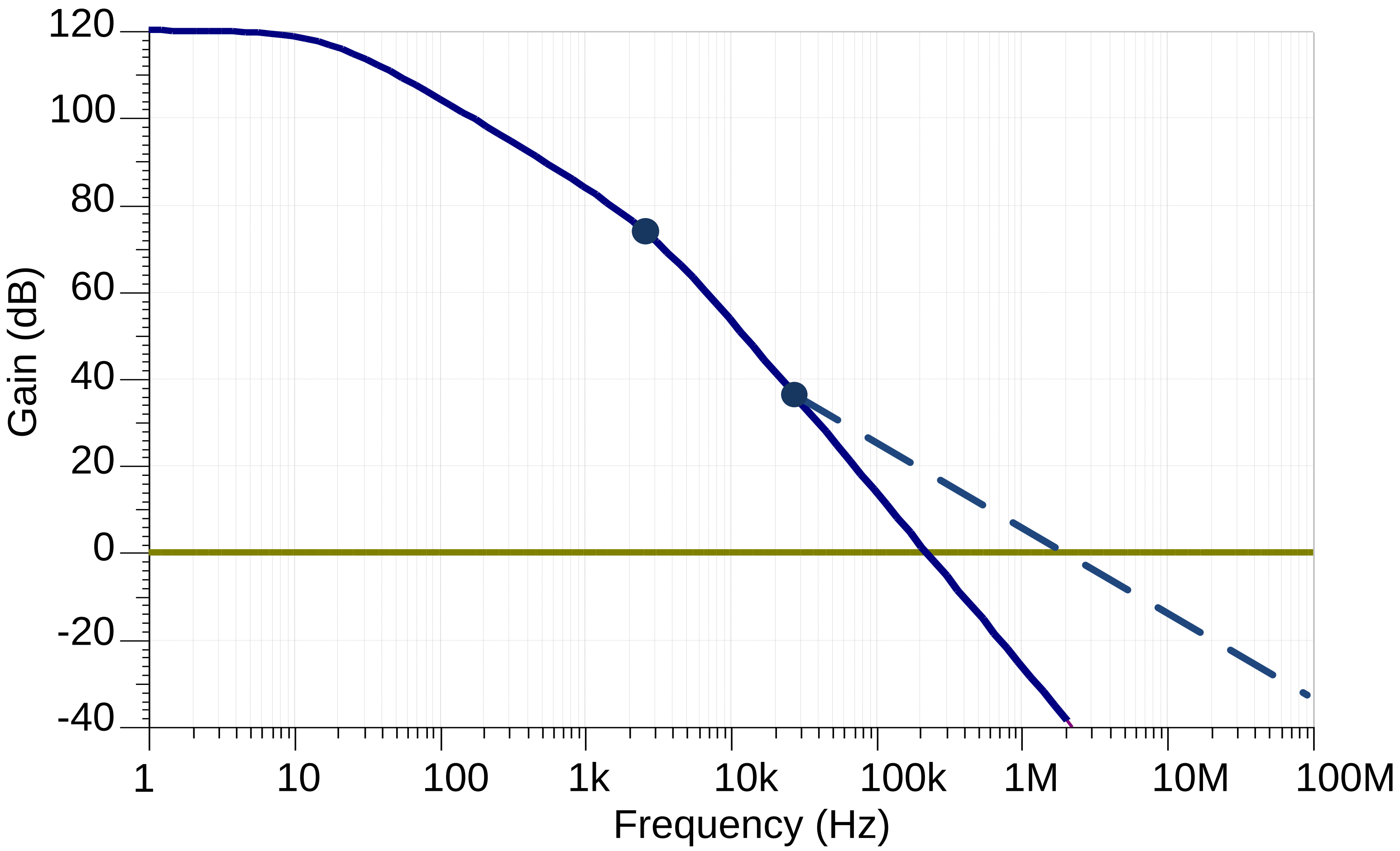
Capacitive Loads – Unity Gain Buffers - Theory



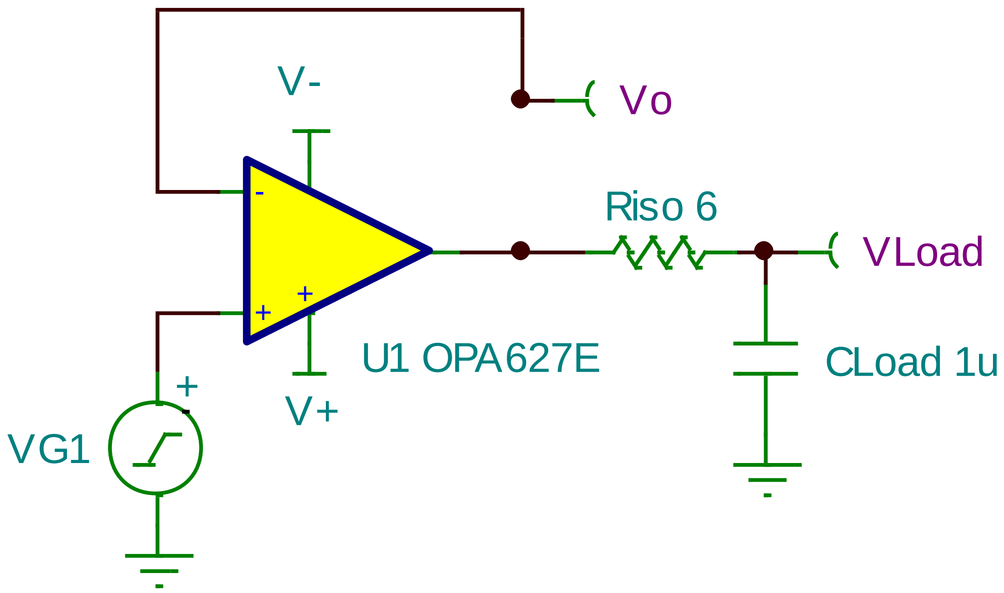
Stabilize Capacitive Loads – Unity Gain Buffers

Stability Options

Unity-Gain circuits can only be stabilized by modifying the AOL load

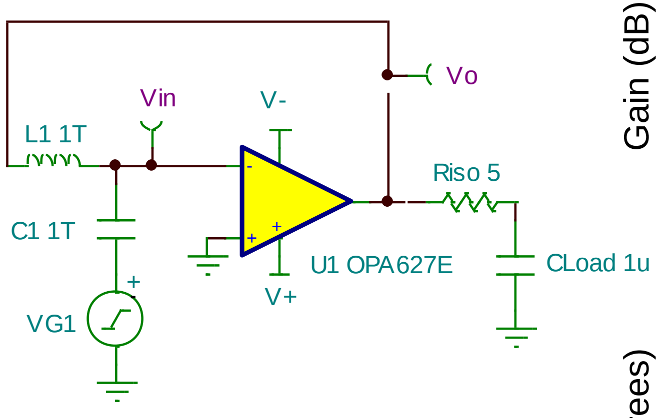


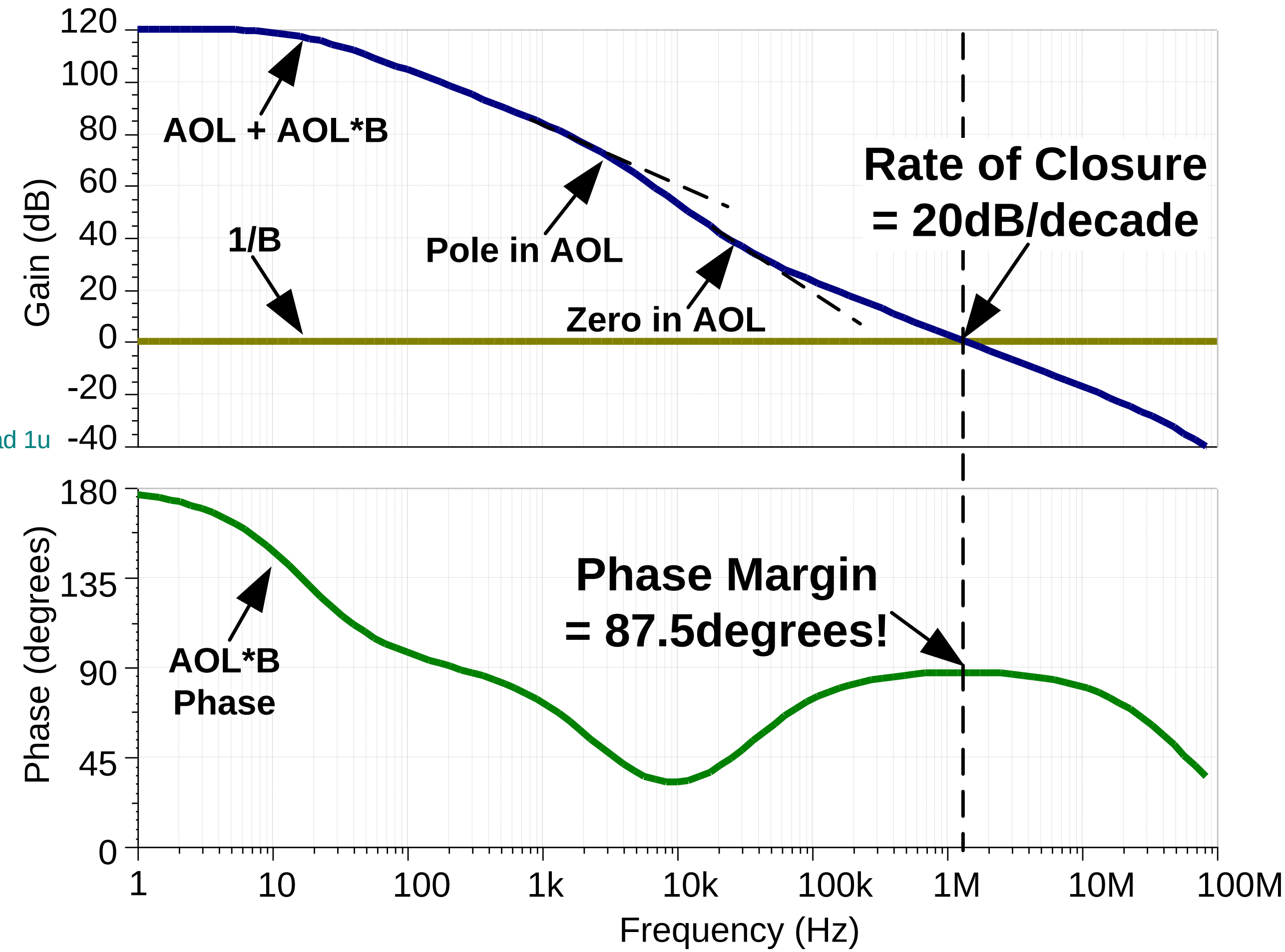
Method 1: Riso



Method 1: Riso - Results

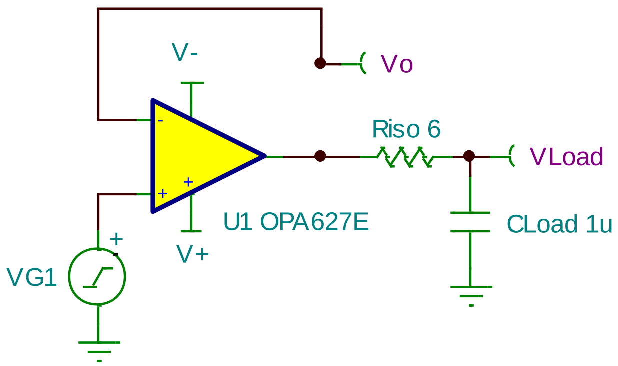
<u>Theory:</u> Adds a zero to the Loaded AOL response to cancel the pole

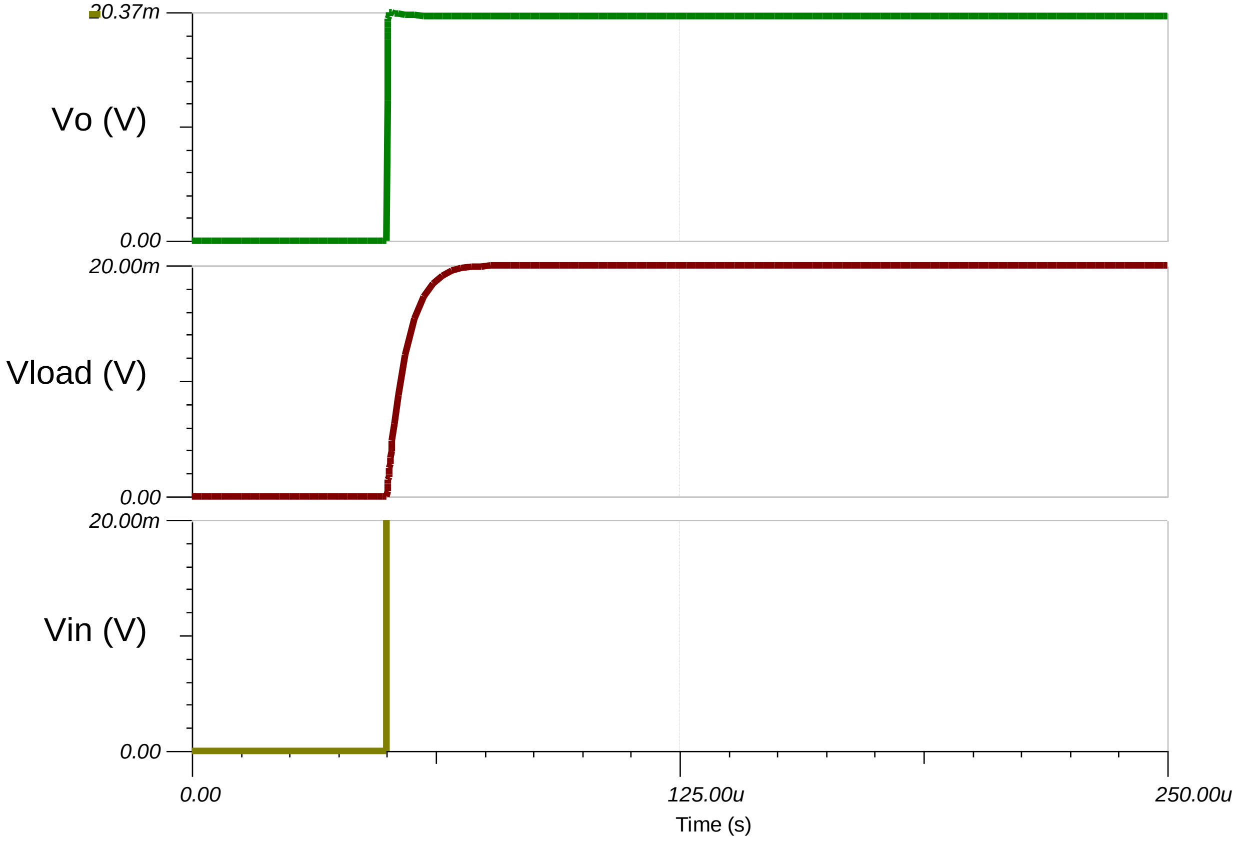




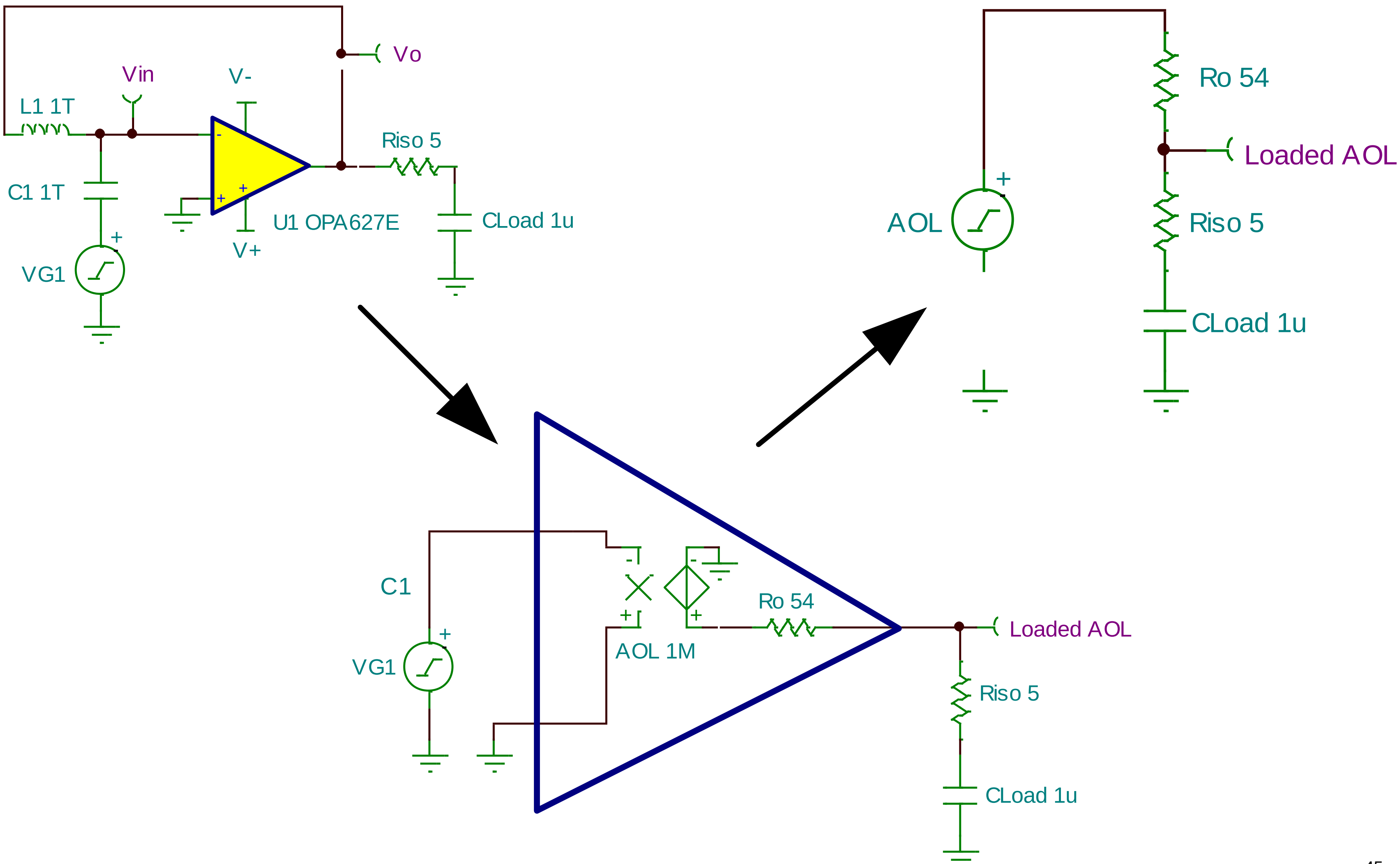
Method 1: Riso - Results

<u>When to use:</u> Works well when DC accuracy is not important, or when loads are very light

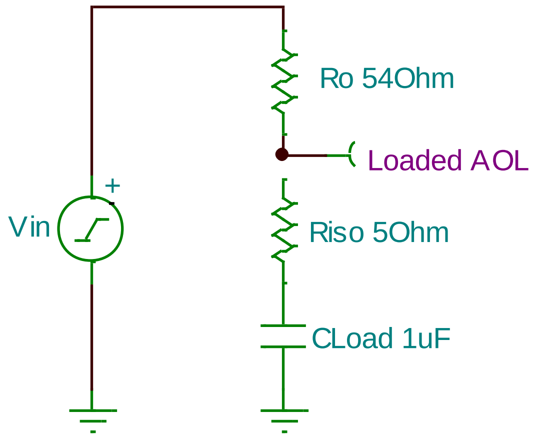


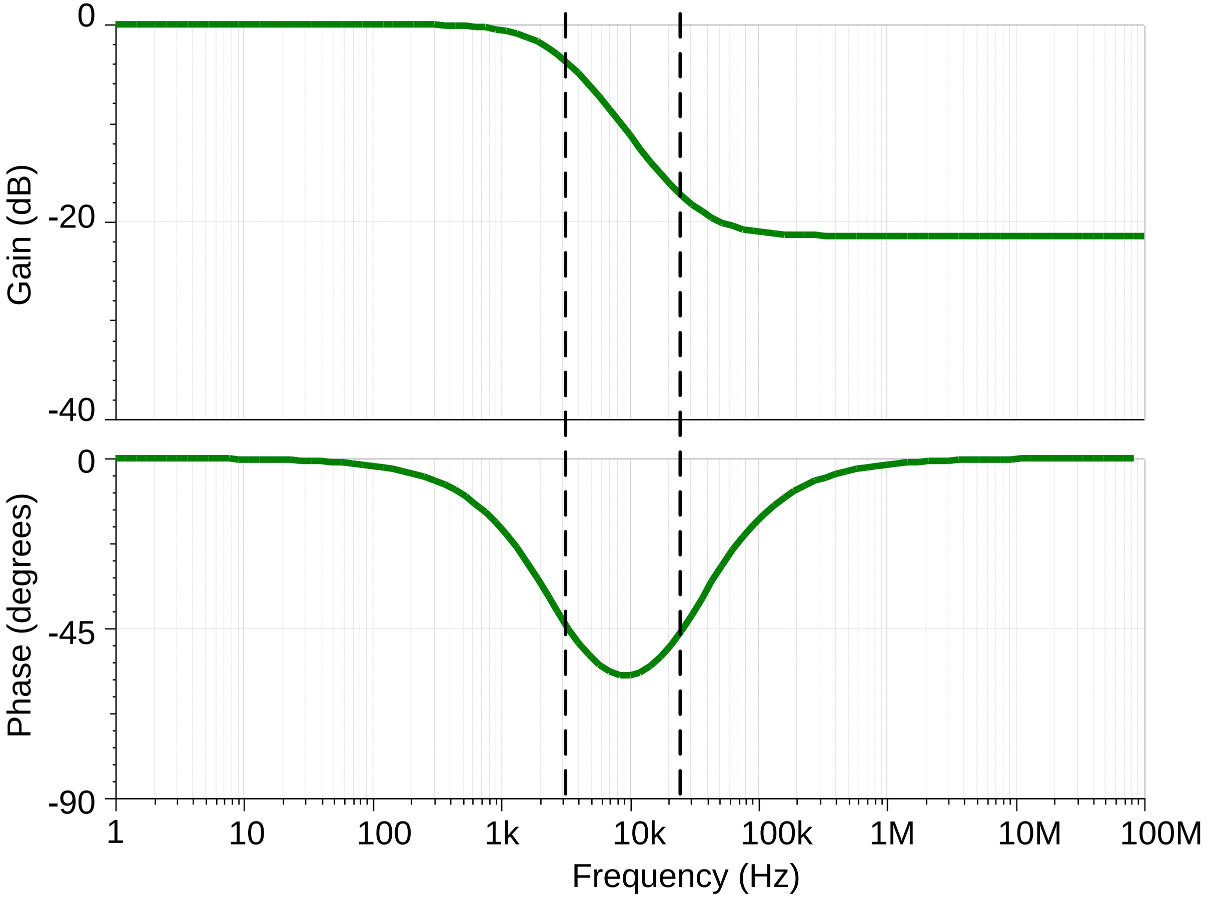


Method 1: Riso - Theory



Method 1: Riso - Theory





Transfer function:

$$\text{Loaded AOL}(s)=\frac{1+C_{Load}\cdot R_{iso}\cdot s}{1+(R_o+R_{iso})\cdot C_{Load}\cdot s}$$

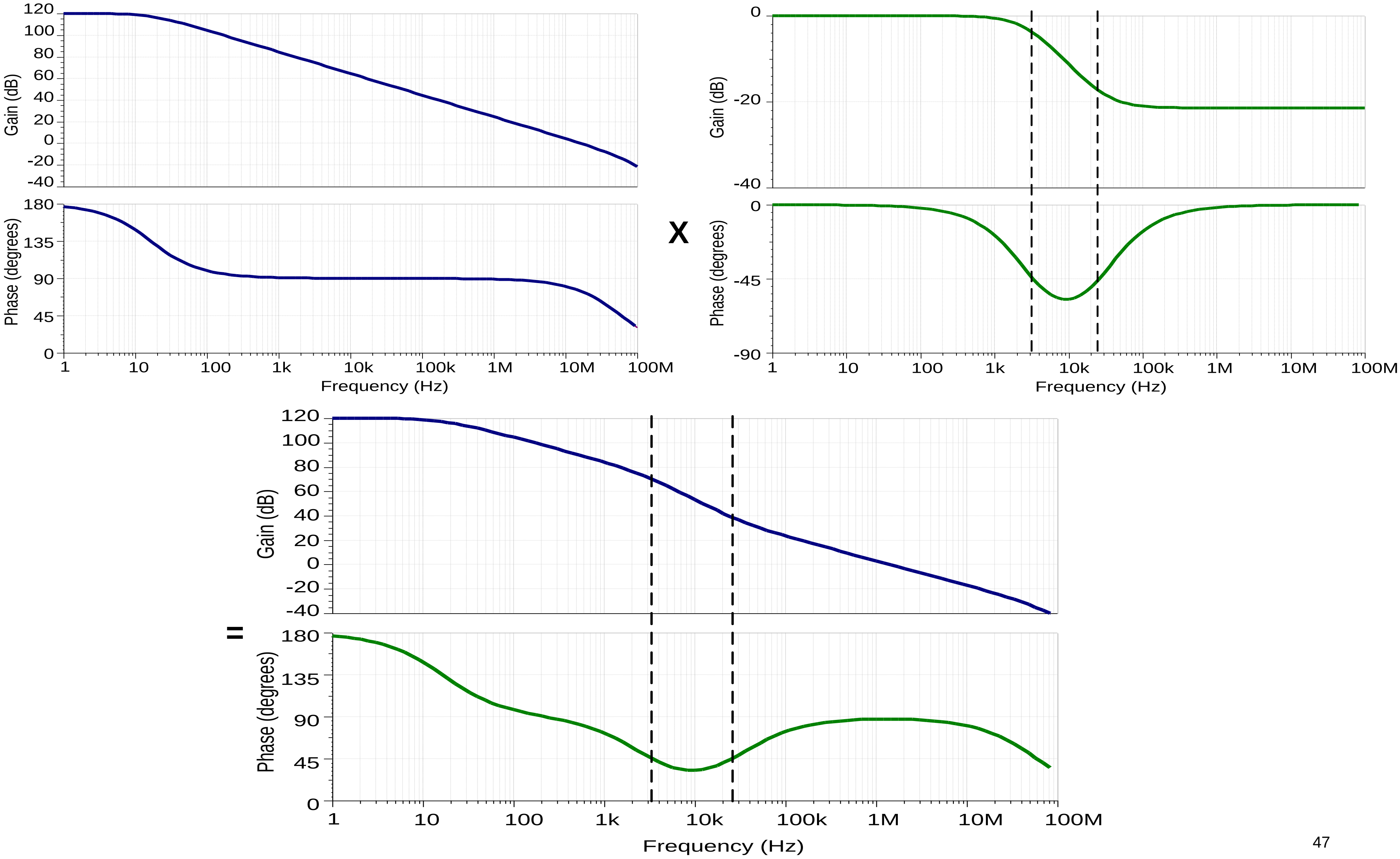
Pole Equation:

$$f(\text{pole})=\frac{1}{2\cdot pi\cdot(R_o+R_{iso})\cdot C_{Load}\cdot s}$$

Zero Equation:

$$f(\text{zero})=\frac{1}{2\cdot pi\cdot R_{iso}\cdot C_{Load}\cdot s}$$

Method 1: Riso - Theory



Method 1: Riso - Design

Ensure Good Phase Margin:

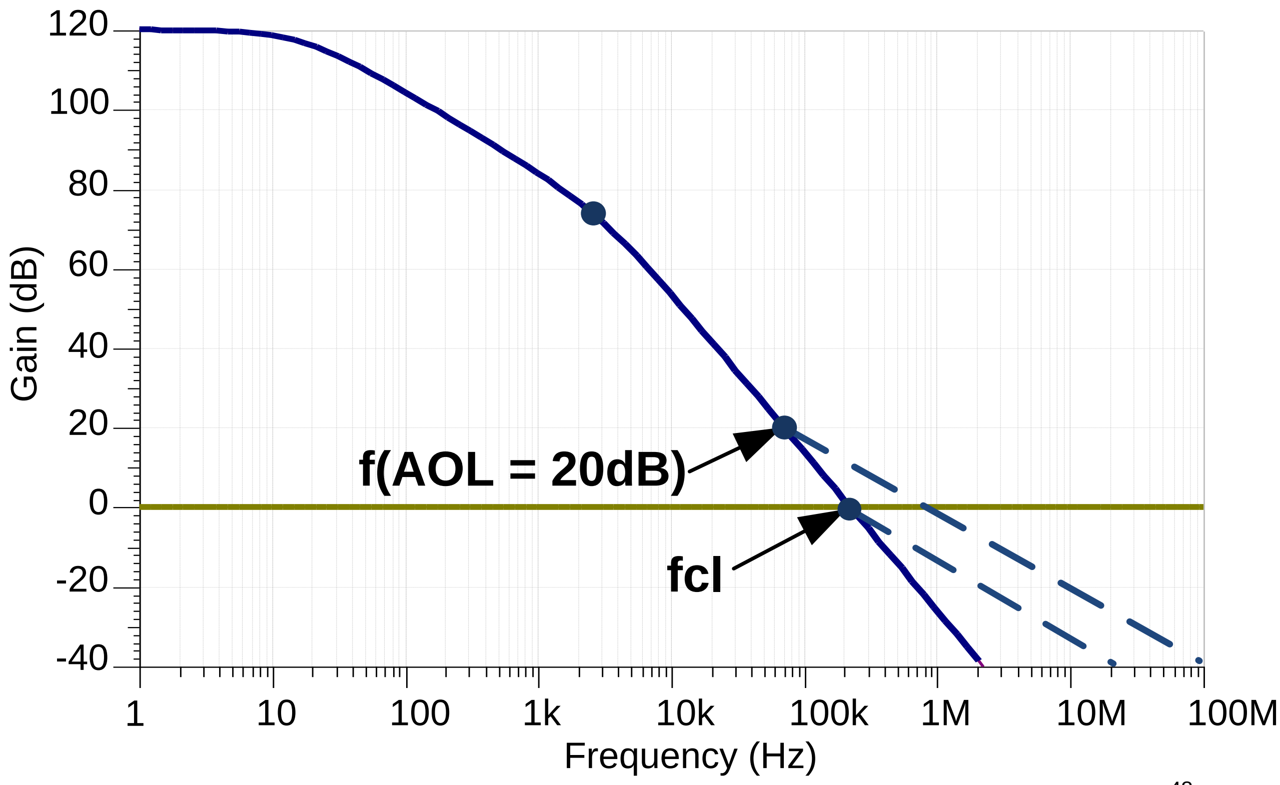
1.) Find: fcl and f(AOL = 20dB)
2.) Set Riso to create AOL zero:
Good: f(zero) = Fcl for PM ≈ 45 degrees.
Better: f(zero) = F(AOL = 20dB) will yield slightly less than 90 degrees phase margin

fcl = 222.74kHz

f(AOL = 20dB) = 70.41kHz

Zero Equation:

$$f(zero) = \frac{1}{2 \cdot pi \cdot R_{iso} \cdot C_{Load} \cdot s}$$



Method 1: Riso - Design

$$f(zero)=\frac{1}{2\cdot pi\cdot R_{iso}\cdot C_{Load}\cdot s}$$

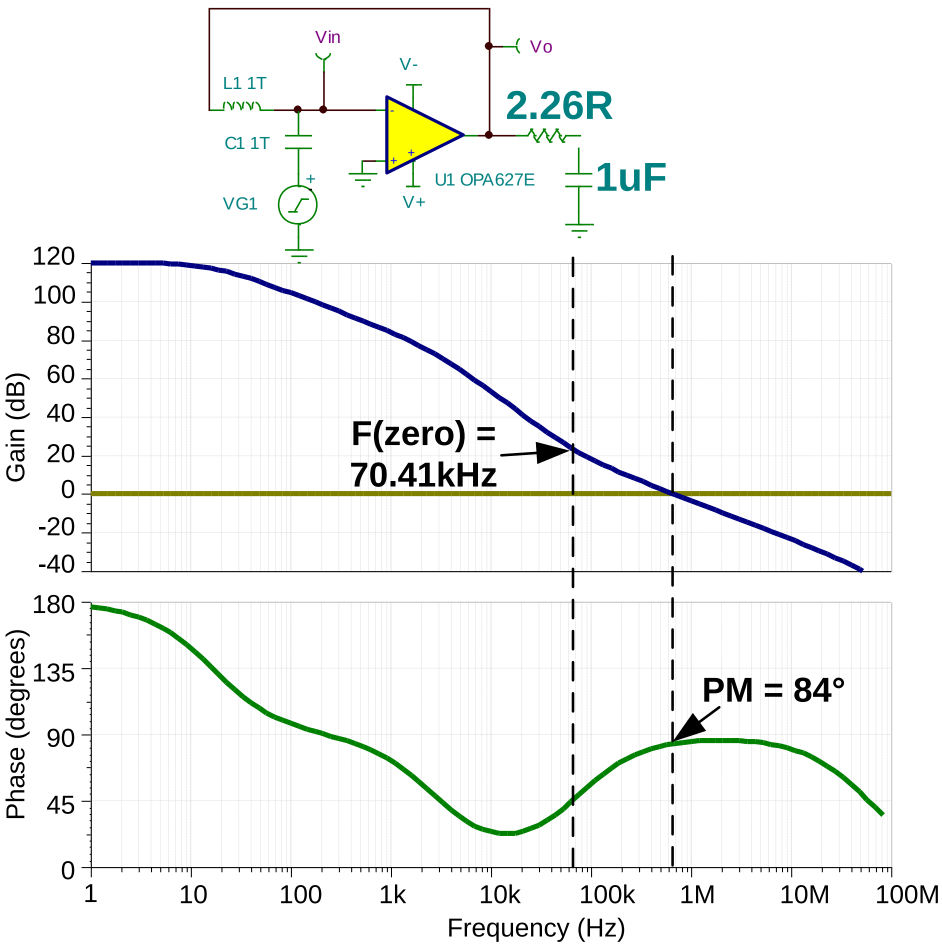
Ensure Good Phase Margin: Test

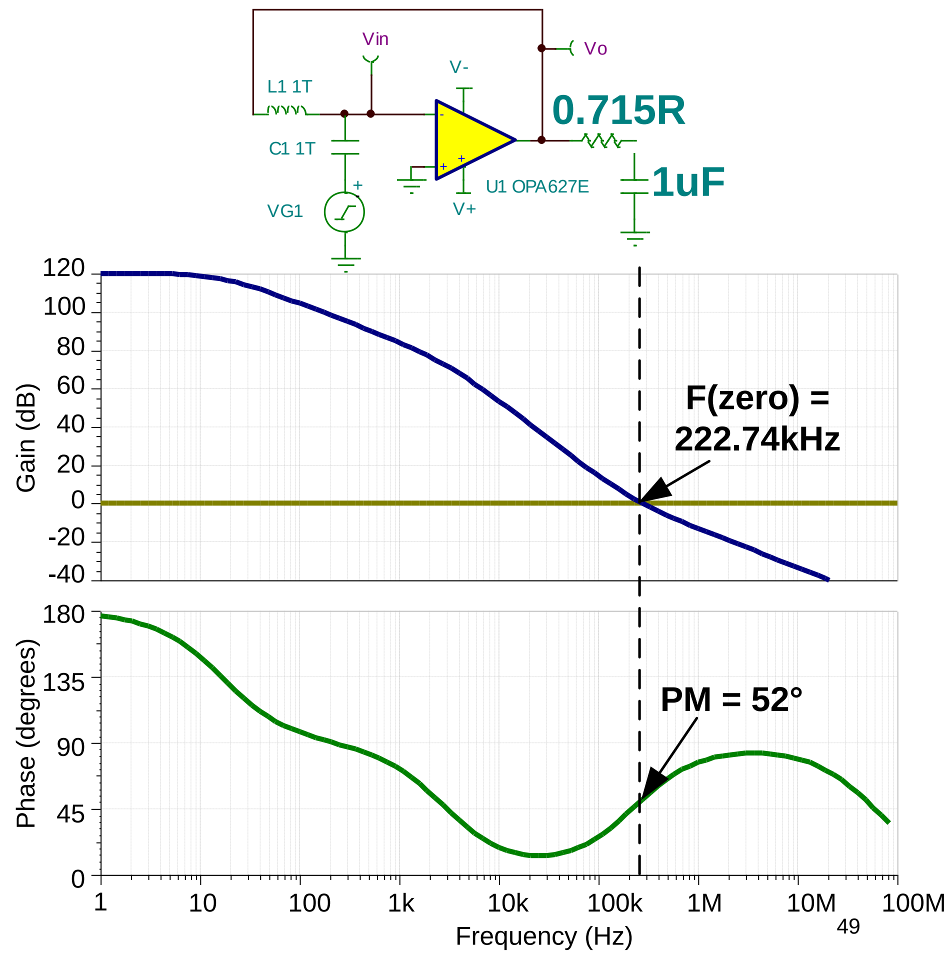
f(AOL = 20dB) = 70.41kHz

→ Riso = 2.26Ohms

fcl = 222.74kHz

→ Riso = 0.715Ohms





Method 1: Riso - Design

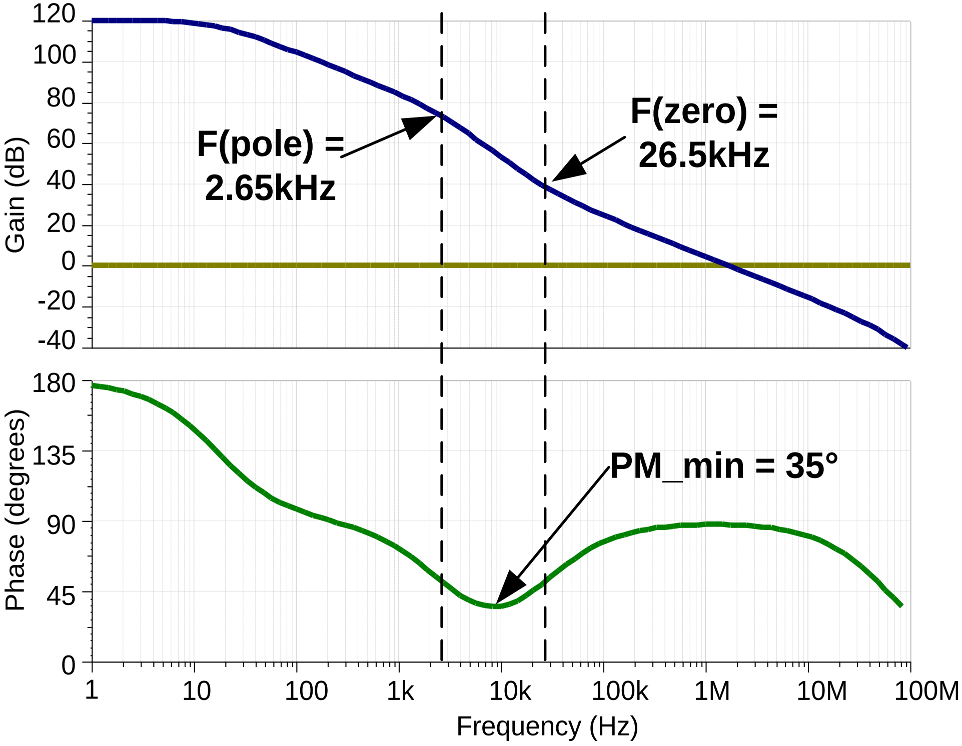
Prevent Phase Dip:

Place the zero less than 1 decade from the pole, no more than 1.5 decades away

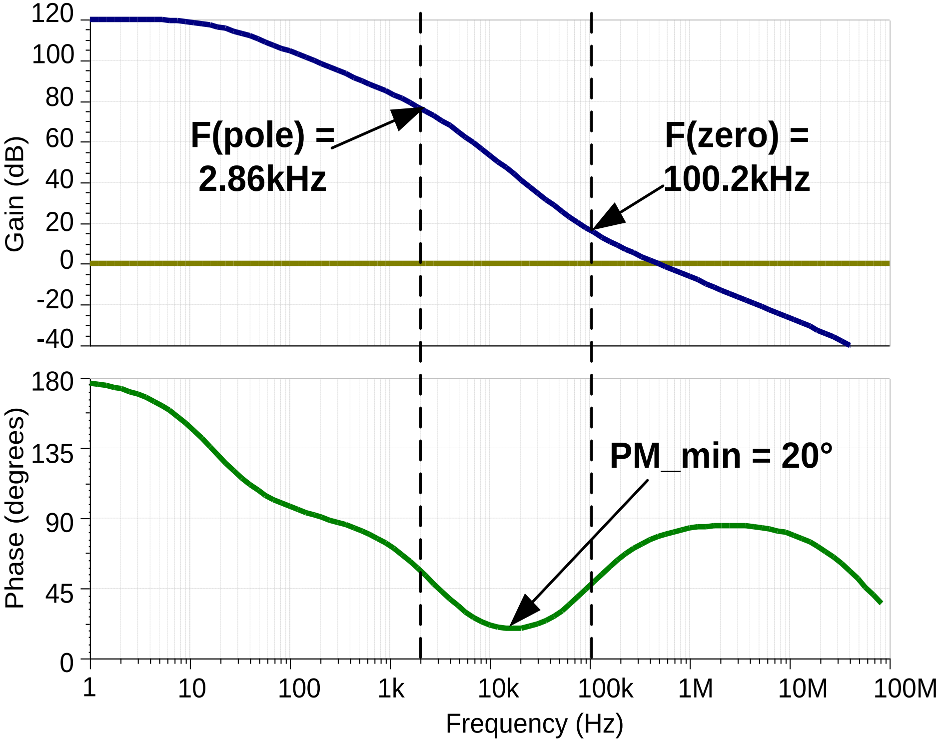
Good: 1.5 Decades: F(zero) ≤ 35*F(pole) → Riso ≥ Ro/34 → 70° Phase Shift

Better: 1 Decade: F(zero) ≤ 10*F(pole) → Riso ≥ Ro/9 → 55° Phase Shift

Riso = Ro/9



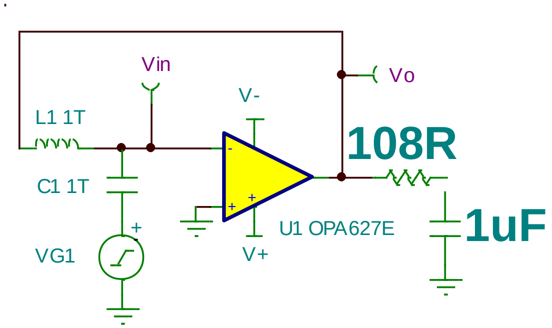
Riso = Ro/34



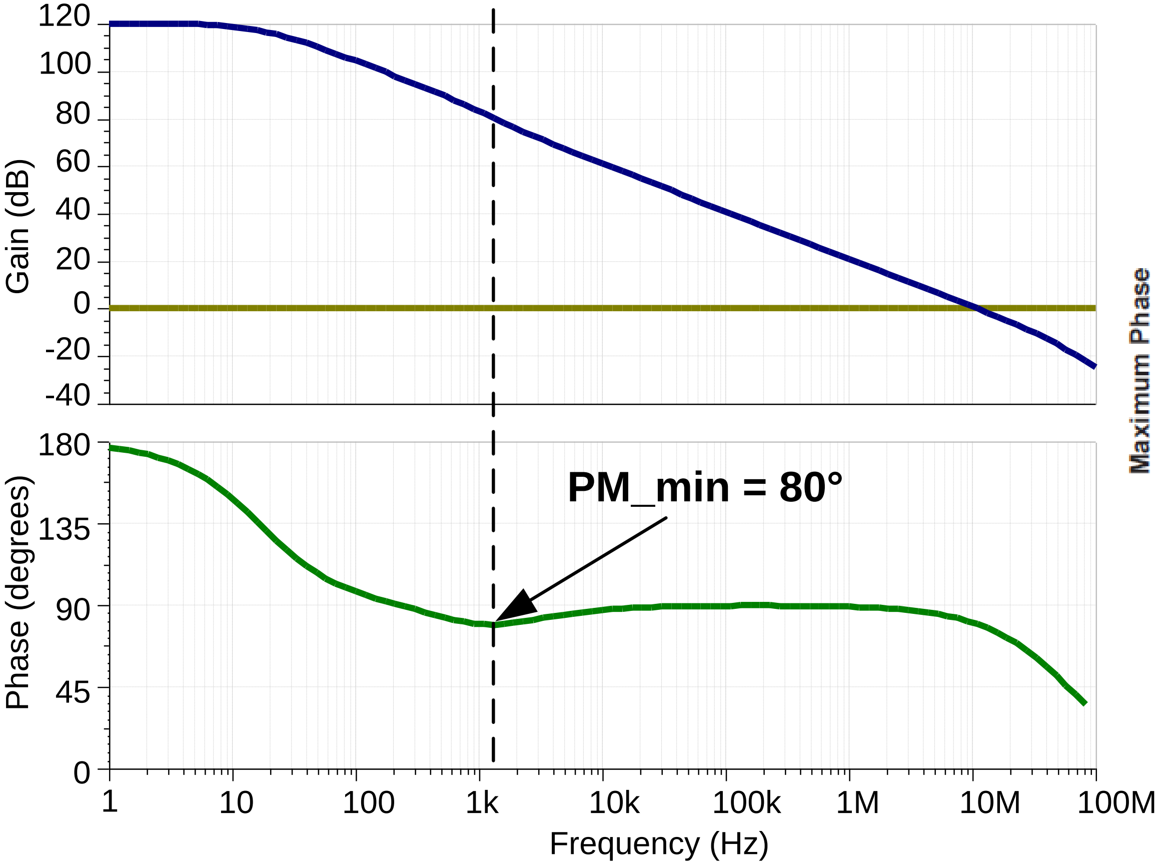
Method 1: Riso - Design

<u>Prevent Phase Dip: Ratio of Riso to Ro</u>

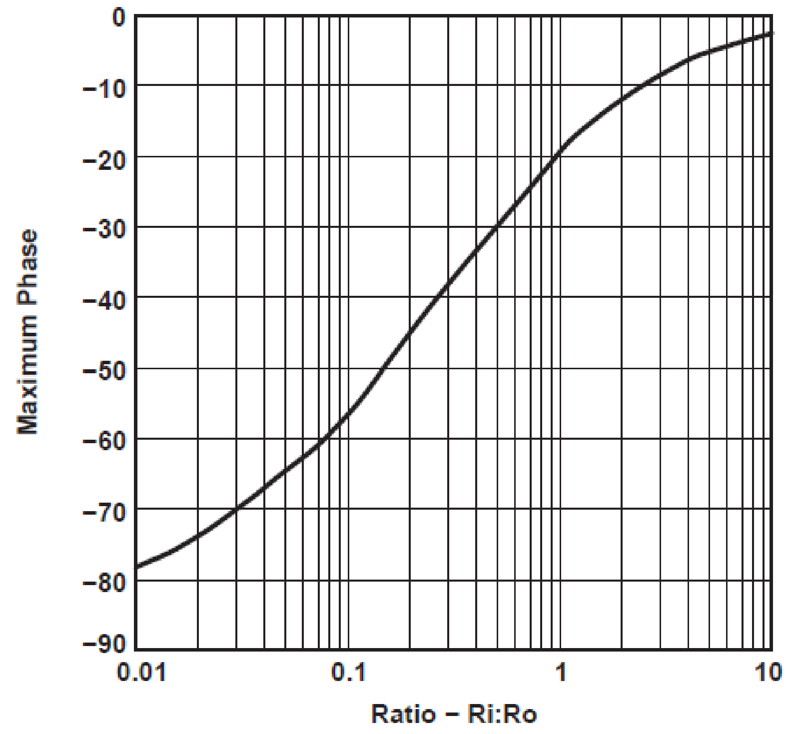
If Riso ≥ 2*Ro → F(zero) = 1.5*F(pole) → ~10° Phase Shift
**Almost completely cancels the pole.



Riso = Ro*2



Phase Shift vs. Riso/Ro

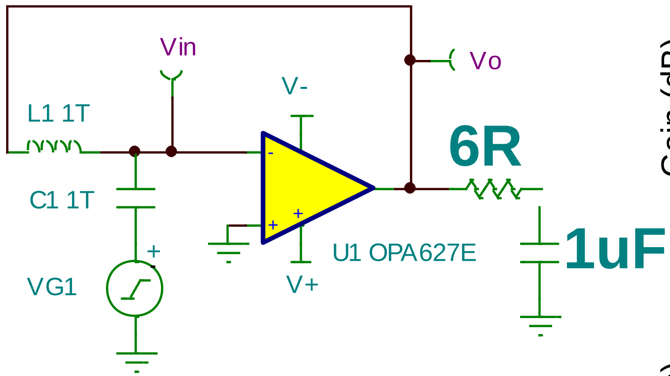


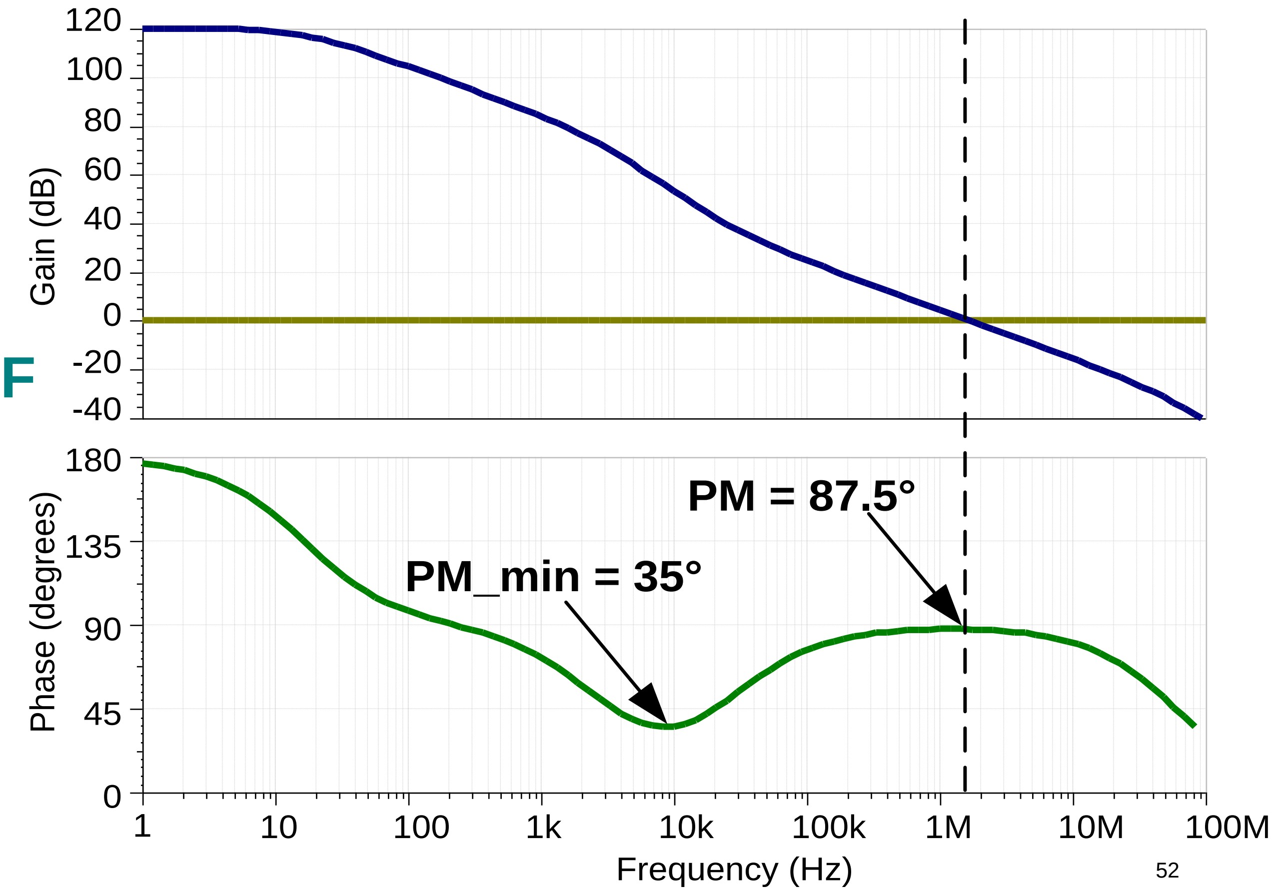
Method 1: Riso – Design Summary

Summary:

1.) Ensure stability by placing Fzero ≤ F(AOL=20dB)
2.) If Fzero is > 1.5 decades from F(pole) then increase Riso up to at least Ro/34
3.) If loads are very light consider increasing Riso > Ro for stability across all loads

Final Circuit

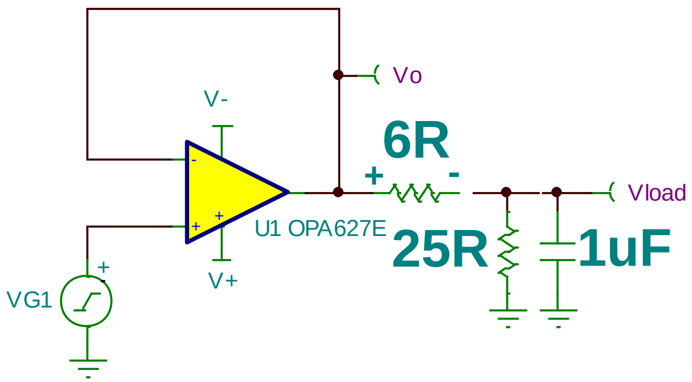


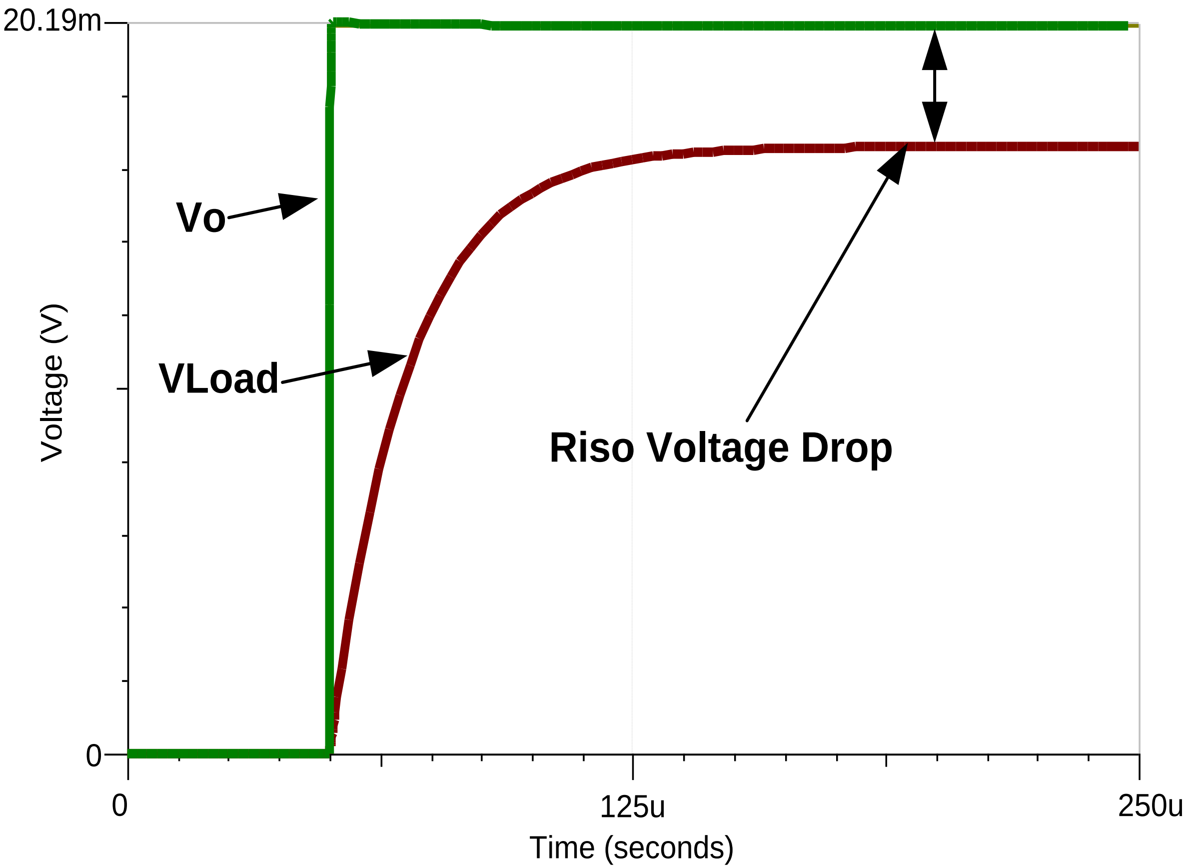


Method 1: Riso - Disadvantage

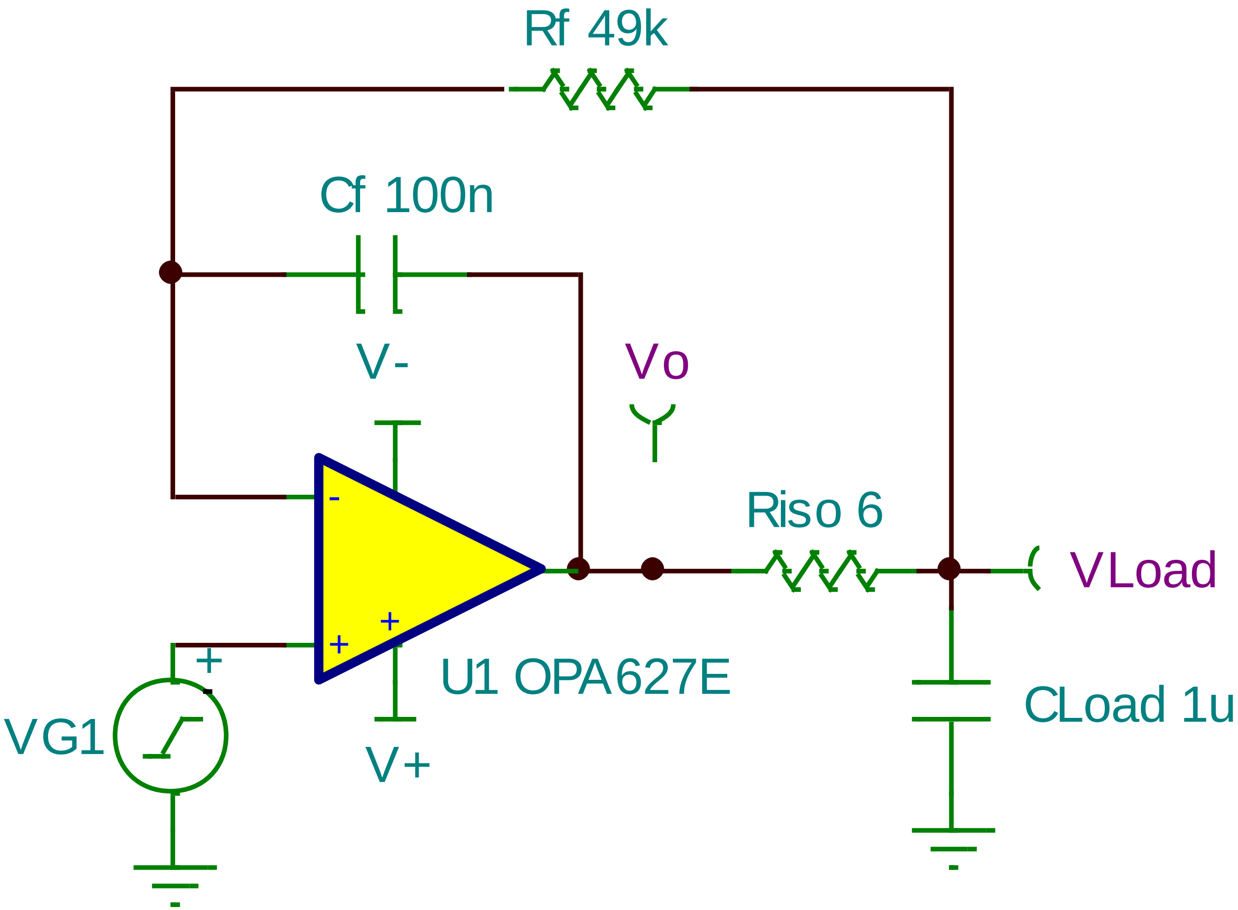
Disadvantage:

Voltage drop across Riso may not be acceptable



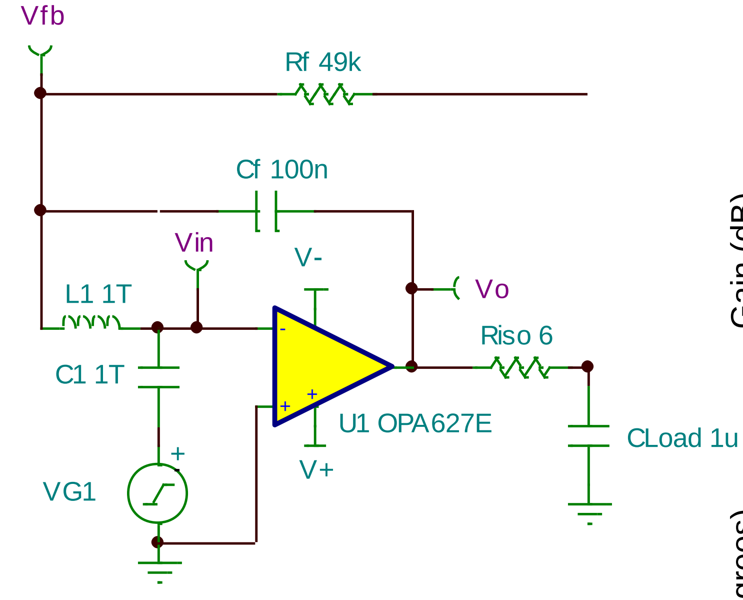


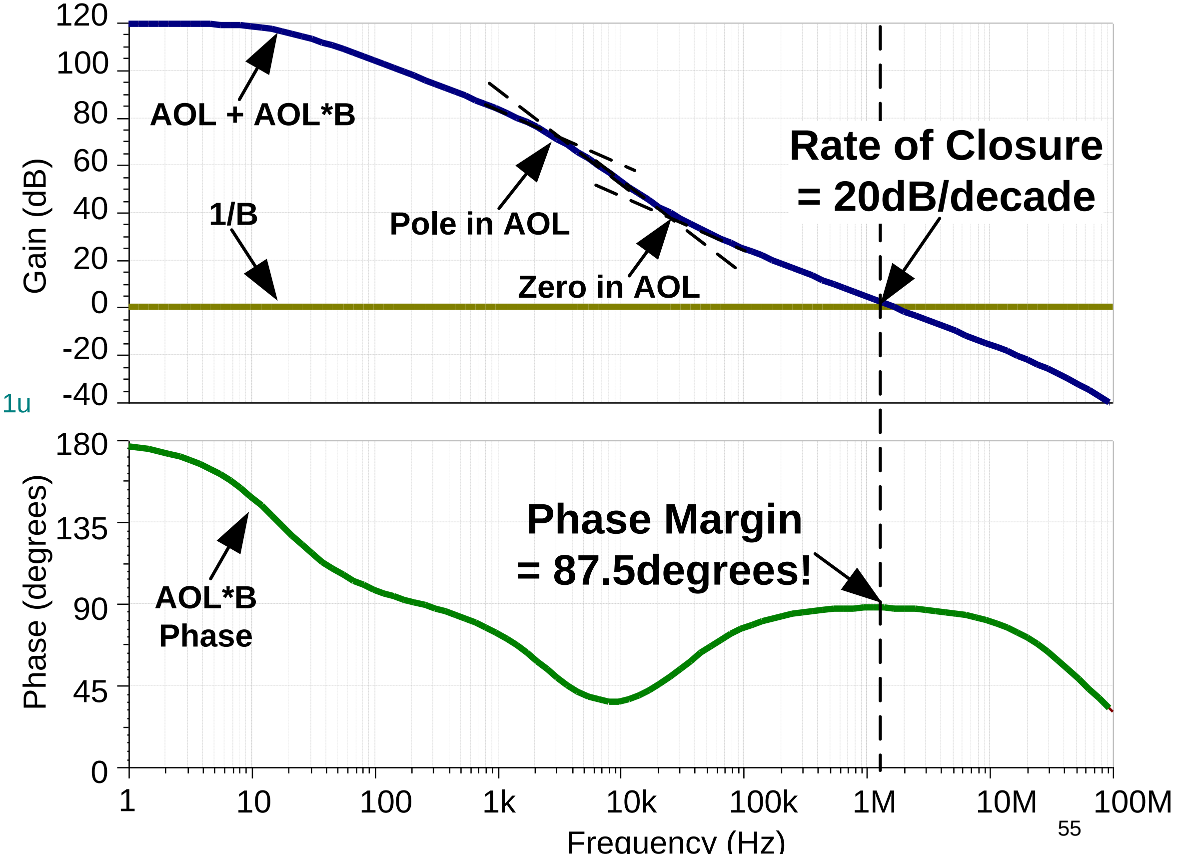
Method 2:
Riso + Dual Feedback



Method 2: Riso + Dual Feedback

<u>Theory:</u> Features a low-frequency feedback to cancel the Riso drop and a high-frequency feedback to create the AOL pole and zero.

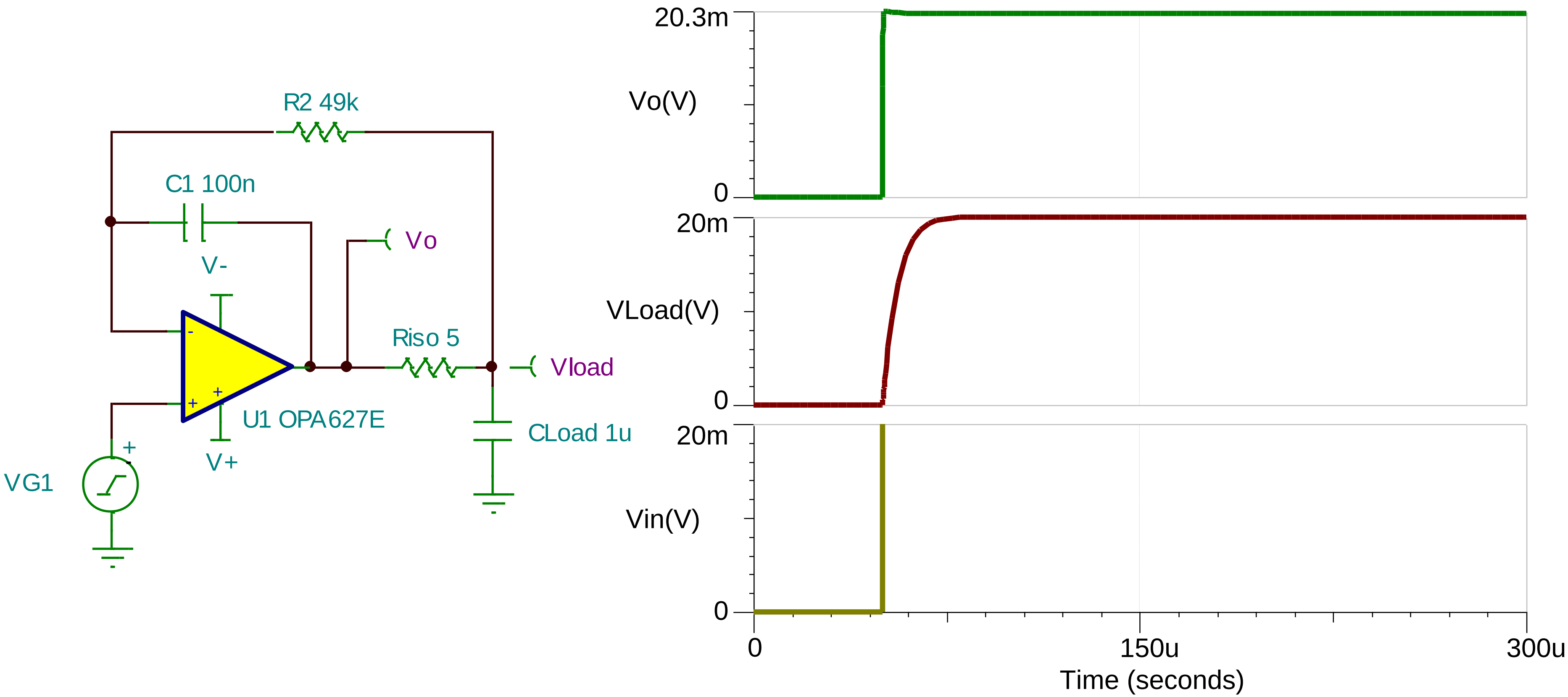




Method 2: Riso + Dual Feedback

<u>When to Use:</u> **Only practical solution for very large capacitive loads ≥ 10uF**

When DC accuracy must be preserved across different current loads



Method 2: Riso + Dual Feedback - Design

Ensure Good Phase Margin:

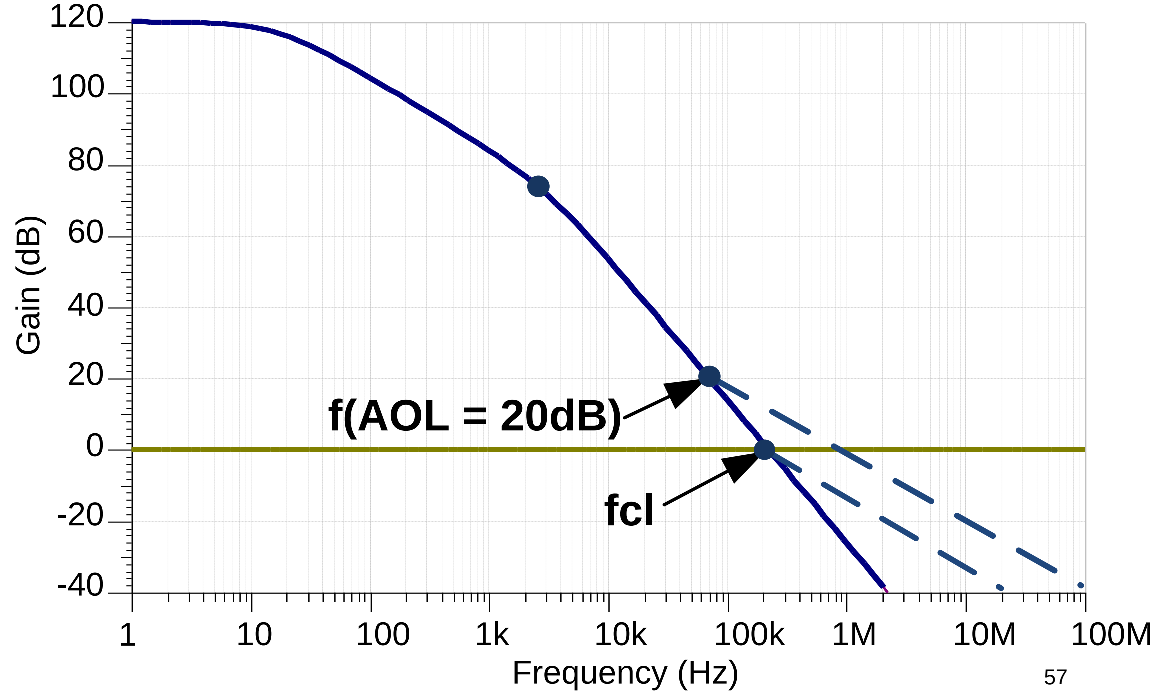
1.) Find: fcl and f(AOL = 20dB)
2.) Set Riso to create AOL zero:
    Good: f(zero) = Fcl for PM ≈ 45 degrees.
    Better: f(zero) = F(AOL = 20dB) will yield slightly less than 90 degrees phase margin
3.) Set Rf so Rf >>Riso
    Rf ≥ (Riso * 100)
4.) Set Cf ≥ (200*Riso*Cload)/Rf

fcl = 222.74kHz

f(AOL = 20dB) = 70.41kHz

Zero Equation:

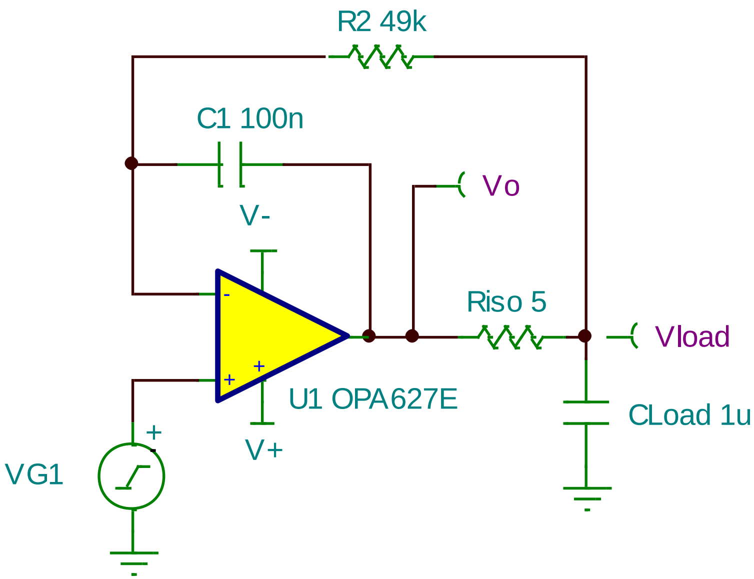
$$f(zero)=\frac{1}{2\cdot pi\cdot R_{iso}\cdot C_{Load}\cdot s}$$

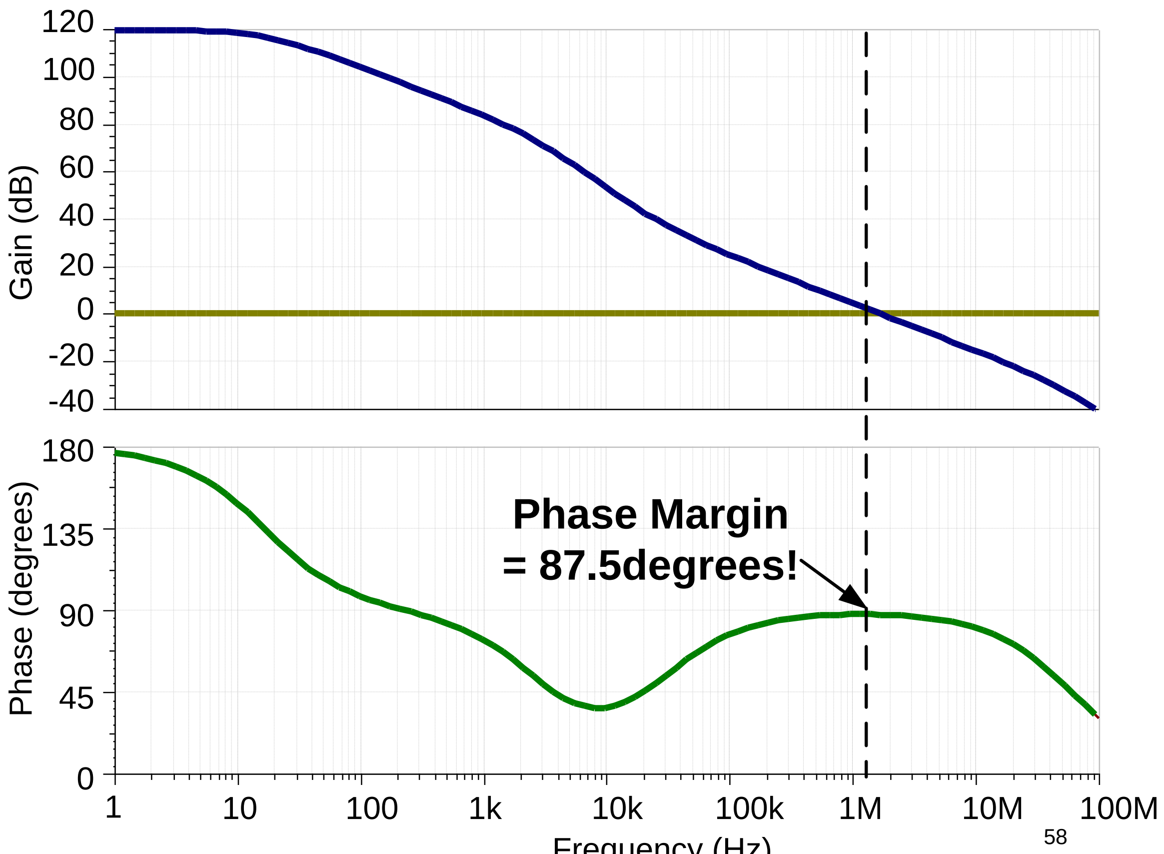


Method 2: Riso + Dual Feedback - Summary

<u>Ensure Good Phase Margin (Same as "Riso" Method):</u>

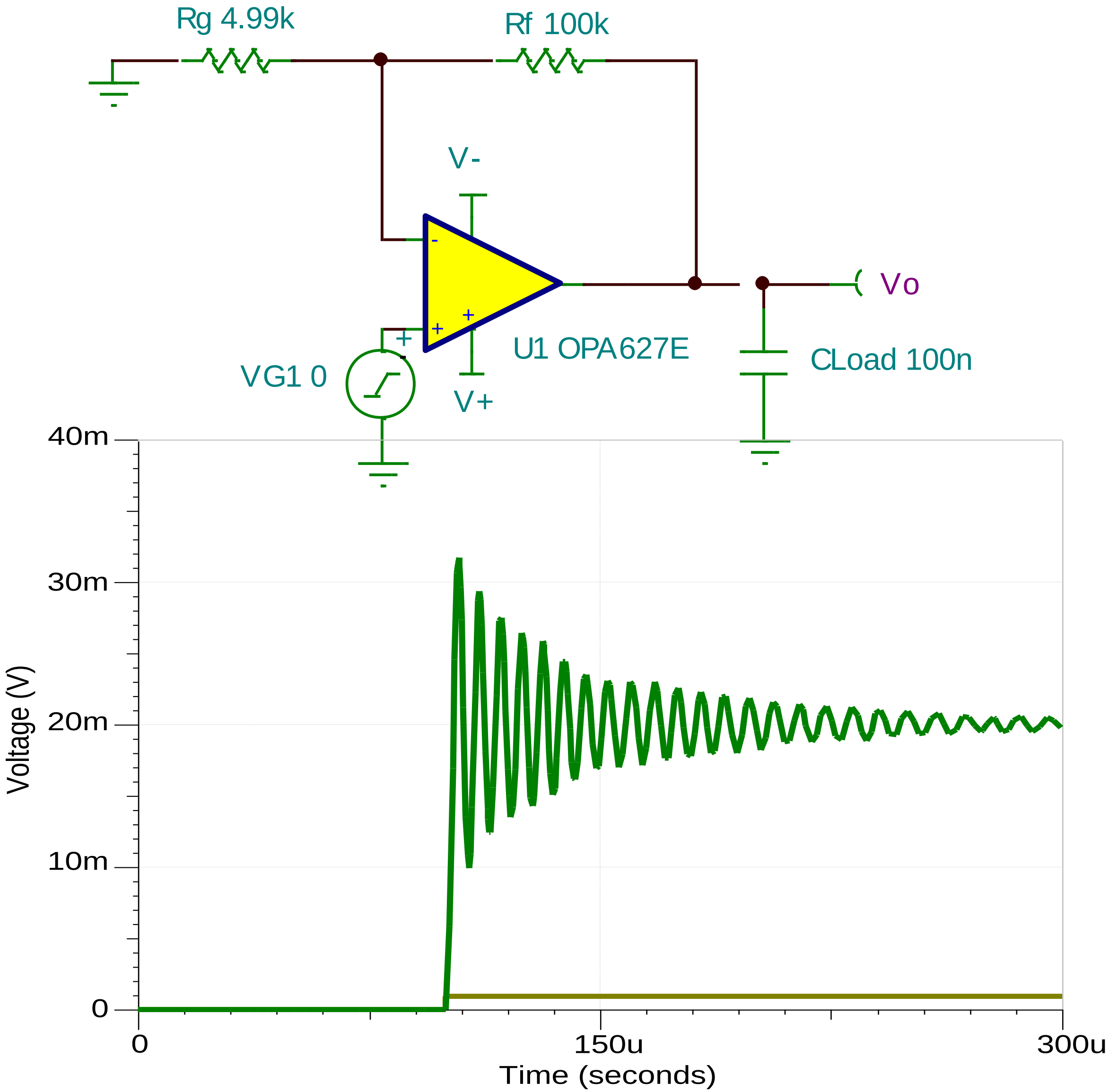
1.) Set Riso so f(zero) = F(AOL = 20dB)
2.) Set Rf: Rf ≥ (Riso * 100)
3.) Set Cf: Cf ≥ (200*Riso*Cload)/Rf





Capacitive Loads – Circuits with Gain

Capacitive Loads – Circuits with Gain



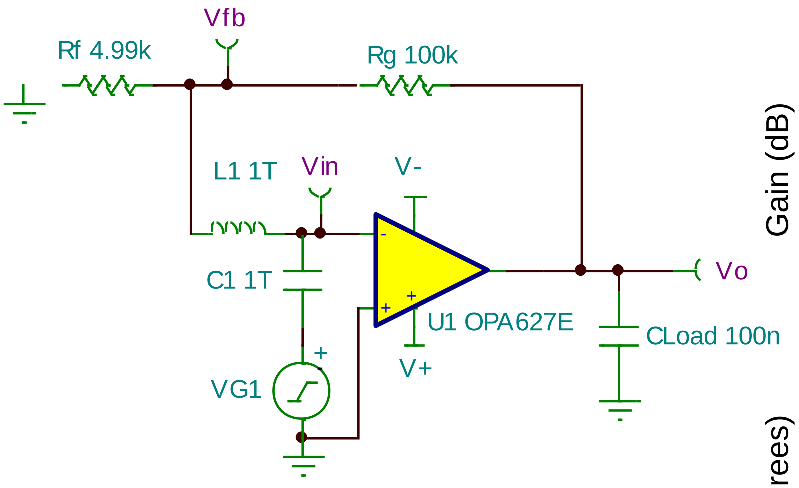
Capacitive Loads – Circuits With Gain - Results

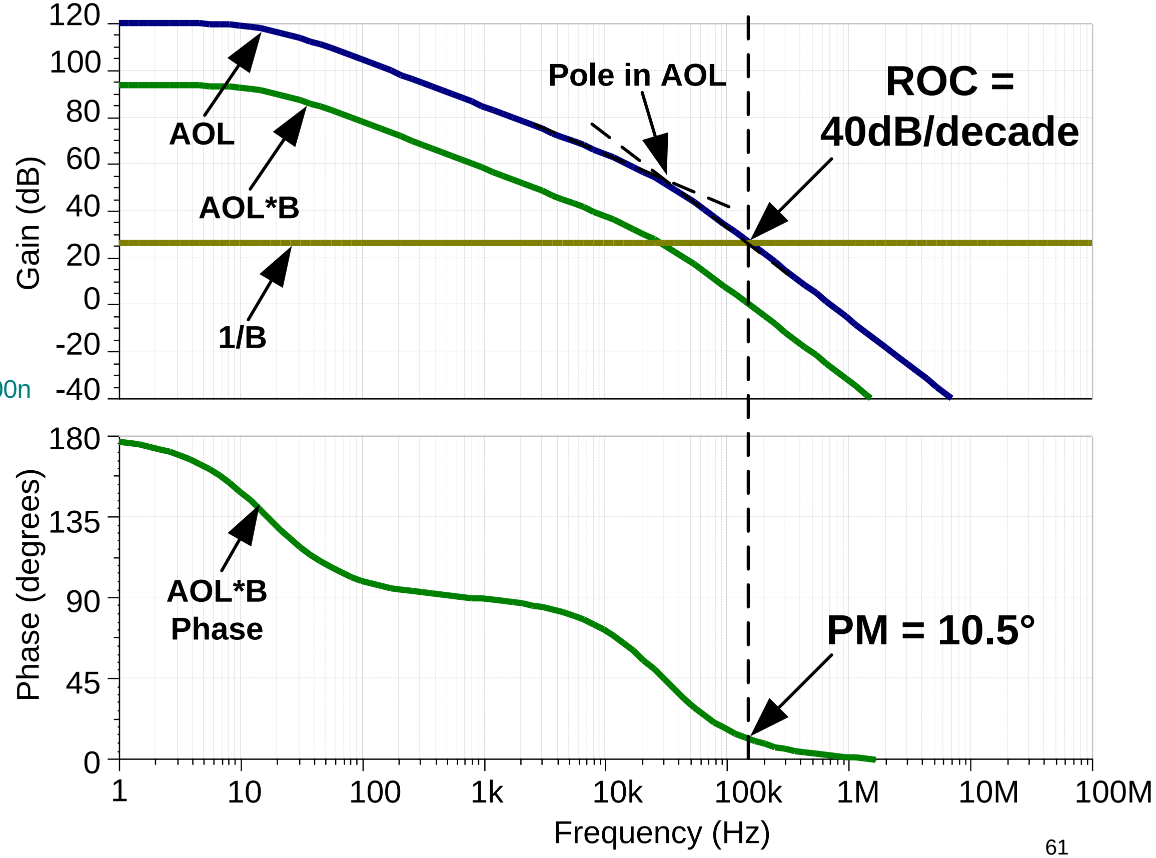
<u>Same Issues as Unity Gain Circuit</u>

Pole in AOL!!

ROC = 40dB/decade!!

Phase Margin = 10°!!

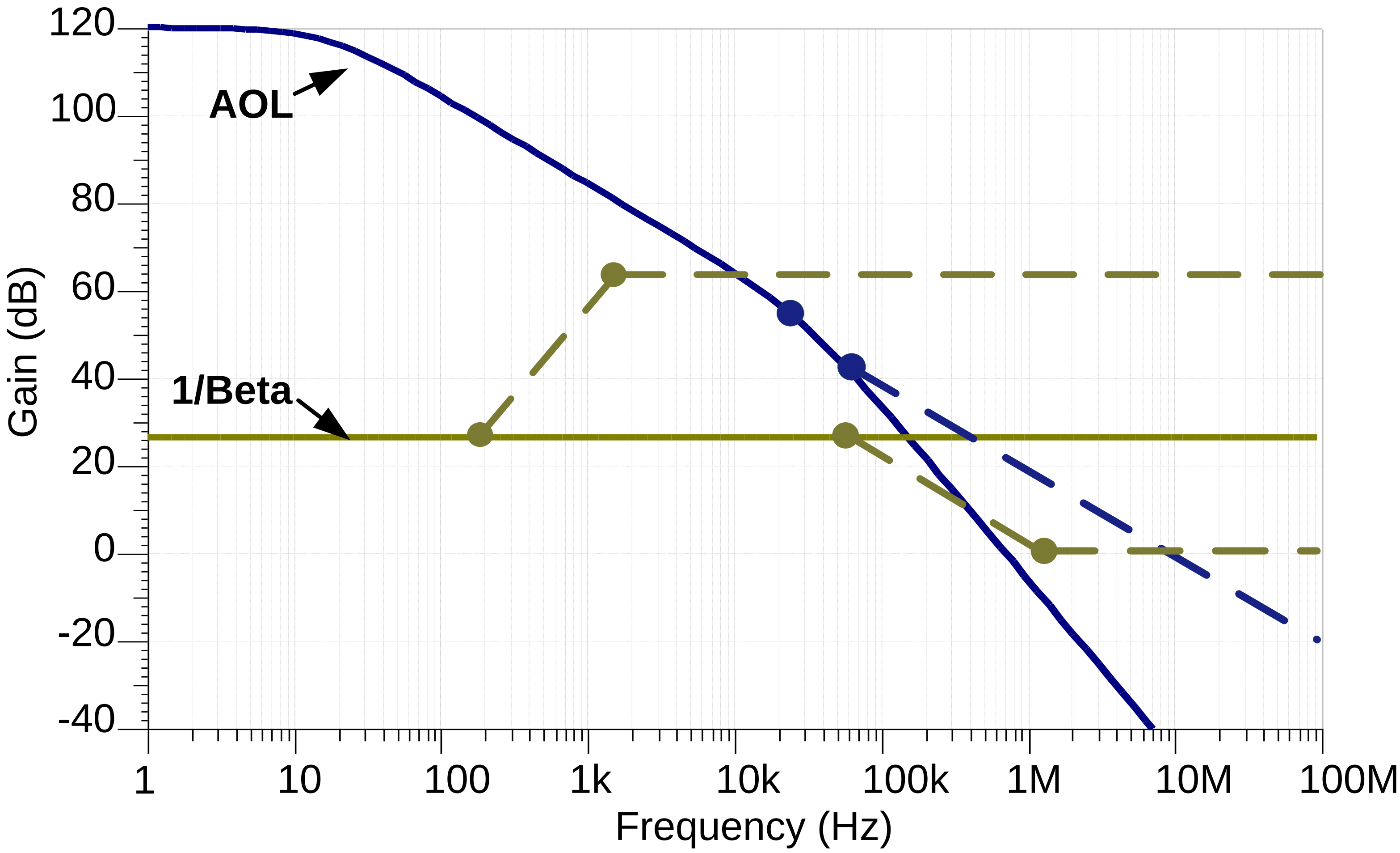




Stabilize Capacitive Loads – Circuits with Gain

Stability Options – Circuits with Gain

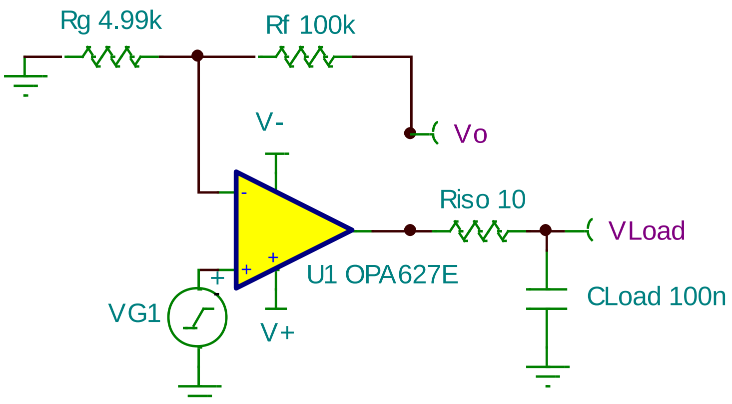
Circuits with gain can be stabilized by modifying the AOL load and by modifying 1/Beta

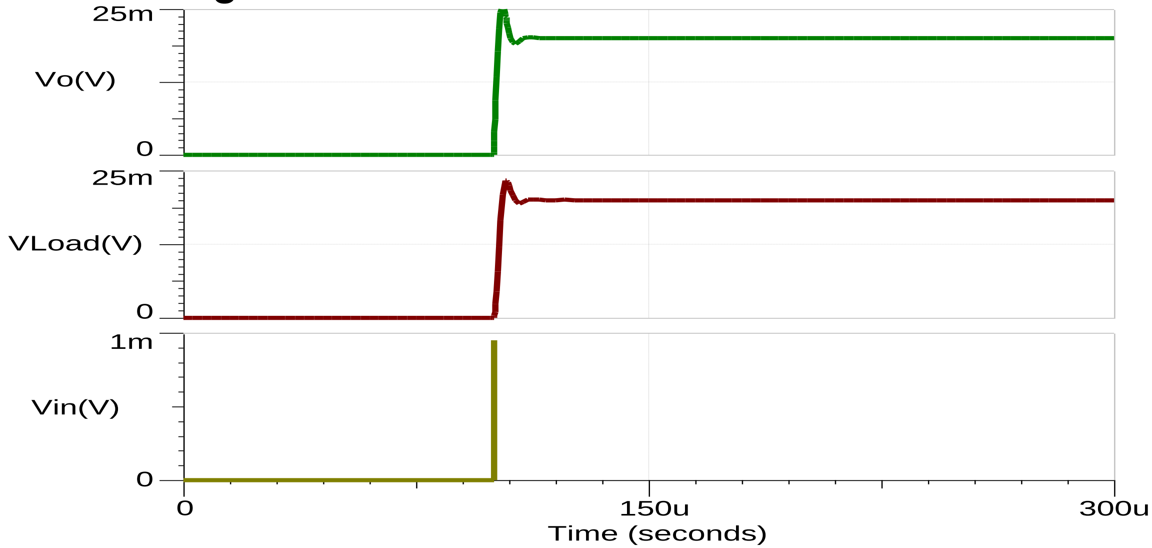


Method 1 + Method 2

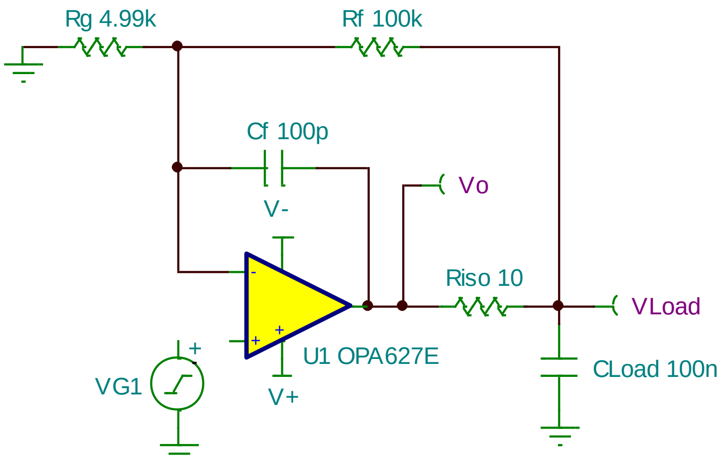
Methods 1 and 2 work on circuits with gain as well!

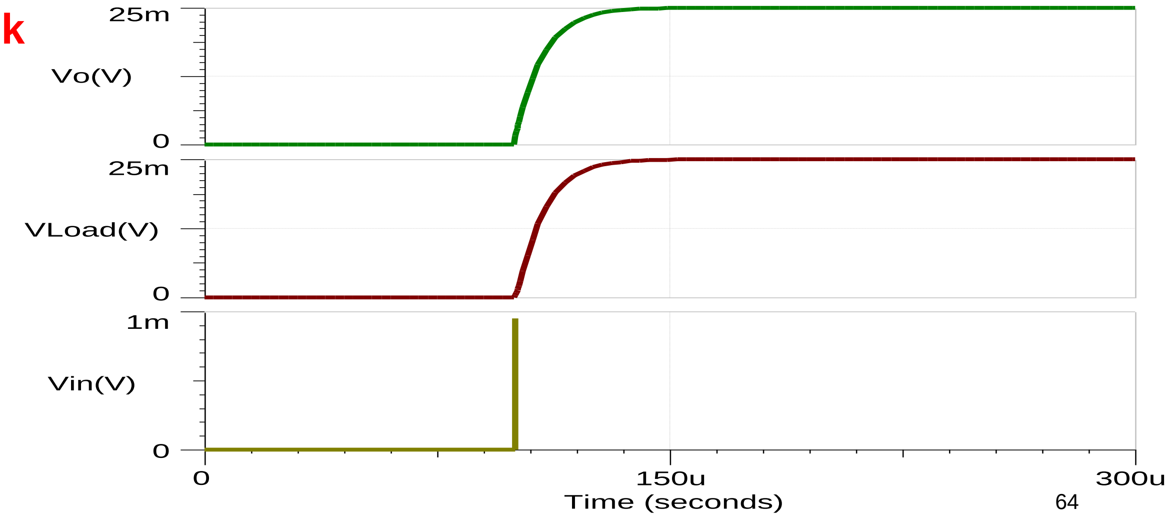
Method 1: Riso



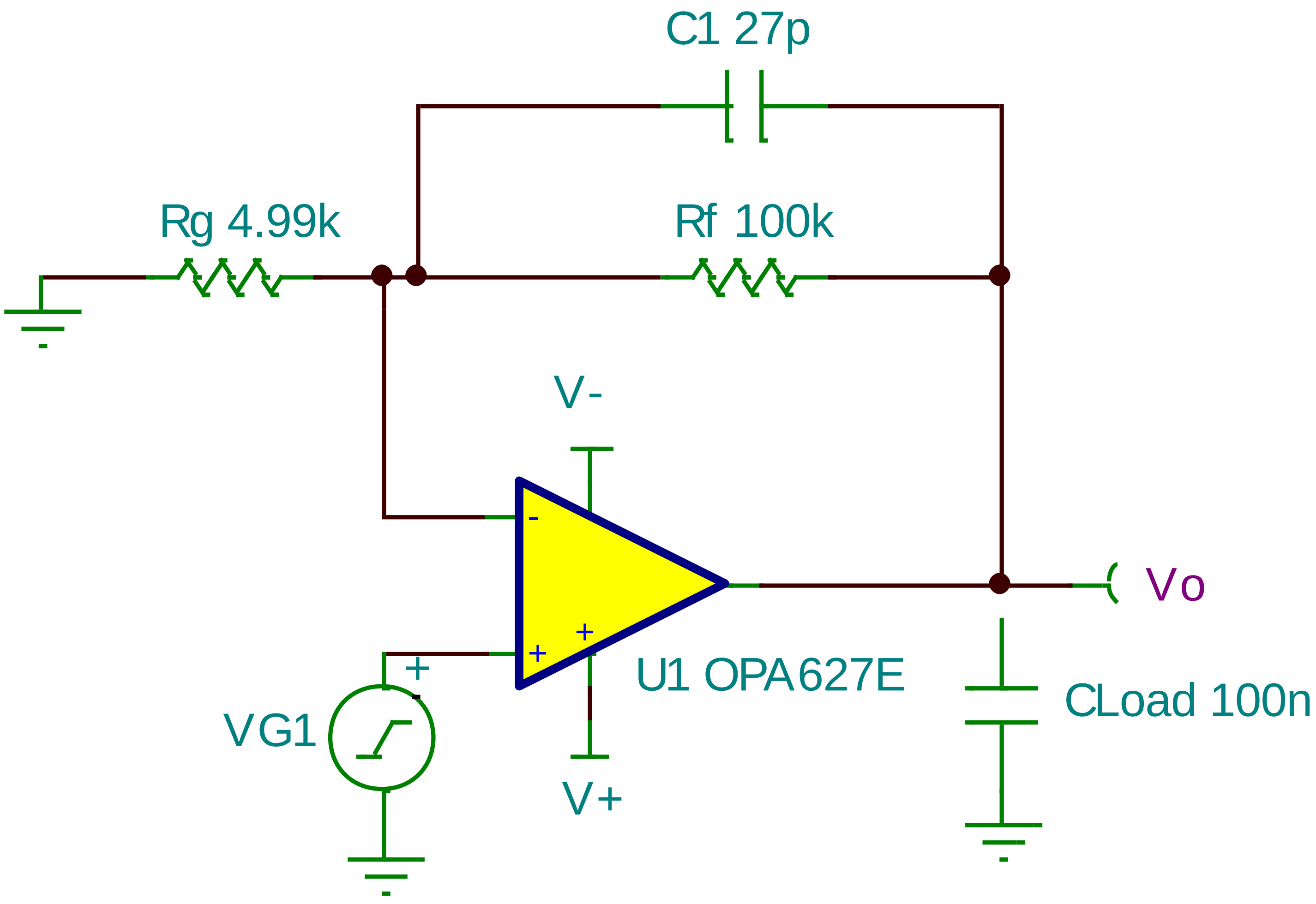


Method 2: Riso+Dual Feedback



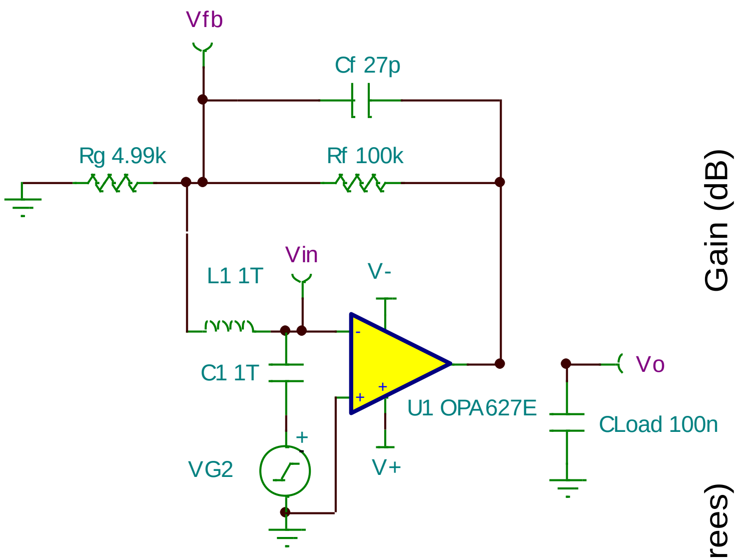


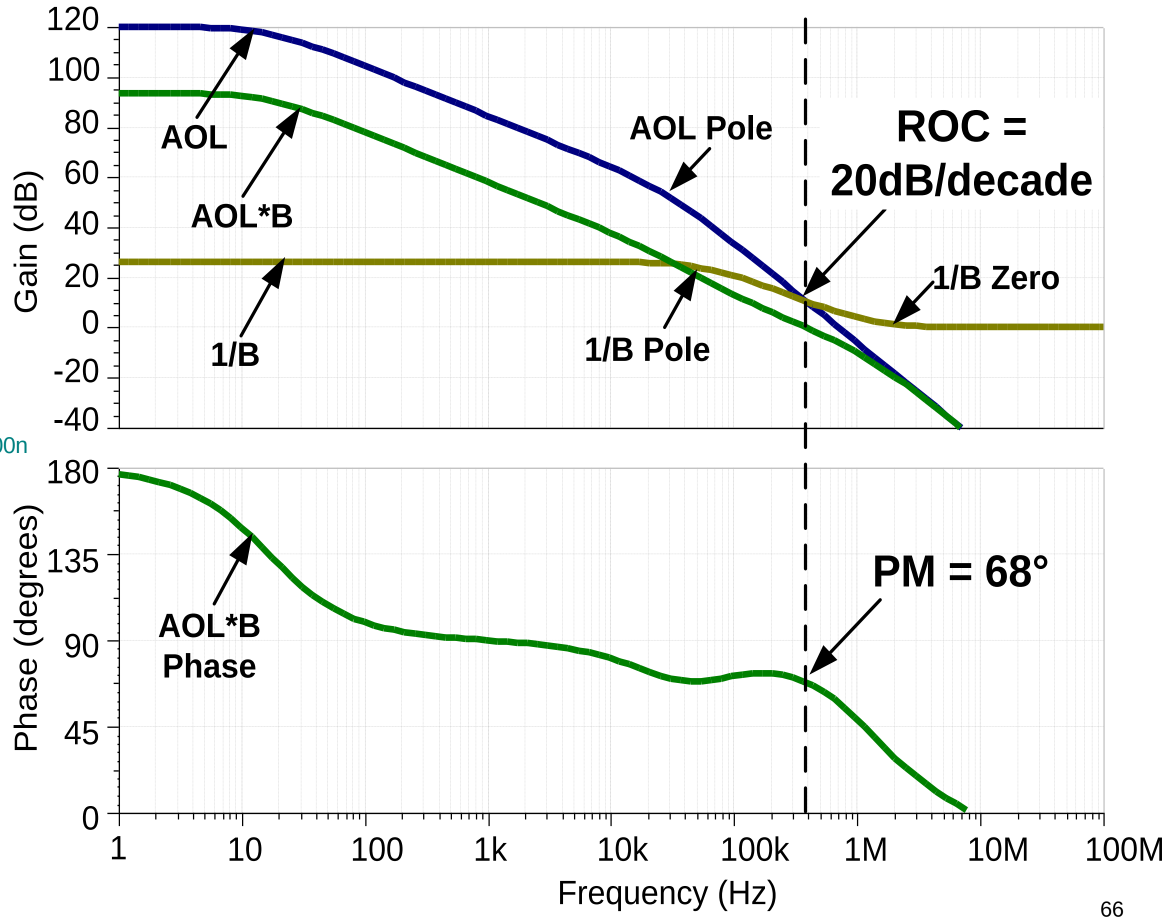
Method 3: Cf



Method 3: Cf - Results

Theory: 1/Beta compensation. Cf feedback capacitor causes 1/Beta to decrease at -20dB/decade and if placed correctly will cause the ROC to be 20dB/decade.



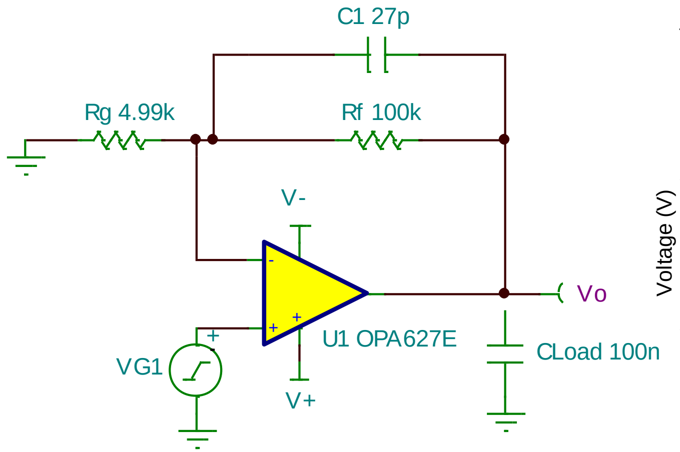


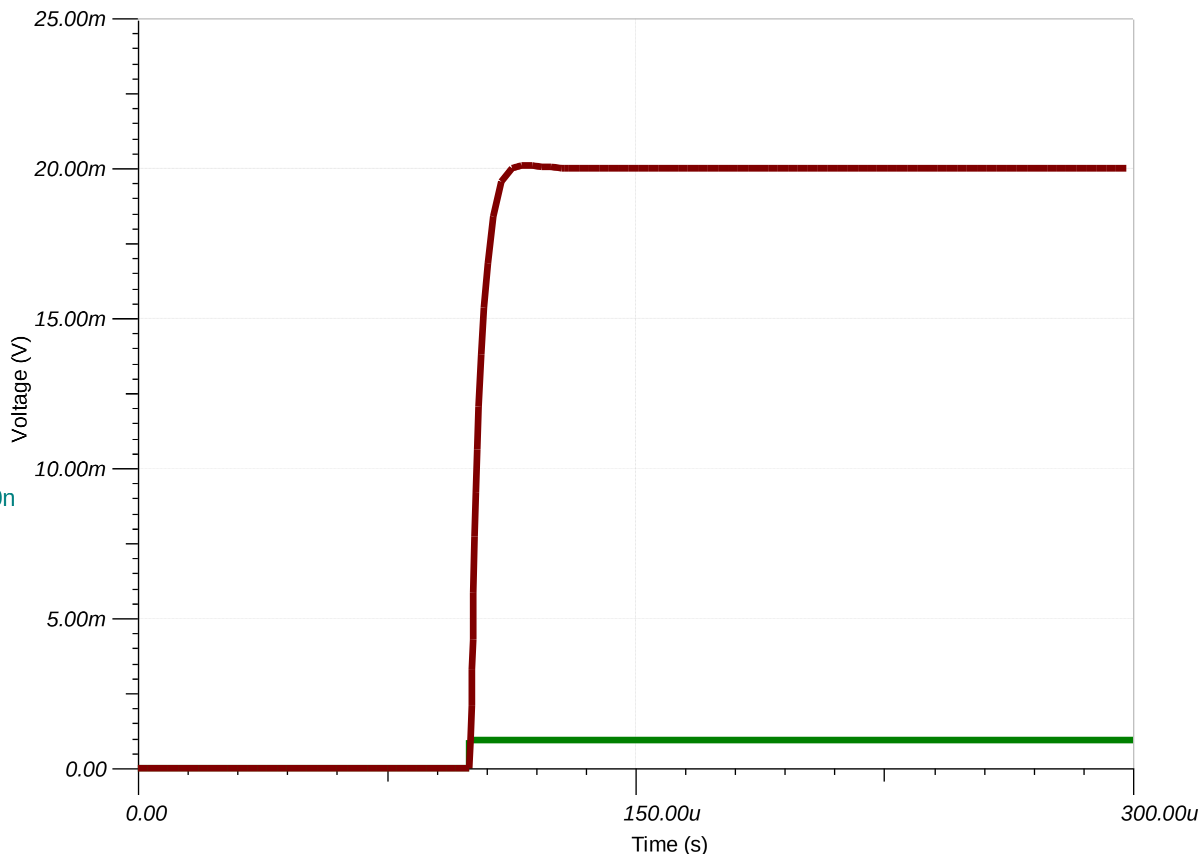
Method 3: Cf - Results

When to use: Especially effective when NG is high, ≥ 30dB.

Systems where a bandwidth limitation is not an issue

- Limits closed-loop bandwidth at 1/(2*pi*Rf*Cf)





Method 3: Cf - Design

Ensure Good Phase Margin:

For 20dB/decade ROC, 1/Beta must intersect AOL while its slope is -20dB/decade.
Therefore: f(1/B pole) < f(cl_unmodified)
f(1/B zero) > f(AOL = 0dB)

f(cl_unmodified) = 152.13kHz

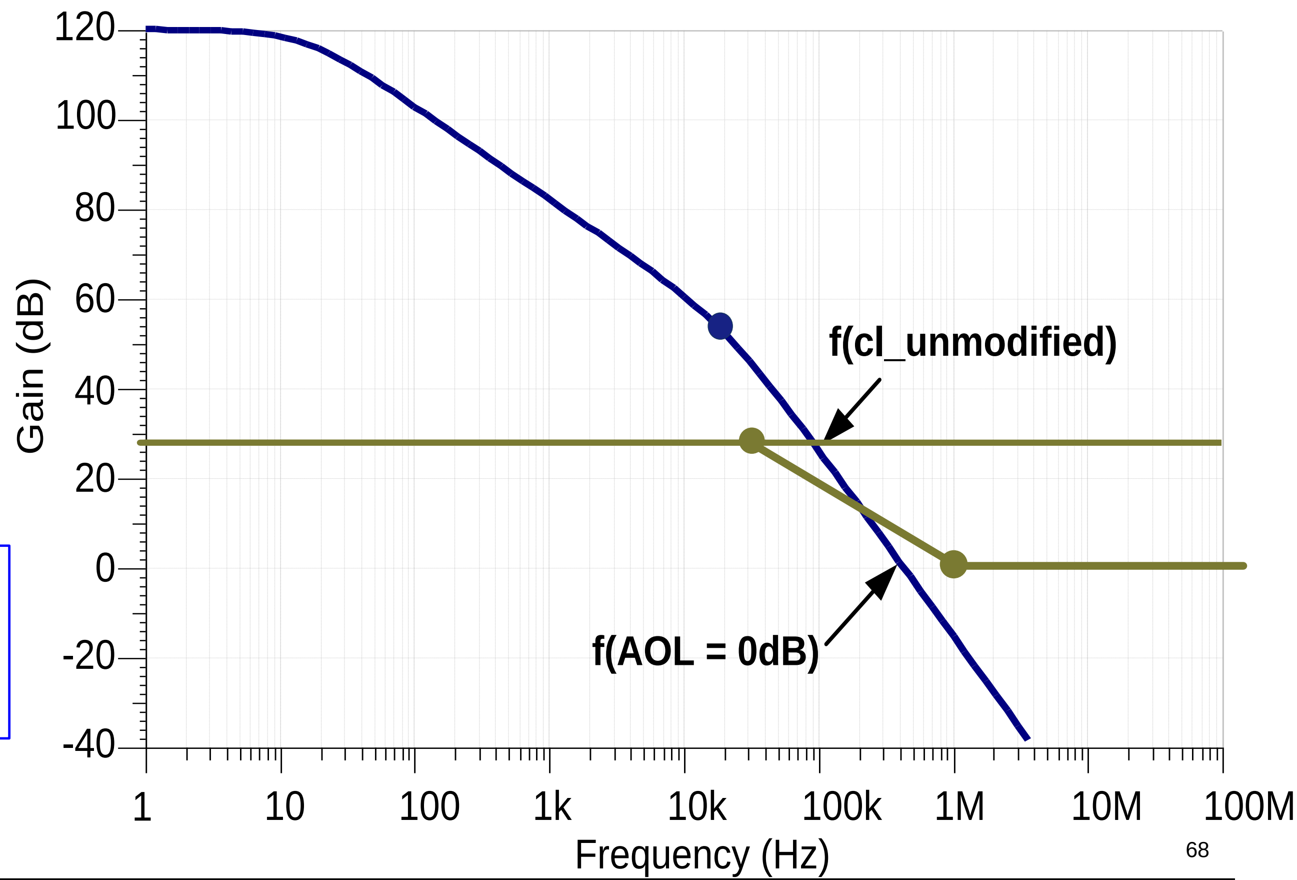
f(AOL = 0dB) = 704.06kHz

1/B Pole Equation:

$$f(1/B\ pole) = \frac{1}{2 \cdot pi \cdot R_f \cdot C_f}$$

1/B Zero Equation:

$$f(1/B\ zero) = \frac{1}{2 \cdot pi \cdot (R_g || R_f) \cdot C_f}$$



Method 3: Cf - Design

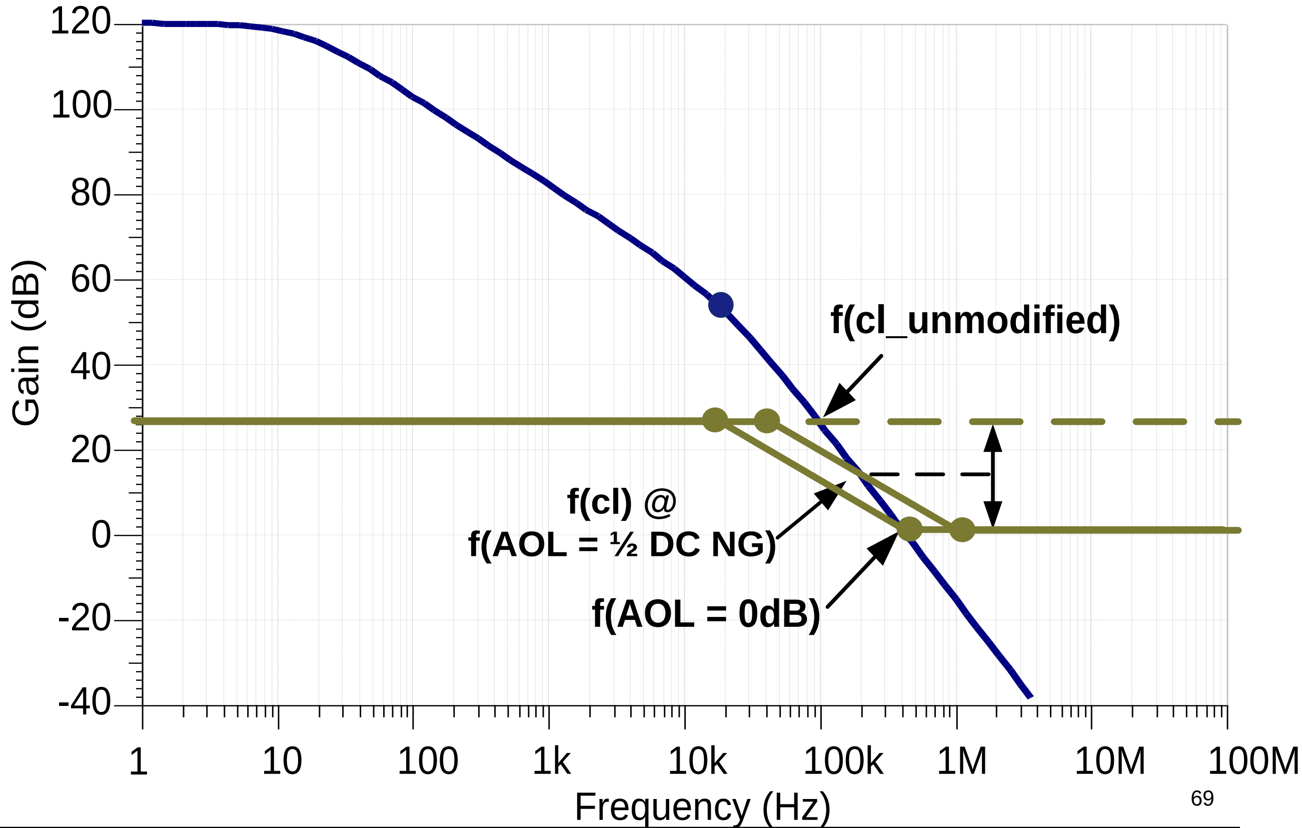
Ensure Good Phase Margin:

1.) Find f(AOL=0dB)
2.) Set f(1/B zero) by choosing Cf:
Good: Set f(1/B zero) = f(AOL = 0dB) for PM ≈ 45 degrees.
Better: Set f(1/B zero) so AOL @ f(cl) = ½ Low-Frequency NG in dB

f(AOL = 0dB) = 704.06kHz

1/B Zero Equation:

$$f(1/B\ zero)=\frac{1}{2\cdot pi\cdot(R_g||R_f)\cdot C_f}$$



TEXAS INSTRUMENTS

Method 3: Cf – Design - Summary

Summary:

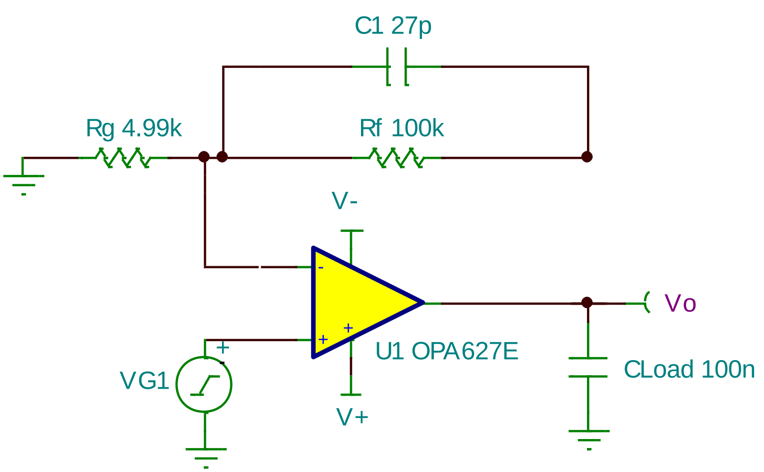
1.) Ensure stability by placing:

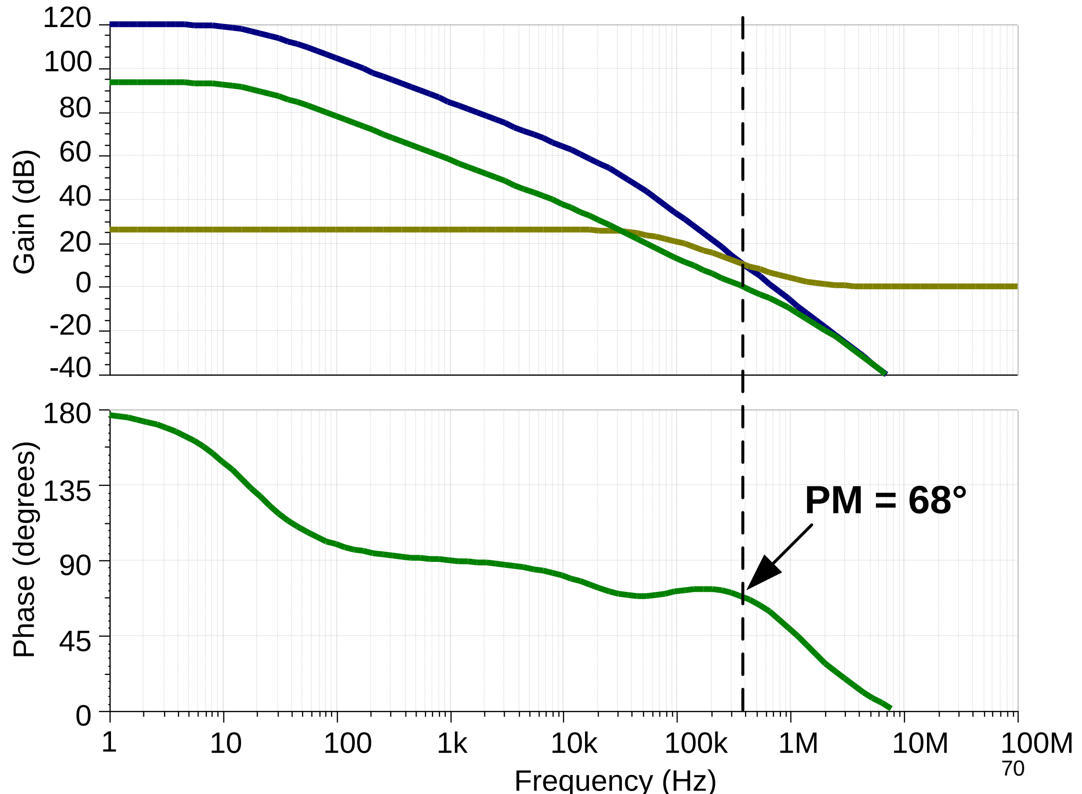
a) f(1/B zero) ≥ f(AOL = 0dB

b) f(1/B pole) ≤ f(cl_unmodified)

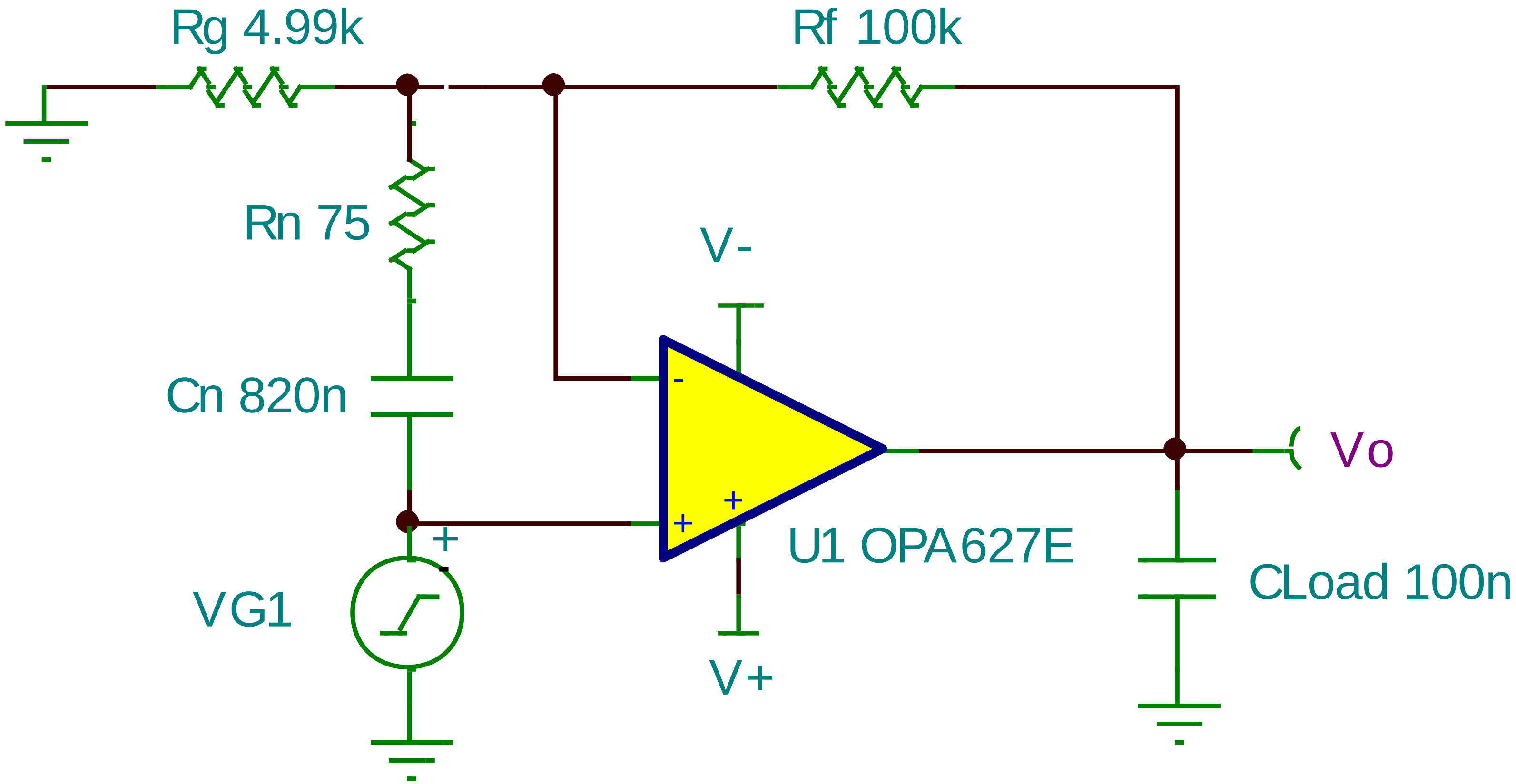
2.) Try to adjust the zero location so the 1/B curve crosses the AOL curve in the middle of the 1/B span allowing for shifts in AOL

Final Circuit



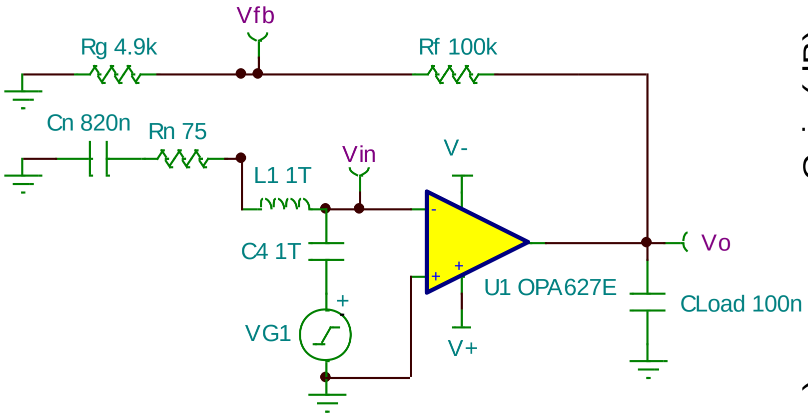


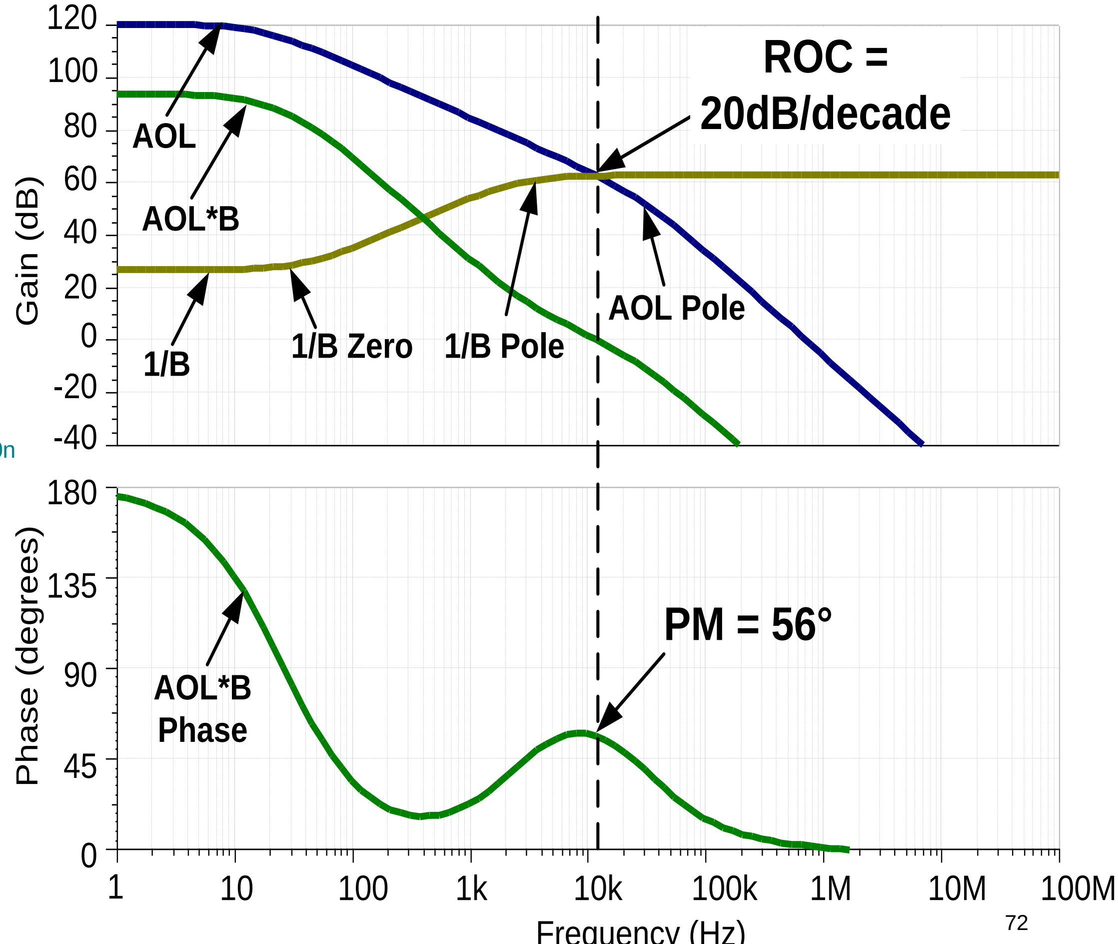
Method 4: Noise-Gain



Method 4: Noise Gain - Results

<u>Theory:</u> 1/Beta compensation. Raise high-frequency 1/Beta so the ROC occurs before the AOL pole causes the AOL slope to change



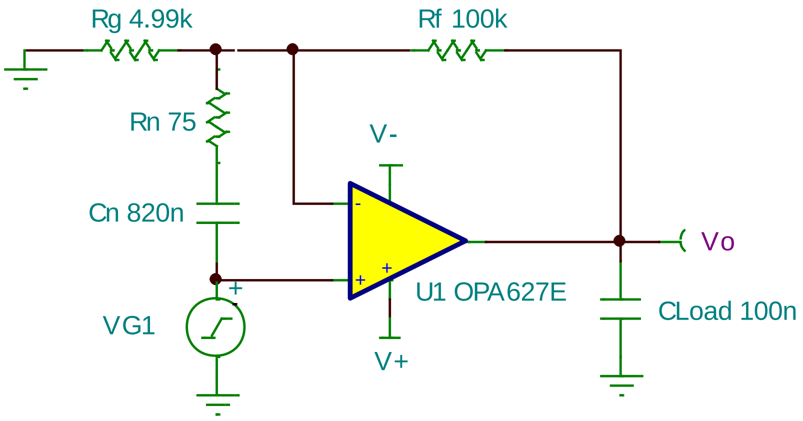


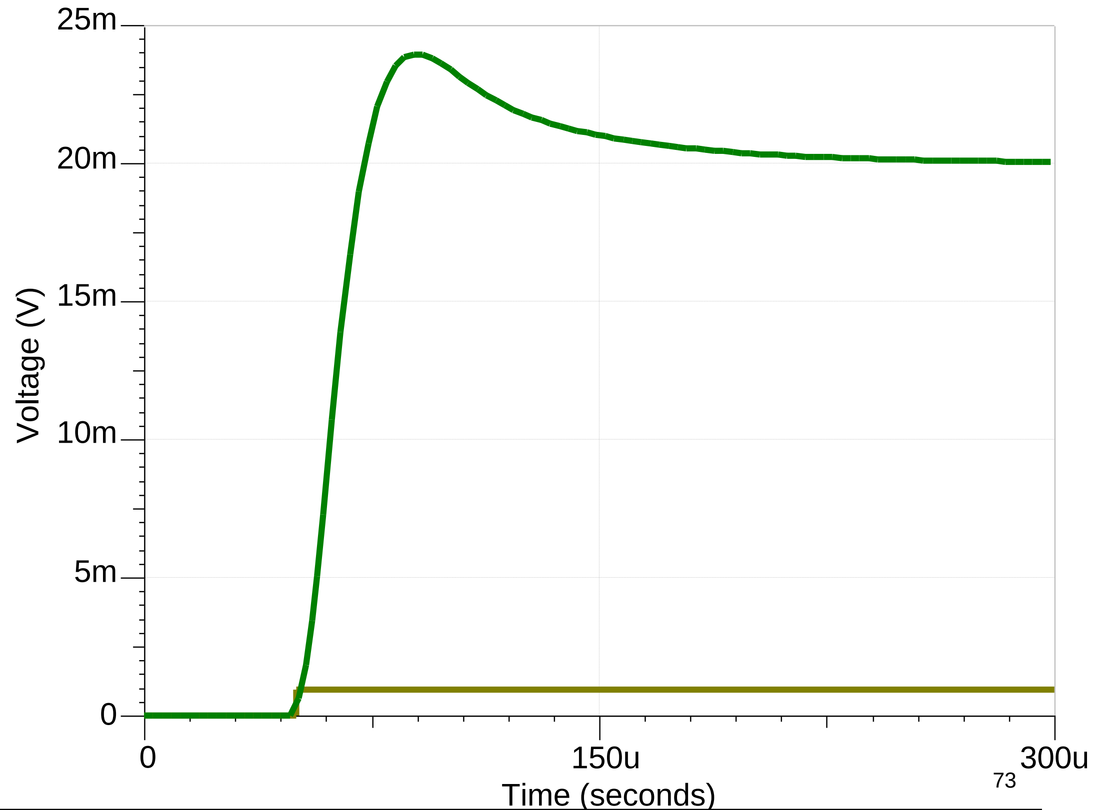
Method 4: Noise Gain - Results

<u>When to use:</u> **Better for lighter capacitive loading**

When AOL @ f(AOL pole) < (Closed loop gain + 20dB)

Due to the increase in noise gain, this approach may not be practical when required noise gain is greater than the low-frequency signal gain by more than ~25-30dB.





Method 4: Noise Gain - Design

Ensure Good Phase Margin:

For 20dB/decade ROC, 1/Beta must intersect AOL above the AOL pole.
Therefore: |High-Freq NG| > |AOL| @ f(AOL pole)
f(1/B zero) < f(AOL = High-Freq NG)

|AOL| @ f(AOL pole) = 52.11dB

f(AOL pole) = 29.49kHz

High-Freq Noise-Gain Equation:

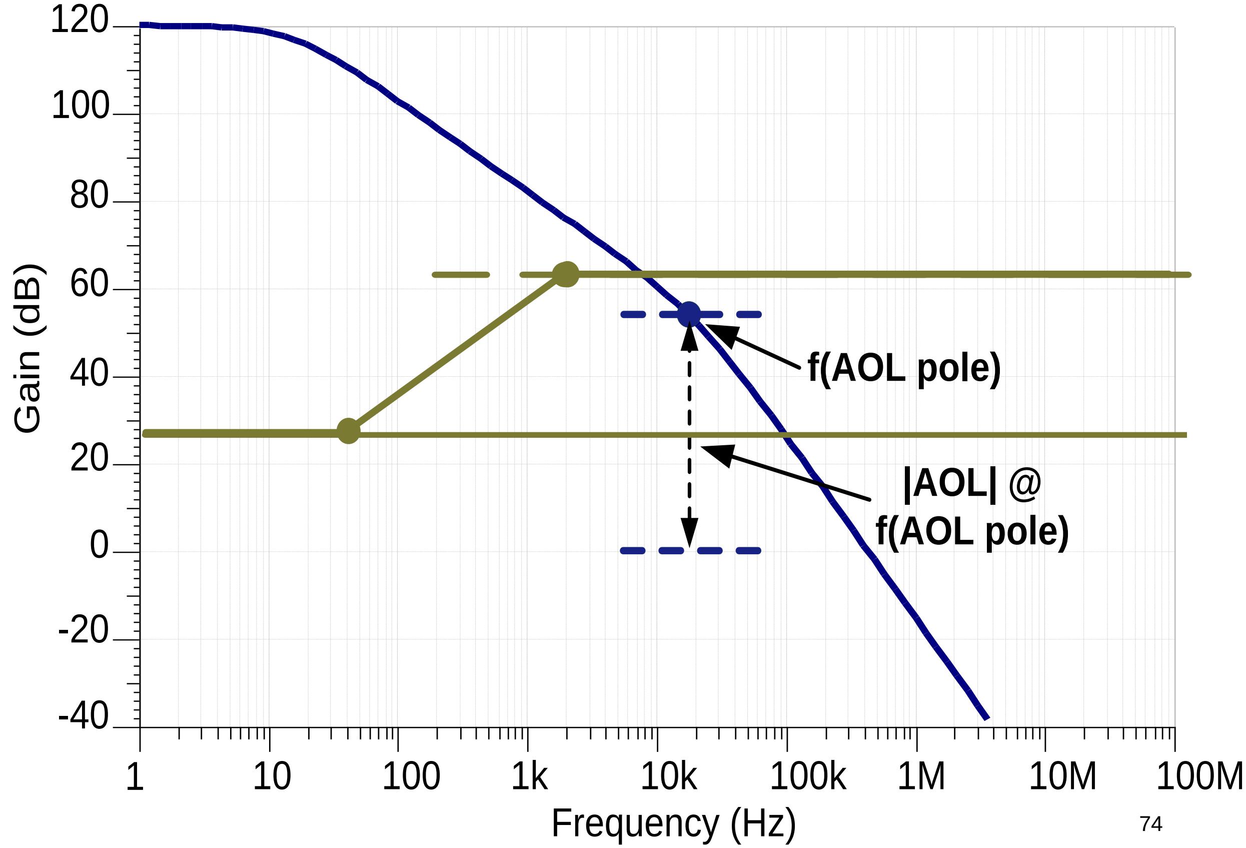
$$HF\ NG = \frac{R_f}{(R_g || R_n)}$$

1/B Zero Equation:

$$f(1/B\ zero) = \frac{1}{2 \cdot pi \cdot R_n \cdot C_n}$$

1/B Pole Equation:

$$f(1/B\ pole) = \frac{1}{2 \cdot pi \cdot (R_n + (R_g || R_f) \cdot C_f}$$



Method 4: Noise Gain - Design

Ensure Good Phase Margin:

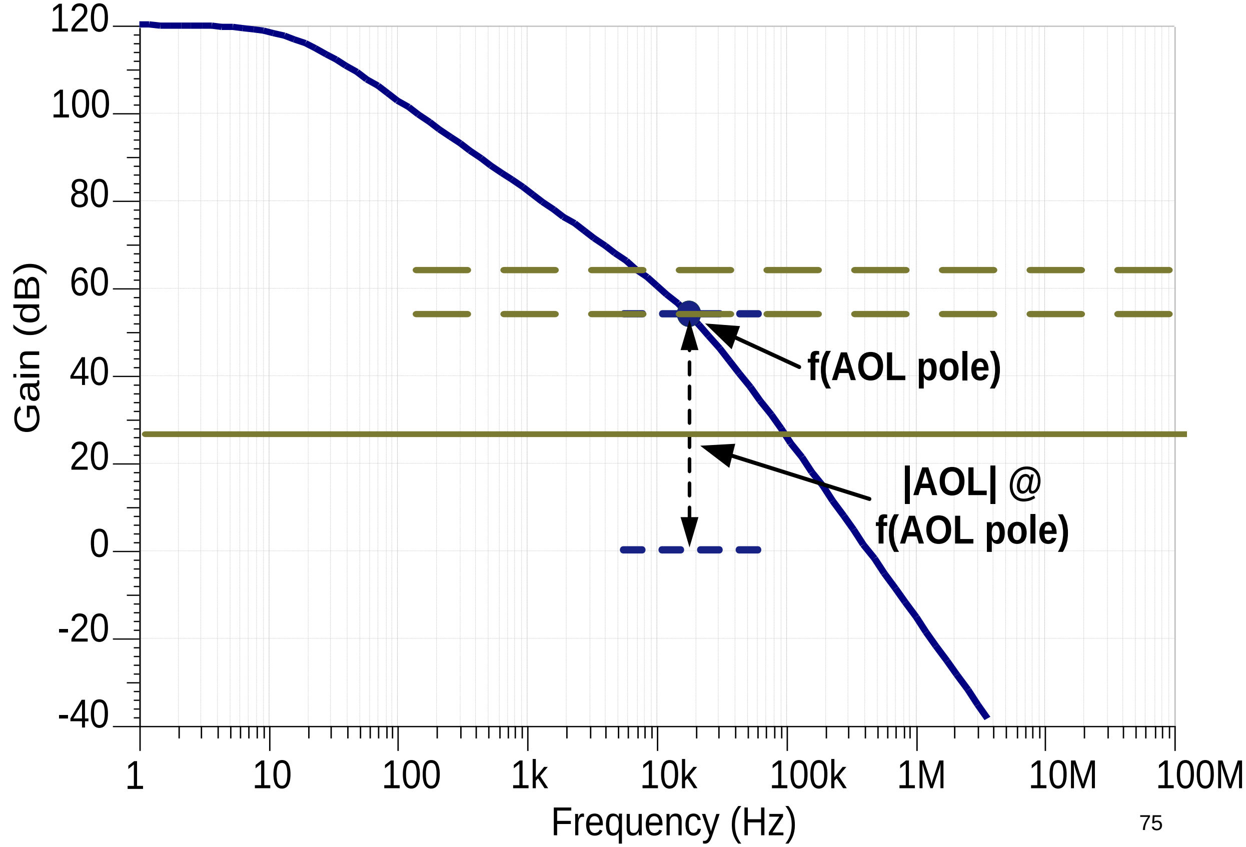
1.) Find f(AOL pole) and |AOL| @ f(AOL pole)
2.) Set High-Freq Noise-Gain by choosing Rn:
Good: |HF NG| ≥ |AOL| @ f(AOL pole)
Better: |HF NG| ≥ |AOL| @ f(AOL pole) + 10dB

|AOL| @ f(AOL pole) = 52.11dB

f(AOL pole) = 29.49kHz

High-Freq Noise-Gain Equation:

$$HF\ NG = \frac{R_f}{(R_g || R_n)}$$



Method 4: Noise Gain - Design

Ensure Good Phase Margin:

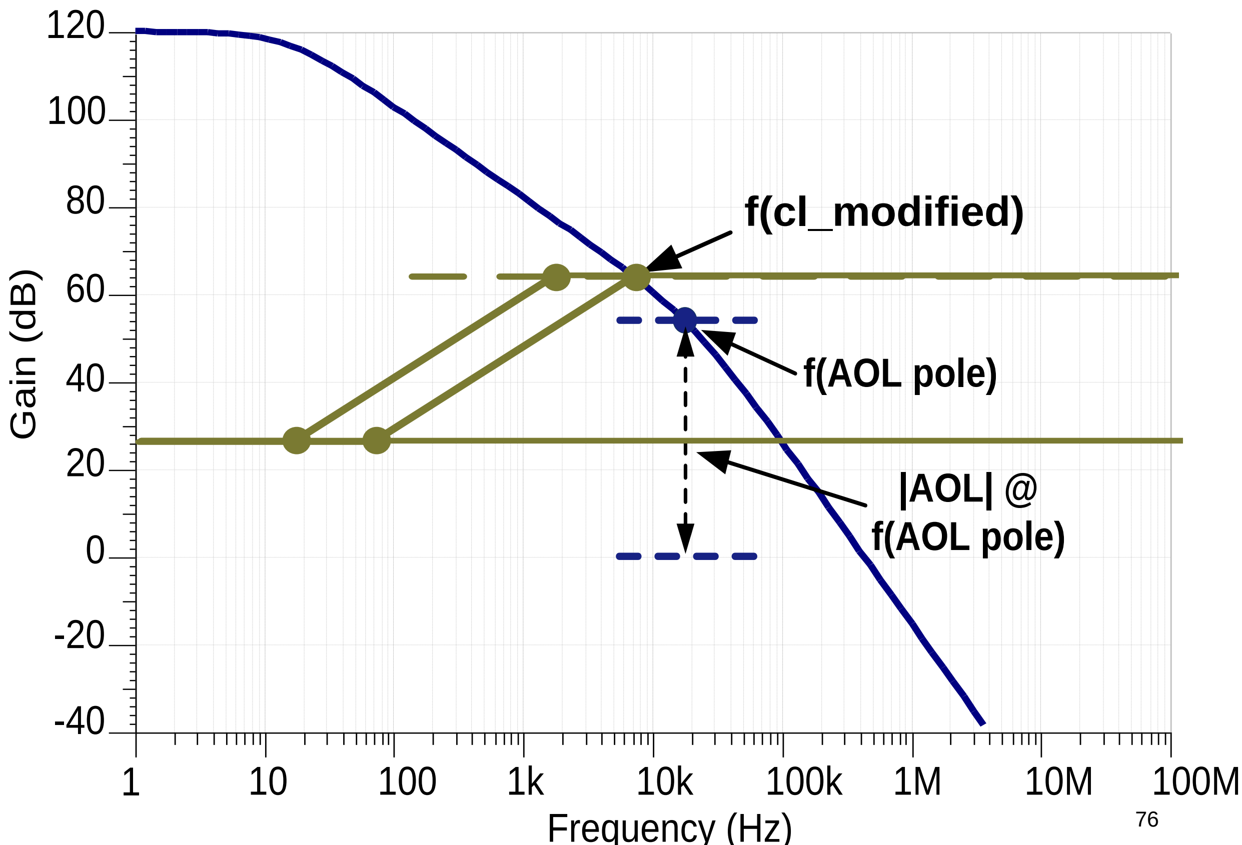
3.) Find f(cl_modified) = f(AOL @ |HF NG|)
4.) Set f(1/B zero) by choosing Cn:
Good: f(1/B zero) ≤ f(cl_modified)
Better: f(1/B zero) ≤ f(cl_modified) / 3.5 (~ ½ decade)

f(cl_modified) = 29.49kHz

-

High-Freq Noise-Gain Equation:

$$\text{HF NG} = \frac{R_f}{(R_g || R_n)}$$



Method 4: Noise Gain - Summary

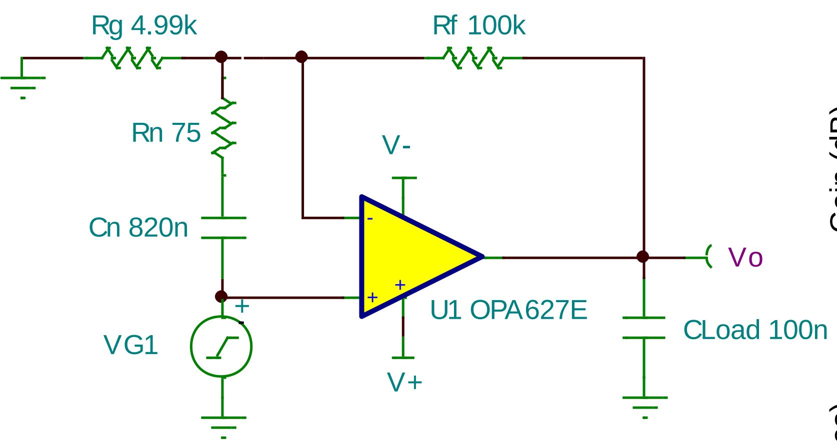
Summary:

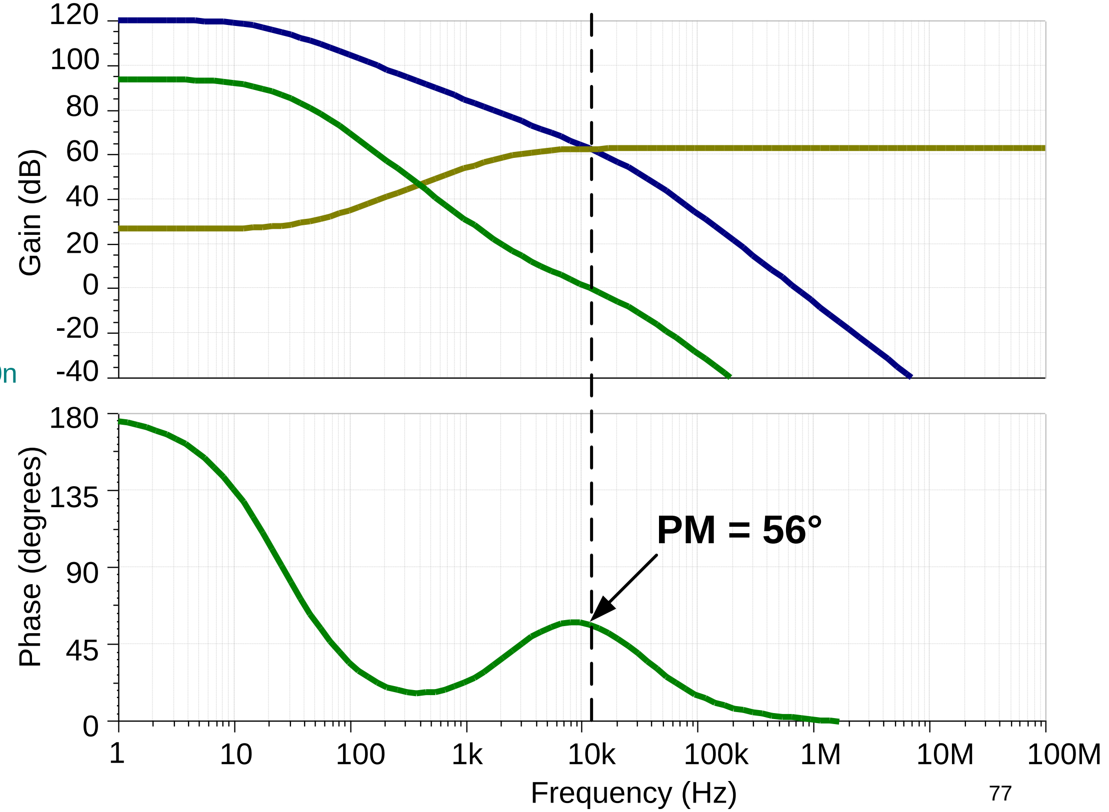
1.) Ensure stability by setting:

a) |HF NG| ≥ (|AOL| @ f(AOL pole) + 10dB)

b) f(1/B zero) ≤ f(cl_modified) / 3.5

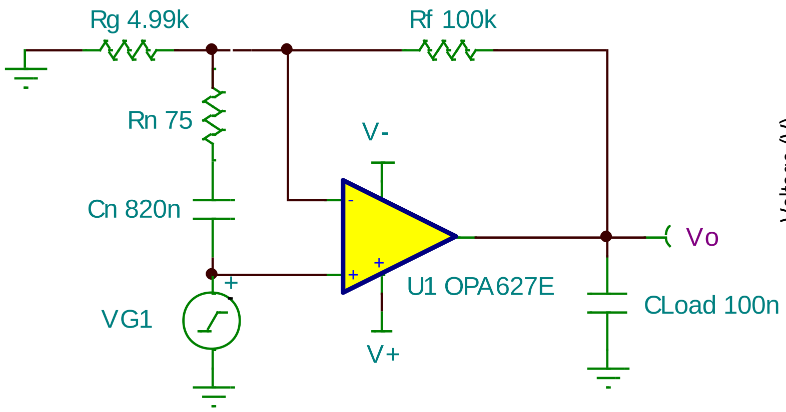
Final Circuit

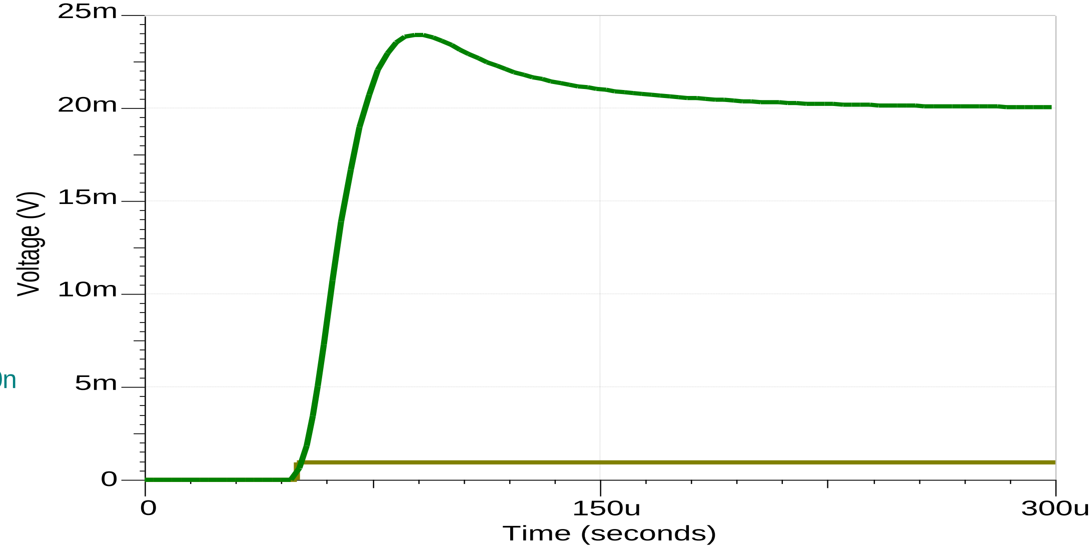


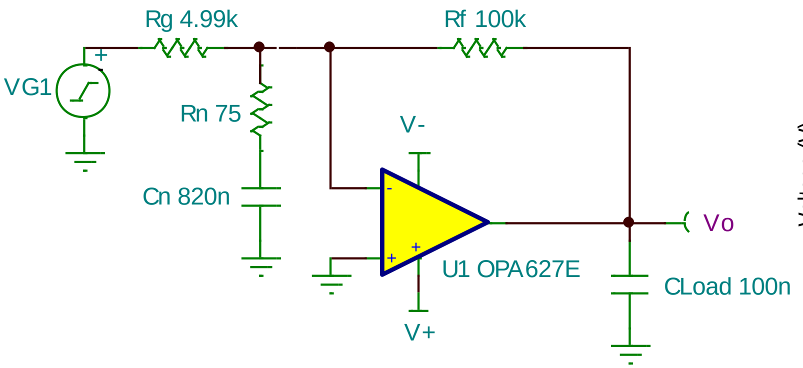


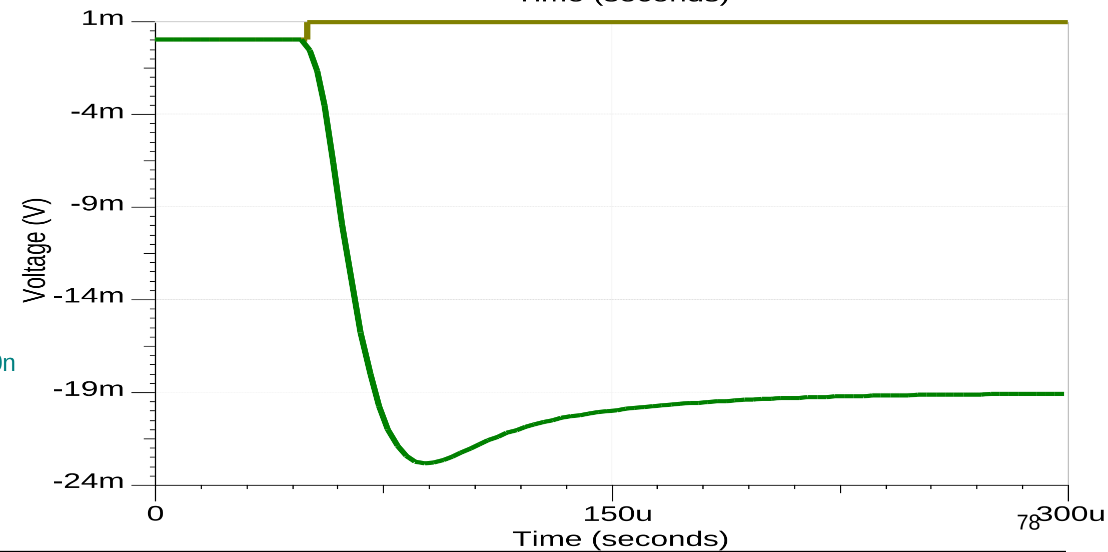
Method 4: Noise Gain

Quick reminder that inverting and non-inverting noise gain circuits are different!



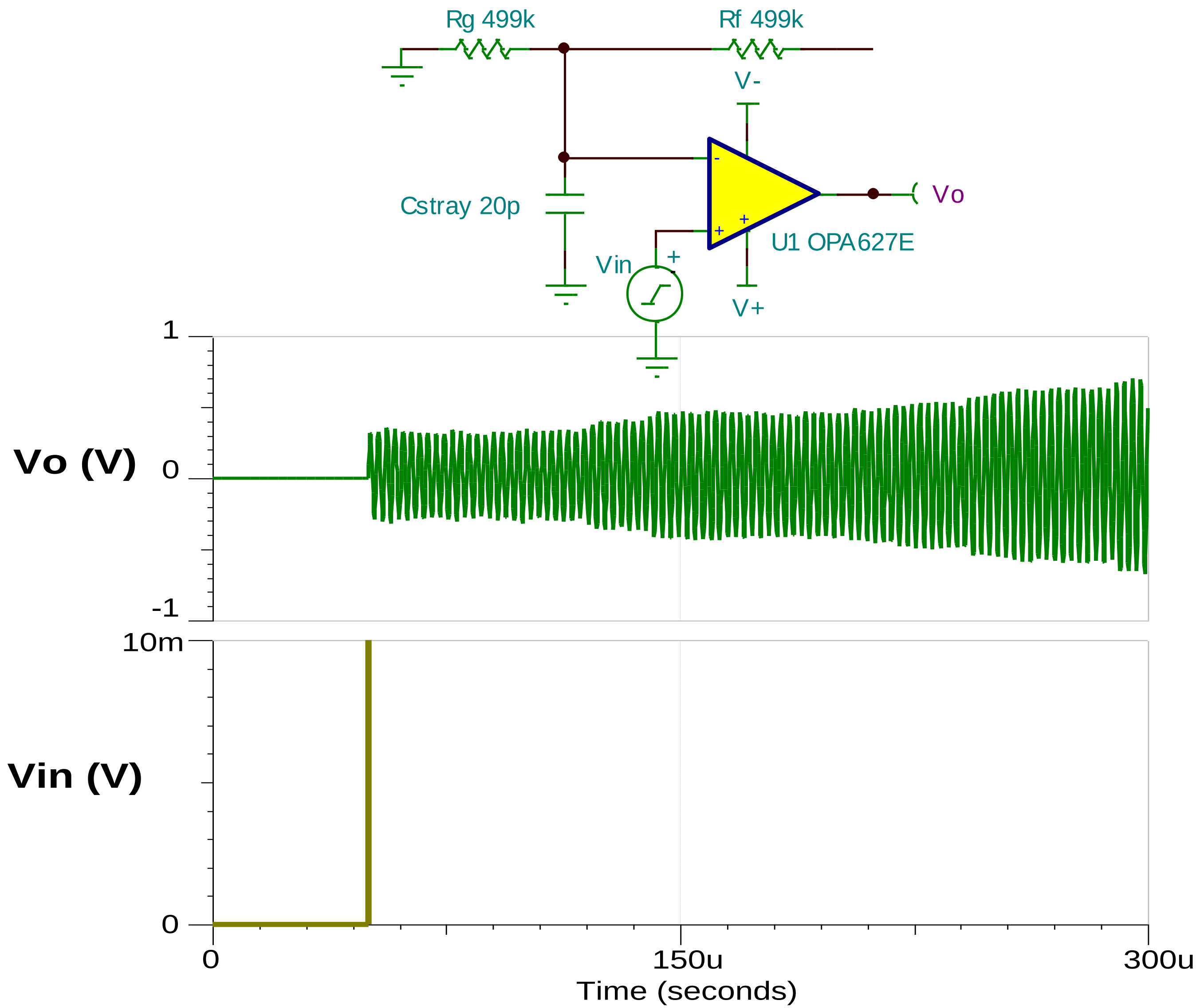






Circuits with High Feedback Network Impedance

Circuits with High Feedback Network Impedance



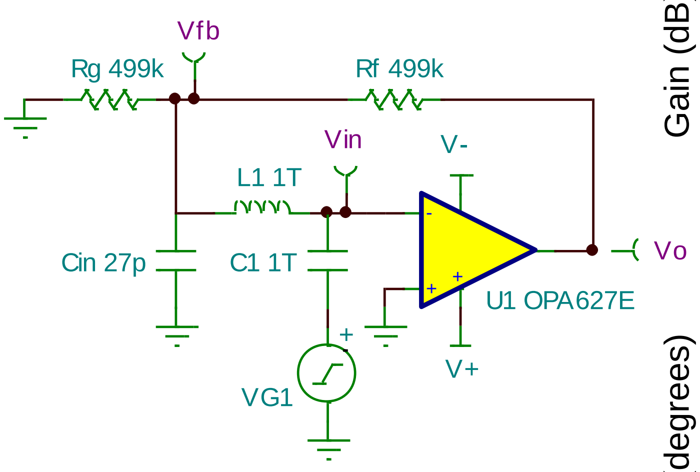
Circuits with High Feedback Network Impedance

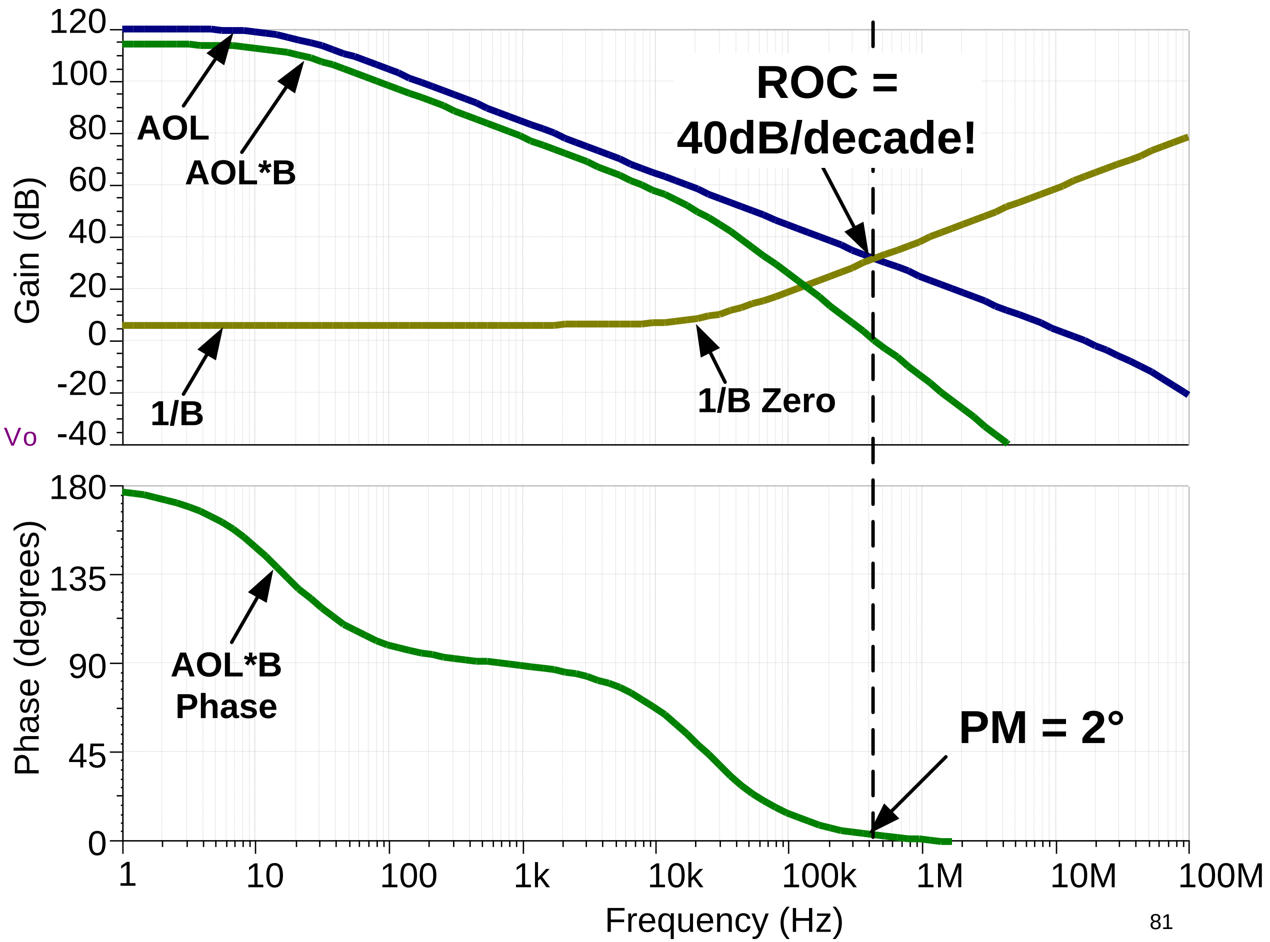
Determine the issue:

Zero in 1/Beta!!

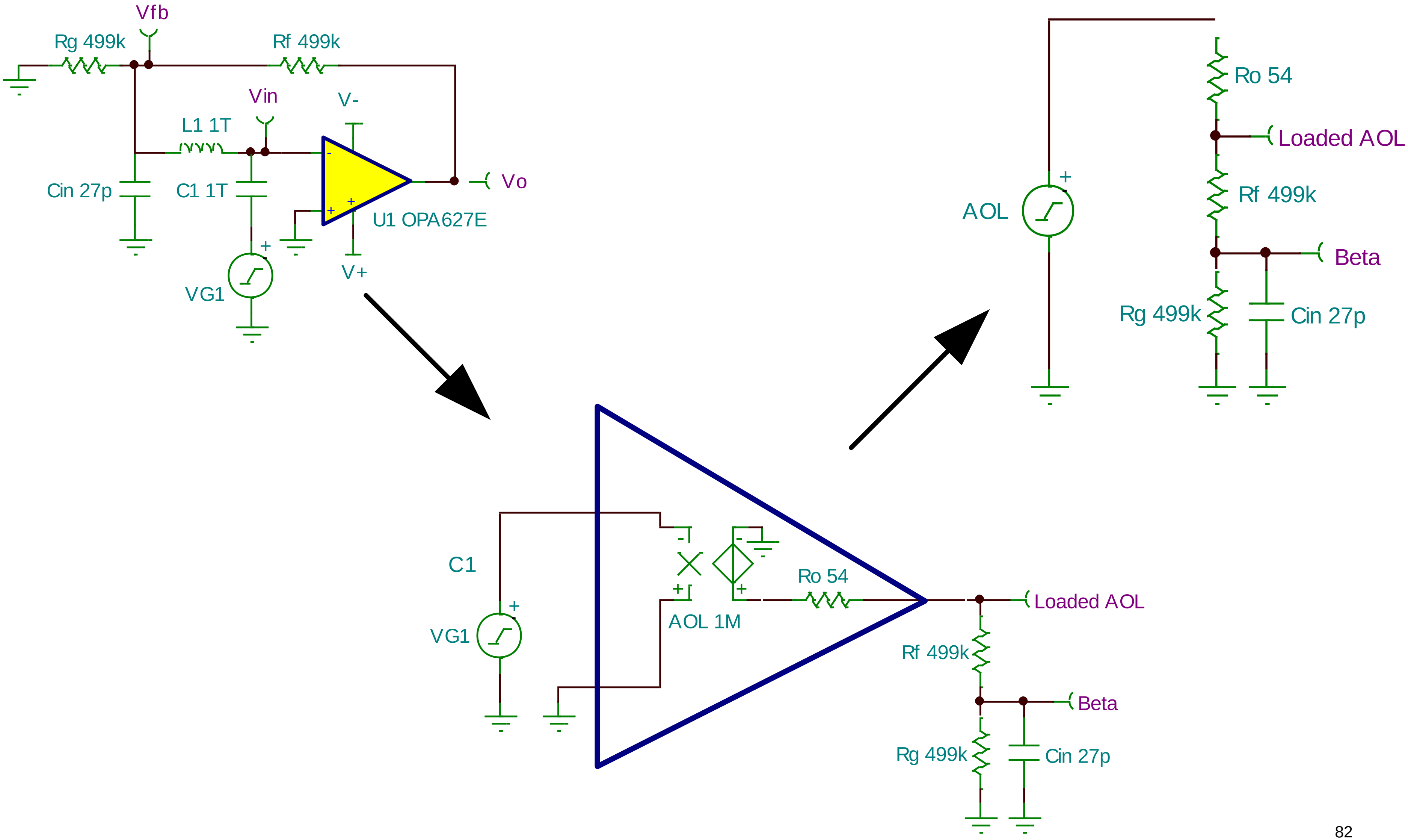
ROC = 40dB/decade!!

Phase Margin 2!!

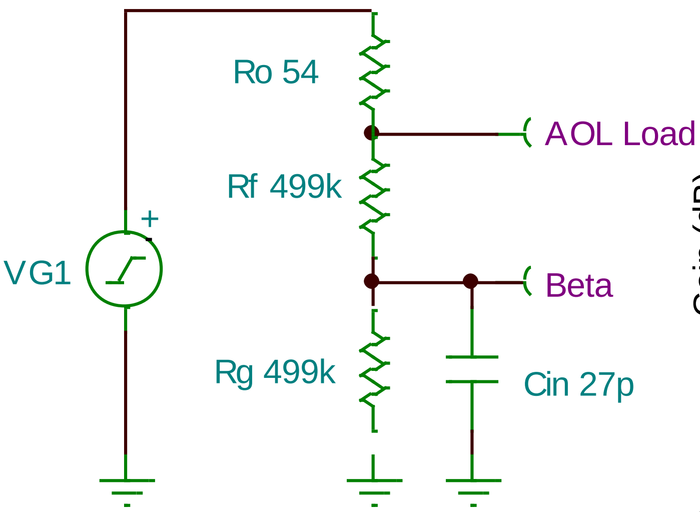




Circuits with High Feedback Network Impedance - Theory

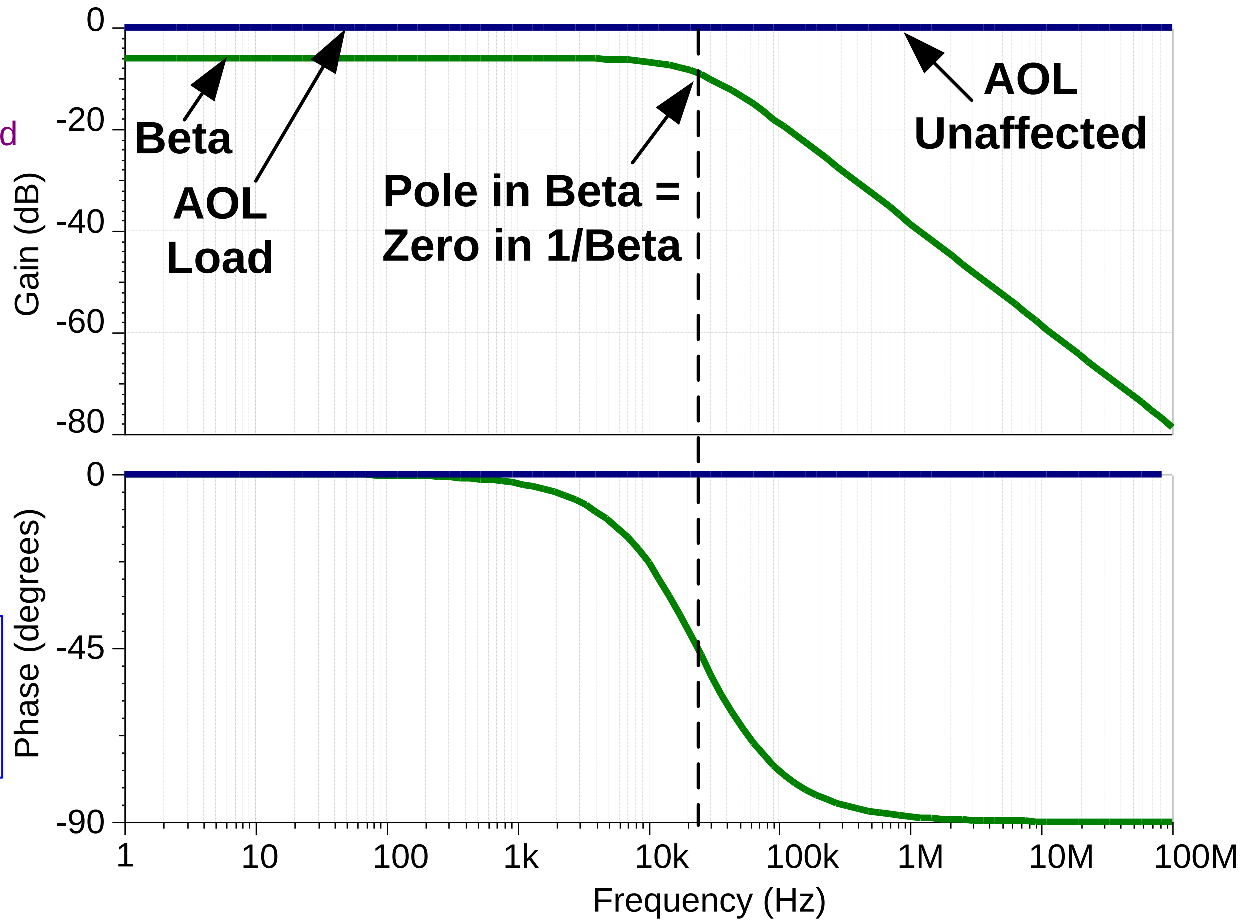


Circuits with High Feedback Network Impedance - Theory



Beta Pole & 1/Beta Zero Equation:

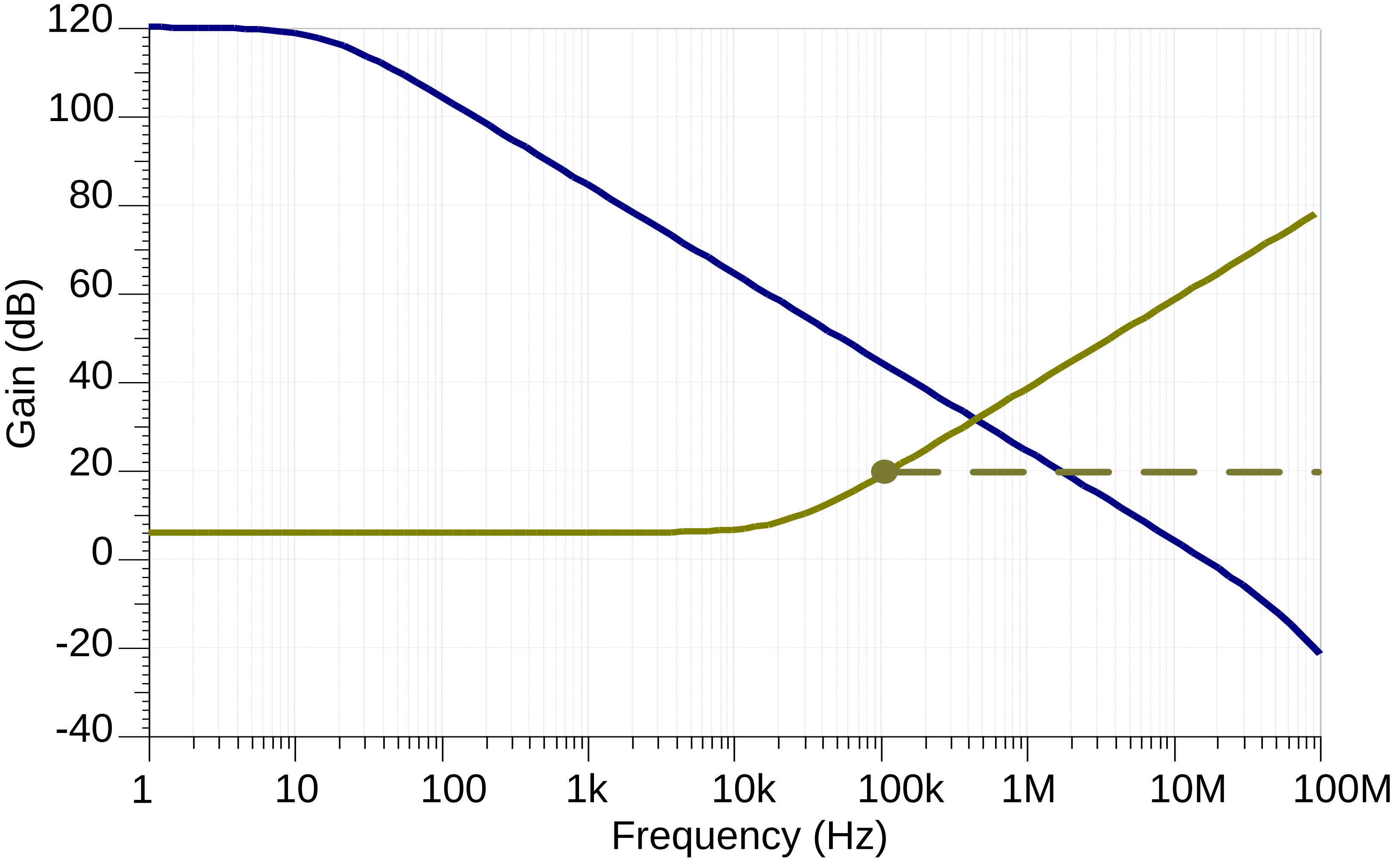
$$f(\text{B pole})=f(1/\text{B zero})=\frac{1}{2\cdot \text{pi}\cdot (R_g||R_f)\cdot C_{in}}$$



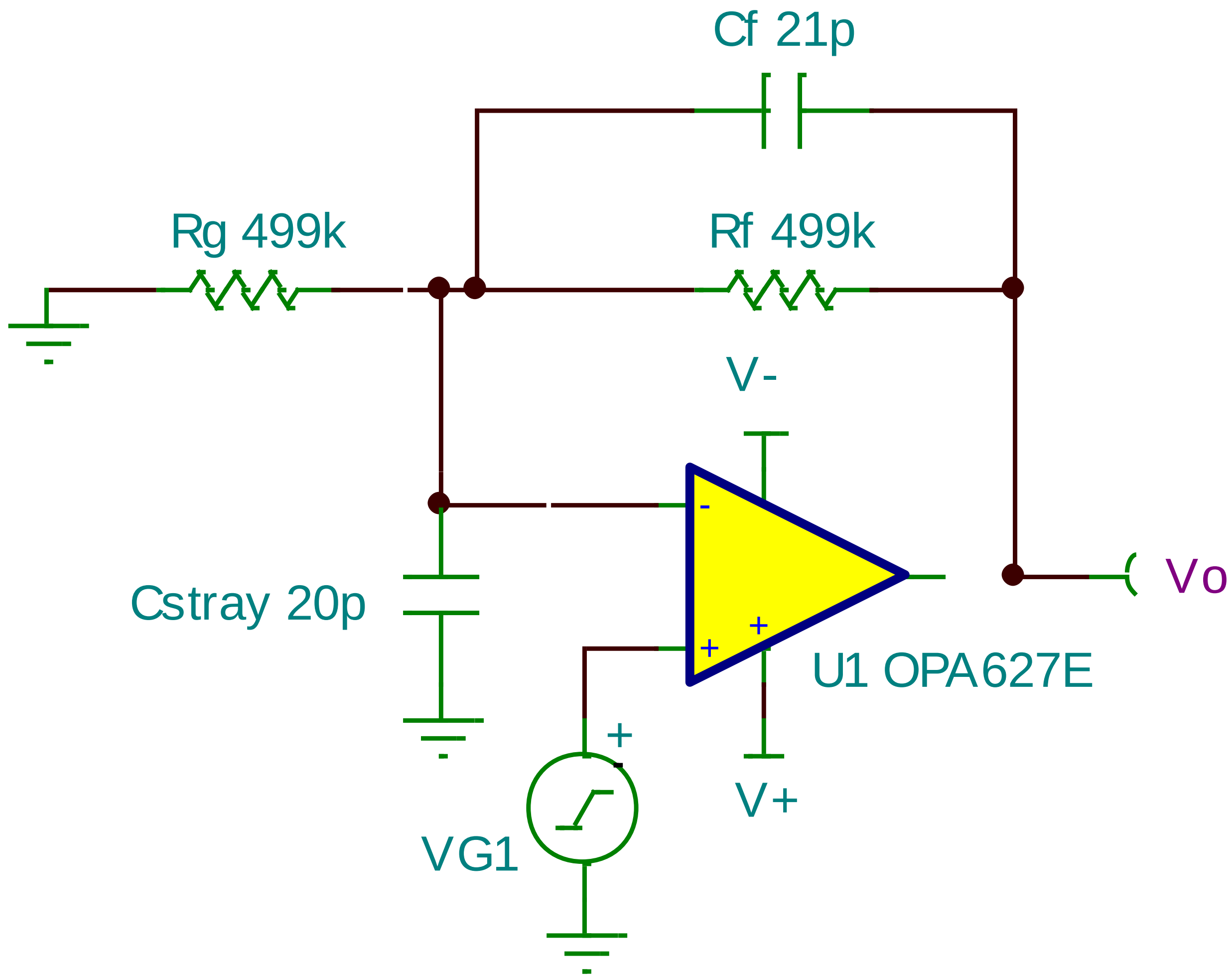
Stabilize Circuits With High Feedback Network Impedance

Stability Options – Zero in 1/Beta

The only practical option is to add a pole to cancel the 1/Beta Zero

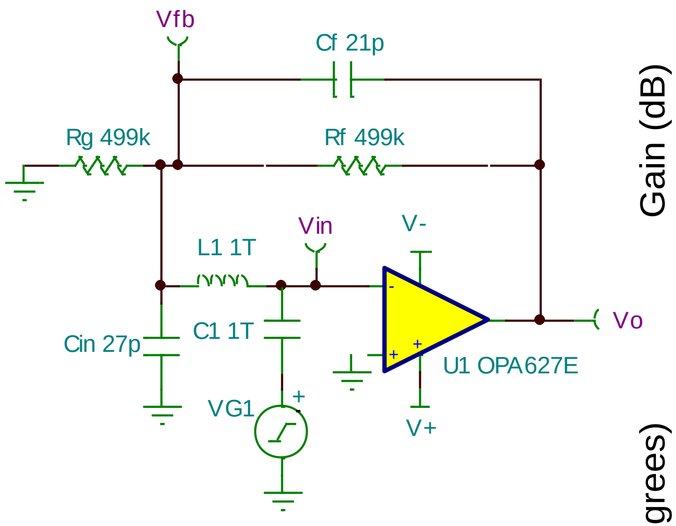


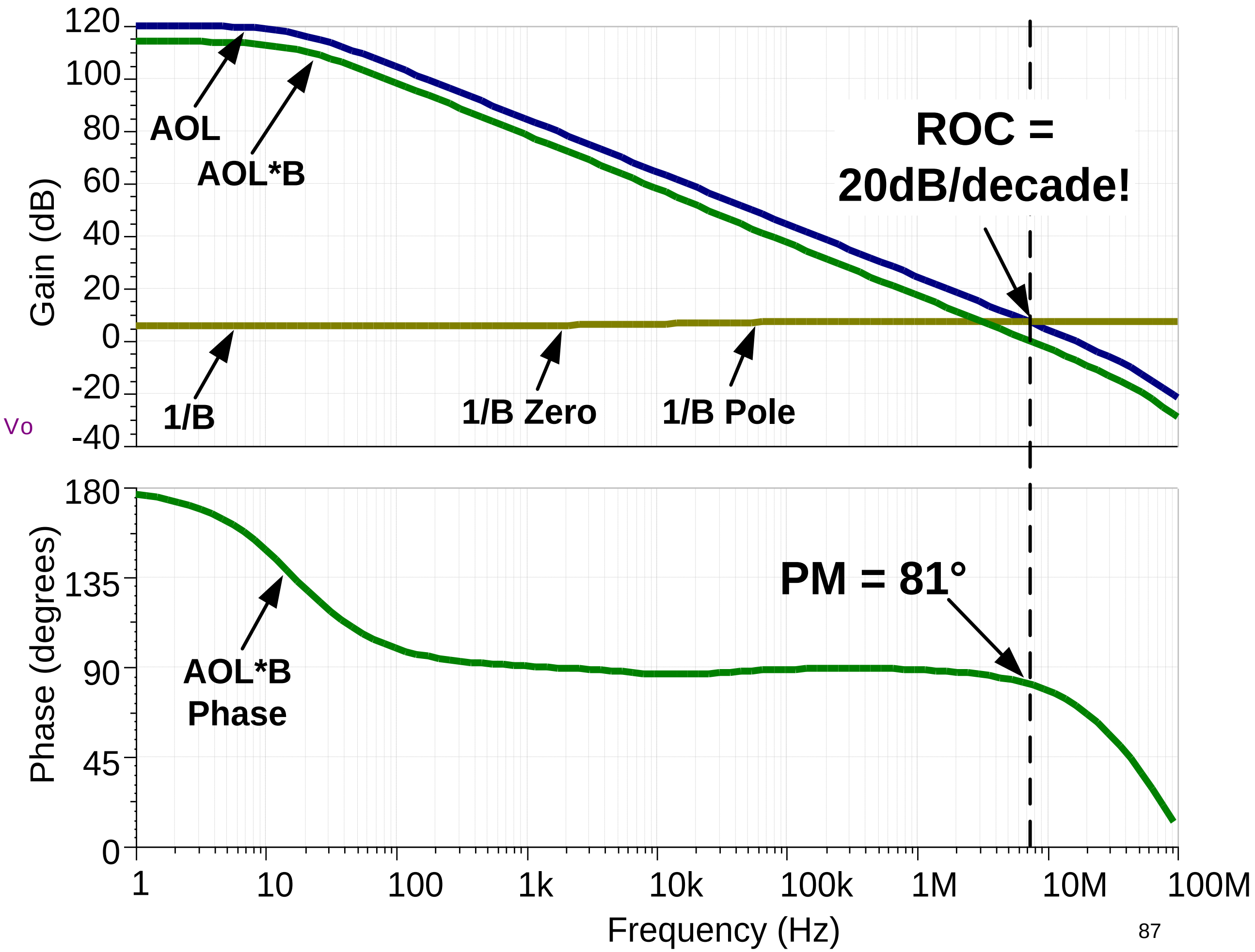
Method 1: Cf



Method 1: Cf - Results

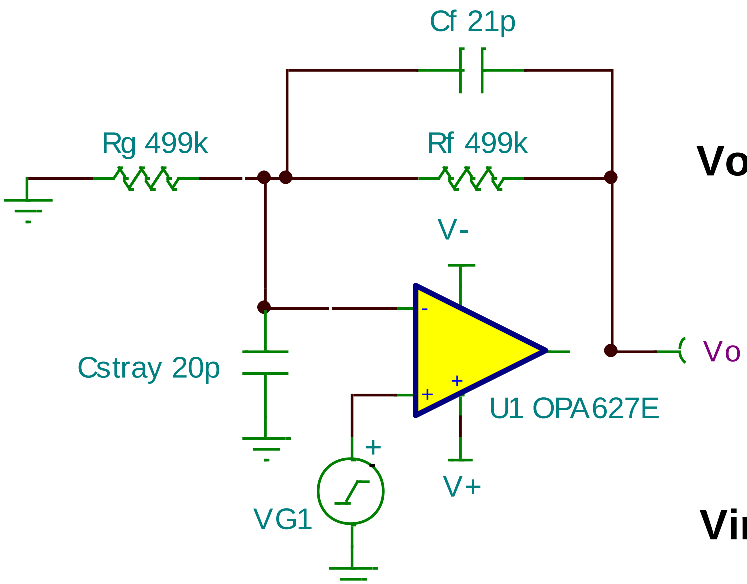
<u>Theory:</u> 1/Beta compensation. Cf feedback places a pole in 1/Beta to cancel the zero from the input capacitance.

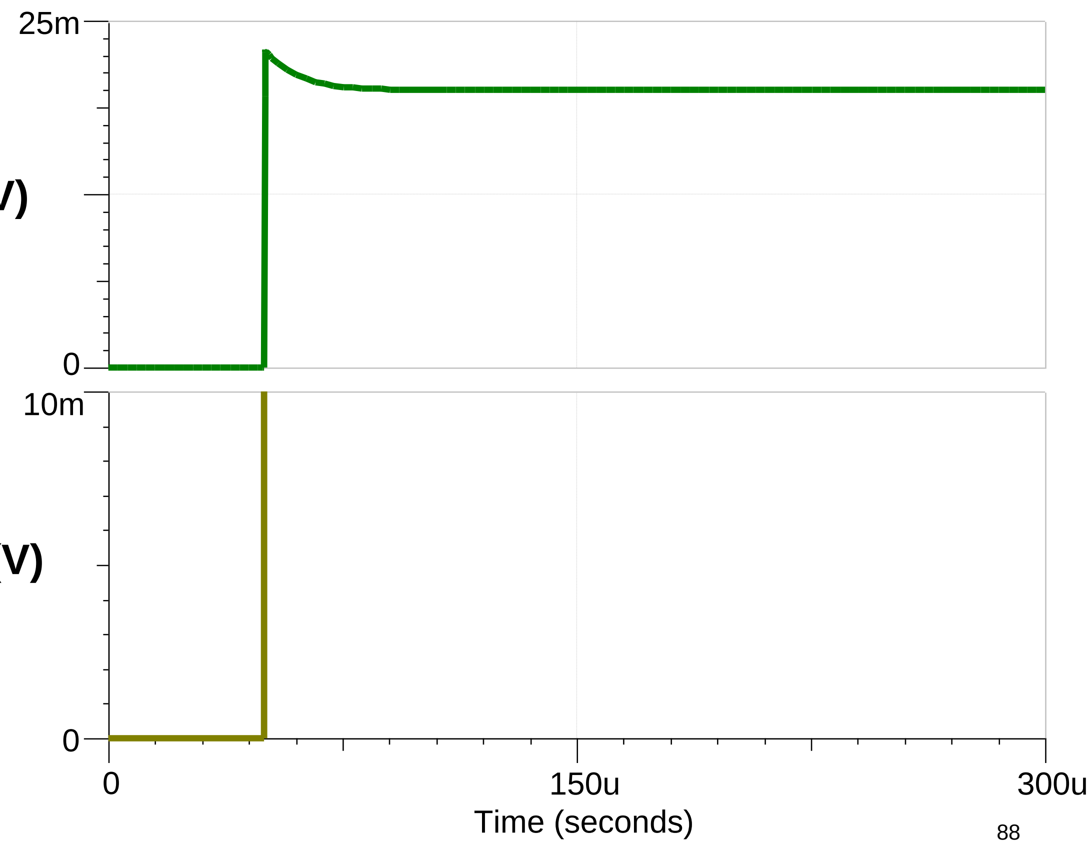




Method 1: Cf - Results

<u>When to use:</u> Almost always a safe design practice.
Limits gain at 1/(2*pi*Rf*Cf)





Method 1: Cf - Design

Ensure Good Phase Margin:

For 20dB/decade ROC, the 1/Beta pole must flatten the 1/Beta Zero before f(cl)
Therefore f(1/Beta pole) ≤ f(cl)

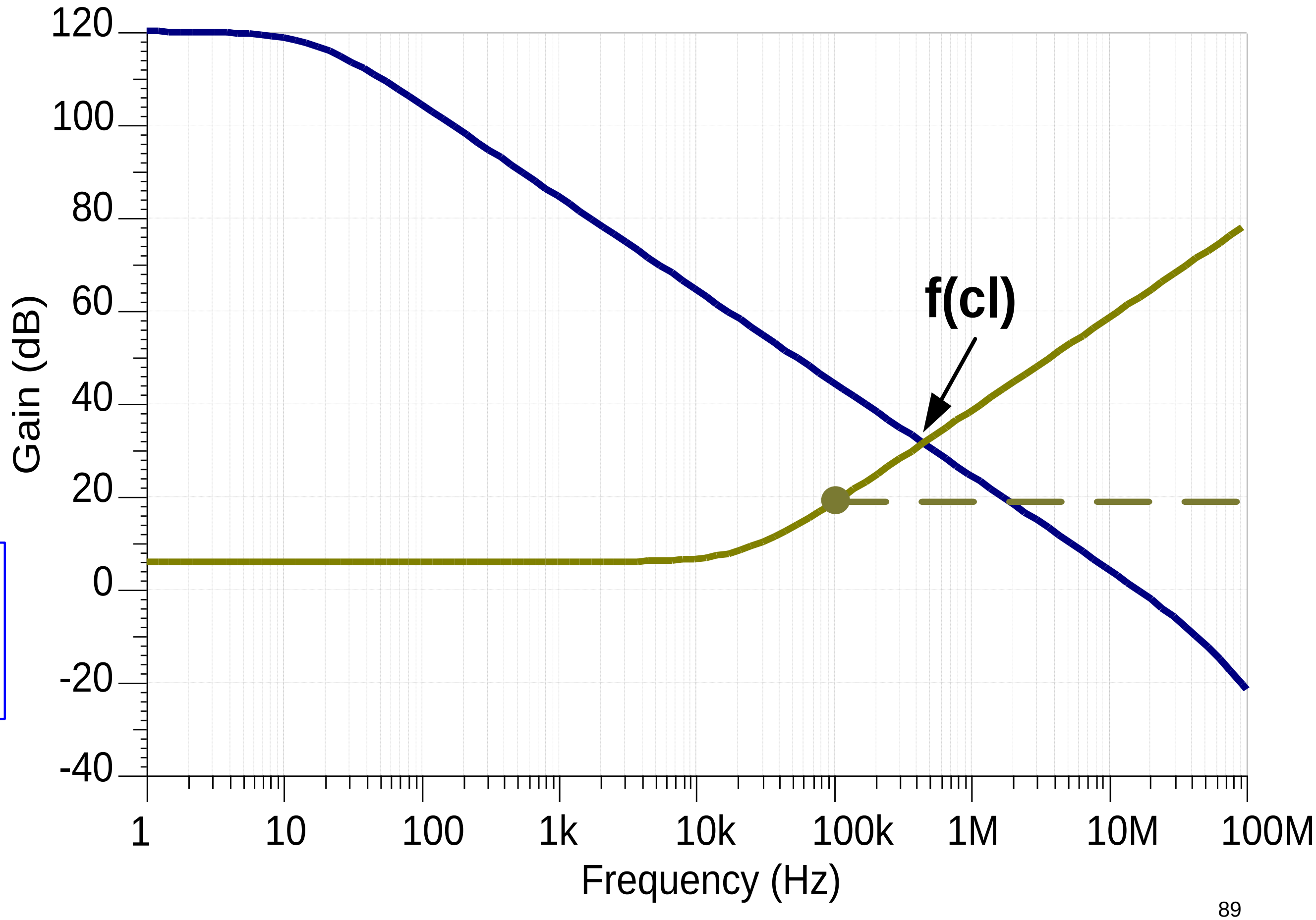
f(cl) = 445.6kHz

1/B Pole Equation:

$$f(1/B\ pole) = \frac{1}{2 \cdot pi \cdot R_f \cdot C_f}$$

1/B Zero Equation:

$$f(1/B\ zero) = \frac{1}{2 \cdot pi \cdot (R_g || R_f) \cdot C_{in}}$$



Method 1: Cf - Design

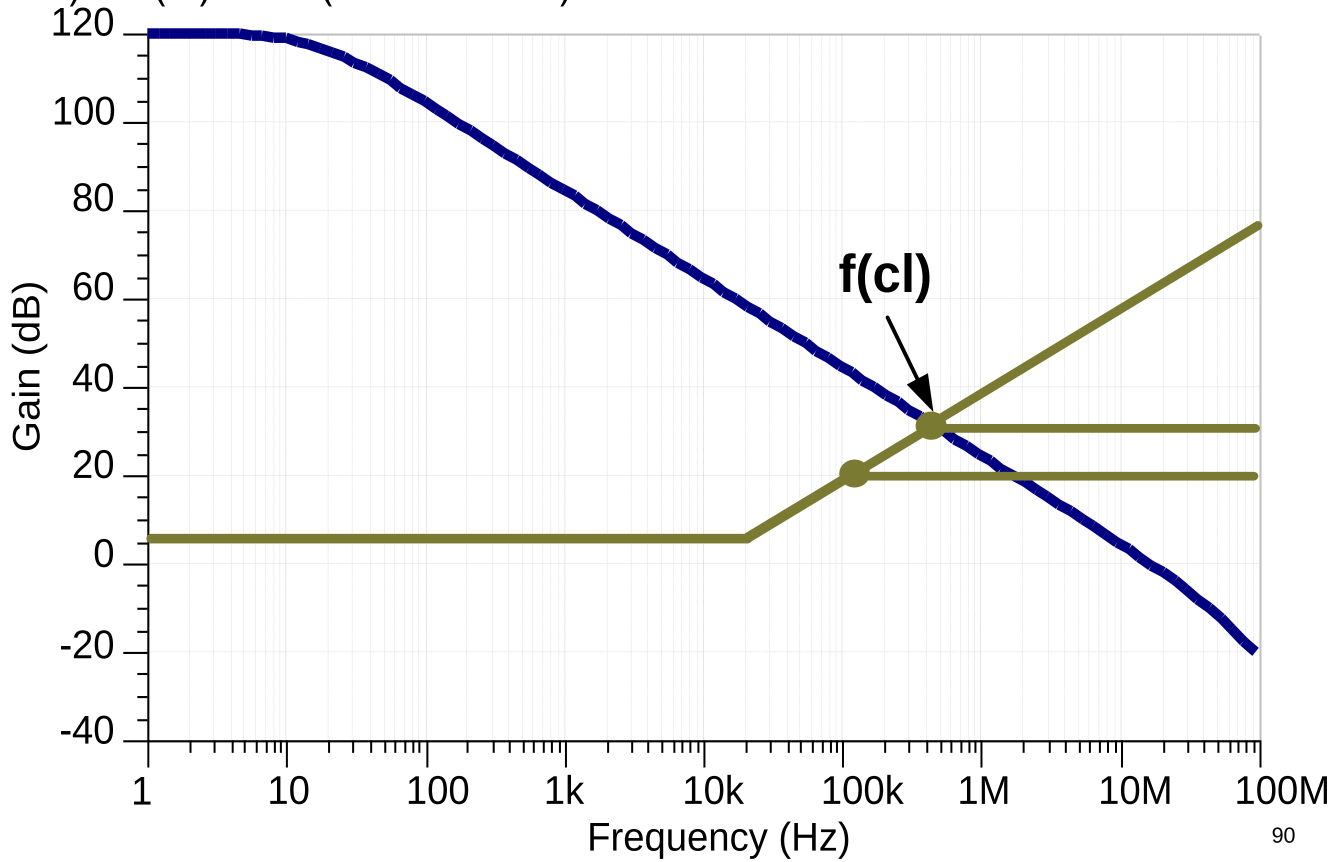
Ensure Good Phase Margin:

1.) Find f(cl)

2.) Set f(1/B pole) by setting Cf:

Good: f(1/B pole) ≤ f(cl)

Better: f(1/B pole) ≤ f(cl)/ 3.5 (~ ½ decade)



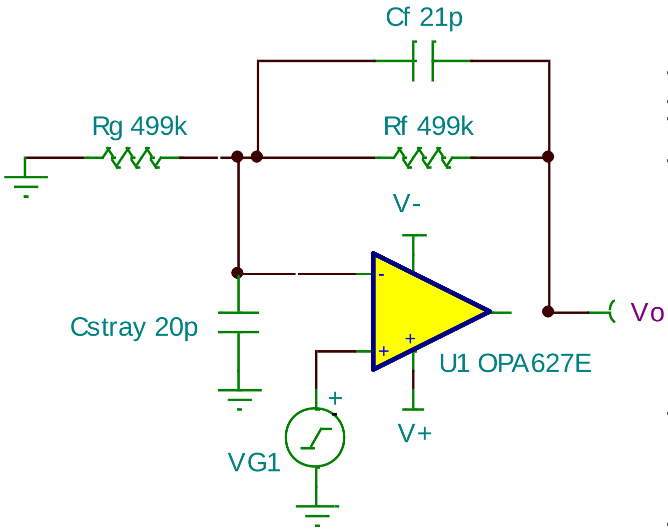
1/B Pole Equation:

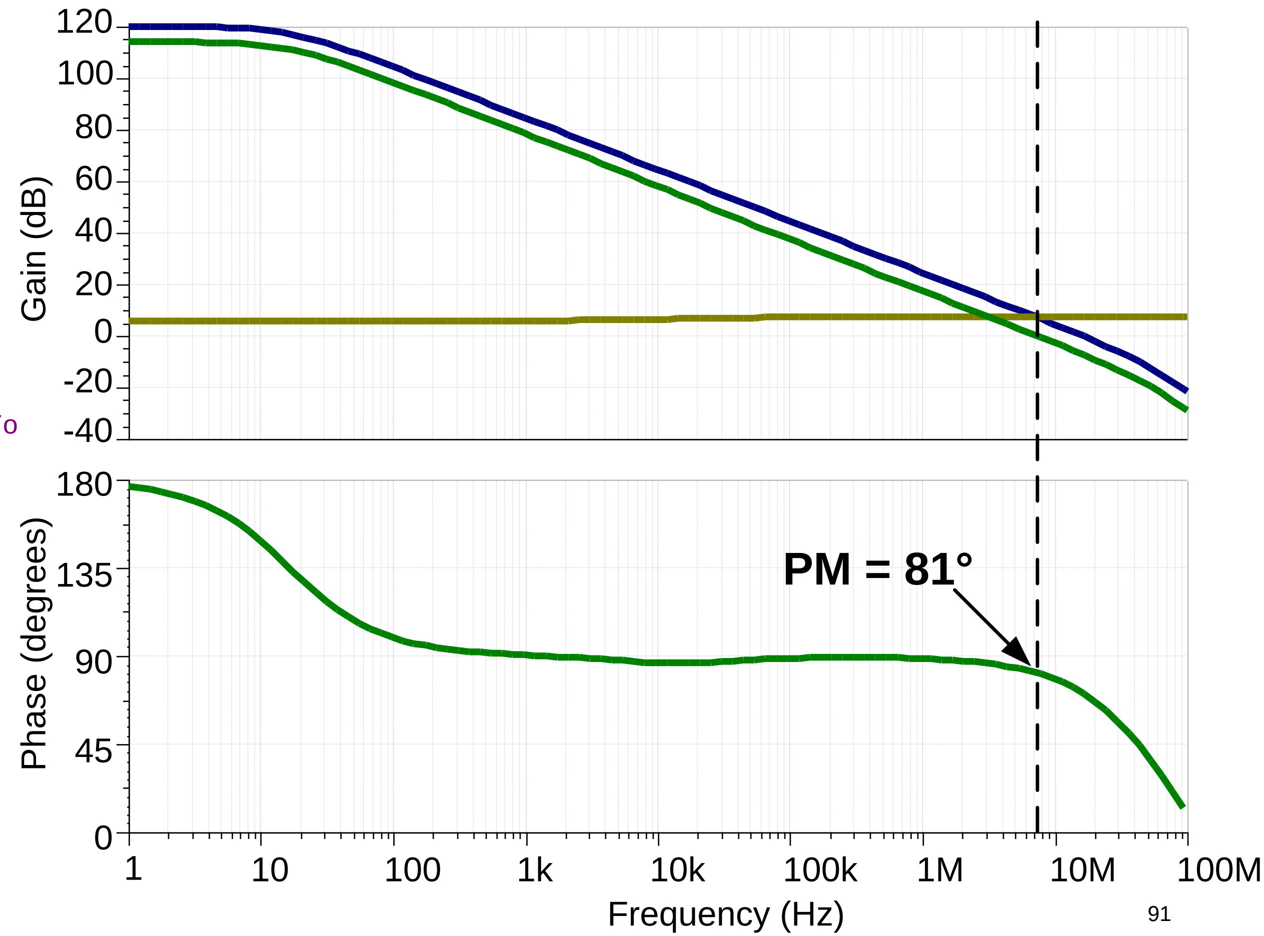
$$f(1/B\ pole) = \frac{1}{2 \cdot pi \cdot R_f \cdot C_f}$$

Method 1: Cf - Summary

Summary:

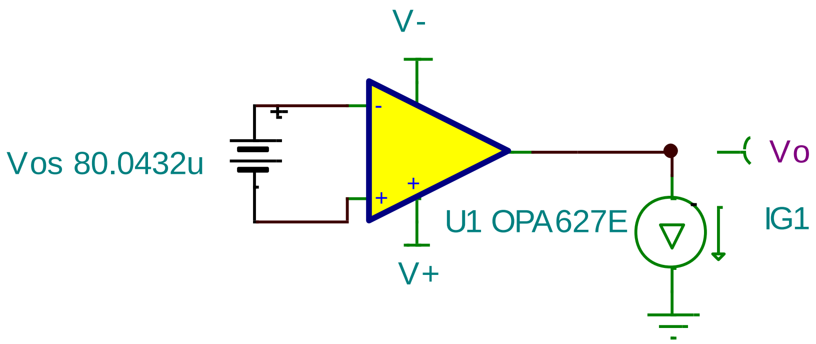
1.) Ensure stability by setting f(1/B pole) ≤ f(cl)/ 3.5 (~ ½ decade)

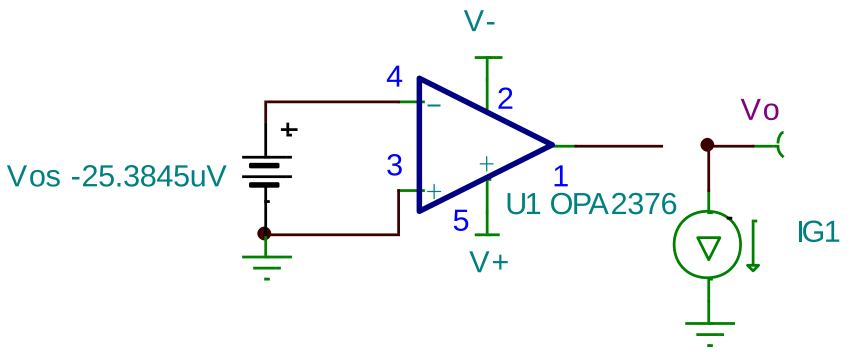


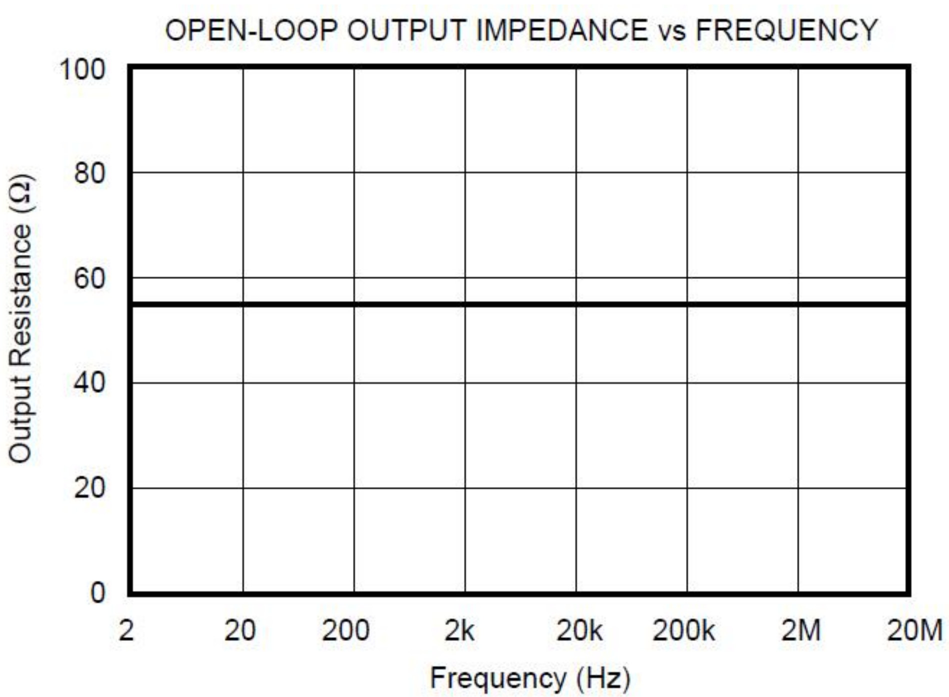


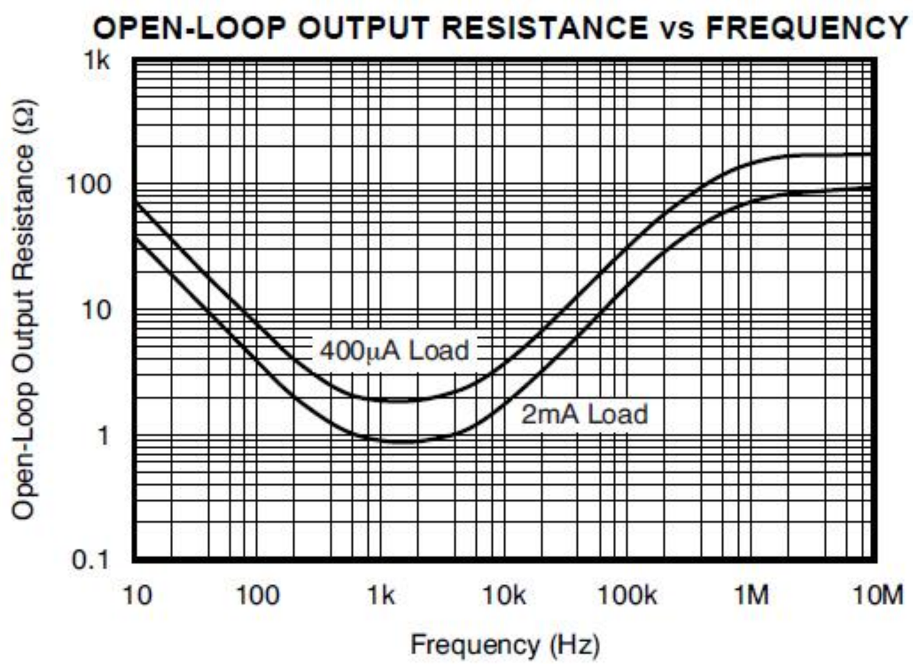
Ro vs. Zo

When Ro is really Zo!!

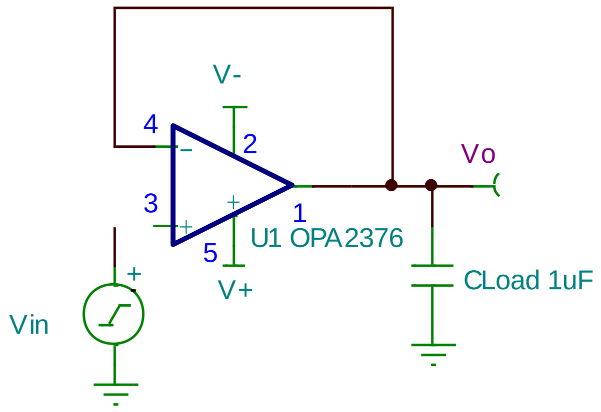


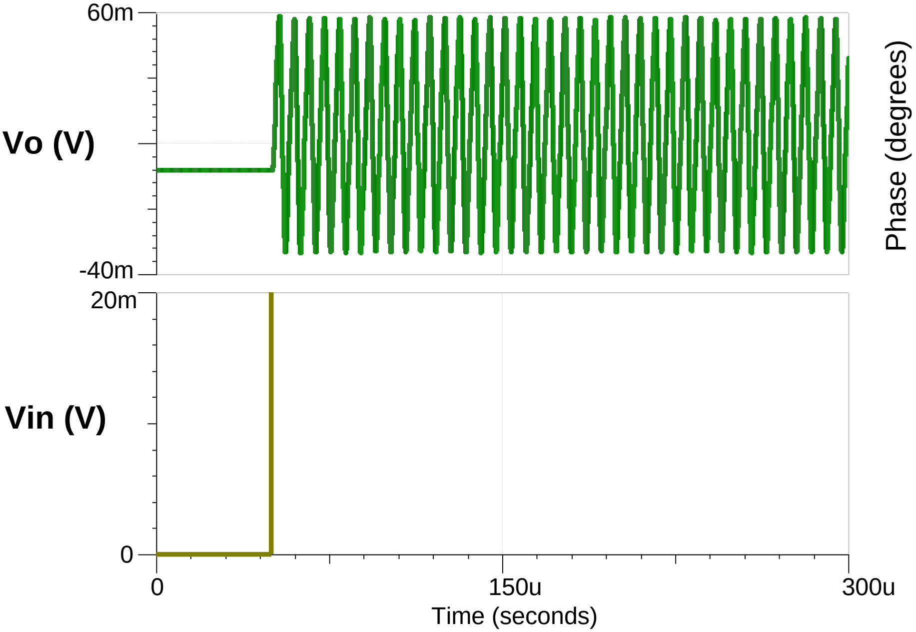


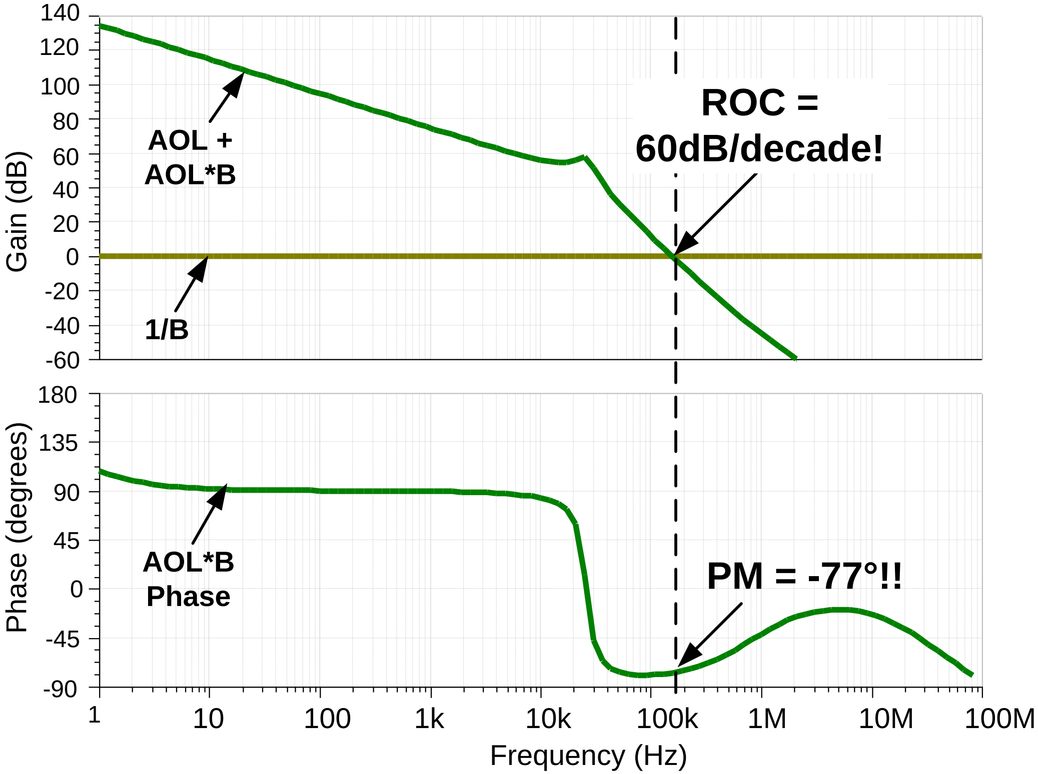




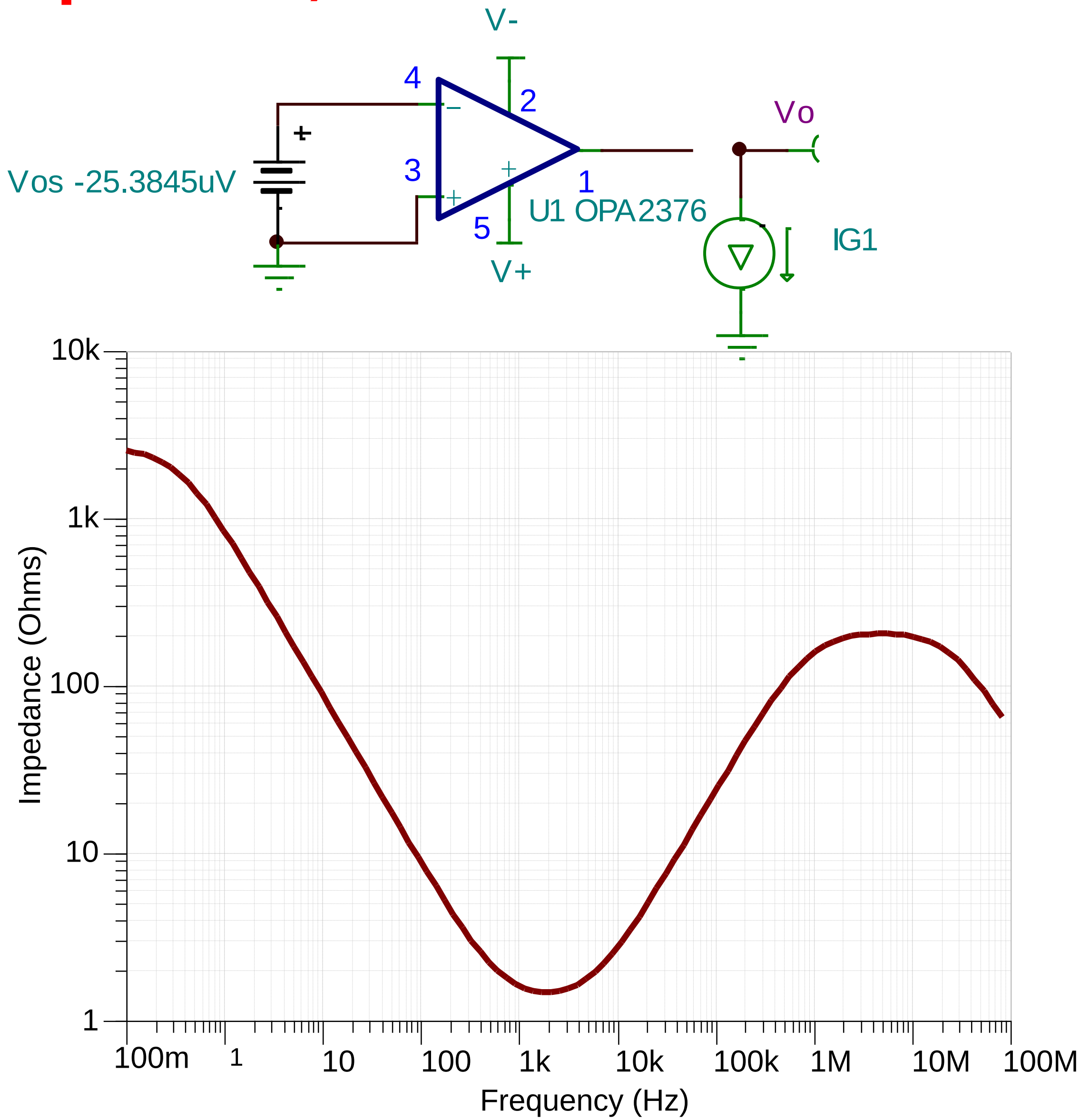
With Complex Zo, Accurate Models are Key!







With Complex Zo, Accurate Models are Key!



Questions/Comments?

Thank you!!

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Tim Green

PA Apps Team