Some redesign work on the ADC32J25 interface with the THS4541 + differential RLC filter

Michael Steffes, 11/7/2022

The redesign that Andrew Baek is very good and enough to start on –



Will come back to the FDA set up R’s in a bit, but let’s tune in the filter 1st,

Andrew had worked from my RLC filter design app note, I had moved this quite a lot forward over the years and opened up my latest design spreadsheet – one thing I had added not too long ago was an extract page to find the intended filter shape, here that is,



So these are our targets, now one thing I am not sure was in the original app note is there are two solutions for the LC values, one is high L, low C, the other is low L and high C. I always use the latter –

1. Lower L will push its self resonance F out
2. Higher C can swamp out the ADC input C,

Incidentally, here is the input Z that the ADC has, will have to adjust external RC for this,



There is also that CM current term into each side, probably not a concern here if we stay with about 50ohm series R in the filter

Here are the two solutions for LC targeting the current filter shape, these are exact here, I also later added a best fit routine for available RLC values,

 

And then if we continue the right side LC to a best fit solution (this is still single ended, need to make differential at the end)



And the best fit R’s



Now convert this to differential and back out the ADC input Z,

The diff C needs to be 91/2 = 45.5pF, back out the ADC 5.2pF and we need 40.3pF diff C – 39pF standard value. Diff R needs to be 2\*392= 784 ohm. Back out the ADC 6.5kohm, external needs to be 891ohm, use 887ohm E96 value. (Coilcraft L’s, Murata C0G C)

Ok, here is the filter piece, 60MHz about a butterworth.



Now the THS4541 FDA stage by itself, looks very promising, this is 6dB higher that from input RG1 as I have this set up to recover the matching loss, adding the filter and getting rid of that 2 in the dependent source (=1 instead) should get to about 0dB gain net,

Ok, this looks pretty promising, 0.4dB midband gain, and still right at 60Mhz F-3dB,



If I put in a +/-1V input square wave at 2Mhz, 5nsec edge, looks pretty good, this would be overdriving the ADC a little due to Gain a net 0.4dB, but just a test,

So this looks pretty good, I would increase the Vocm pin cap to 100nF.

