Stability Issues and Resolutions for High Speed Voltage Feedback Op Amps (The Signal Sped Up, Insight #6)

Michael Steffes – Sr. Applications Manager

March, 2019

While there has been a vast record of earlier work (ref. 1) on this topic, here we will combine a few concepts to show some emerging issues and paths to improve the Phase Margin (PM) for VFA stages that have slipped into perhaps an unsuitably low margin condition. Starting with the most ubiquitous issue of load capacitance induced problems, we will move on to how to improve that and correctly assess if indeed you are going in the right direction. What will emerge is perhaps a combination of approaches should sometimes be considered. Some of this will apply to CFA and FDA's as well, but those also have their own special issues considered in upcoming insights.

What is the Deal with Load Capacitance Induced Phase Margin Loss?

Most op amps and FDA's (with one exception, in insight #7) will, to varying degrees, be adversely affected by parasitic or intentional load capacitance. The literature approaches this effect from a number of directions – the best I have found is to think of it in terms of what that C_{load} is doing with a simple open loop output resistance (R_{ol}) to the overall Loop Gain (LG) phase. This simple approach breaks down again with more reactive open loop Z_{ol} (fig. 6, ref. 2) but is valuable for its intuitive insight.

An unloaded VFA op amp (the 2kΩ R_{load} is a typical sense path load) starts out with some Loop Gain (LG) Phase Margin (PM) that can then get degraded by adding a capacitive load. Figure 1 shows this example using a relatively simple OPA725 TINA model (ref. 3) with 2 real poles in the A_{ol} response and resistive open loop output R_{ol}. This gain of +2V/V case using 2kΩ values is already showing what looks like a lower phase margin than a simple 90deg. This is using the TINA simulator tool (ref. 4).

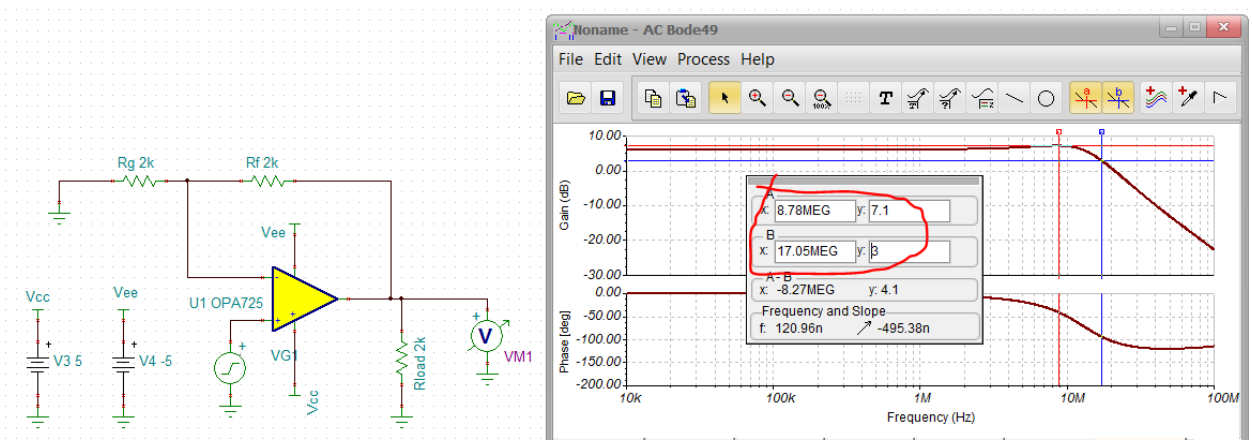


Figure 1. Gain of +2V/V closed loop response with no capacitive load.

The input capacitance in the model (9pF) is interacting with the $R_f||R_g$ driving impedance in the feedback network to introduce a feedback pole at 1/(2π*1kΩ*9pF) = 17.7MHz. The LG phase margin extract in Figure 2 (ref. 2) shows a LG=0dB x-over at 9.46MHz with 56deg phase margin.

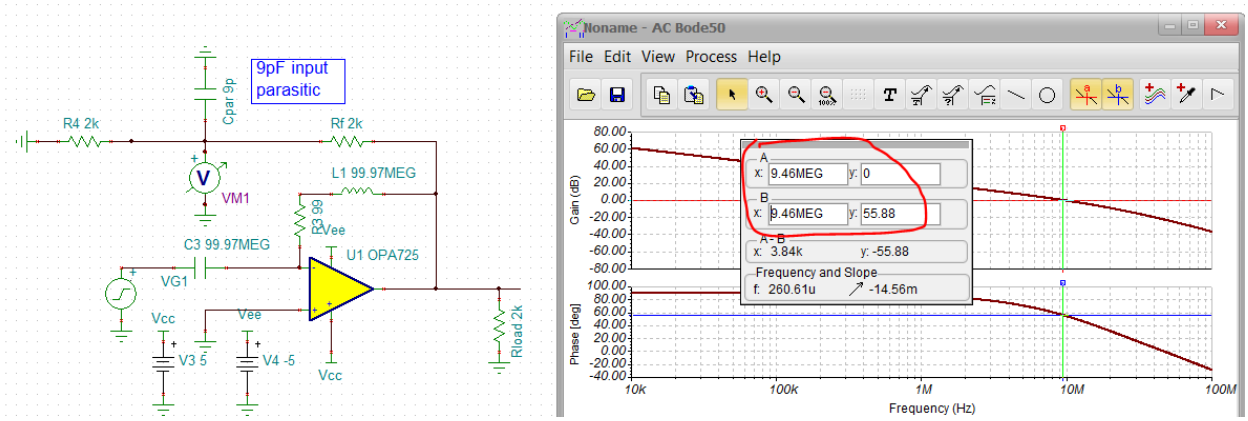


Figure 2. LG phase margin simulation including the 9pF input parasitic C in the OPA725 model.

The 1.1dB closed loop peaking in fig. 1 agrees with the expected peaking for 56deg phase margin (fig. 2, ref. 2) while the 17.1Mhz F_{-3dB} is reasonably close to the expected $1.6*F_{xover}$ = 15.1Mhz (fig. 4, ref. 2).

This simple design is already starting with a bit lower 56deg phase margin before any C_{load} is added – which will only move the phase margin down due to the pole that will be introduced by the 112ohm open loop output impedance in this model (fig. 6, ref. 2 for setup). Adding a 100pF load does indeed raise the peaking to 6dB suggesting a phase margin near 30deg (fig. 2, ref. 2). Adding a 100pF load to the fig. 2 LG simulation shows 31deg phase margin.

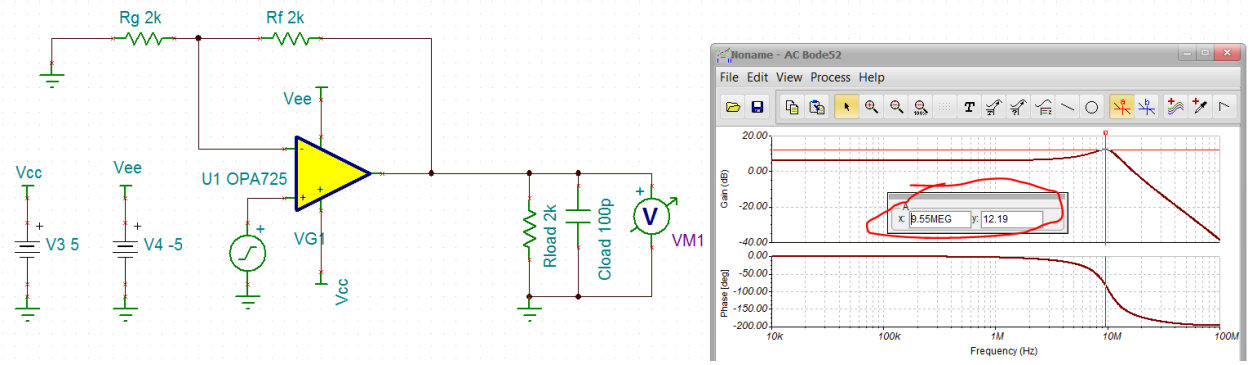


Figure 3. Direct 100pF load response peaking with gain of +2V/V using the OPA725

One way to see what is happening is to set up a simulation for the signal from the output stage to the inverting node and look at the response right at the output pin as shown in Figure 4. This is the β in the LG where that direct 100pF capacitive load has introduced a pole in the β at 15MHz – which becomes a zero in the Noise Gain (NG) response. The phase of that zero in the NG (a positive number now) is subtracted from the op amp Aol to get the LG phase. Or, equivalently, the β phase is added to the Aol phase shift.

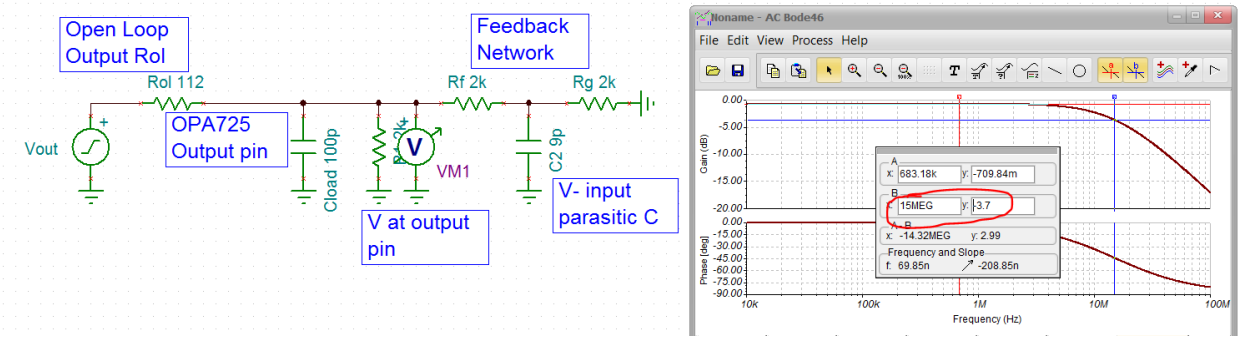


Figure 4. Response at output pin with direct capacitive load.

The most common fix for phase margin loss due to capacitive loads (ref. 1d) is to add a series R_{iso} before that C_{load}. This acts to change the simple pole at the output pin to a pole/zero pair pulling the phase shift back up at the output pin before the feedback signal heads back the inverting node. Since this example starts out with only 56deg phase margin, adding an R_{iso} cannot improve the phase margin beyond that. However, targeting an improvement from 31deg to 45deg adding an R_{iso} before the 100pF in the LG simulation of fig. 2 shows 120Ω would be required. Starting out with an unloaded PM > 65deg would allow much lower R_{iso} values to be used as capacitive loads are added (fig. 16 below). Adding an R_{iso} to the circuit in fig. 5 shows we have added a zero to the β phase response – it is this pulling up of the phase that makes this approach effective.

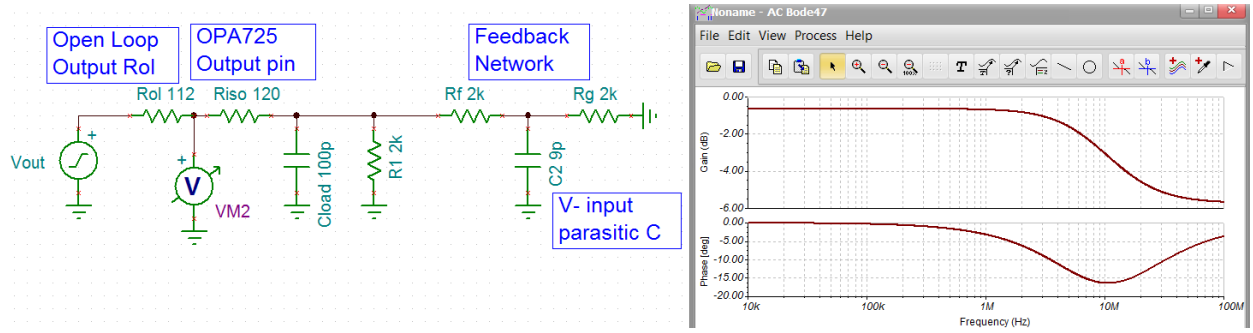


Figure 5. Response at output pin with Riso added before Cload

Putting R_{iso} = 120Ω into the closed loop gain of +2V/V OPA725 circuit of Fig.6 certainly reduced the peaking where the 2.7dB peaking over the 6dB DC gain at the output pin approximately agrees with a 45deg phase margin peaking (fig. 2, ref. 2). The response at C_{load} is now attenuated to 5.52dB DC gain by the 120Ω R_{iso} where that simple RC reduces the peaking at the C_{load} to 1.6dB.

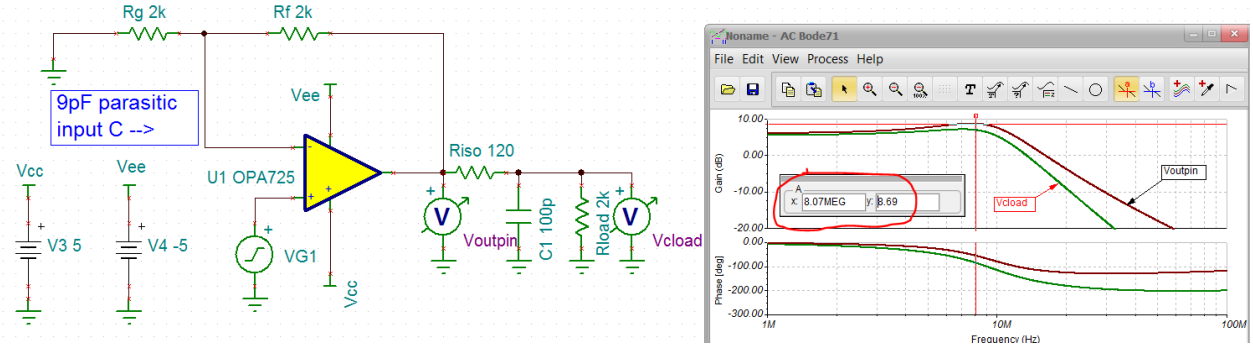


Figure 6. Adding an R_{iso} to improve phase margin and reduce peaking driving a C_{load}.

Changing a simple pole at the output pin by adding an R_{iso} into a pole/zero pair can also be done effectively by adding the R in series to ground with the C_{load} (and out of the output pin line) when that is an option. This is often seen in SAR reference line buffer designs such as Figure 7. (fig. 10, ref. 5). Here, a composite amplifier circuit using the OPA837 (ref. 6) as the output stage drives directly into the 10uF load capacitors. This OPA837 circuit also improves the capacitive load phase margin using the dual loop approach (fig. 32, ref. 7) but then adds 0.2Ω in series with each of the load caps to ground as well. Testing just this OPA837 output stage for phase margin showed 49 degrees.

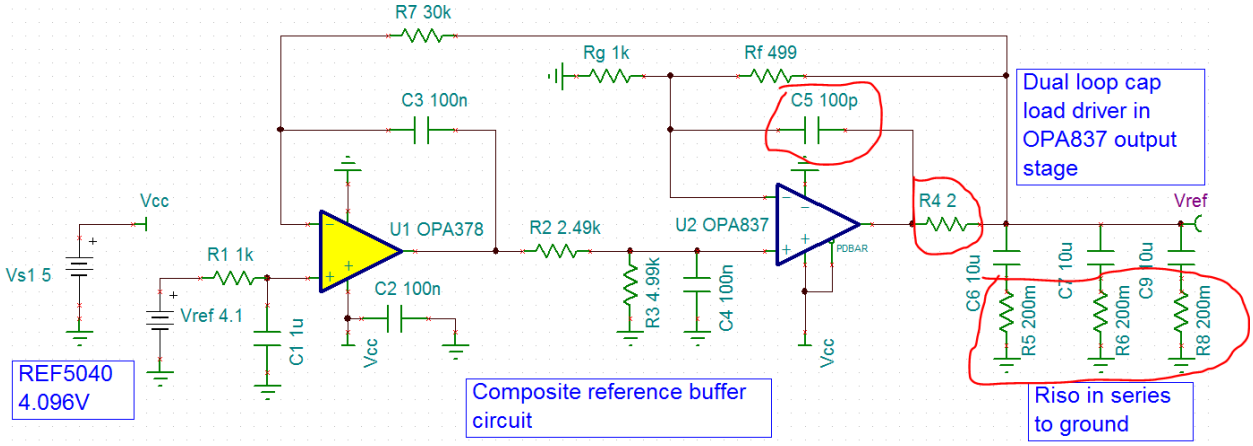


Figure 7. Adding series R to ground with the filter capacitors in a SAR reference buffer design.

When the load capacitance is known, and cannot endure the effects of an outside the loop R_{iso}, the dual loop approach can be used. This technique to directly driving a capacitive load closes the loop at DC with the outer resistive loop to get gain accuracy to the capacitive load. The inner loop effectively shorts out the outer loop as the frequency increases putting the op amp in a unity NG condition with the R_x inside the loop isolating the C_{load} from the op amps' open loop output impedance.

There are several descriptions of this design (ref.1c,e,f), but the simplest approach is shown in Eq. 1&2 (from fig. 32, ref. 7). Here, a desired closed loop Butterworth F_{-3dB} is selected to be well below the op amp Gain Bandwidth Product (GBP) and the inside the loop R_x and feedback capacitor C_f solved as shown.

$$R_x = \frac{1}{2\pi C_L \sqrt{2}\, f_{-3dB}} \qquad \text{Eq.1}$$

$$C_f = \frac{\sqrt{2}}{2\pi R_f\, f_{-3dB}} \qquad \text{Eq.2}$$

Figure 8 shows an example using the OPA725 driving a 1nF load and targeting a 2.5MHz F_{-3dB}. Running non-inverting gain of +2V/V this is approximate with its 1dB peaking and 3.1MHz F-3dB due to the 9pF parasitic input C on the inverting input. Placing a 9pF compensating capacitor across the feedback resistor flattens this response (fig. 16). Figure 8 also shows the op amp output pin is peaking even more -but the simple $1/(2\pi R_x C_{load})$ pole rolls this off a bit. Using this approach, you should check your step response at the op amp output pin to confirm clipping is not occurring. If this slight peaking is not acceptable, simply increase C_f until the desired response shape is achieved and/or add a compensating capacitor across R_f (fig. 16).

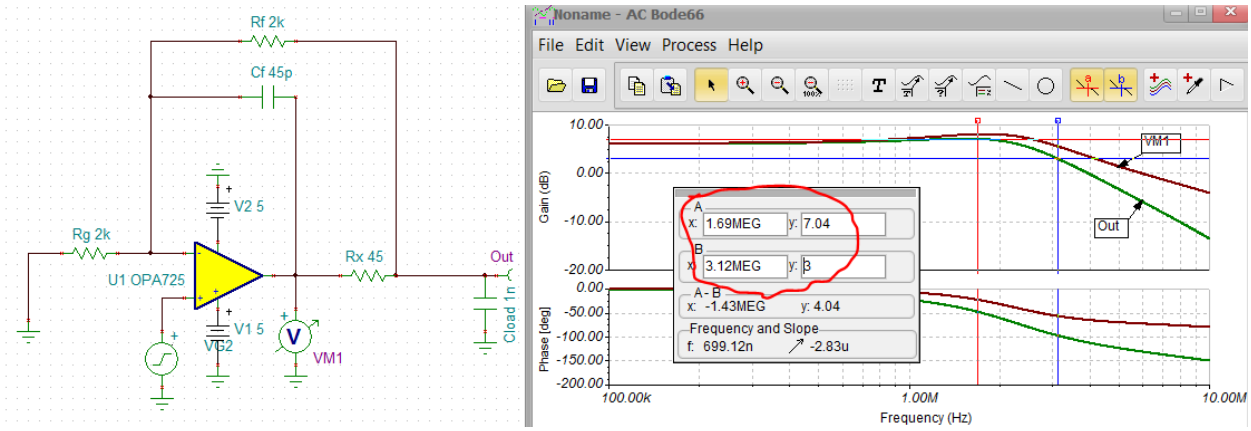


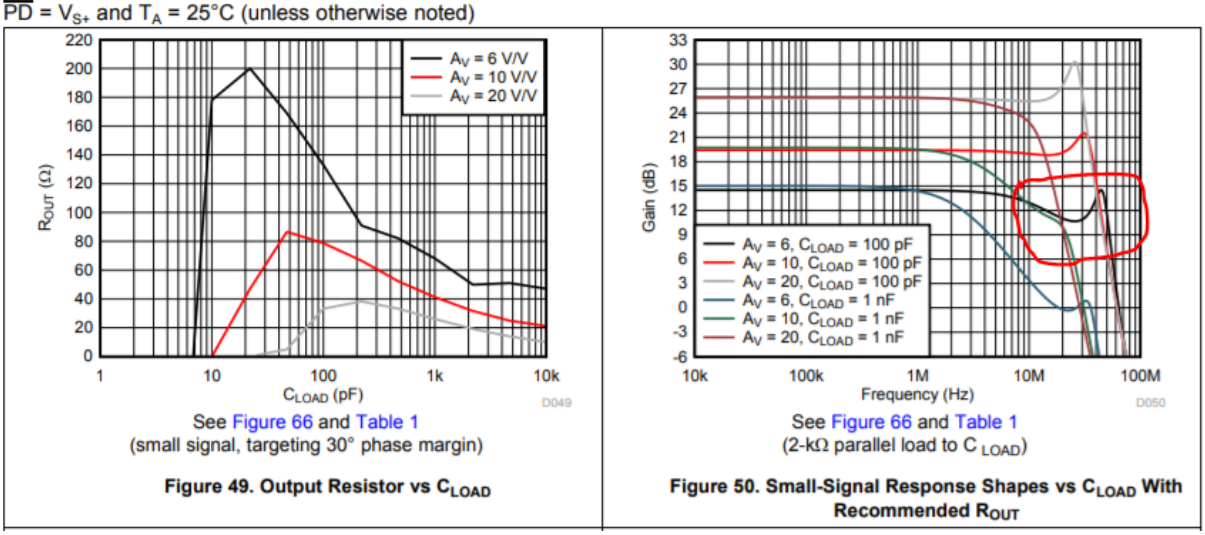
Figure 8. Non-inverting gain of +2V/V dual loop capacitive load drive with the OPA725.

Emerging Capacitive Load Drive Issues with Newer Parts and Updated Resolutions

The R_{iso} and dual loop approaches have been pretty standard where the latter only applies to unity gain stable VFA. So what options are available when you need to drive a capacitive load using a decompensated op amp like the recent OPA838 (ref. 8)? First, a hidden risk inside the typical R_{iso} vs. C_{load} plots shown in Figure 9 (ref. 8) where the circled curve should give cause for caution. The total measured response is always a combination of whatever peaking is happening at the output pin rolled off by the $1/(2\pi R_{iso} C_{load})$ pole. The circled curve is showing an RC rolloff at 12.2MHz that is then getting overridden by what might be significant peaking at the output pin.

Typical Characteristics: Over Supply Range (continued)

$\overline{PD}$ = V_{S+} and T_A = 25°C (unless otherwise noted)



See Figure 66 and Table 1
(small signal, targeting 30° phase margin)

Figure 49. Output Resistor vs C_{LOAD}

See Figure 66 and Table 1
(2-kΩ parallel load to C_{LOAD})

Figure 50. Small-Signal Response Shapes vs C_{LOAD} With Recommended R_{OUT}

Figure 9. Recommended R_{iso} vs C_{load} parametric on gain from the OPA838 data sheet.

The fact there are different R_{iso} curves parametric on gain in fig. 9 is another way of saying what you need to improve the phase margin depends a lot on where you are starting from. Hence, higher gain settings start out with more phase margin and will show lower required R_{iso} for the same C_{load}. However, zooming in on that gain of +6V/V 100pF load curve suggesting an R_{iso} = 130Ω, shows there is perhaps more output pin peaking than desired in Figure 10.

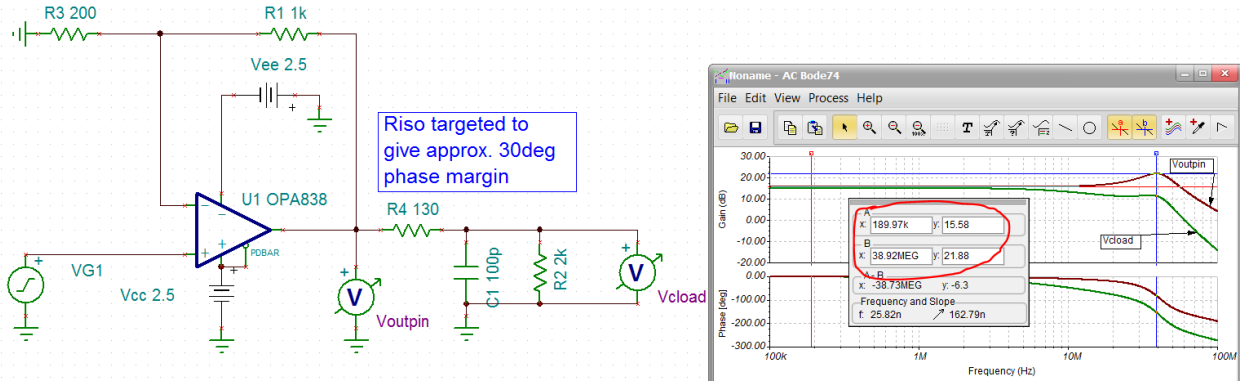


Figure 10. Closed loop gain of +6V/V with 130Ω Riso into 100pF load.

This is another instance where the peaking at the op amp output pin is much higher than the RC rolled off version measured at the C_{load}. Figure 11 shows the LG simulation for this where the 28deg phase margin corresponds to the 6.2dB peaking in Figure 10. (fig. 2, ref. 2). The LG meter is rotated in fig. 11 to report phase margin directly. This 28deg phase margin closely matches the reported 30deg target in fig. 8.

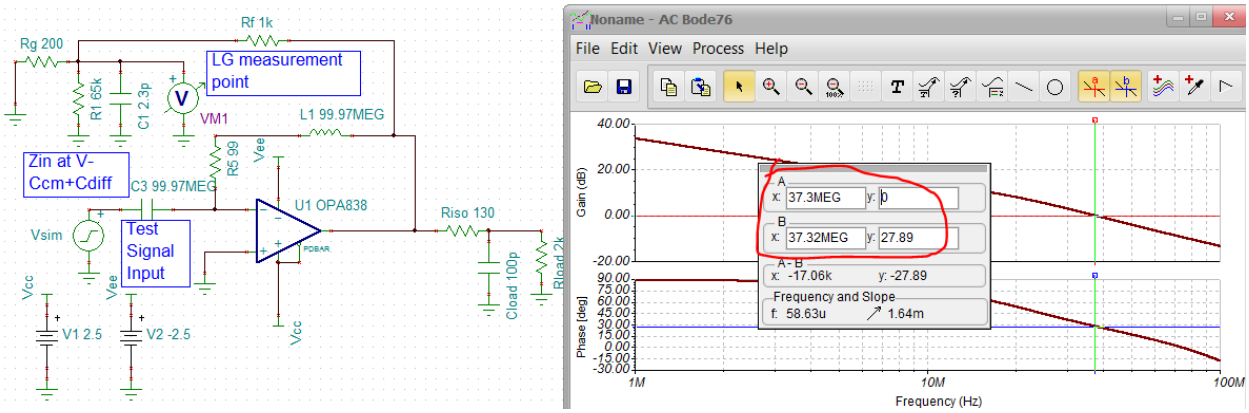


Figure 11. LG phase margin extract for the OPA838 gain of +6V/V, 100pF load with 130Ω R_{iso}.

This circuit is peaking at the op amp output 6dB at about 39MHz where the simple $1/(2\pi R_{iso}C_{load})$ pole is rolling that off at 12MHz. Beware this hazard for faster parts showing a higher recommended R_{iso} than you might expect. It is always best to run a LG phase margin test confirm adequate margin and not depend only on the final C_{load} response.

Shaping the Noise Gain to Higher Initial Phase Margin

Many of the older references note that operating with higher noise gain (before the C_{load} is added) can improve the initial phase margin and allow lower R_{iso}. Those suggestions are normally fixed resistors or RC networks across the inputs – both increase the broadband noise. If the design can operate inverting, an older inverting compensation technique can be applied here to shape the noise gain up over frequency. This has the benefit of retaining the lower frequency loop gain, lower noise, and the higher slew rate of a decompensated device while shaping to a higher noise gain only at higher frequencies. This inverting compensation (recently rebuilt from the August 1997 original and reposted on EDN, ref. 9) can be used to shape to a higher phase margin with no load to allow lower R_{iso} values when a capacitive load is added. Let's set up some targets for the OPA838 and see what this will take.

1. Gain = -5V/V with Rg = 400Ω, Rf = 2kΩ, Low frequency NG1 = 6 (min. specified gain)
2 High frequency noise gain target NG2 = 24V/V --$(1+C_s/C_f)$ sets this.
3 Cload = 100pF
4 Riso = ??

Using the design equations below (page 12, ref. 10), and the 300MHz GBP for the 1mA OPA838 (ref. 8) , first find the Z_o frequency for this nominally 2nd order Butterworth response solution – Z_o is where the projection of the rising portion of the noise gain going down in frequency intersects 0dB in the Bode LG plot (ref. 9).

$$Z_0 = \frac{GBP}{NG_1^2}\left[\left(1-\frac{NG_1}{NG_2}\right)-\sqrt{1-2\frac{NG_1}{NG_2}}\right] \qquad \text{Eq. 3}$$

Zo = 357kHz

Now solve for the required capacitor across the 2kΩ feedback resistor. This is a case where the reactive open loop output impedance in the OPA838 model will interact with this feedback C_f to yield results

slightly mismatching the 2nd order phase margin to Q estimates (ref. 2) as this becomes a >2nd order situation.

$$C_f = \frac{1}{2\pi R_f Z_0 NG_2}$$ Eq. 4

C_f = 9.3pF

And then to hit the higher frequency noise gain of 24V/V, add a capacitor on the inverting node to ground -

$$C_s = (NG_2 - 1)C_f$$ Eq. 5

Which gives

C_s = 214pF where the approximate closed loop bandwidth (before C_{load} is added) will be -

$$F_{-3dB} \cong \sqrt{Z_0 GBP}$$ Eq.6

F_{-3dB} ≈ 10.4MHz where the actual increase in the noise gain due to the noise gain zero starts at (ref. 9).

$NG_1 * Z_o$ = 2.14MHz.

This inverting circuit, with the compensation capacitors, is shown in Figure 12 where the resulting shape looks very close to the expected Butterworth with 11.3MHz F_{-3dB}. Without these NG shaping caps, the closed loop response is peaking approximately 3.3dB with much higher bandwidth. The NG shaping caps are improving the phase margin at the cost of lower closed loop bandwidth.

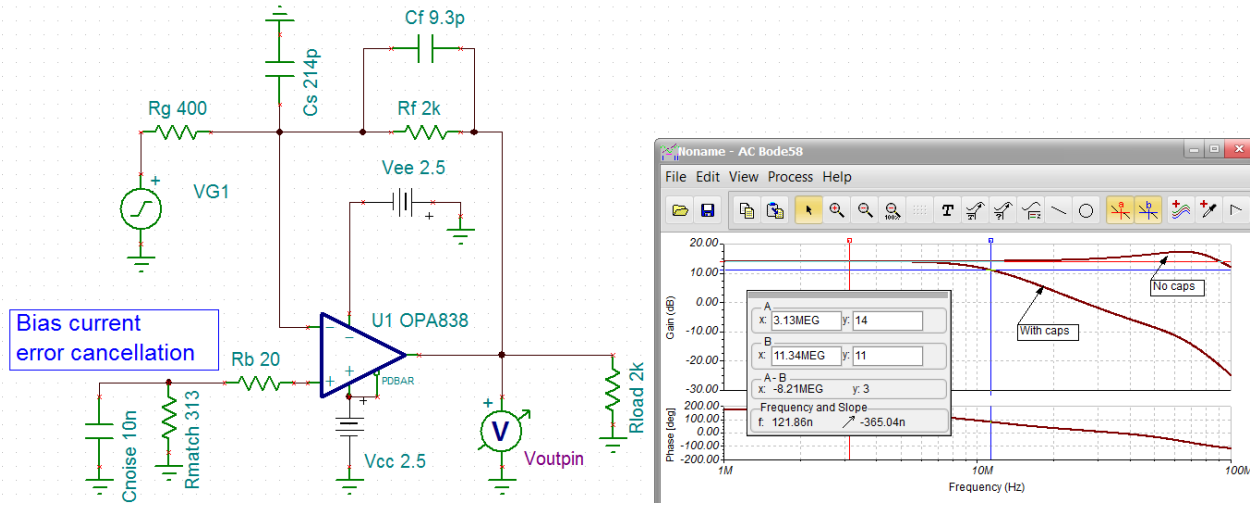


Figure 12. Response shape for the gain of -5V/V with inverting compensation using the OPA838

Now, before we add a C_{load} and find the right R_{iso}, run a LG simulation in Figure 13 where the Butterworth would be near 65deg phase margin. The actual results show 58deg phase margin due to the

reactive Z_{ol} interacting with C_f – but a better place to start as the capacitive load is added and R_{iso} resolved than the 39deg implicit in the 3.3dBp peaked curve in fig. 12.

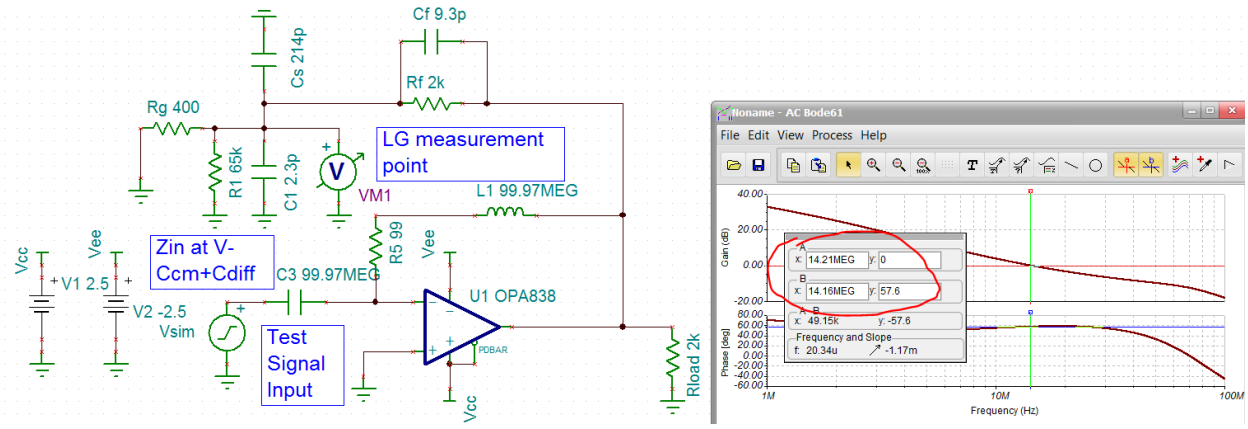


Figure 13. LG phase margin for the compensated circuit of fig. 12.

Going back to the closed loop circuit and adding the C_{load} allows a much lower (than fig. 10) R_{iso} = 70Ω to be found that shows a more well controlled response shape at both the output pin and C_{load} points. Figure 14 shows the bandwidth has extended out to 18.8MHz in what is clearly more than a 2nd order response shape due to the peaking Z_{ol} in the OPA838 model.

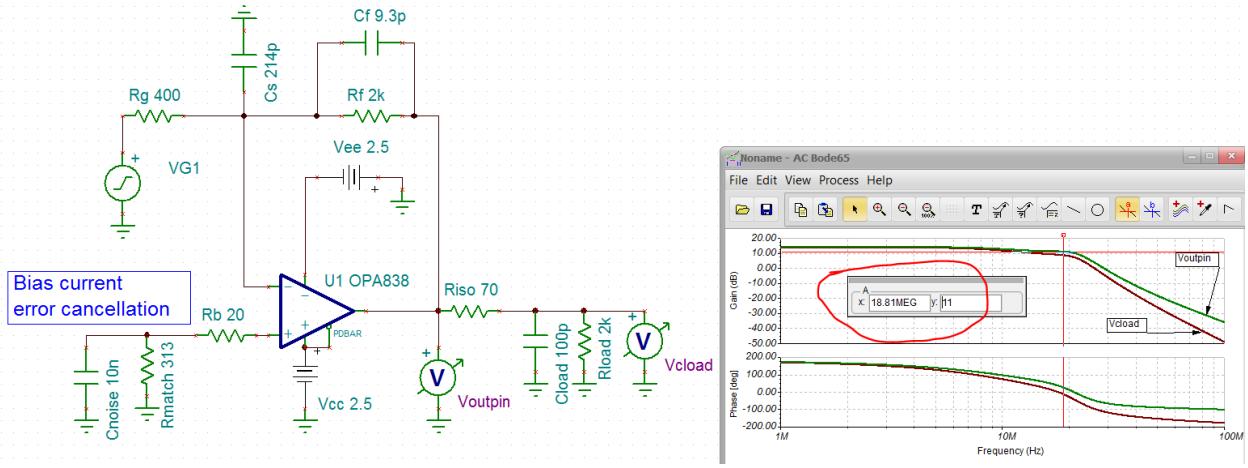


Figure 14. Closed loop inverting with noise gain shaping giving lower R_{iso} to a 100pF load.

This shaped noise gain approach appears to give an excellent response shape with the 100pF capacitive load and R_{iso} = 70Ω. This is essentially moving the core op amp into a better phase margin place before the R_{iso} & C_{load} are added and could also be applied to unity gain stable op amps if needed. It is peaking the noise gain over frequency, so check the spot noise at the output pin and capacitive load. Figure 15 shows the added simple $1/(2\pi R_{iso}C_{load})$ pole at 23MHz is rolling off the more peaked spot noise at the op amp output pin that starts rising at the noise gain zero of 2.1MHz.

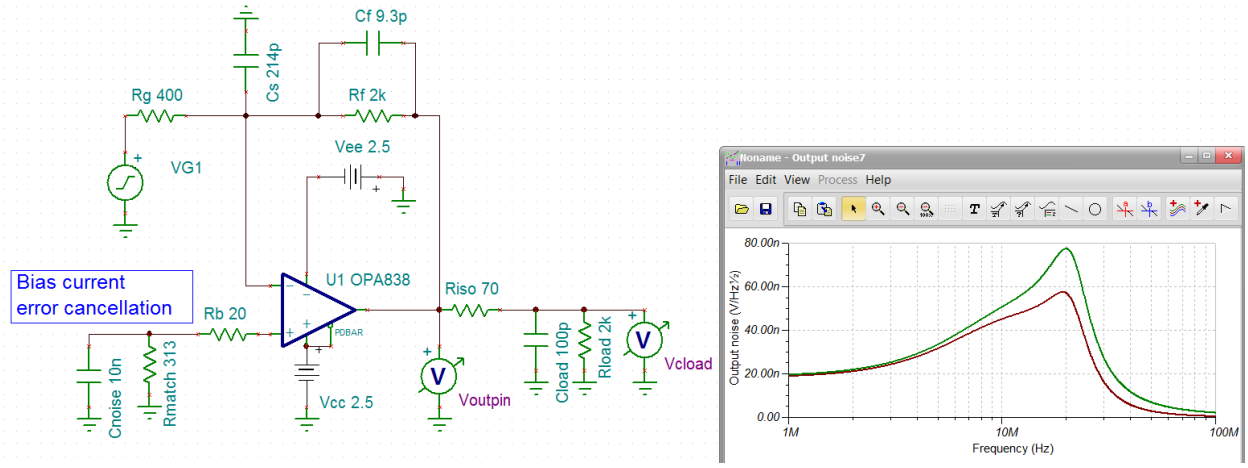


Figure 15. Spot output noise for inverting compensated capacitive load driver.

Improving Response Flatness for the Non-inverting Case with an Inverting Node Parasitic Pole

Of course, these two capacitors are identical topologically to the typical suggestion to improve flatness in the non-inverting case when the there is added phase shift due to capacitance on the inverting node interacting with higher $R_f||R_g$ source driving that node – as in Figure 1. Essentially, that suggestion (ref. 11) is setting $R_gC_s = R_fC_f$ making the feedback β flat across frequency – exactly the same operation when tuning the flatness of a 10X scope probe.

Adding a 9pF feedback capacitor to the non-inverting gain of +2V/V of figure 1 indeed gives a much flatter response in fig. 16. The noise gain is now flat at 6dB across frequency and the resulting closed loop response depends only on the open loop phase shift at crossover.

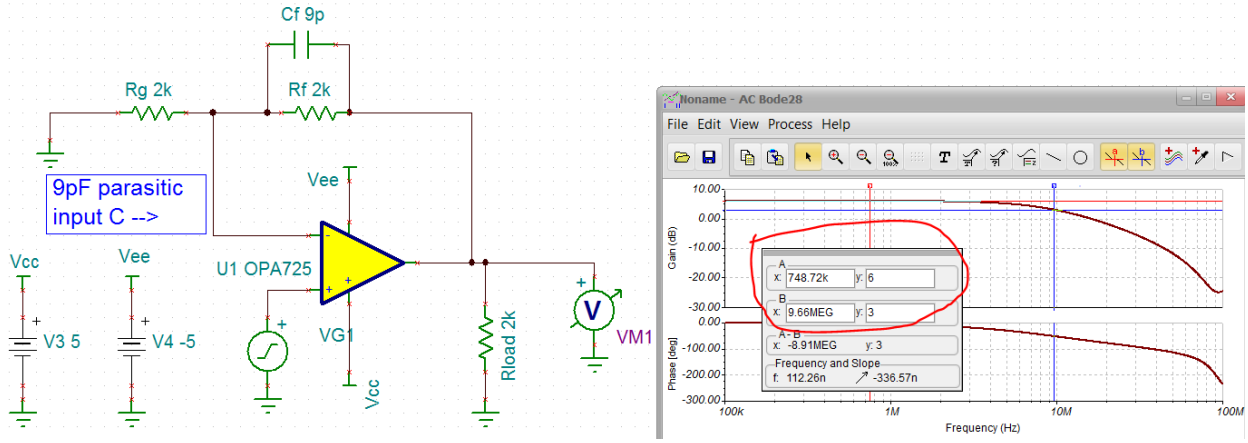


Figure 16. Non-inverting parasitic input C compensation with a feedback C_f.

Taking this updated circuit into the LG phase margin simulation now shows a very good 82deg phase margin in Figure 17. At this F_{xover} of 10.8MHz, the higher pole in the OPA725 Aol model has only added 8deg of added phase shift from the 90deg arising from the dominant pole where the NG is now adding no phase shift.

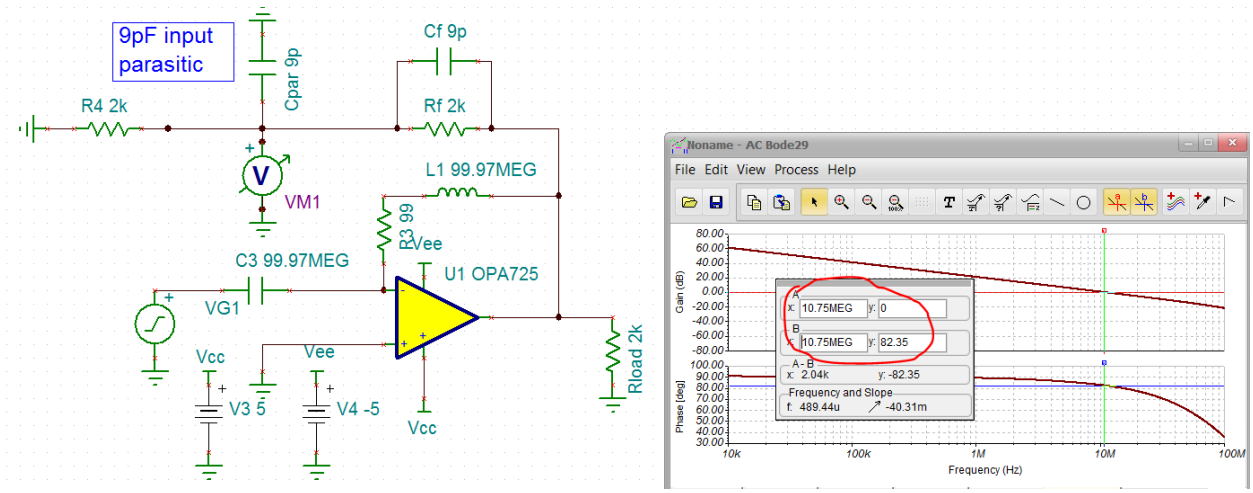


Figure 17. Loop Gain (LG) phase margin with compensating feedback capacitor.

This is another technique to improve an already low phase margin in the non-inverting case before adding the capacitive load and finding R_{iso}. With this pre-conditioning, the required R_{iso} adding a 100pF will be much lower than the 120Ω of fig. 6. Adding the 100pF C_{load} and tuning R_{iso} for 60deg phase margin shows only 30Ω is now required, giving the closed loop response of Fig. 18.

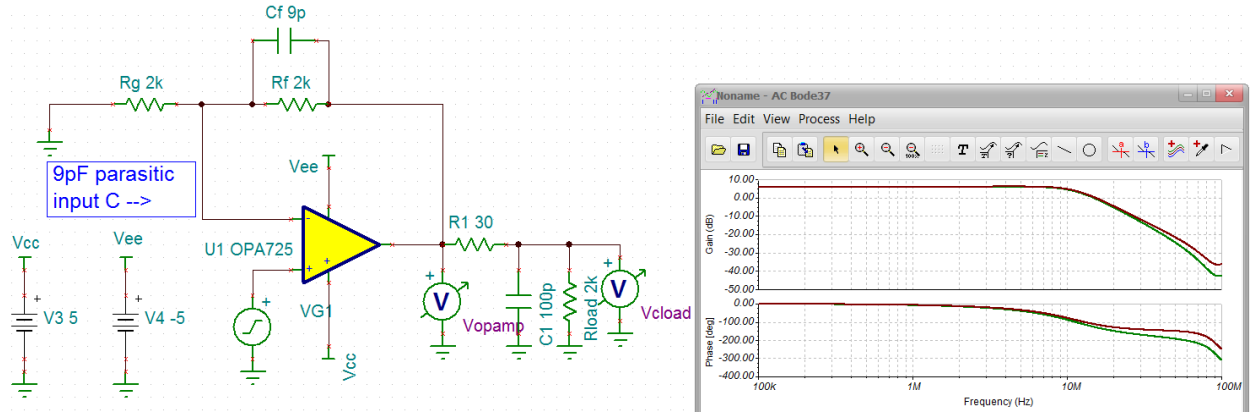


Figure 18. Lower R_{iso} solution driving 100pF using phase margin pre-conditioning.

Another way to approach this loss of phase margin due to inverting input parasitic C issue is to constrain the resistor values to lower levels to limit this effect. As part of the resistor value solution in the Intersil (now Renesas) online non-inverting op amp design tool (ref. 12), I developed a solution (eq.7) for the maximum R_f to limit the loss of phase margin due to the β pole back to the inverting input capacitance to < 10deg.

$$R_{f_{phase}} \leq \frac{A_v^2}{2\pi C_p (4 * GBP)}$$

Eq. 7

This limit applied to the A_v= 2V/V circuit for the OPA725 with C_p = 9pF and a 23MHz GBP (fig.10, ref.2) will suggest a maximum R_f < 770Ω. Re-running a simple gain of +2V/V simulation with Rf=Rg=750Ω will give the flat response of fig. 18 – compare this to fig. 1 with 2kΩ R's.

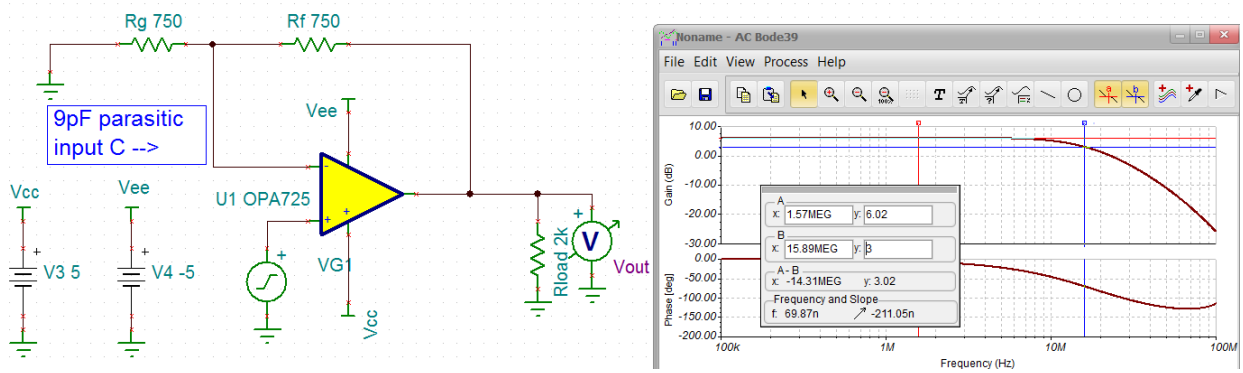


Figure 19. Lower Rf gain of +2V/V response using the OPA725

Testing the phase margin for this yields 72deg - exactly 10deg lower than the perfectly equalized NG of fig. 17. This phase margin loss limit (eq.7) was one of several constraints considered in assembling Table 1 of recommended R_f and R_g values across non-inverting gains in the OPA838 data sheet (ref. 8). Adding a C_{load} =100pF in fig. 19 would now require a lower R_{iso} (than fig. 6) with R_f=R_g=750Ω to hit a Butterworth response at the output pin.

There are many contributors to VFA closed loop phase margin. When adding a capacitive load, there are several options to tune into an improved phase margin. First, for either a non-inverting or inverting design, consider "pre-conditioning" the unloaded phase margin to a higher level to get a lower required R_{iso} when the C_{load} is added as described here. Where a C_{load} must be driven with no R_{iso}, consider the dual loop approach with the design equations shown here or putting that R_{iso} in series with the load capacitor to ground where possible. Up next – stability issue and resolutions for Current Feedback Amplifiers (CFAs).

References for stability issues and resolutions for VFA op amps.

1. Prior work relating to VFA capacitive load stability
    a. Bruce Trump "The Signal" part 12, Aug. 2013, "Why op amps oscillate: an intuitive look at two frequent causes" https://e2e.ti.com/blogs_/archives/b/thesignal/archive/2012/05/23/why-op-amps-oscillate-an-intuitive-look-at-two-frequent-causes
    b. LTC Application note 148, "Does your op amp oscillate" Barry Harvey, Sept. 2014, https://www.analog.com/media/en/technical-documentation/application-notes/an148fa.pdf
    c. TI Analogwire, "Do-it-yourself: Three ways to stabilize op amp capacitive loads", Collin Wells, Aug. 2017, https://e2e.ti.com/blogs_/b/analogwire/archive/2017/08/01/do-it-yourself-three-ways-to-stabilize-op-amp-capacitive-loads
    d. TI Designs, "Capacitive Load Driver Solution using an Isolation Resistor", Peter Semig, Timothy Claycomb, Nov. 2014, http://www.ti.com/lit/ug/tidu032c/tidu032c.pdf

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