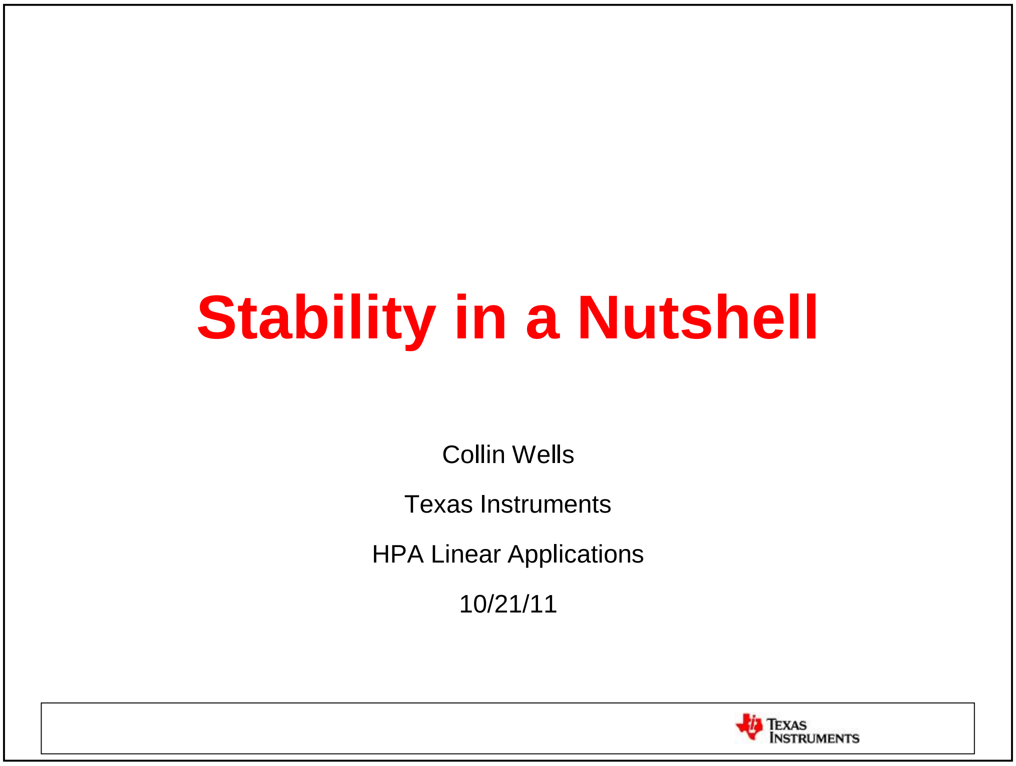

Stability in a Nutshell

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HPA Linear Applications

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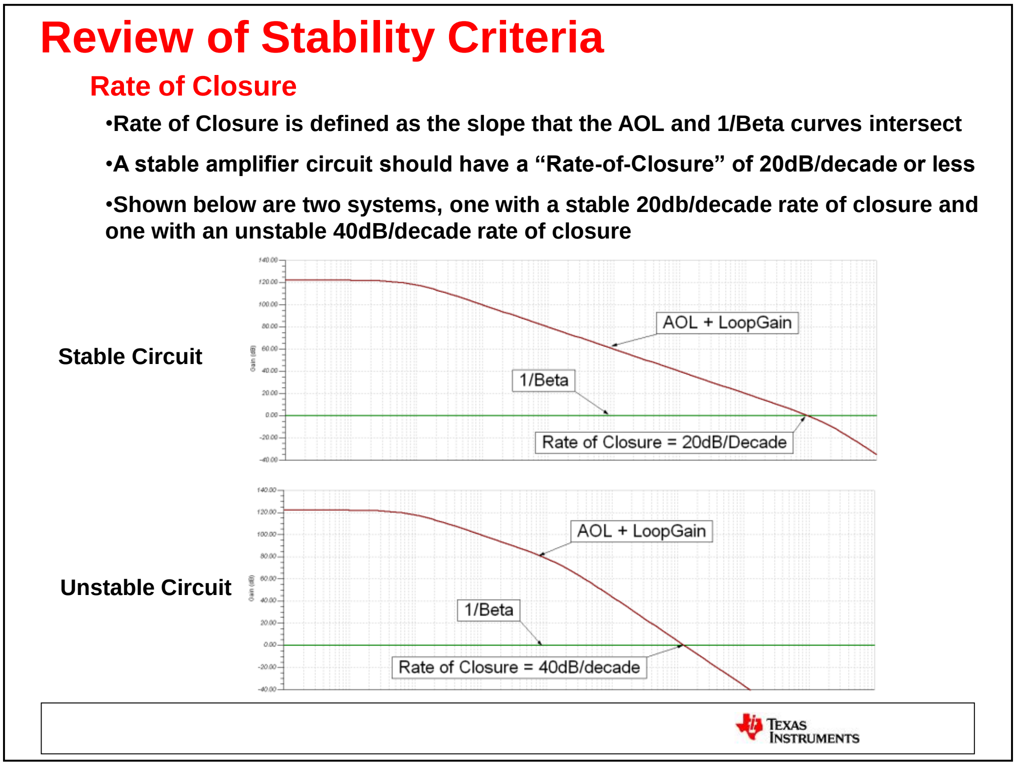
This presentation will step through an overview on RTD sensors and their non-linearity, RTD measurement circuits, Analog Linearization and output methods, and Digital acquisition and lineariziation.



Review of Stability Criteria

Rate of Closure

- Rate of Closure is defined as the slope that the AOL and 1/Beta curves intersect
- A stable amplifier circuit should have a “Rate-of-Closure” of 20dB/decade or less
- Shown below are two systems, one with a stable 20db/decade rate of closure and one with an unstable 40dB/decade rate of closure

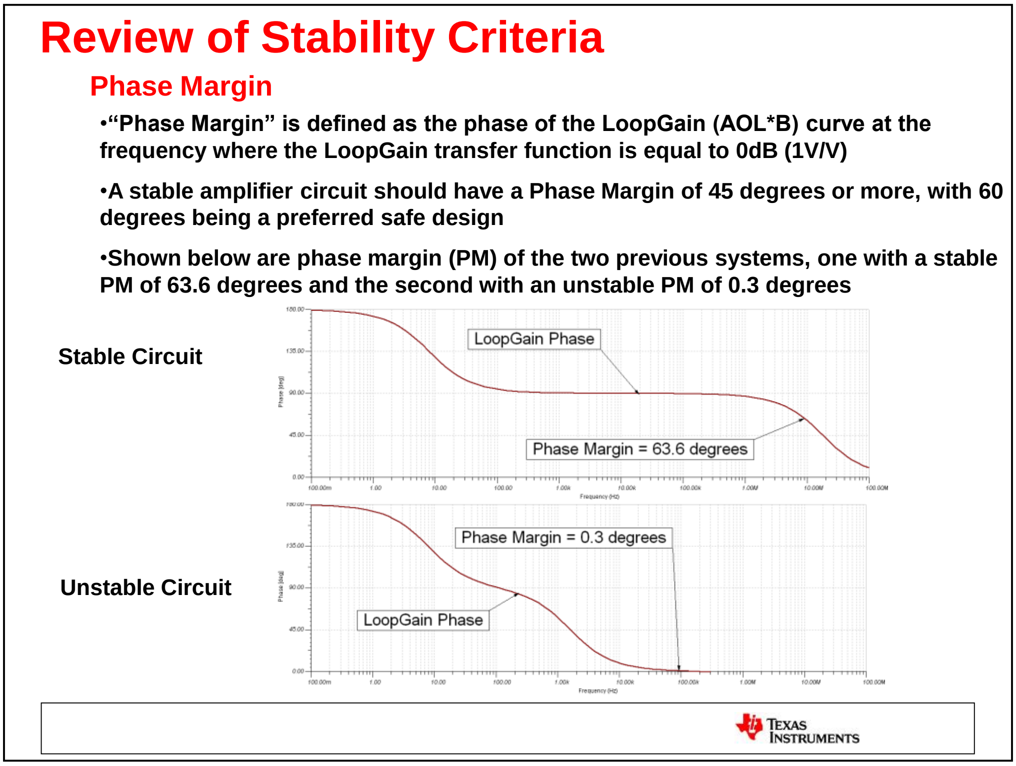
Stable Circuit

Unstable Circuit

The rate of closure of the circuit is defined as the slope at which the AOL intersects the 1/Beta (Feedback Factor) curve. The rate of closure (ROC) is a first order approximation regarding the remaining phase margin left in a circuit. The circuit begins with 180 degrees of available phase shift, and a phase margin of 45 degrees or more is considered a stable system.

Basically if the loop is closed (where 1/Beta intersects AOL) at a slope less than or equal to 20dB/decade we can assume we are dealing with a single pole system in the loop which should account for only 90 degrees of phase shift.

If the ROC is greater than 20dB/decade then we can infer that there must have been a second pole in the system which will account for an additional 90 degrees of phase shift. The phase shift related to a pole begins 1 decade before the pole and finishes 1 decade after the pole, so depending on where this second pole is located it will reduce the system phase margin by at least another 45 degrees (likely more) before the loop is closed reducing the phase margin to an unstable level.



Review of Stability Criteria

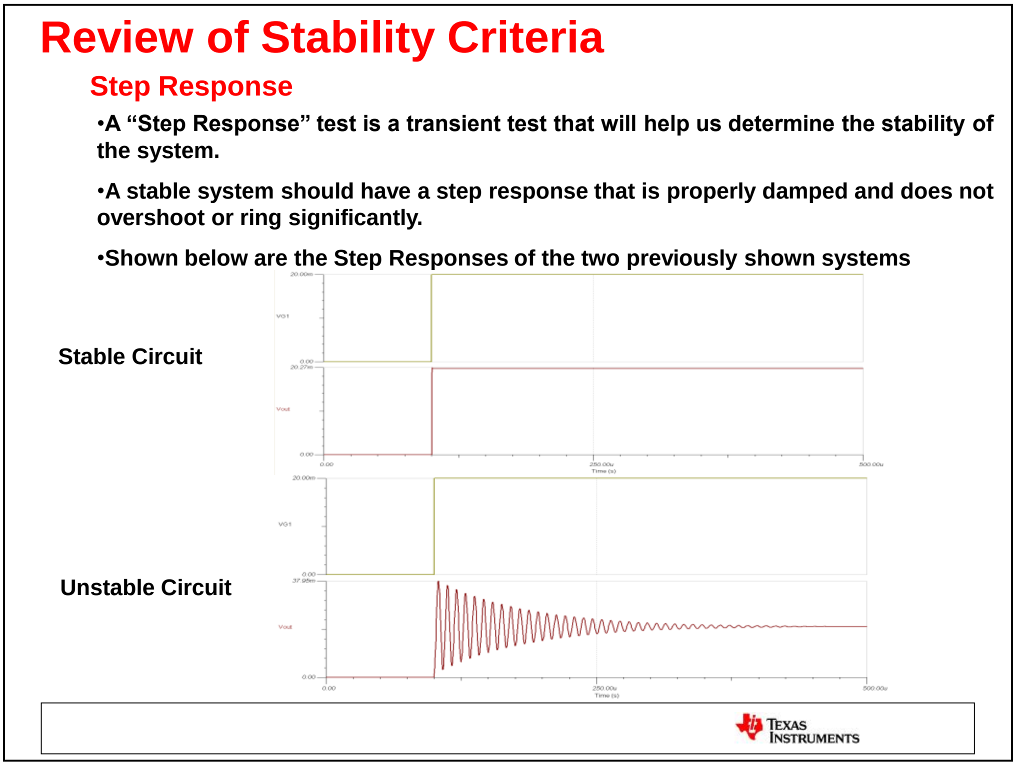
Phase Margin

- "Phase Margin" is defined as the phase of the LoopGain (AOL*B) curve at the frequency where the LoopGain transfer function is equal to 0dB (1V/V)
- A stable amplifier circuit should have a Phase Margin of 45 degrees or more, with 60 degrees being a preferred safe design
- Shown below are phase margin (PM) of the two previous systems, one with a stable PM of 63.6 degrees and the second with an unstable PM of 0.3 degrees

Stable Circuit

Unstable Circuit

The phase margin (PM) of a circuit directly defines its stability. Systems with a phase margin of 45 degrees or less are considered marginally stable or unstable and will have very poor reactions to system input or output step responses.



Review of Stability Criteria

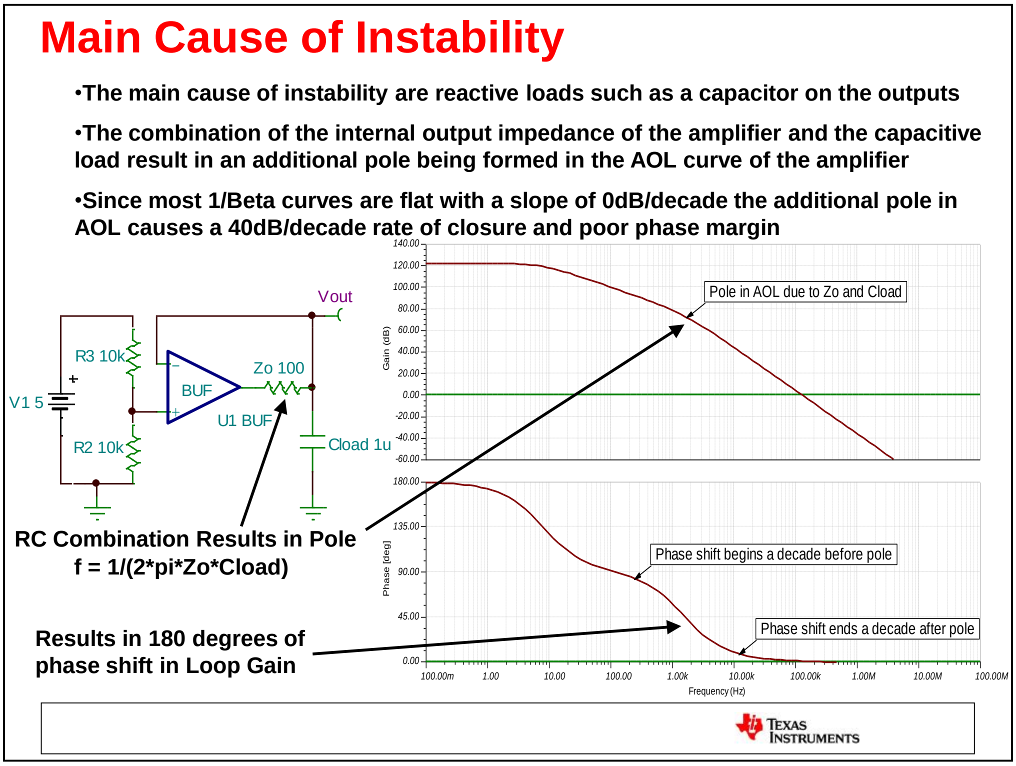
Step Response

- A “Step Response” test is a transient test that will help us determine the stability of the system.
- A stable system should have a step response that is properly damped and does not overshoot or ring significantly.
- Shown below are the Step Responses of the two previously shown systems

Stable Circuit

Unstable Circuit

By simulating the “Step Response” of the circuit the transient stability can be observed. Stable circuits do not overshoot by much and quickly settle to the final value. An unstable circuit will overshoot, ring heavily, and may or may not damp out eventually.



Main Cause of Instability

- The main cause of instability are reactive loads such as a capacitor on the outputs
- The combination of the internal output impedance of the amplifier and the capacitive load result in an additional pole being formed in the AOL curve of the amplifier
- Since most 1/Beta curves are flat with a slope of 0dB/decade the additional pole in AOL causes a 40dB/decade rate of closure and poor phase margin

RC Combination Results in Pole
f = 1/(2*pi*Zo*Cload)

Results in 180 degrees of phase shift in Loop Gain

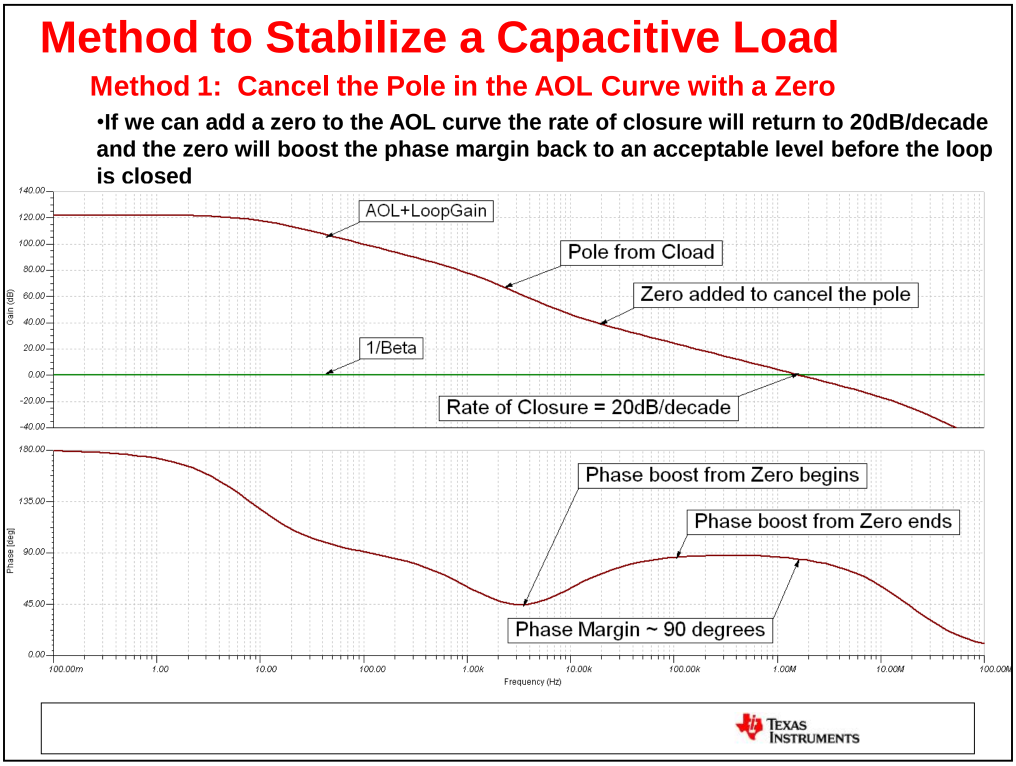
Pole in AOL due to Zo and Cload

Phase shift begins a decade before pole

Phase shift ends a decade after pole

The main cause of stability issues comes from reactive loads on the outputs of the amplifiers. Capacitors are the most common reactive load and are often found when using an amplifier to buffer a voltage for a reference. The circuit shown in the figure here is almost never stable!!!!

The internal Zo of the amplifier interacts with the capacitive load and forms an additional pole in the AOL curve of the amplifier. This causes 1/B curves with a slope of 0dB/decade to close the loop at an unstable 40dB/decade rate of closure.



Method to Stabilize a Capacitive Load

Method 1: Cancel the Pole in the AOL Curve with a Zero

- If we can add a zero to the AOL curve the rate of closure will return to 20dB/decade and the zero will boost the phase margin back to an acceptable level before the loop is closed

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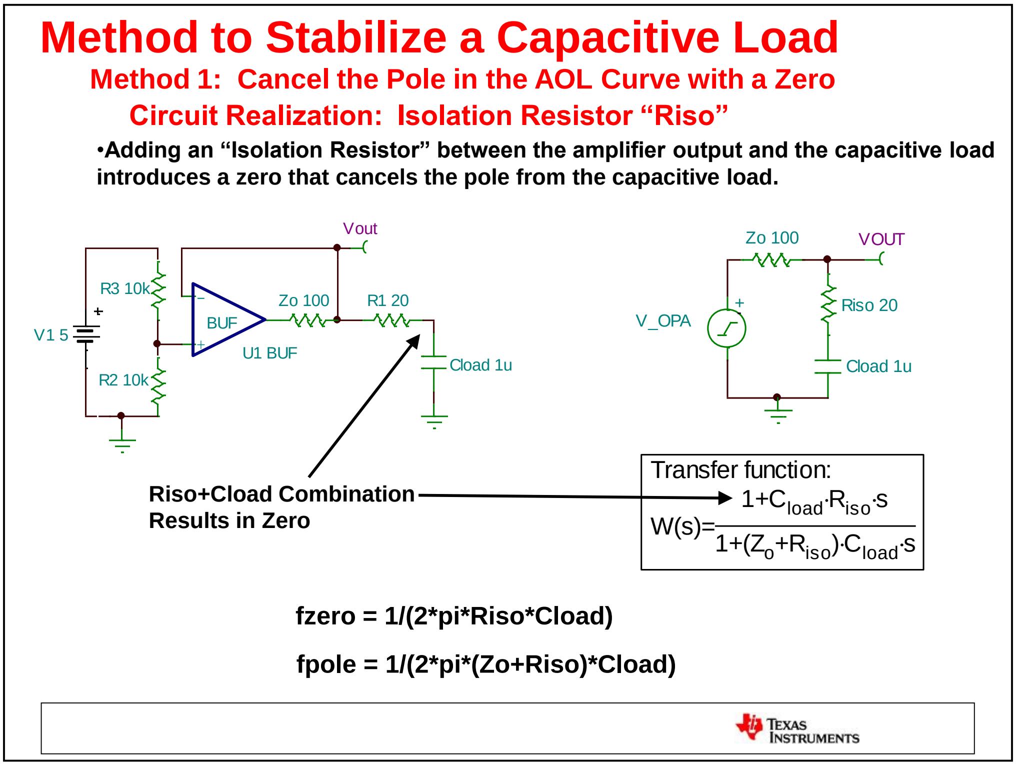
Now we will examine methods to stabilize op-amp circuits with capacitive loads. The first method shown here involves modifying the AOL response by inserting a zero to cancel the pole from the Zo+Cload. The zero will cancel the pole and cause the AOL curve to return to a stable rate of 20dB/decade.



Method to Stabilize a Capacitive Load

Method 1: Cancel the Pole in the AOL Curve with a Zero

Circuit Realization: Isolation Resistor “Riso”

•Adding an “Isolation Resistor” between the amplifier output and the capacitive load introduces a zero that cancels the pole from the capacitive load.

Riso+Cload Combination Results in Zero

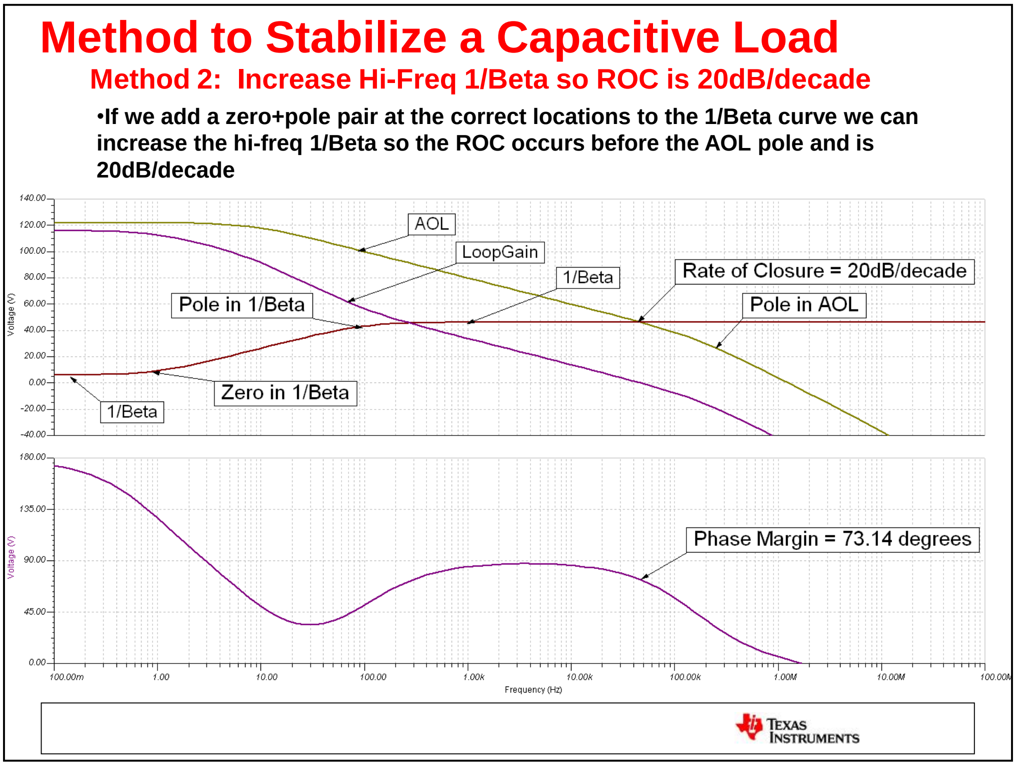
Transfer function:

$$W(s)=\frac{1+C_{load}\cdot R_{iso}\cdot s}{1+(Z_o+R_{iso})\cdot C_{load}\cdot s}$$

fzero = 1/(2*pi*Riso*Cload)

fpole = 1/(2*pi*(Zo+Riso)*Cload)

Shown here is the circuit realization to cancel the pole in the AOL curve with a zero. Simply add an isolation resistor “Riso” between the OPA output and the cap load. As shown with the divider circuit the AOL now has both a pole and a zero in the response.

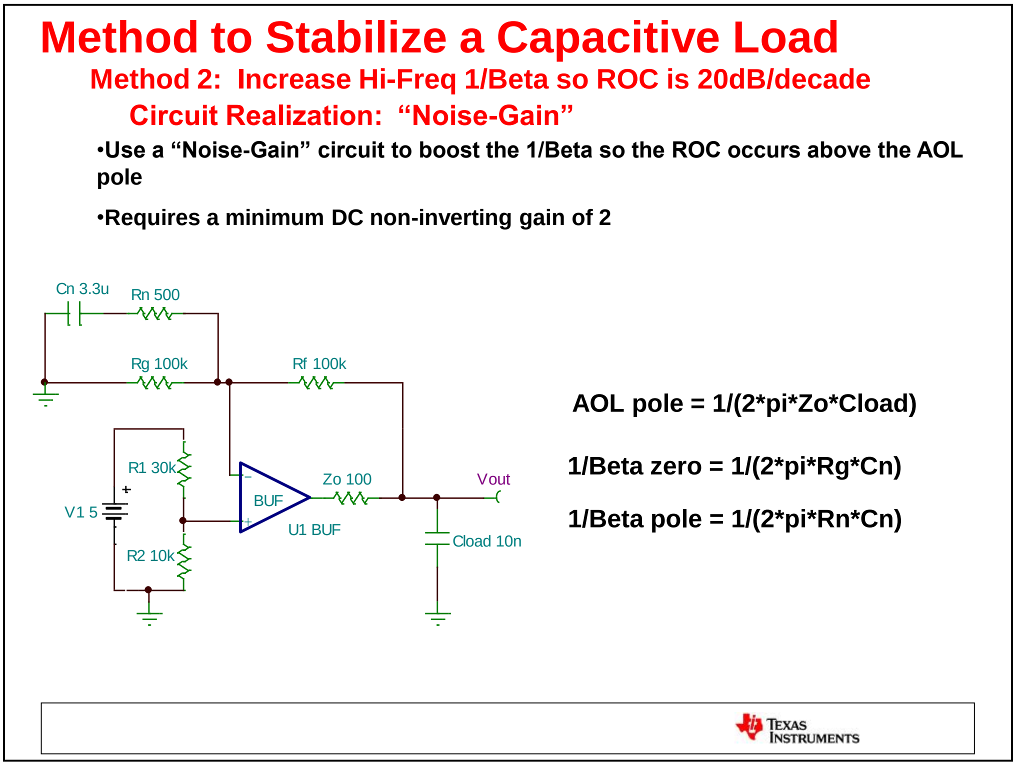


Method to Stabilize a Capacitive Load

Method 2: Increase Hi-Freq 1/Beta so ROC is 20dB/decade

- **If we add a zero+pole pair at the correct locations to the 1/Beta curve we can increase the hi-freq 1/Beta so the ROC occurs before the AOL pole and is 20dB/decade**

The second method we will examine is to modify the 1/Beta curve so that the loop closes before the pole in the AOL curve where the rate of closure will be 20dB/decade. This will involve creating a pole/zero pair in the 1/Beta response.



Method to Stabilize a Capacitive Load

Method 2: Increase Hi-Freq 1/Beta so ROC is 20dB/decade

Circuit Realization: “Noise-Gain”

- Use a “Noise-Gain” circuit to boost the 1/Beta so the ROC occurs above the AOL pole
- Requires a minimum DC non-inverting gain of 2

AOL pole = 1/(2*pi*Zo*Cload)

1/Beta zero = 1/(2*pi*Rg*Cn)

1/Beta pole = 1/(2*pi*Rn*Cn)

The circuit realization for the second method is called a “Noise Gain” circuit. It is called a noise gain circuit because the DC gain can be as low as 2V/V, but the AC hi-frequency gain (Where the noise is) is much higher. Ensure that the hi-frequency gain will be greater than the frequency where the AOL pole occurs.