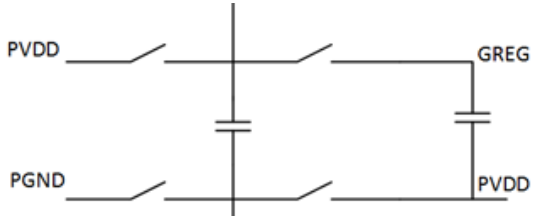
TAS2562HYFPR – Debug Update

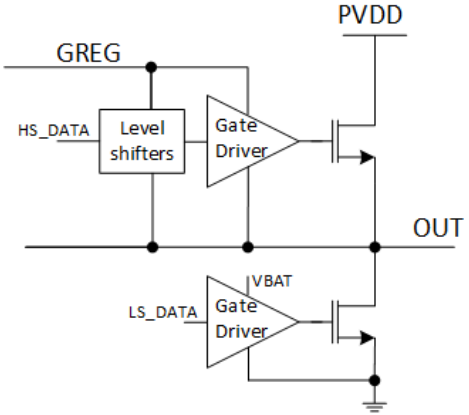
27th August, 2019

TAS2562HYFPR | GREG Voltage & OC

- GREG voltage is used by the ClassD gate-driver circuitry to control ON/OFF of the power FETs
- Under the presence of higher parasitics(specified in the datasheet) either on GREG capacitor or on PVDD trace, GREG voltage can have higher ripple
  - Ripple will be higher on devices with higher output impedance on GREG ChargePump
- With higher ripple on GREG, relative timings between the high-side/low-side gate drivers can be affected, causing violations on break-before-make circuitry
  - This could cause shoot-through currents through the driver, which can trigger the OC circuitry



GREG ChargePump Circuitry

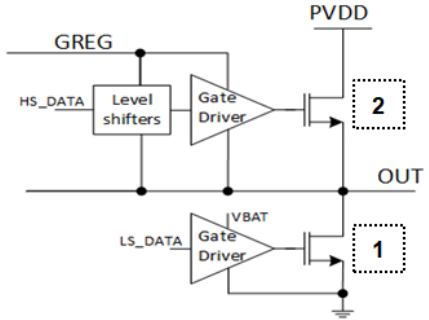


Gate Driver Circuitry

TAS2562HYFPR | GREG Test Screen

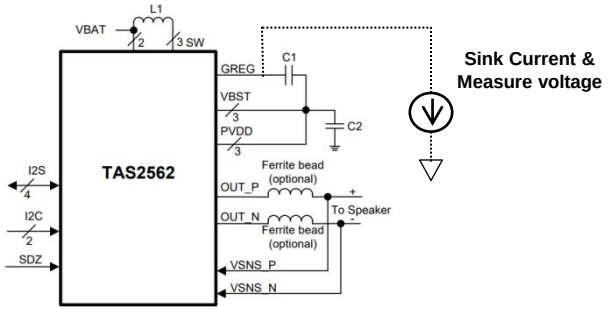
Updated Production Screen

- The stringent screen added along with the existing OVST sequence applies an increased DC current on the ChargePump output
- GREG voltage is measured to ensure that it meets the required voltage range with this load current condition
- This screen ensures higher margin on GREG load regulation capability(output impedance), allowing reliable operation with higher on-board parasitic inductance



Procedure

1. **Class D low side gate enabled[1] , and Class D high side gate disabled [2] →Removes the GREG current requirement by the gate driver**
2. **Measure load regulation of GREG with higher external current loading**



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