TMS320F2837x, SAR ADC and THP210
SAR ADC Input Drive Simulation
Single-Ended to Differential Conversion

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Summary

1. TMS320F2837 SAR ADC (16-B Differential) Equivalent Input Circuit (from Datasheet).
2. TMS320F2837 SAR ADC (16-B Differential Input) Signal Requirements: Full-Scale Range and Common-Mode
3. TMS320F2837 SAR ADC (16-B Differential) Least Significant Bit (LSB) Resolution
4. THP210 (and OPA325) Fully-Differential Amplifier Circuit: Single Ended to Differential Configuration.
5. THP210 and TMS320F283716-B SAR ADC: S/H TINA Transient Settling Simulation, ~1-MSPS, 380ns acquisition
6. THP210 and TMS320F283716-B SAR ADC: S/H TINA Transient Settling Simulation, ~1.1-MSPS, 320ns acquisition

Device settles within ~1/2-LSB at 1-MSPS (tacq= 380ns)
Device settles within ~1-LSB at 1.06-MSPS (min tacq= 320ns)

Assumption: S/H capacitor looses only ~20% of charge from conversion to conversion
Single channel on ADC continuous conversion (non-multiplexed)

Note: All TINA-TI simulations can be run on the embedded schematics in this presentation by downloading the free TI SPICE simulator, TINA-TI, at:
http://www.ti.com/tool/tina-ti

SAR ADC Differential Mode Input Parameters

TMS320F28377D 16-B, 1.1-MSPS, Differential Mode ADC

ADC Input Equivalent Circuit (16-B, Differential Mode):

Switch Sampling Resistance R_{ON} = 700Ω
Sampling Capacitor C_H = 16.5pF (Table 5-47, p107)

Table 5-47. Differential Input Model Parameters

	DESCRIPTION	VALUE (16-BIT MODE)
C_p	Parasitic input capacitance	See Table 5-49
R_{on}	Sampling switch resistance	700 Ω
C_h	Sampling capacitor	16.5 pF
R_s	Nominal source impedance	50 Ω

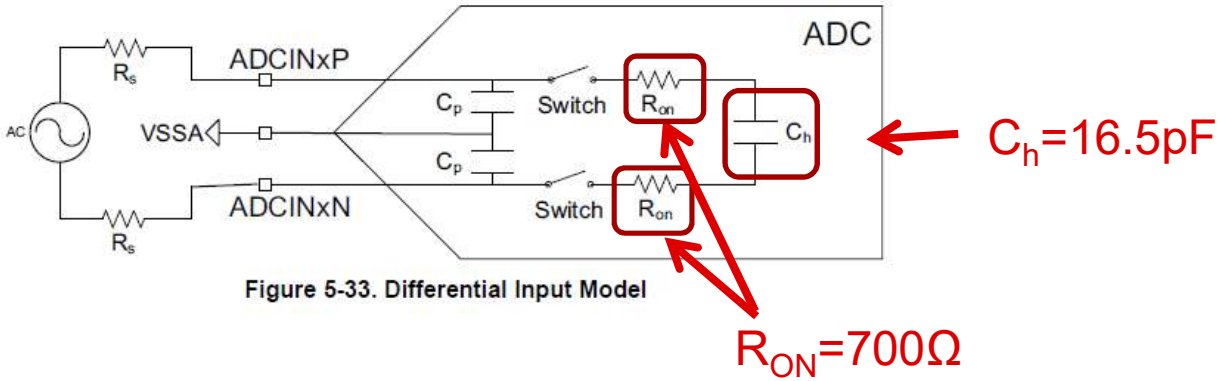


Figure 5-33. Differential Input Model

SAR ADC Differential Mode Input Parameters

TMS320F28377D 16-B, 1.1-MSPS, Differential Mode ADC

SAR ADC Input Signal Requirements:

Assuming REFHI = 3.0V (VDDA); REFLO = 0V

Full-Scale Range = ± VREF = ±3.0V

ADC Input Common-Mode $V_{REFCM} = (V_{REFHI}-V_{REFLO}) / 2 = 1.5V$

ADC Input Common-Mode Range =>

$V_{REFCM} \pm 50mV = 1.5V \pm 50mV$

Table 5-42. ADC Operating Conditions (16-Bit Differential Mode)

over recommended operating conditions (unless otherwise noted)

	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)	5		50	MHz
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	320			ns
V_{REFHI}	2.4	2.5 or 3.0	V_{DDA}	V
V_{REFLO}	V_{SSA}	0	V_{SSA}	V
$V_{REFHI} - V_{REFLO}$	2.4		V_{DDA}	V
ADC input conversion range	V_{REFLO}		V_{REFHI}	V
ADC input signal common mode voltage(2)(3)	$V_{REFCM} - 50$	V_{REFCM}	$V_{REFCM} + 50$	mV

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) $V_{REFCM} = (V_{REFHI} + V_{REFLO})/2$
(3) The V_{REFCM} requirements will not be met if the negative ADC input pin is connected to V_{SSA} or V_{REFLO}.

SAR ADC Differential Mode Input Parameters

TMS320F28377D 16-B, 1.1-MSPS, Differential Mode ADC

SAR ADC Resolution:

Least Significant Bit (LSB)

$$LSB = \frac{FullScaleRange}{2^N}$$

$$LSB = \frac{\pm VREF}{2^N} = \frac{\pm 3.0V}{2^{16}} = \frac{2 \cdot 3.0V}{2^{16}} = 91.55\mu V$$

$$\frac{1}{2} LSB = 45.83\mu V$$

SAR ADC Differential Mode Input Parameters

TMS320F28377D 16-B, 1.1-MSPS, Differential Mode ADC

SAR ADC Timing:

Assume Max Sampling Rate = ~1-MSPS, ADCCLK @ 50MHz (20ns) from TMS320 datasheet

Conversion Time:

t_{EOC} = 31*ADCCLK s (from Table 5-52, p111 datasheet)

t_{EOC} = t_{conv}= 31*20ns = 620ns (ADCCLK @ 50MHz)

Acquisition Time (Sample Window):

$t_{acquisition}$= 1000ns – 620ns, $t_{acquisition}$= ~380ns @1-MSPS

$t_{acquisition}$= ~320ns @ 1-MSPS (Minimum Sample window duration from Table 5-42, p103 datasheet)

Table 5-42. ADC Operating Conditions (16-Bit Differential Mode)

over recommended operating conditions (unless otherwise noted)

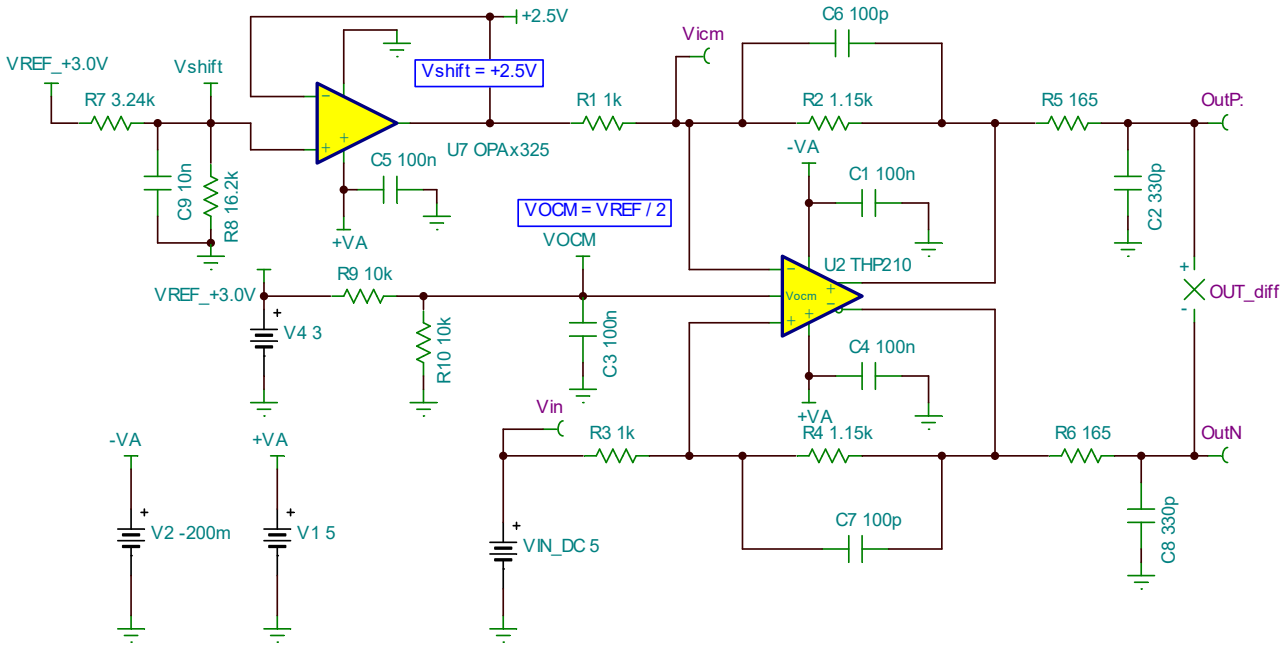
	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)	5		50	MHz
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	320			ns
V_{REFHI}	2.4	2.5 or 3.0	V_{DDA}	V
V_{REFLO}	V_{SSA}	0	V_{SSA}	V
V_{REFHI} – V_{REFLO}	2.4		V_{DDA}	V
ADC input conversion range	V_{REFLO}		V_{REFHI}	V
ADC input signal common mode voltage(2)(3)	V_{REFCM} – 50	V_{REFCM}	V_{REFCM} + 50	mV

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) V_{REFCM} = (V_{REFHI} + V_{REFLO})/2
(3) The V_{REFCM} requirements will not be met if the negative ADC input pin is connected to V_{SSA} or V_{REFLO}.

THP210 Fully-Differential Amplifier Circuit

Single-Ended to Differential Configuration

1. VIN: 0-5V Single-Ended.
2. Gain : (±3V*2)/5V = 1.2V/V. Used Gain = 1.150V/V for margin.
3. VOCM driven to VREF/2 to set Output Common Mode:
   VOCM= VREF/2 = 3.0V / 2 =1.5V
4. THP210 Inverting Input needs to be driven to +2.5V with low impedance source: OPA325 used as buffer

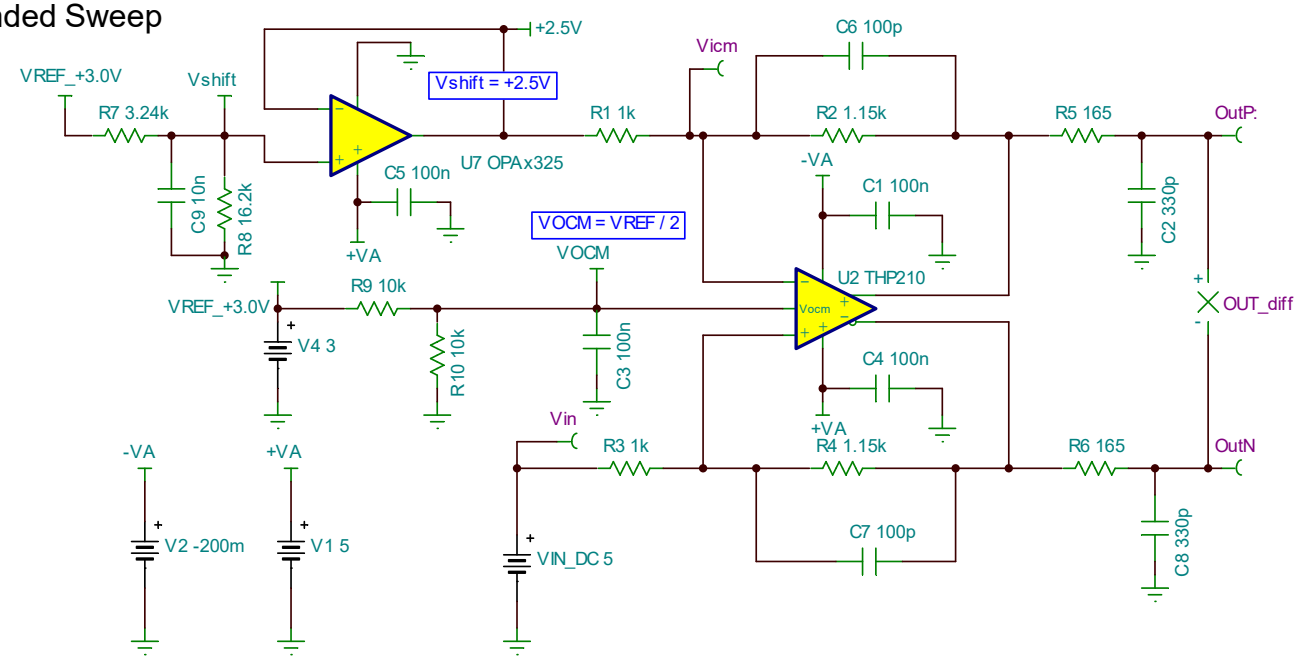


THP210 Fully-Differential Amplifier Circuit

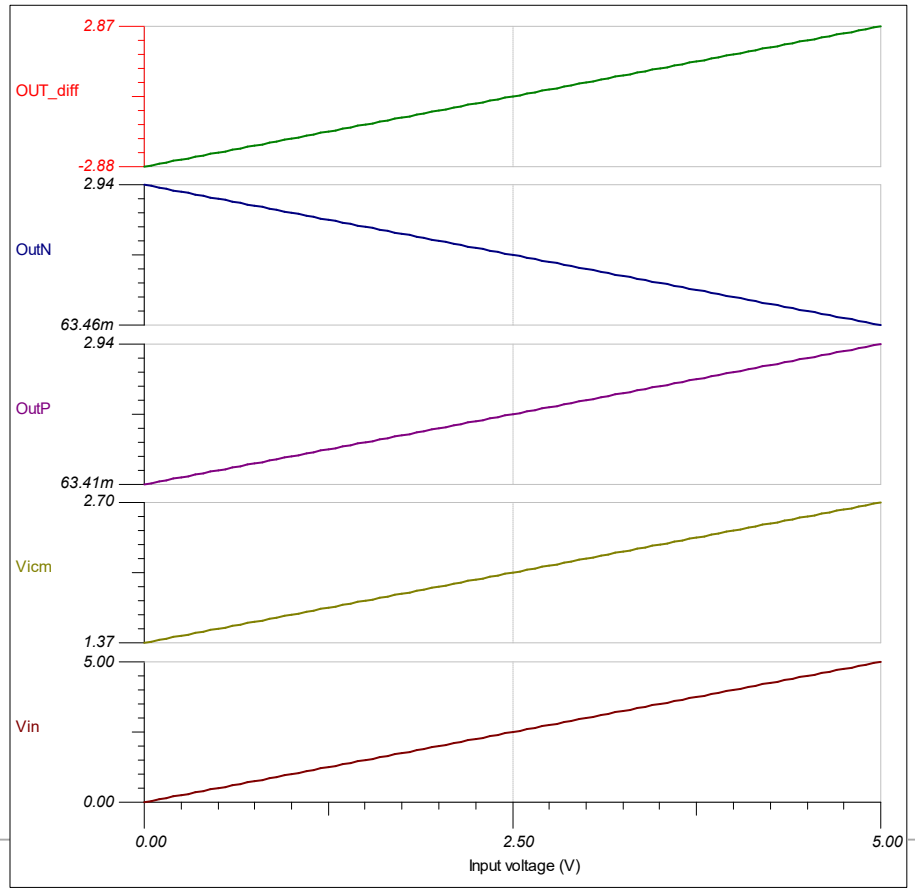
THP210/OPA320 stand-alone

DC Sweep

VIN=1-kHz, 0-5V Single-Ended Sweep
VOCM = VREF/2 = 1.5V
VOUT_DIFF = ± 2.88V



THP210 Fully-Differential Amplifier Circuit



THP210/OPA320 stand-alone DC Sweep

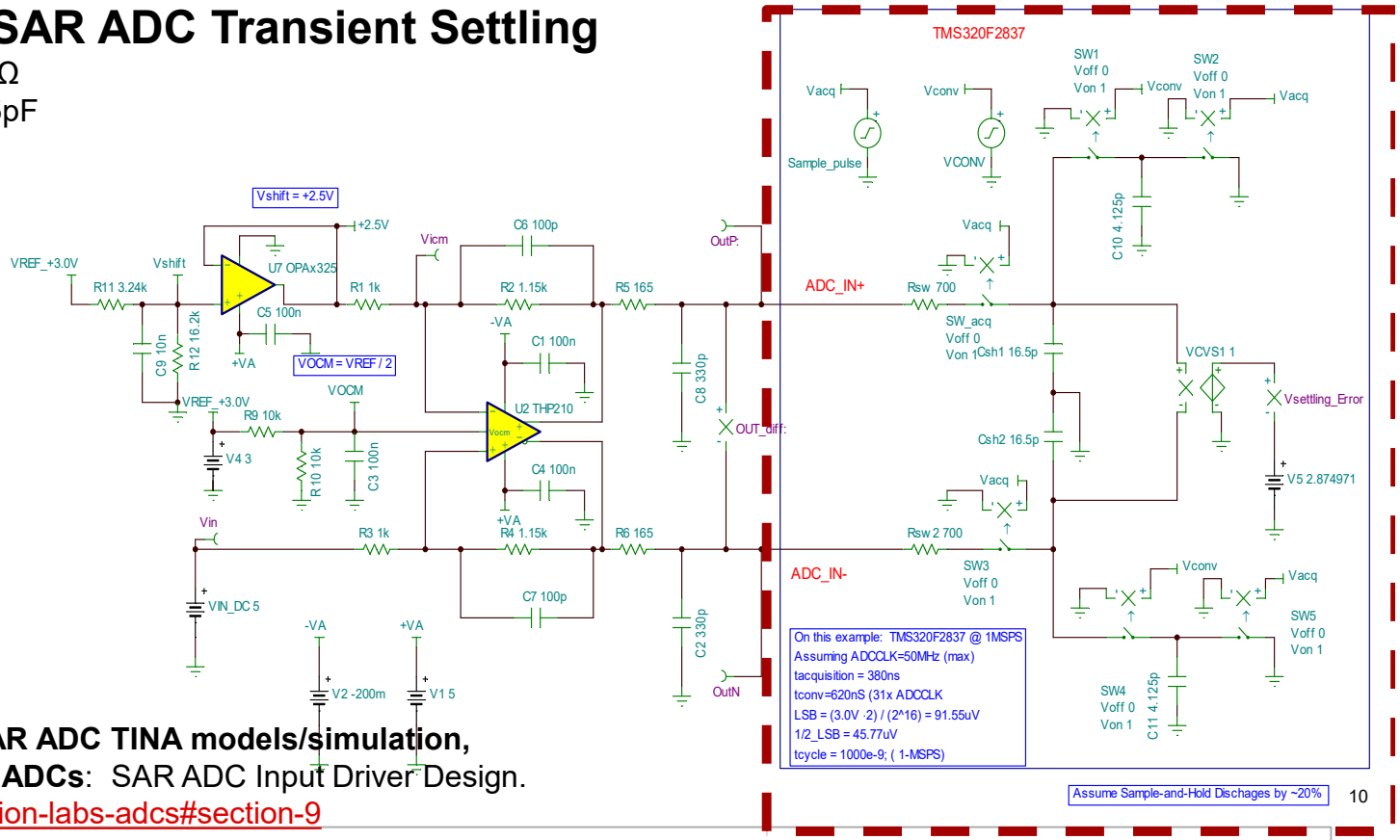
VIN=1-kHz, 0-5V Single-Ended Sweep
VOCM = VREF/2 = 1.5V
VOUT_DIFF = ± 2.88V

THP210 and TMS320F2837 16-B SAR ADC 1-MSPS

Sample-and-Hold SAR ADC Transient Settling

Switch Resistance R_{ON} = 700Ω
Sampling Capacitor C_H = 16.5pF
Acquisition Period = 380ns
Conversion Period = 620ns
Tcycle = 1000ns
Sampling Rate = 1 / 1000ns
= ~1-MSPS
VREF = 3.0V
Full-Scale Range = ±3.0V
LSB = 91.6µV
½ LSB =45.8µV

SAR ADC TINA Model



For more Information on SAR ADC TINA models/simulation,
Consult TI Precision Labs - ADCs: SAR ADC Input Driver Design.
https://training.ti.com/ti-precision-labs-adcs#section-9

THP210 and TMS320F2837 16-B SAR ADC

Sample-and-Hold SAR ADC Transient Settling 1-MSPS

$t_{acquisition}$= ~380ns @1-MSPS

Settling Error = -52.44µV < ~1/2- LSB

1-LSB = 91.6µV
½ LSB =45.8µV

Settles close to ½-LSB at 1-MSPS

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SAR ADC Input Driver Design.
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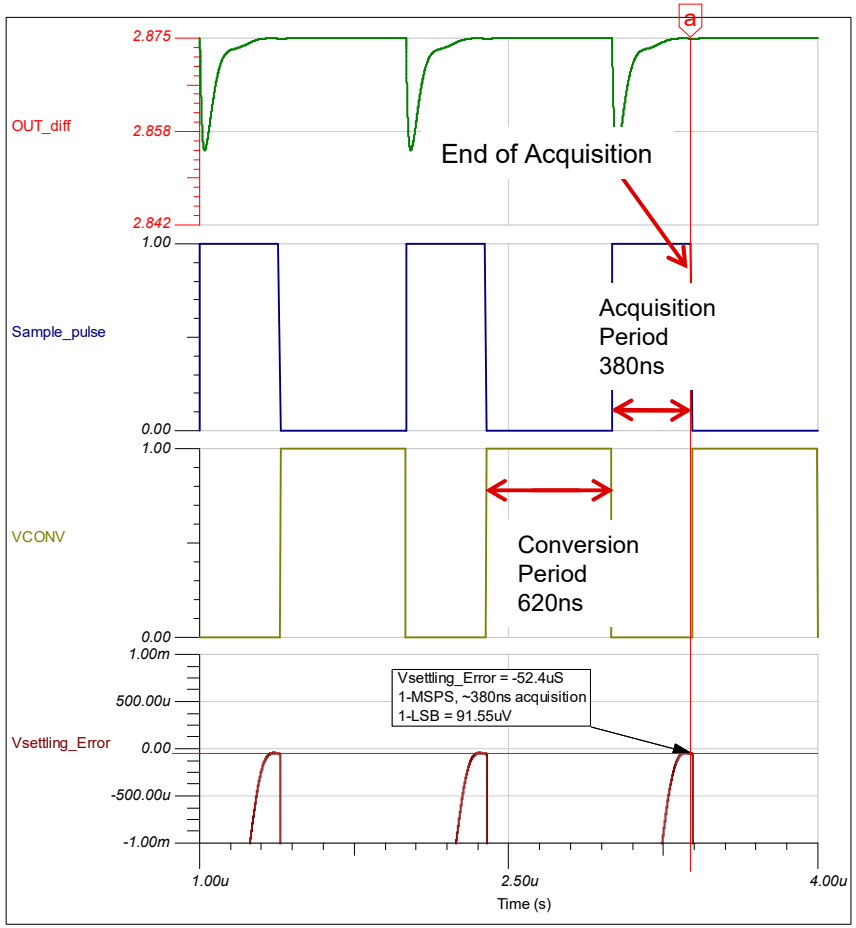
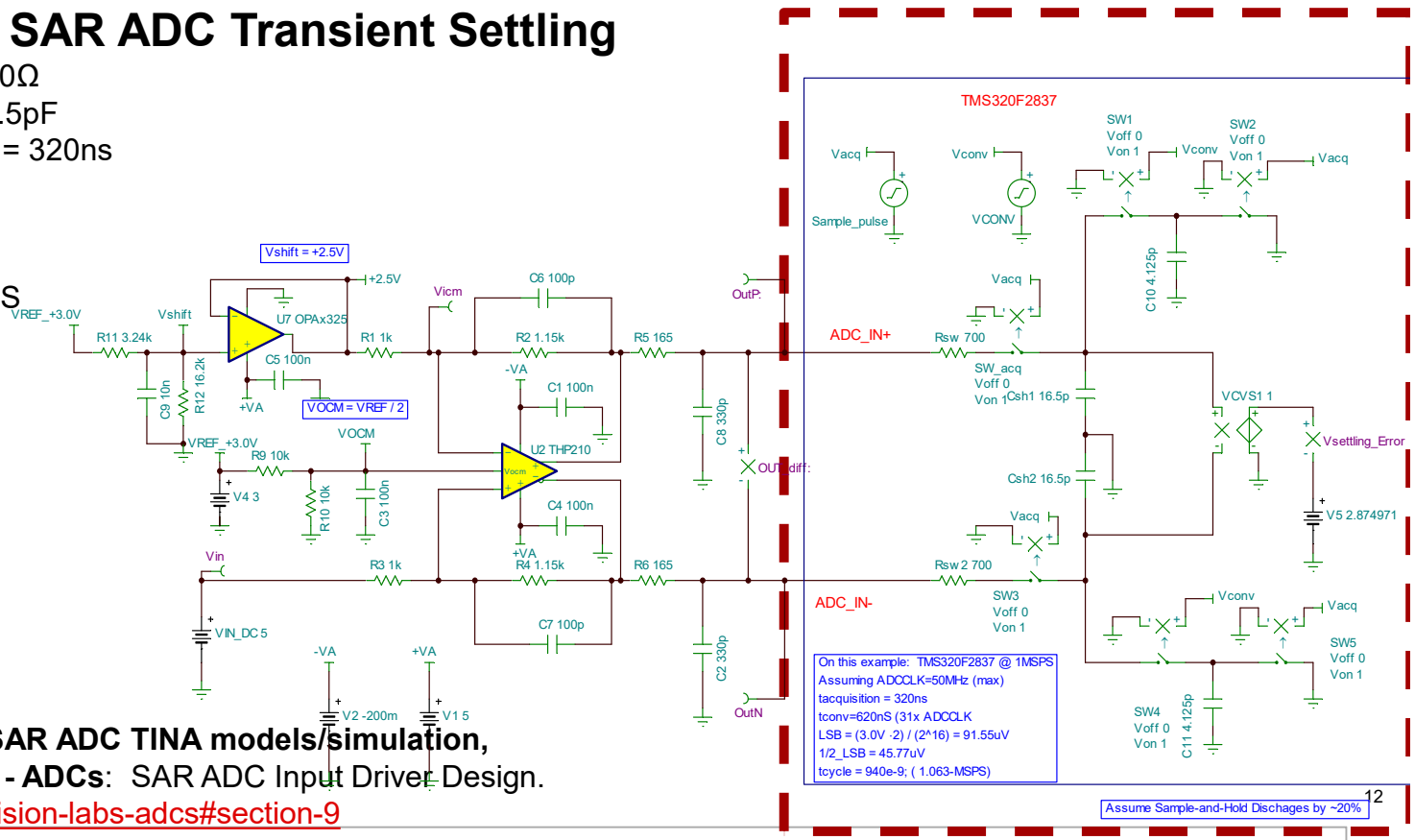


THP210 and TMS320F2837 16-B SAR ADC 1.1-MSPS

Sample-and-Hold SAR ADC Transient Settling

Switch Resistance R_{ON} = 700Ω
Sampling Capacitor C_H = 16.5pF
Minimum Acquisition Period = 320ns
Conversion Period = 620ns
Tcycle = 940ns
Sampling Rate = 1 / 940ns
= ~1.063-MSPS
VREF = 3.0V
Full-Scale Range = ±3.0V
LSB = 91.6µV
½ LSB =45.8µV

SAR ADC TINA Model



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THP210 and TMS320F2837 16-B SAR ADC

Sample-and-Hold SAR ADC Transient Settling 1.06-MSPS

$t_{acquisition}$= ~320ns @1.06-MSPS

Settling Error = -92.21µV = ~ 1- LSB

1-LSB = 91.6µV
½ LSB =45.8µV

Settles close to ½-LSB at 1-MSPS

For more Information Consult TI Precision Labs - ADCs:
SAR ADC Input Driver Design.
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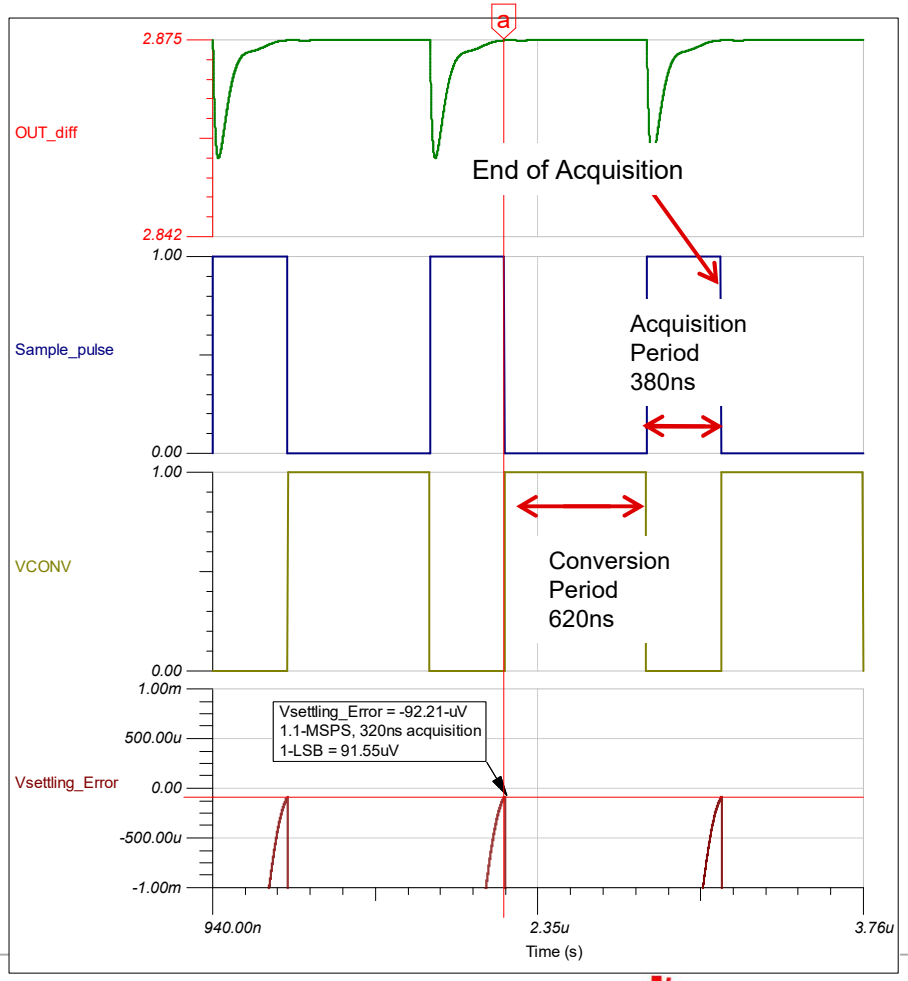

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