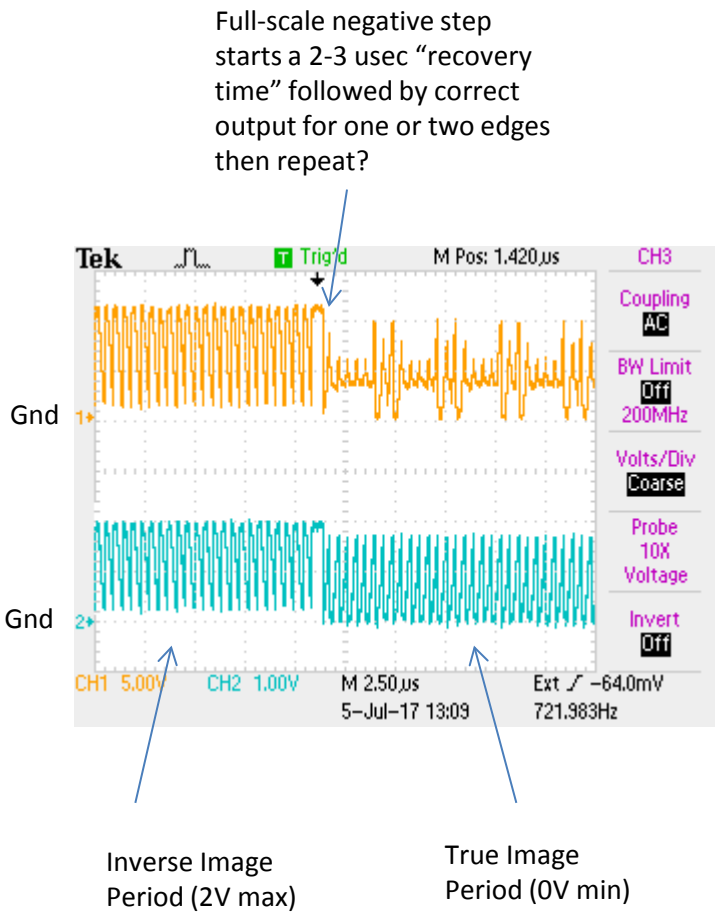
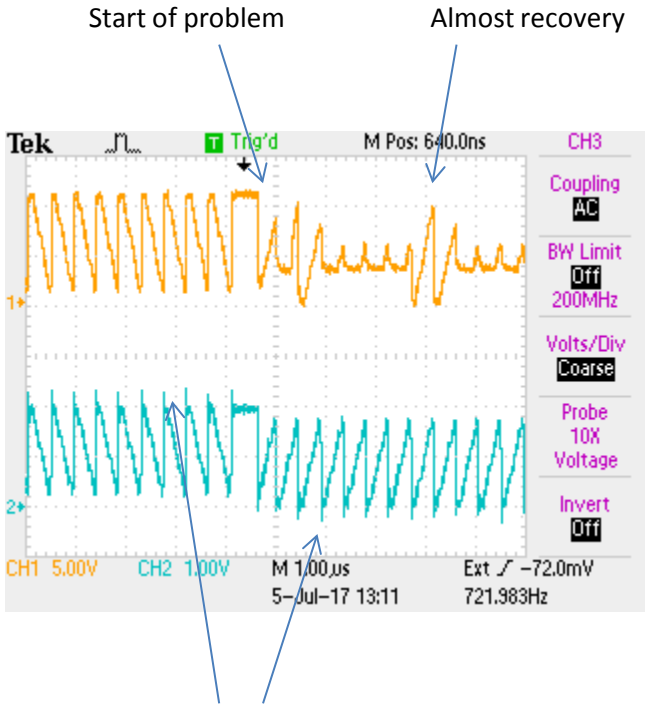
THS6002 Challenges

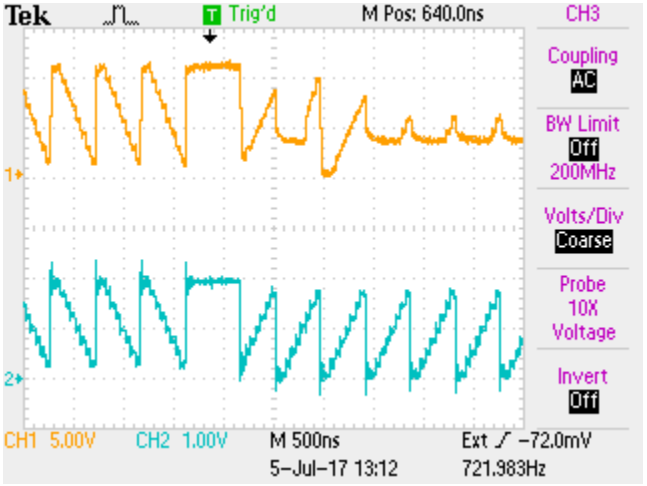
Problem Behavior Overview



- Bottom (Blue) Trace is Op-Amp Input, 0-2Vp
- Top (Orange) Trace is Op-Amp Output, 0-12Vp
- Left side is inverse image period, right side is true image period
- Yes, there’s a slight DC offset between the two due to test image used.
- First full-scale negative going step (at trigger point) precipitates a saturated behavior in op-amp.
- Ignore Ch3 menu display left over from scope button push.

Horizontal Scale Zoom In



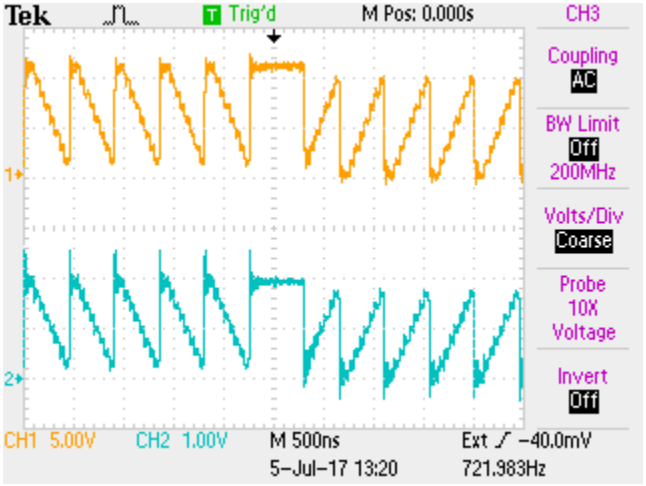


Video buffer (op-amp input) has significant overshoot/undershoot (ringing) due to high BW and fast edge rates.

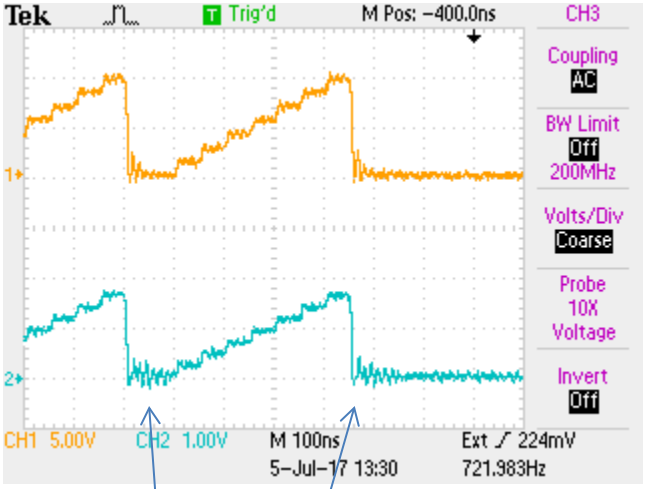
We are looking at adding filtering to slow its edges down at bit.

One Chan Works OK (not many)

One channel works OK, same image, same pcb layout, same circuit!



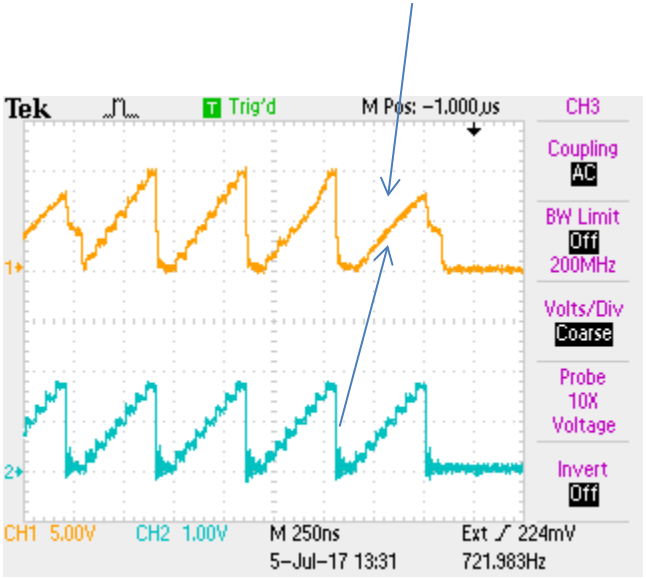
Just to illustrate the desired input signal – provided by a high-speed D/A converter running at 25 Msps (goal). This test image generates an 8-step ramp between #00 an #FF values before repeating.



Close-up of undesirable video buffer ringing, although this op-amp doesn't seem to have a problem with it.

One Chan Works OK (not many)

Oops – the beginning of a problem.



- The test image illustrates intended multi-level operation.
- Real worst case design needs are to produce an alternate sample full-scale output (essentially a 0-12Vp square wave with 40ns pulse widths).