

Automotive 400-V Battery to 12 V, 3.6-kW DC/DC Converter Reference Design



Description

This reference design is a 3.6-kW, automotive 400-V to 12-V Unidirectional Converter which converts the 200-V to 450-V DC input to 12-V, 300-A maximum output. A circuit breaker is applied for overcurrent and overvoltage protections. The converter is designed with SiC MOSFETs on the high-voltage side and driven by 5.7-kV_{RMS}, reinforced isolated dual-channel gate drivers. The enhanced phase-shifted full-bridge controller implements programmable delays which ensure Zero Voltage Switching (ZVS) over a wide range of operating conditions. It offers multiple light-load management features including burst mode and dynamic SR on and off control when transitioning in and out of Discontinuous Current Mode (DCM) operation. The output implements synchronous rectification, which enables fast transient response and a high loop bandwidth.

Resources

TIDA-020031	Design Folder
UCC28951-Q1, UCC21530-Q1	Product Folder
UCC27712-Q1, UCC27524-Q1	Product Folder
LM74801-Q1, NA293-Q1	Product Folder
SN6505B-Q1, LMV393-Q1	Product Folder

Features

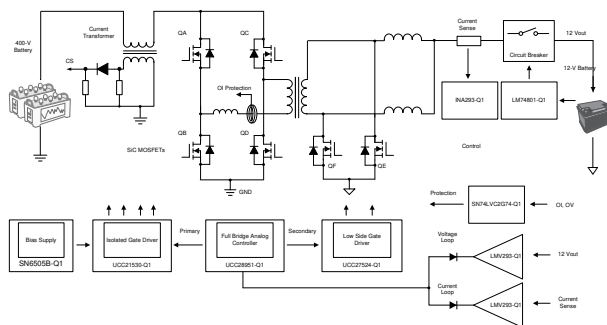
- Phase-shifted full bridge converter over 200- to 450-V DC input, 10- to 15-V output, power up to 3.6 kW
- Scalable to 800-V input systems, with tight regulation of $< \pm 1\%$
- Soft-switching, using phase-shifted full bridge analog control loop
- Soft switching with zero voltage switching (ZVS) on the primary; dynamic on and off control on the secondary enabling higher efficiency
- Synchronization achievable for multiple phase operation
- Host MCU for supervision and current and voltage loop control

Applications

- [Onboard \(OBC\) and wireless charger](#)
- [DC/DC converters](#)



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1 System Description

The design accepts 200-V to 470-V input voltage, with up to 300-A output current without losing regulation. A fast circuit breaker is implemented to comply with safety in automotive.

1.1 Key System Specifications

[Table 1-1](#) shows the key system specifications of TIDA-020031.

Table 1-1. Key System Specifications

Parameter	Specification
Input	200 V to 470 V, 400 V nominal
Output	9 V to 15 V DC adjustable 300-A peak output current - Ripple < 3% V_{OUT} - Load step 3% to 100% with voltage deviation < 5%
Features	- Soft-Switching, Phase-Shifted Full Bridge topology with peak efficiency > 95% - Current-doubler topology with low-side gate driver and Si MOSFET at the secondary side for synchronous rectification - Switching frequency (approximately 100 kHz) - SiC MOSFETs being used with reduced reverse recovery losses - Reinforced dual-channel isolated gate driver with high CMTI immunity - Fast circuit breaker control to comply with automotive safety - Shunt-based output current sense with high bandwidth amplifier for increased accuracy - Analog comparator sub-systems for fast speed overcurrent and overvoltage protections

This reference design is a 3.6-kW DC/DC converter that generates the 12-V rail from the 400-V car battery for Hybrid Electric Vehicle and Electric Vehicle (HEV, EV) applications. The design implements Phase Shifted Full Bridge topology with analog control loop. The enhanced phase-shifted full bridge controller UCC28951-Q1 implements programmable delays which ensure Zero Voltage Switching (ZVS) over a wide range of operating conditions. The output side implements current doubler topology and synchronous rectification. Reinforced dual-channel isolated gate drivers are used to drive the SiC MOSFET at the primary side, which leads to higher reliability and higher power density. SiC MOSFETs are implemented for easy adaption to the 800-V input design.

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the TIDA-020031 system block diagram. The design consists of 4 main functional elements:

1. Current sensing at the primary side via the current transformer, which is for cycle-by-cycle overcurrent protection and adaptive delay.
2. Power stage of the phase shifted full bridge at the primary side. The design implements the zero voltage soft-switching scheme and variable power saving features for improved efficiency over a wide load current range.
3. Synchronous rectification MOSFETs at the secondary side have several benefits:
 - a. Boosts the system efficiency by reducing the voltage drop over the drain-to-source
 - b. Reduces voltage overshoots and undershoots caused by the load steps
 - c. Enables fast transient response and a high loop bandwidth.
4. Fast controlled 300-A circuit breaker at output side for increased safety level.

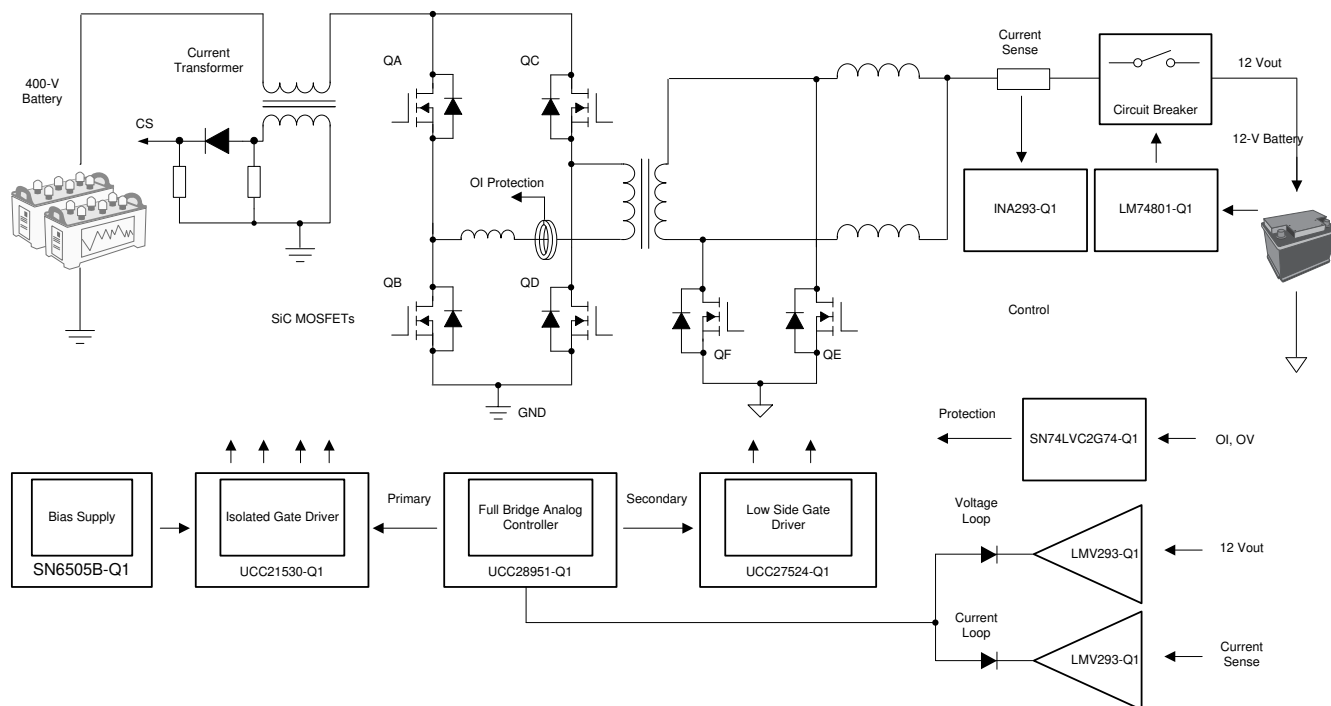


Figure 2-1. TIDA-020031 System Block Diagram

2.2 Design Considerations

This reference design implements phase-shifted full-bridge (PSFB) topology which targets to achieve greater than 95% peak efficiency. ZVS, or LVS switching are achieved across a majority of the operating range. The control algorithm is implemented on an analog controller, UCC28951-Q1. The controller interacts with the PSFB power stage by way of feedback signals and PWM outputs. The controller is placed on the secondary side on this design.

2.3 Highlighted Products

The TIDA-020031 reference design features the following Texas Instruments devices.

2.3.1 UCC28951-Q1

The UCC28951-Q1 is an enhanced phase-shifted full bridge controller which implements programmable delays to ensure Zero Voltage Switching (ZVS) operation over a wide range of operating conditions. The device contains all of the features and multiple light load management to ensure maximized efficiency at overall conditions. The UCC28951-Q1 includes support for current or voltage mode control. Programmable switching frequency up to 1 MHz and a wide set of protection features including cycle-by-cycle current limit, UVLO and thermal shutdown are available.

2.3.2 UCC27524-Q1

The UCC27524-Q1 device is a dual-channel, low side driver with 5-A sink, 5-A source peak drive current capability. The UCC27524A-Q1 device is able to handle -5 V directly at the input pins for increased robustness. The driver offers fast rise and fall time (7-ns and 6-ns typical) and propagation delays (13-ns typical).

2.3.3 UCC21530-Q1

The UCC21530-Q1 is an isolated dual-channel gate driver with 4-A source and 6-A sink peak current and designed to drive IGBTs and SiC MOSFETs up to 5-MHz with best-in-class propagation delay and pulse-width distortion. The input side is isolated from the two output drivers by a 5.7-kV_{RMS} reinforced isolation barrier, with a minimum of 100-V/ns common-mode transient immunity (CMTI).

2.3.4 INA293-Q1

The INA293-Q1 is a high bandwidth, unidirectional, voltage-output, current-sense amplifier that senses voltage drops across external sense (shunt) resistors over a wide common-mode voltage range from -4 V to 110 V. The INA293-Q1 amplifier has a bandwidth of 1 MHz at gain of 20 V/V. The 1-MHz bandwidth in combination with a low offset of < 200 μ V (maximum).

2.3.5 SN6505B-Q1

The SN6505x-Q1 is a low-noise, low-EMI push-pull transformer driver with integrated MOSFETs, specifically designed for small form factor, isolated power supplies. The device drives low profile, center-tapped transformers from a 2.25-V to 5-V DC power supply. The internal protection features include a 1.7-A current limiting, undervoltage lockout, and thermal shutdown.

2.4 System Design Theory

This TI Design implements phase-shifted full bridge topology to achieve high efficiency over a wide range of operating conditions. The ZVS on the primary side of the converter reduces the switching losses and EMI. Synchronous rectification on the secondary side is implemented to enable fast transient response and a high loop bandwidth^[2].

2.4.1 Power Budget

To meet the efficiency goal, the power budget is set as:

$$P_{BUDGET} = P_{OUT} \times \frac{(1 - \eta)}{\eta} = 190 \text{ W} \quad (1)$$

where:

- η is the efficiency target which is 95% at full load

2.4.2 Transformer Calculations

This section introduces the calculations of transformer parameters, which includes turns ratio, magnetizing inductance, leakage inductance, and so forth^[3].

Transformer turns ratio is calculated with [Equation 2](#).

$$a_1 = \frac{N_p}{N_s} \quad (2)$$

where:

- N_p is the number of turns at the transformer primary side
- N_s is the number of turns at the transformer secondary side

The voltage drop from C3M0065100K SiC MOSFET ($V_{RDS(ON)}$) is calculated as:

$$V_{RDS(ON)} = I_{DS} \times R_{DS(ON)} = 0.585 \text{ V} \quad (3)$$

where:

- I_{DS} is the current flowing through drain-to-source of the primary MOSFETs

The maximum duty cycle (D_{sec_max}) is set as 90% at minimum specified input voltage (V_{INMIN}). The transformer turns ratio is calculated as:

$$N_1 = \frac{V_{in_nom} \cdot D_{sec_max}}{V_{OUT} + V_{mos}} = 11 \quad (4)$$

The duty cycle loss on the secondary side is calculated as:

$$D_{sec_max} = \frac{(V_{OUT_max} + V_{RDS(ON)})}{V_{sec_min}} = 0.45 \quad (5)$$

The magnetizing inductance (L_{MAG}) of the primary of the transformer (T1) needs to be sufficient to ensure the converter operates in the peak current mode control. Small L_{MAG} results in large magnetizing current, which causes the converter to operate in voltage mode instead. L_{MAG} is calculated at the maximum input voltage:

$$L_{MAG} \geq \frac{V_{IN_Max} \times (1 - D_{TYP})}{\frac{\Delta I_{LOUT} \times 0.5}{N_1} \times F_{SW}} = 900 \mu H \quad (6)$$

where:

- F_{SW} is the switching frequency of the converter
- ΔI_{LOUT} is the output current ripple
- N_1 is the transformer turns ratio

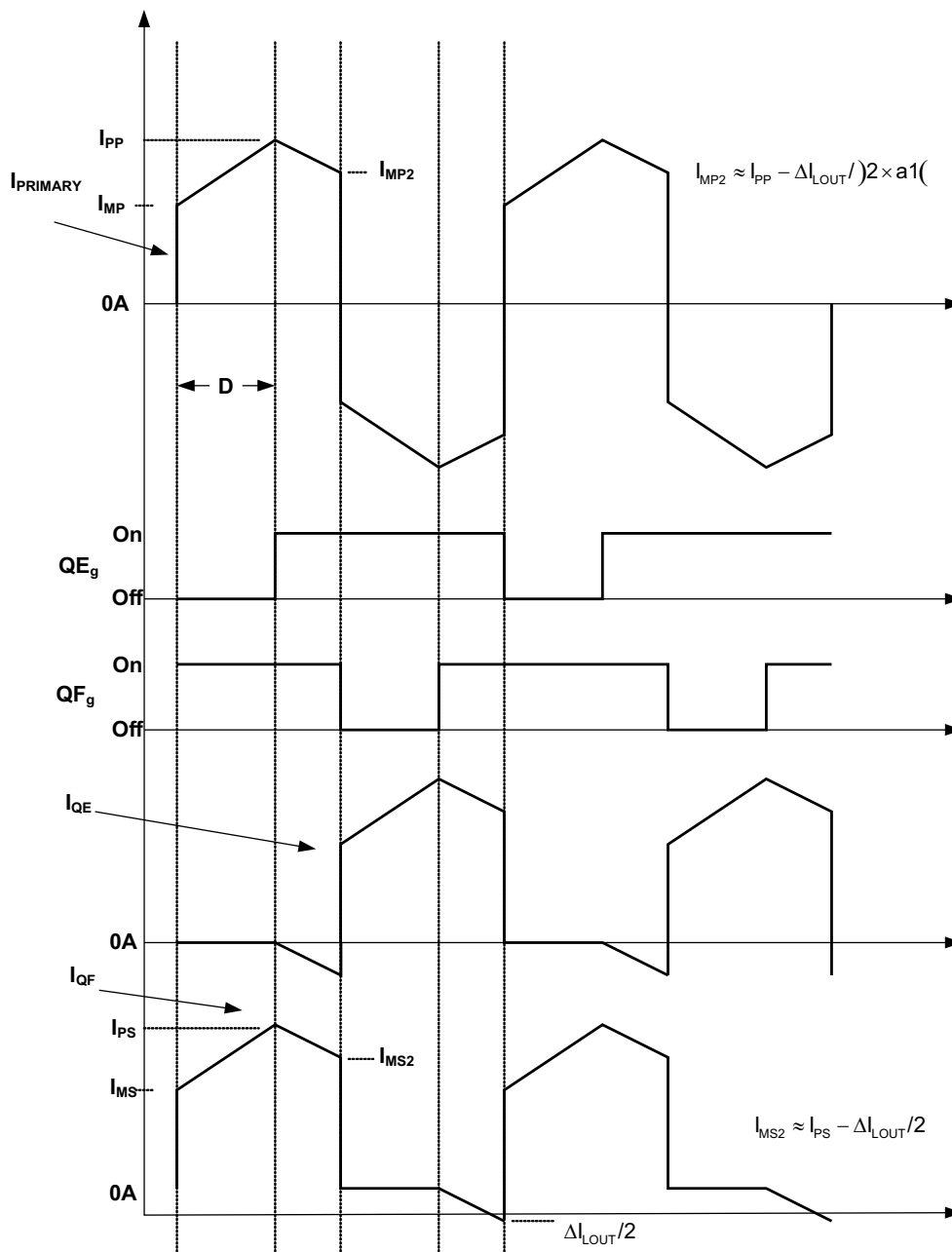


Figure 2-2. Transformer Primary Side and Secondary Side Currents

Figure 2-2 shows the primary ($I_{PRIMARY}$) and secondary side currents flowing through the transformer (I_{QE} and I_{QF}). I_{QE} and I_{QF} are also the currents flowing through the synchronous rectifiers. Calculations of the current values are given respectively, as follows:

The peak current (I_{PS}) and the minimum current (I_{MS}) of the transformer secondary side are calculated as:

$$I_{PS} = \frac{P_{OUT}}{V_{OUT}} + \frac{\Delta I_{LOUT}}{2} = 330 \text{ A} \quad (7)$$

$$I_{MS} = \frac{P_{OUT}}{V_{OUT}} - \frac{\Delta I_{LOUT}}{2} = 270 \text{ A} \quad (8)$$

$$I_{MS2} = I_{PS} - \frac{\Delta I_{LOUT}}{2} = 300 \text{ A} \quad (9)$$

The secondary RMS current (I_{SRMS1}) when energy is being delivered to the secondary:

$$I_{SRMS1} = \sqrt{\left(\frac{D_{MAX}}{2}\right) \times \left[I_{PS} \times I_{MS} + \frac{(I_{PS} - I_{MS})^2}{3}\right]} = 201.6 \text{ A} \quad (10)$$

The secondary RMS current (I_{SRMS2}) when current is circulating through the transformer when MOSFETs Q1 Q4 Q5, and Q6 A7 Q8 are all on is calculated as:

$$I_{SRMS2} = \sqrt{\left(\frac{1 - D_{MAX}}{2}\right) \times \left[I_{PS} \times I_{MS2} + \frac{(I_{PS} - I_{MS2})^2}{3}\right]} = 211.4 \text{ A} \quad (11)$$

The secondary RMS current (I_{SRMS3}) caused by the negative current in the opposing winding during the freewheeling period is calculated as:

$$I_{SRMS3} = \frac{\Delta I_{LOUT}}{2} \times \sqrt{\left(\frac{1 - D_{MAX}}{2 \times 3}\right)} = 3.9 \text{ A} \quad (12)$$

As a result, the total RMS current flowing into the transformer secondary (I_{SRMS}) is calculated as:

$$I_{SRMS} = \sqrt{I_{SRMS1}^2 + I_{SRMS2}^2 + I_{SRMS3}^2} = 292 \text{ A} \quad (13)$$

The input inductor ripple current (ΔI_{LMAG}) is calculated as:

$$\Delta I_{LMAG} = \frac{V_{INMIN} \times D_{MAX}}{L_{MAG} \times F_{SW}} = 2 \text{ A} \quad (14)$$

The peak current flowing into the transformer primary side (I_{PP}) is calculated as:

$$I_{PP} = \left(\frac{P_{OUT}}{V_{OUT} \times \eta} + \frac{\Delta I_{LOUT}}{2}\right) \times \frac{1}{a_1} + \Delta I_{LMAG} = 33.4 \text{ A} \quad (15)$$

The minimum current flowing into the transformer primary side (I_{MP}) is calculated as:

$$I_{MP} = \left(\frac{P_{OUT}}{V_{OUT} \times \eta} + \frac{\Delta I_{LOUT}}{2}\right) \times \frac{1}{a_1} - \Delta I_{LMAG} = 30 \text{ A} \quad (16)$$

The minimum current at primary (I_{MP2}) when converter primary side switches are free wheeling:

$$I_{MP2} = I_{PP} - \left(\frac{\Delta I_{LOUT}}{2}\right) \times \frac{1}{a_1} = 30.7 \text{ A} \quad (17)$$

The RMS current at transformer primary side (I_{PRMS2}) when the converter is free wheeling is calculated as:

$$I_{PRMS2} = \sqrt{\left(1 - D_{MAX}\right) \times \left[I_{PP} \times I_{MP2} + \frac{(I_{PP} - I_{MP2})^2}{3}\right]} = 10.15 \text{ A} \quad (18)$$

The total RMS current flowing through transformer primary side (I_{PRMS}) is calculated as:

$$I_{PRMS} = \sqrt{I_{PRMS1}^2 + I_{PRMS2}^2} = 31.7 \text{ A} \quad (19)$$

2.4.3 Primary Side MOSFET Losses

The selection of the MOSFET is important to meet the system efficiency and electric safety. C3M0065100K 1 kV (V_{DS}), 35-A MOSFETs with 35-nC gate charge (Q_g) are selected for this design. The drain-to-source on-resistance $R_{DS(ON)}$ is 65 m Ω . The output capacitance (C_{OSS_SPEC}) is 60 pF measured under $V_{DS} = 600 \text{ V}$ according to the data sheet.

The average output capacitance $C_{OSS_QA_AVG}$ is calculated as:

$$C_{OSS_QA_AVG} = C_{OSS_SPEC} \times \sqrt{\frac{V_{DS}}{V_{INMAX}}} = 69 \text{ pF} \quad (20)$$

The total applied gate voltage is $V_g = 19 \text{ V}$. The losses of one MOSFET are calculated as:

$$P_Q = \int_0^{T_s} I_{PRMS}^2 \times R_{ds(on)} dt + \frac{1}{6 \cdot T_s} \times V_{in} \times I_{PRMS} \times T_{OFF} = 9.9 \text{ W} \quad (21)$$

2.4.4 Shim Inductor

The transformer primary side requires certain values of inductance to be equivalently in series to achieve the Zero Voltage Switching. This is called shim inductance (L_S). Obtain this inductance from either the transformer leakage inductance or from an externally added series inductor. The value is calculated based on the amount of energy required by the resonance. This inductance needs to be able to deplete the energy from the parasitic capacitance at the switch node. The parasitic capacitance is the sum of output capacitance of MOSFET, transformer winding capacitance, and the capacitance from the PCB layout.

The shim inductance (L_S) is calculated as:

$$L_S = \frac{E_{oss}}{\left(\frac{1}{2} \cdot I_{P_OFF}\right)^2} = 4.7 \text{ } \mu\text{H} \quad (22)$$

TI recommends the VT-19151B transformer from Cyntec for this reference design.

2.4.5 Output Inductor Selection

The power converter uses current-doubler rectifier at the output. It combines two advantages – efficient usage of the transformer secondary winding (like a bridge rectifier) and easy self-drive of two N-channel MOSFET synchronous rectifiers (like a full-wave center tap). It has the disadvantage of utilizing two inductor windings coupled into one common core. The output inductance is designed for obtaining the 20% ripple current (ΔI_{L_OUT}) at the output. The ripple current is calculated as:

$$\Delta I_{L_OUT} = \frac{P_{OUT} \times 0.2}{V_{OUT}} = 60 \text{ A} \quad (23)$$

The required inductance (L_{OUT}) is calculated as:

$$L_{OUT} = \frac{V_{OUT} \times (1 - D_{TYP})}{\Delta I_{L_OUT} \times F_{SW}} = 1.3 \text{ } \mu\text{H} \quad (24)$$

The RMS current of the output inductor ($I_{L_OUT_RMS}$) is calculated as:

$$I_{L_OUT_RMS} = \sqrt{\left(\frac{P_{OUT}}{V_{OUT}}\right)^2 + \left(\frac{\Delta I_{L_OUT}}{\sqrt{3}}\right)^2} = 301 \text{ A} \quad (25)$$

TI recommends the coupled inductor VI-19158A (1.3 μH) from Cyntec for this reference design.

2.4.6 Selection of Synchronous MOSFETs

Four times of MOSFETs are paralleled at the secondary side for each current freewheeling cycle to share the current and minimize the losses. To meet the power requirements 80-V, 120-A MOSFETs are selected for synchronous rectification at the secondary side with the following parameters:

$$Q_{gs} = 43 \text{ nC} \quad (26)$$

where:

- Q_{gs} is the gate-to-source charge

$$R_{DS(ON)} = 2.5 \text{ m}\Omega \quad (27)$$

The average output capacitance (C_{oss_AVG}) is calculated based on the data sheet parameters for C_{oss} , drain-to-source voltage where C_{oss_spec} was measured (V_{ds_spec}), and the maximum drain-to-source voltage in the design (V_{dsQE}) that will be applied to the MOSFET in the circuit. The voltage across the MOSFET when they are switched off is calculated as:

$$V_{dsQE} = \frac{V_{INMAX}}{a_1} = 41 \text{ V} \quad (28)$$

The average output capacitance is specified in the data sheet as $C_{oss_avg} = 2.5 \text{ nF}$.

The RMS current flowing into the MOSFETs is calculated as:

$$I_{QE_RMS} = \frac{I_{SRMS}}{4} = 55 \text{ A} \quad (29)$$

The typical gate charge curve is taken from the MOSFET data sheet as shown in [Figure 2-3](#). The gate charge at the beginning of the Miller plateau is determined as:

$$Q_{E_MILLER_MIN} = 45 \text{ nC} \quad (30)$$

The gate charge at the end of the Miller plateau is determined as:

$$Q_{E_MILLER_MAX} = 70 \text{ nC} \quad (31)$$

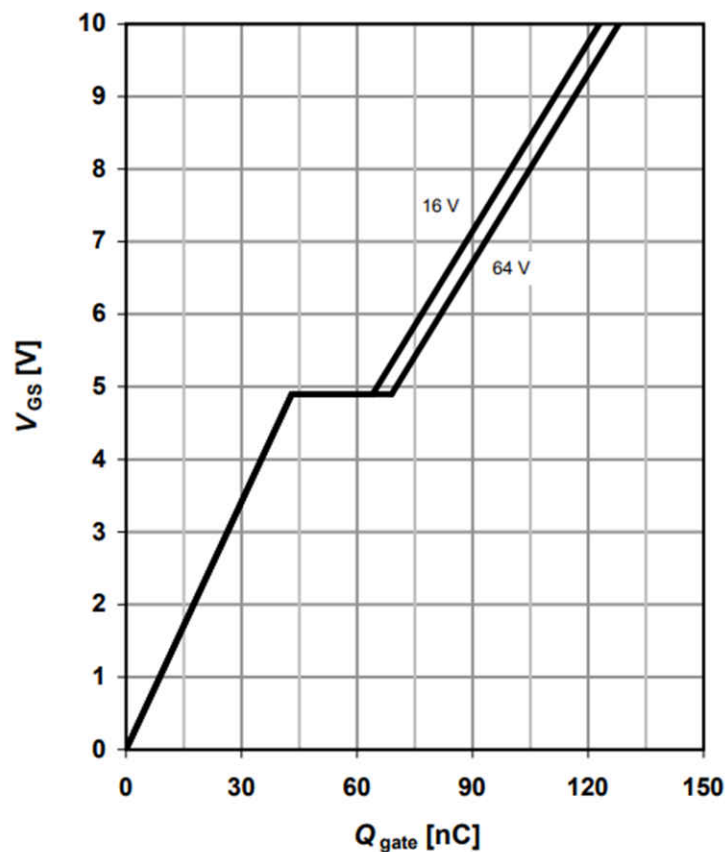


Figure 2-3. Gate Charge Curve of the IPP120N08S4

The gate driver (UCC27524A-Q1) peak source current is:

$$I_P = 5 \text{ A} \quad (32)$$

Therefore, the MOSFET switching rise and fall time are estimated as:

$$t_r \approx t_f = \frac{Q_{E_{MILLER_max}} - Q_{E_{MILLER_min}}}{I_P} = 12.5 \text{ ns} \quad (33)$$

The losses of the MOSFETs are calculated as:

$$P_{QE} = \int_0^{T_S} I_{SRMS}^2 \times R_{DS(ON)} dt + \frac{1}{8 \cdot T_S} \times V_{in} \times I_{SRMS} \times T_{OFF_S} = 7.9 \text{ W} \quad (34)$$

2.4.7 UCC28951-Q1 Configuration

The phase-shifted full bridge controller UCC28951-Q1 must be configured properly to ensure the system works correctly and reliably. The component surrounding the controller is shown in [Figure 2-4](#).

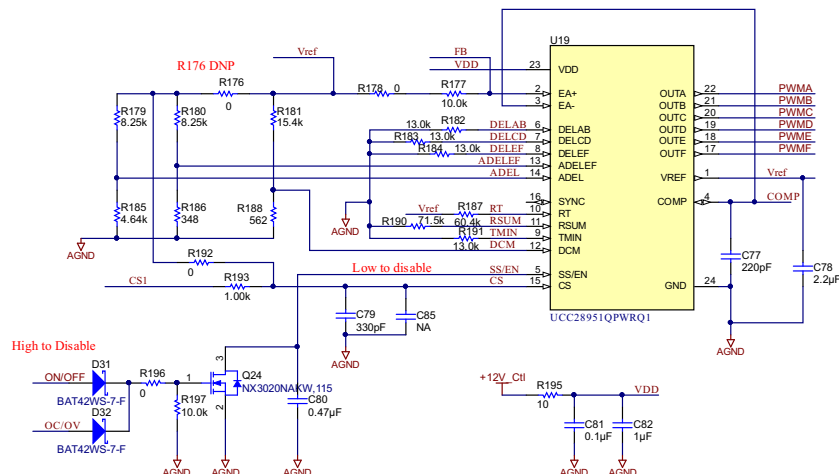


Figure 2-4. Configuration of the UCC28951-Q1

2.4.7.1 Current Sense Network

The current sense network must be designed such that it has strong noise immunity to avoid it being injected into the adaptive delay circuit, which will cause fault PWM driving signals.

The nominal peak current (I_{P1}) flowing at the minimum input voltage V_{INMIN} is calculated as:

$$I_{P1} = \left(\frac{P_{OUT}}{V_{OUT} \times \eta} + \frac{\Delta I_{LOUT}}{2} \right) \times \frac{1}{a_1} + \frac{V_{INMAX} \times D_{MAX}}{L_{MAG} \times F_{SW}} = 36 \text{ A} \quad (35)$$

Therefore the Current Transformer (T1) for this design needs to have the current rating higher than the 36 A. Figure 2-5 shows the schematic of the current transformer. The cycle by cycle current limit threshold of the CS pin is $V_P = 2 \text{ V}$. With 200-mV headroom left for slope compensation, the current sense resistor (R15 in parallel with R16) is calculated as:

$$R_S = \frac{V_P - 0.2 \text{ V}}{\frac{I_{P1}}{a_2} \times 1.1} = 9.4 \Omega \quad (36)$$

R_S is selected as two times of 20- Ω resistors in parallel, which results in 10 Ω in total.

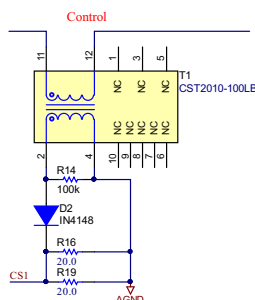


Figure 2-5. Current Sense Network at Input

The maximum voltage across D3 (V_{DA}) is calculated as:

$$V_{DA} = V_P \times \frac{D_{CLAMP}}{1 - D_{CLAMP}} = 98 \text{ V} \quad (37)$$

A fast reverse recovery diode part number IN4148W with 100-V breaking down voltage is chosen for this design. The power losses (P_{DA}) for D3 is calculated as:

$$P_{DA} = \frac{P_{OUT} \times 1.3 V}{V_{INMIN} \times 95\% \times a_2} = 0.25 W \quad (38)$$

The reset resistor R17 is placed to demagnetizing the current transformer. The buildup voltage during the on time of current transformer is calculated as:

$$V_{T1ON} = V_f + \left(\frac{I_{PRMS1}}{a_2} \right) \times R_S = 2.3 V \quad (39)$$

2.4.7.2 Voltage and Current Regulation Loop

The output voltage and current feedback loops are designed with high-bandwidth operational-amplifier-based feedback circuits. The outputs of the amplifiers are connected with reversely connected ORing diodes as shown in Figure 2-6. The implementations permit the loop channel with lower regulation output being dominant.

For the voltage regulation loop, the DC reference voltage is set as 2.5 V by the voltage divider R111, R127, and R130. This represents the regulated voltage of 12 V when the feedback voltage reaches 2.5 V. For the current regulation loop, the reference voltage is set as 3.75 V by the voltage divider R89, R92, and R106. This represents the regulated current of 300 A when the current sense output voltage reaches 3.75 V.

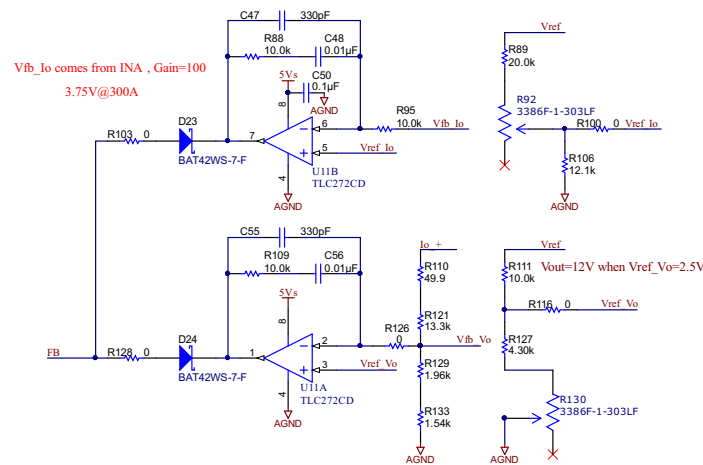


Figure 2-6. Output Voltage and Current Regulation Feedback Networks

2.4.7.3 Adaptive Delay DELAB, DELCD, and ADEL

The UCC28951-Q1 offers two different adaptive delay management techniques which improves the efficiency over a wide load current range:

1. ADEL, which sets and optimizes the dead-time control for the primary switches over a wide load current range. ADEL sets the delay between one of the outputs OUTA or OUTB going low and the other output going high.
2. ADELEF, which sets and optimizes the delay-time control between the primary side switch OUTA or OUTB going low and the secondary side switch OUTF or OUTE going low.

The resistor R51 from DELAB pin to GND, along with the resistor divider R41 and R53 from the CS pin to GND set the delay time between PWM outputs to the MOSFETs at the same bridge, pin OUTA or OUTB going low and the other output going high, which is represented as T_{ABSET1} or T_{ABSET2} as shown in Figure 2-7.

The CS signal fed into the ADEL pin sets and dead time control for the primary switches is dependent on the load current change. The delay time varies reversely proportional the CS signal amplitude. It gradually increases from T_{ABSET1} , which is measured at $V_{CS} = 1.5 V$, to T_{ABSET2} , which is measured at $V_{CS} = 0.2 V$. The delay time is fixed, independent of the load, when a fixed voltage is applied to the ADEL pin.

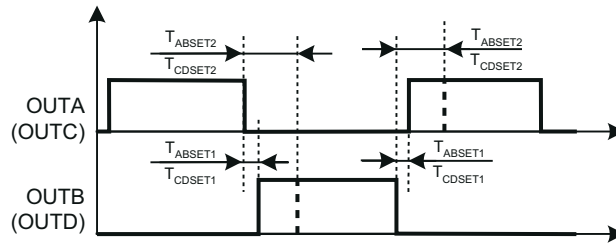


Figure 2-7. Delay Definitions Between OUTA and OUTB, OUTC and OUTD

The turn-on delay of primary MOSFETs Q16 (PWM signal OUTB) after Q1 (PWM signal OUTA) is initially set based on the interaction of leakage inductance L_s and the theoretical switch node capacitance. The resonant tank frequency is calculated as:

$$f_R = \frac{1}{2 \times \pi \times \sqrt{L_s \times (2 \times C_{OSS_QA_AVG})}} = 7.5 \text{ MHz} \quad (40)$$

The initial t_{ABSET} is calculated as:

$$t_{ABSET} = \frac{2.25}{f_R \times 4} = 75 \text{ ns} \quad (41)$$

The coefficient K_A defines how significantly the delay time depends on the CS voltage. K_A varies from 0, where the ADEL pin is shorted to ground and the delay does not depend on CS voltage, to 1 where ADEL is tied to CS ($R_{192} = 0$). In this design, K_A is set as:

$$K_A = \frac{R_{179}}{R_{185} + R_{179}} = 0.64 \quad (42)$$

Therefore the resistor from DELAB to GND R_{182} is calculated as:

$$R_{182} = \frac{T_{ABSET} \times (0.26V + V_{CS} \times K_A \times 1.3)}{5} = 13 \text{ k}\Omega \quad (43)$$

where:

- V_{CS} is the voltage seen from pin CS when ZVS is expected to occur

The turn on delays of OUTC and OUTD are set the same as T_{ABSET} ; therefore, R_{183} is selected as 13 k Ω as well. The reflected output current is present in the primary of the transformer at SiC MOSFET Q2 and Q17 switching.

2.4.7.4 Adaptive Delay DELEF, ADELEF

The resistor R_{184} from DELEF pin to GND, along with the resistor divider R_{180} and R_{186} from CS pin to GND set the delay time between PWM outputs to the MOSFETs at primary side, pin OUTA or OUTB going low and related output OUTF or OUTE going low, which is represents as T_{AFSET1} or T_{AFSET2} shown in **Figure 8**.

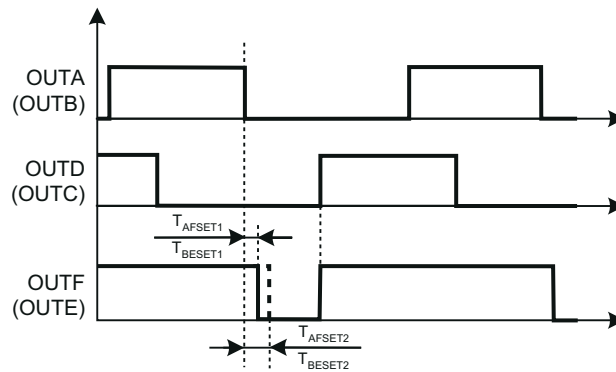


Figure 2-8. Delay Definitions Between OUTA and OUTF, OUTB and OUTE

The turn-off delay of synchronous MOSFET SR5, SR6, SR7 and SR8 (PWM signal OUTE) after turn off of primary MOSFET Q16 (PWM signal OUTB) is set as 90 ns.

The CS voltage influence to T_{AFSET} implies the same as adaptive delay mechanism as ADEL circuitry. The coefficient K_{EF} is defined as:

$$K_{EF} = \frac{R_{186}}{R_{186} + R_{180}} = 0.04 \quad (44)$$

The resistor from DELEF to GND R184 is calculated as:

$$R_{49} = \frac{(T_{AFSET} - 4ns) \times (2.65V - V_{CS} \times K_{EF} \times 1.32)}{5} = 13 \text{ k}\Omega \quad (45)$$

Figure 2-9 shows the overview of PWM switching and output waveforms of the phase-shifted full bridge converter.

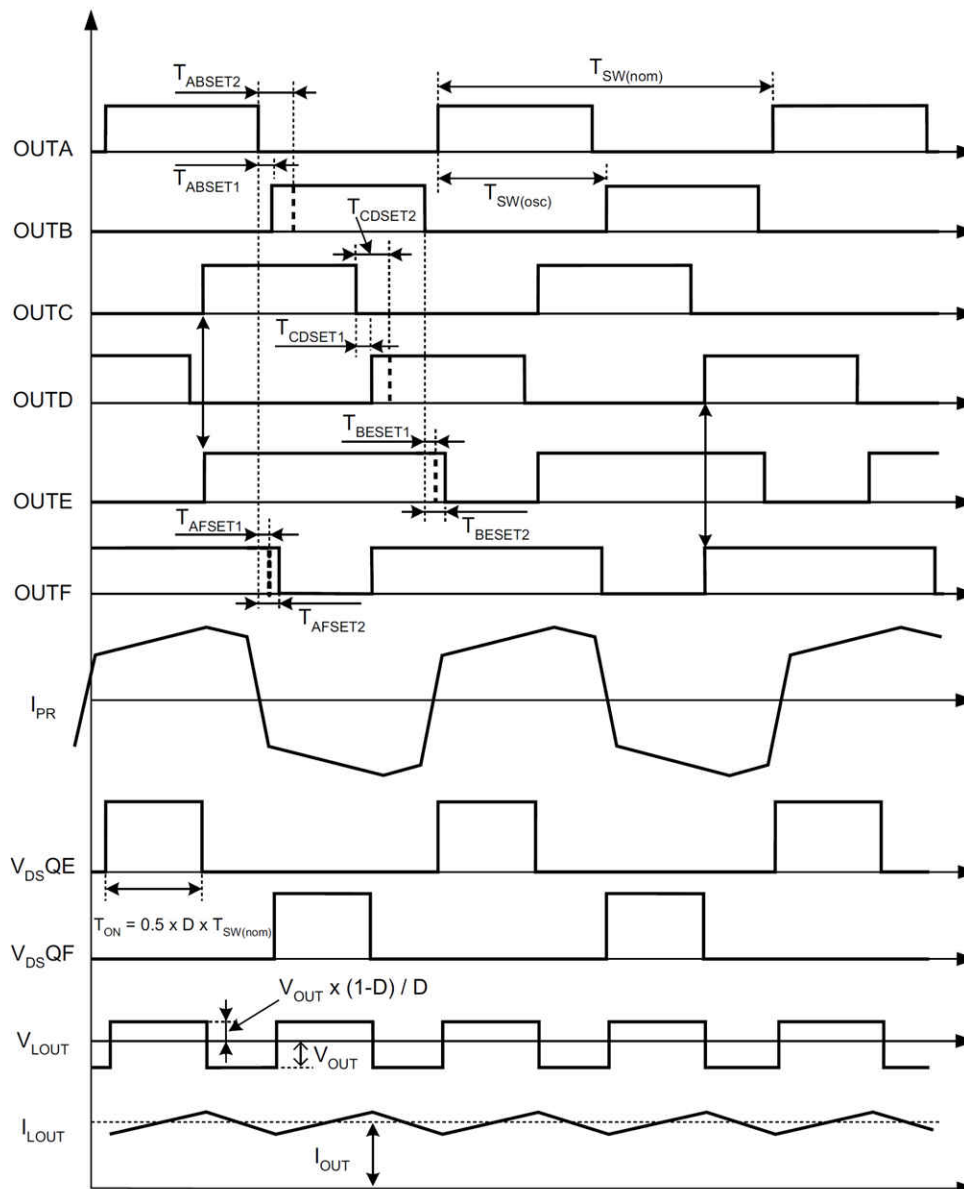


Figure 2-9. PWM Control and Output Waveforms of the Phase-Shifted Full Bridge Converter

2.4.7.5 Minimum Pulse (T_{MIN})

To enable ZVS at light load, a resistor R_{TMIN} is placed between the T_{MIN} pin to GND to set a fixed minimum pulse width. If the output PWM pulse demanded by the feedback loop is shorter than T_{MIN}, the converter goes to burst mode where an even number of T_{MIN} pulses are followed by the off time dictated by the feedback loop. T_{MIN} duration needs to be selected such that it is sufficient for raising the magnetizing current in the power transformer to maintain ZVS. The typical start-up waveform and burst mode operation of the UCC28951-Q1 is shown in Figure 2-10.

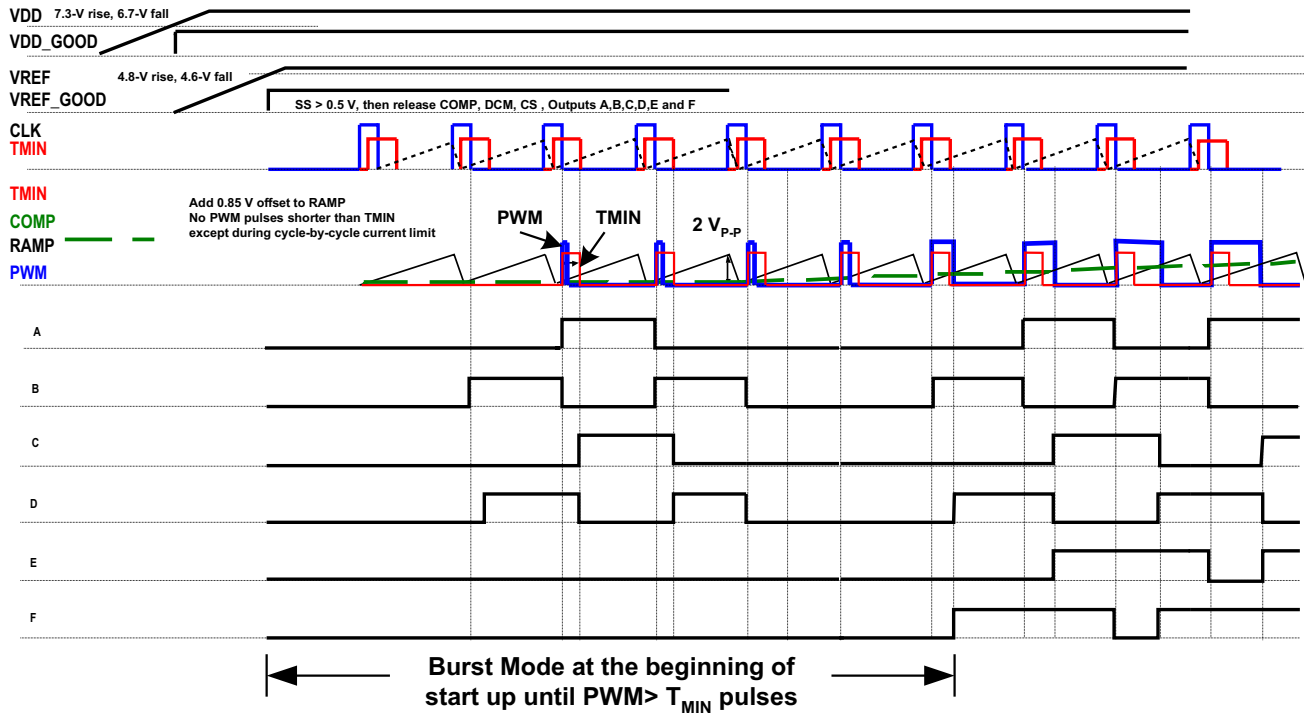


Figure 2-10. UCC28951-Q1 Start-up Waveform and Burst Mode Operation

The minimum on time for this design is set to 80 ns. R_{TMIN} is calculated as:

$$R_{TMIN} = \frac{t_{MIN}}{5.92} = 13 \text{ k}\Omega \quad (46)$$

2.4.7.6 Switching Frequency

The external resistor, R_T , which is connected from the RT pin to the VREF pin sets the switching frequency of the UCC28951-Q1. A switching frequency of 100 kHz is selected as a compromise between component size and efficiency. The value of R_T is calculated as:

$$R_T = \left(\frac{2.5 \times 10^6}{F_{SW}} - 1 \right) \times (V_{REF} - 2.5V) = 60.4 \text{ k}\Omega \quad (47)$$

2.4.7.7 Slope Compensation

Slope compensation is needed to prevent a sub-harmonic oscillation in the peak current mode control^[4]. This can be set by setting R_{SUM} with the following equations. The inductor current ramp downslope as seen at the CS pin input is calculated as:

$$m_0 = \frac{V_{OUT}}{L_{OUT}} \times \frac{R_S}{a_1 \times a_2} = 0.08 \frac{V}{\mu s} \quad (48)$$

where:

- L_{OUT} is the output inductance
- R_s is the current sense resistor
- a_1 is the turns ratio of power transformer (N_P / N_S)
- a_2 is the turns ratio of the current transformer (I_P / I_S)

The slope of the additional ramp (m_e) which is added to the CS signal is obtained by placing the resistor (R_{SUM}) to ground. m_e is calculated as:

$$m_e = \left(\frac{2.5}{0.5 \times R_{SUM}} \right) \frac{V}{\mu s} \quad (49)$$

Let m_e equalize m_0 ; therefore, R_{SUM} is calculated as:

$$R_{SUM} = \left(\frac{2.5 \times 2}{0.08} \right) k\Omega = 62.5 k\Omega \quad (50)$$

A 71.5-k Ω resistor (R190) is chosen for this application.

2.4.7.8 Dynamic SR ON and OFF Control

The voltage at the DCM pin is provided by the resistor divider R_{DCMHI} (R181) between the VREF pin and DCM. R_{DCM} (R188) from DCM pin to GND, sets the percentage of 2-V current limit threshold for the Current Sense pin, (CS). If the CS pin voltage falls below the DCM pin threshold voltage, then the controller initiates the light load power saving mode, and shuts down the synchronous rectifiers, OUTE and OUTF. If the CS pin voltage is higher than the DCM pin threshold voltage, then the controller runs in CCM mode.

This design sets the percentage to roughly 10% of the load current. The threshold is calculated as:

$$V_{RS} = \frac{\left(\frac{P_{OUT} \times 0.15}{V_{OUT}} + \frac{\Delta I_{LOUT}}{2} \right) \times R_S}{a_1 \times a_2} = 0.3 V \quad (51)$$

Set a standard resistor value for R_{DCMHI} :

$$R_{DCMHI} = 15 k\Omega \quad (52)$$

The resistor value of R_{DCM} is calculated as:

$$R_{DCM} = \frac{R_{DCMHI} \times V_{RS}}{V_{REF} - V_{RS}} = 957 \Omega \quad (53)$$

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware

Figure 3-1 shows the assembled board image of TIDA-020031 DC/DC converter system. The input and output connectors, resonant inductor at primary side, power transformer, coupled output inductor, and isolated gate driver daughter cards are indicated.

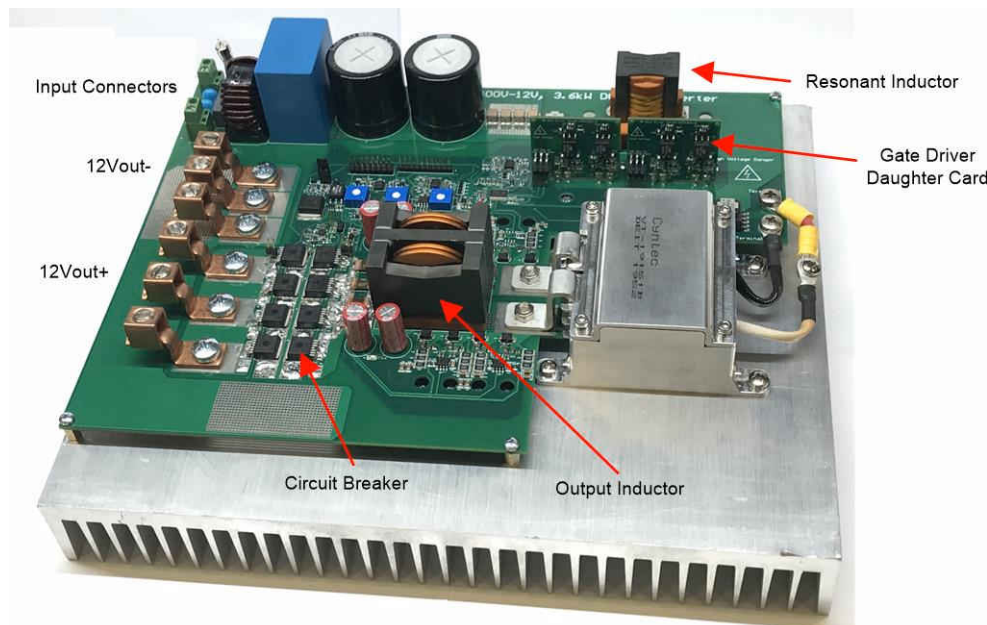


Figure 3-1. TIDA-020031 DC/DC Converter Board Image

3.2 Testing and Results

3.2.1 Test Setup

Test equipment needed to perform the measurements for this reference design include:

1. Power supply (or 12-V battery) to drive control electronics
2. 4-channel oscilloscope with high-voltage differential probes to measurement the PWM and MOSFET drain-to-source signals
3. 400-V output, larger than 3.6 kW high-voltage DC power supply
4. 300-A current output electronic load

3.2.2 Test Results

3.2.2.1 Start-up and Power Down

The start-up waveform of the converter is shown in Figure 3-2. Figure 3-3 shows the power down of the converter.

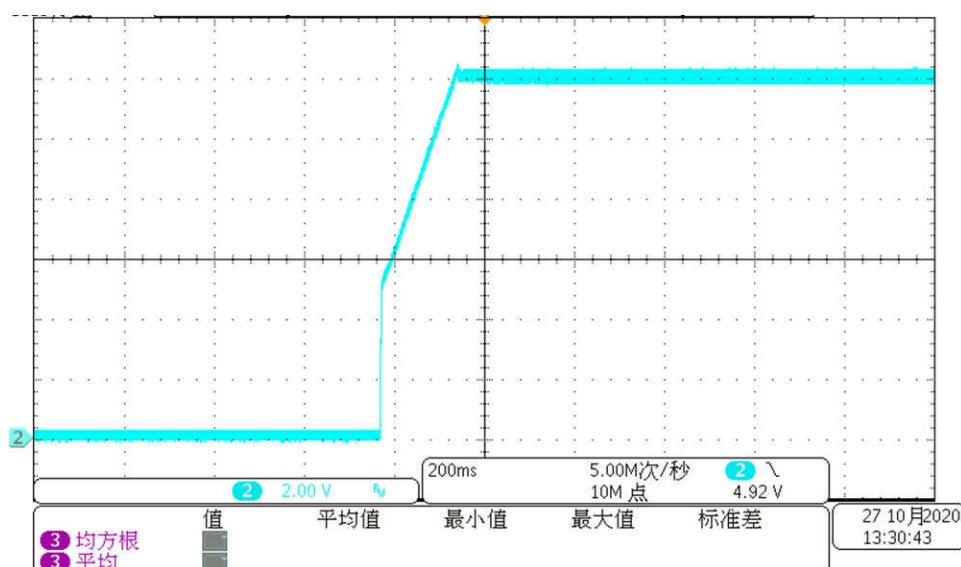


Figure 3-2. TIDA-020031 Start-up Waveforms

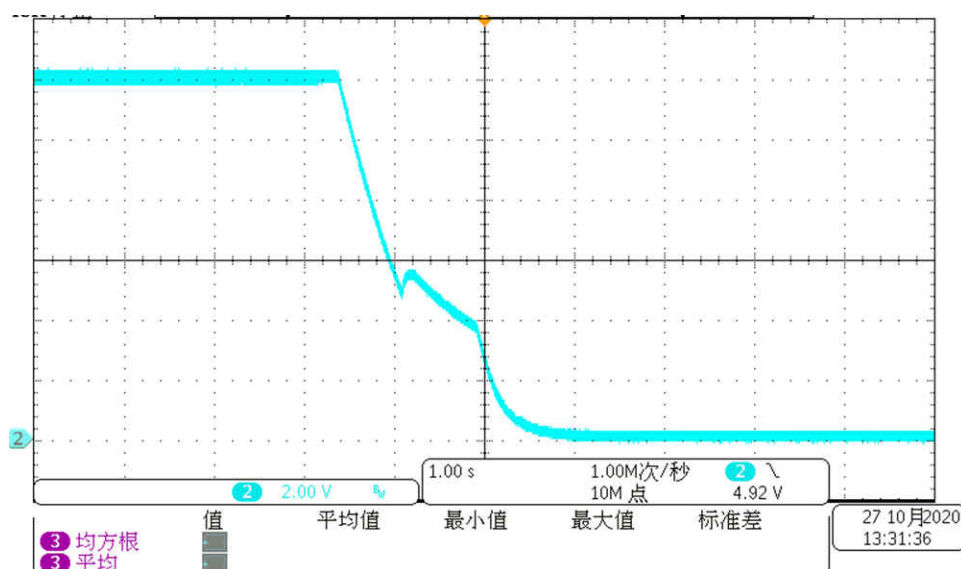


Figure 3-3. TIDA-020031 Power Down Waveform

3.2.2.2 Output Voltage Ripple

Output voltage ripple of TIDA-020031 is measured under light load and 100-A load conditions respectively. The input voltage is 400 V for both measurements. The waveforms are shown in Figure 3-4 and Figure 3-5. The images illustrate that at around 200-mV peak-to-peak ripple voltage is obtained at 100-A load condition.

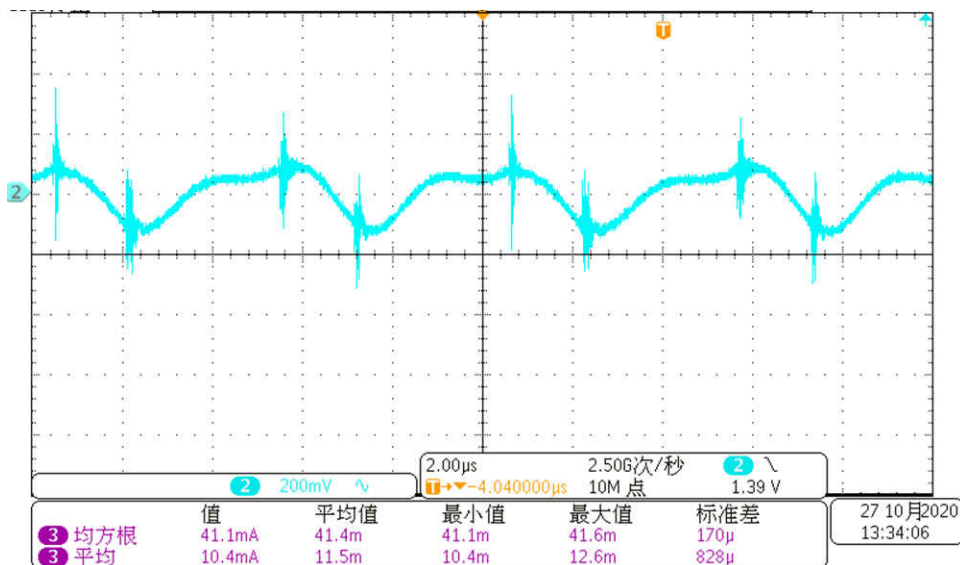


Figure 3-4. TIDA-020031 Output Voltage Ripple Under $V_{IN} = 400$ V and No Load

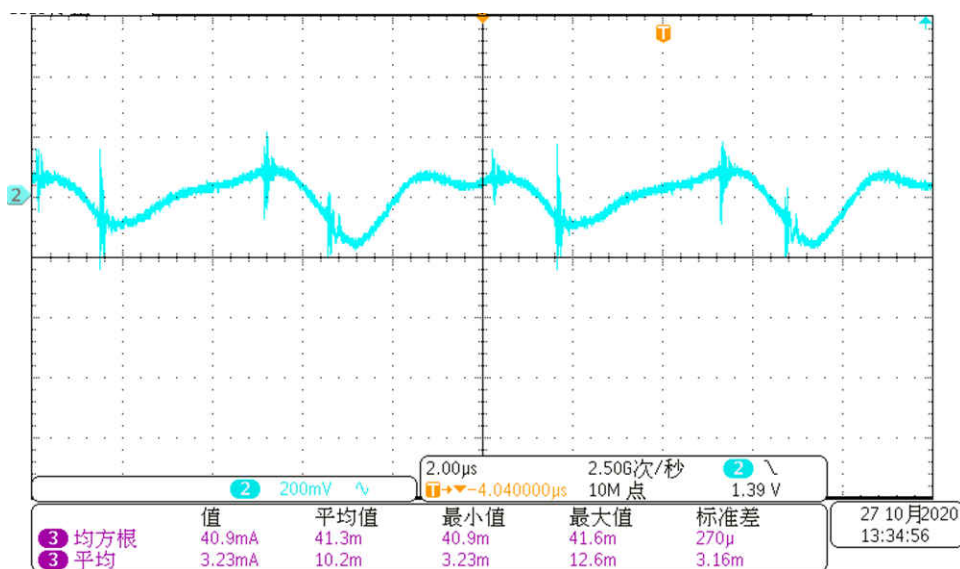


Figure 3-5. TIDA-020031 Output Voltage Ripple Under $V_{IN} = 400$ V and $I_{OUT} = 100$ A

3.2.2.3 Full Bridge Primary Switch Node Voltages

The gate drive signals versus the switch node voltages of the primary side switches are measured under varies load conditions and shown from Figure 3-6 to Figure 3-9. The images illustrate that the ZVS resonance occurs earlier when the load current increases.

3.2.2.3.1 Under 10-A Load

Figure 3-6 and Figure 3-7 show the gate drive signals versus the switch node voltages of the primary side switches under 5-A load.

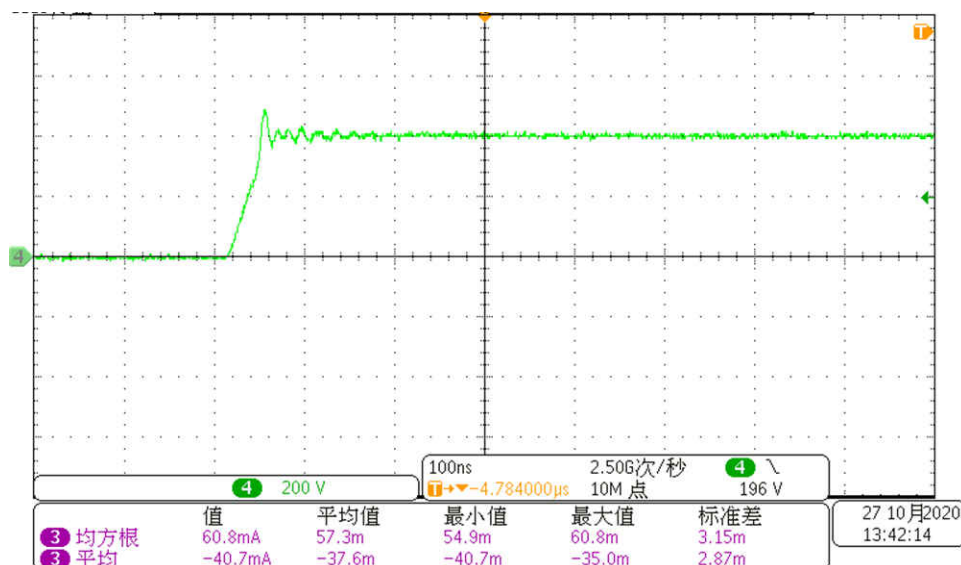


Figure 3-6. Leading Bridge Switch Node at 10 A

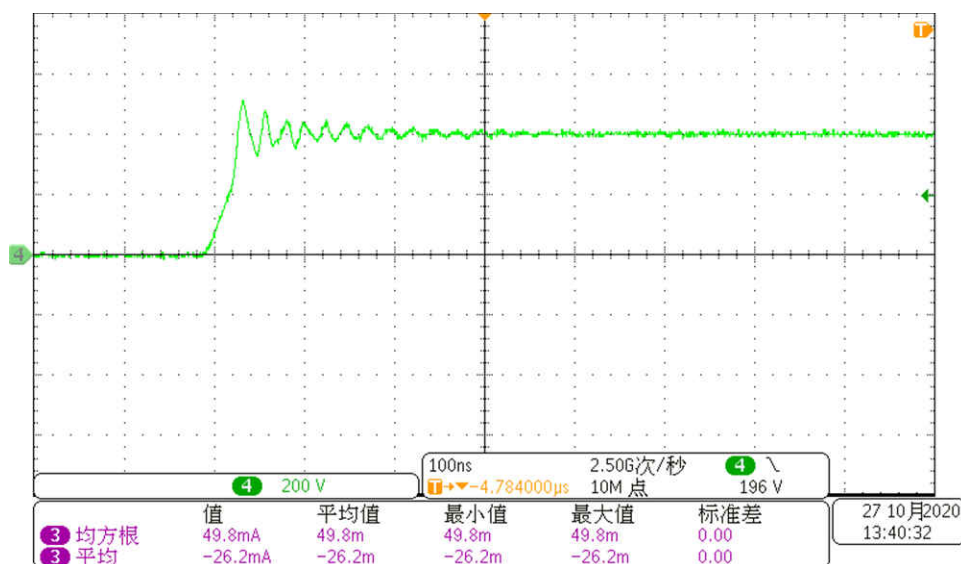


Figure 3-7. Lagging Bridge Switch Node at 10 A

3.2.2.3.2 Under 100-A Load

Figure 3-8 and Figure 3-9 show the gate drive signals versus the switch node voltages of the primary side switches under 15-A load.

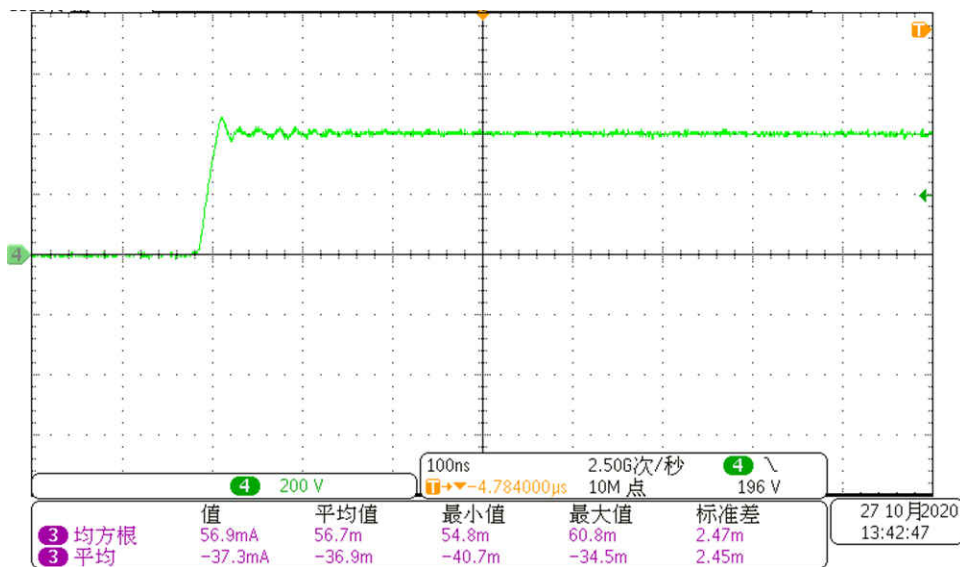


Figure 3-8. Leading Bridge Switch Node at 100 A

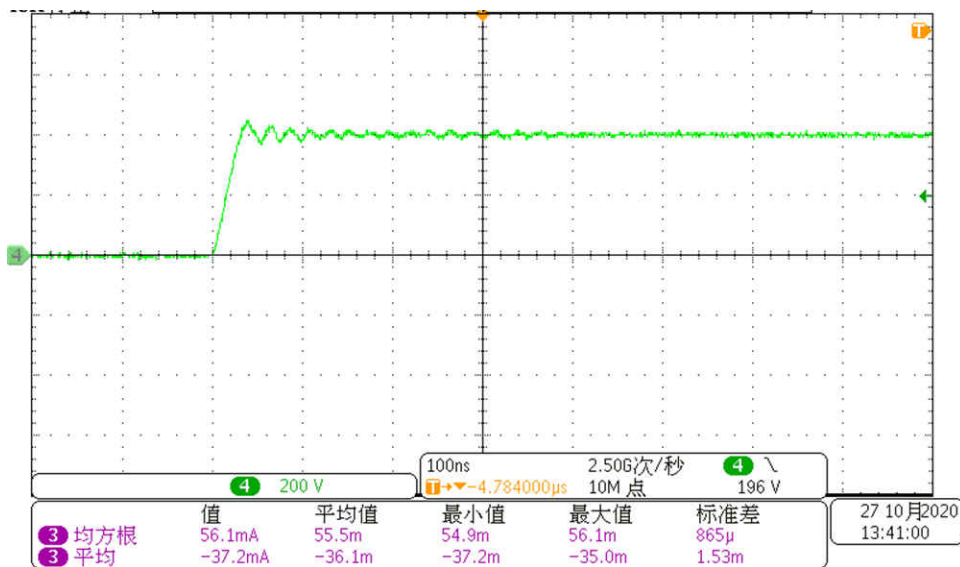


Figure 3-9. Lagging Bridge Switch Node at 100 A

3.2.2.4 Efficiency

Efficiency of the TIDA-020031 is measured under conditions of different input voltages. Figure 3-10 shows the measurement setup. Two precision digital multimeters are placed at the input for measuring the input voltage and input current respectively. Another multimeter is placed at the output for measuring the output voltage. The output current is indirectly measured by the voltage drop from a precision shunt resistor.

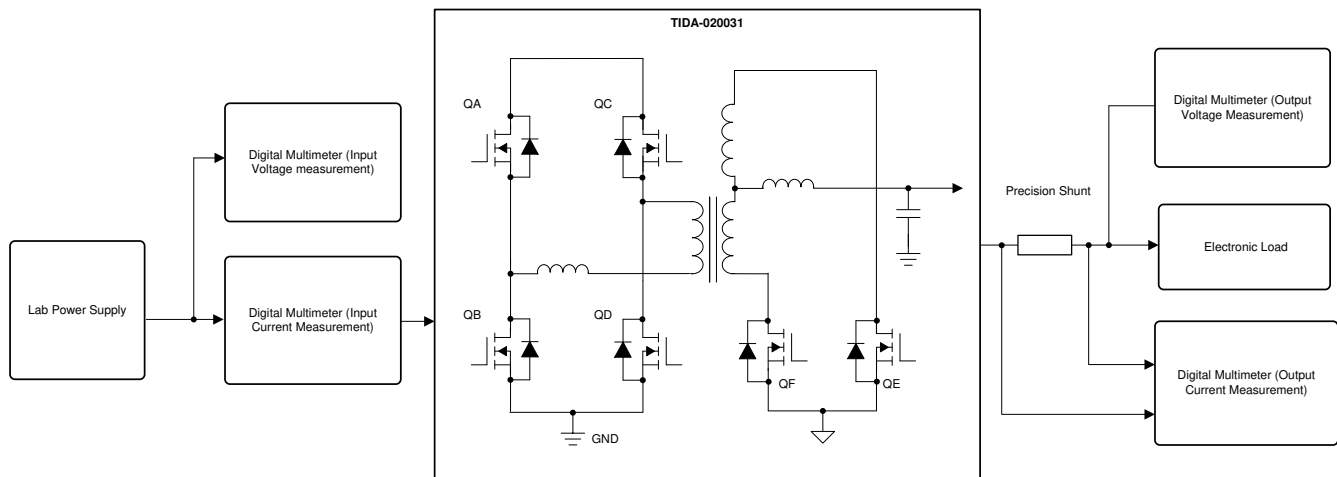


Figure 3-10. Experiment Setup for Measuring the Efficiency of TIDA-020031

Figure 3-11 shows the measured efficiency of TIDA-020031. The image illustrates a peak efficiency of 96.5% is achieved at 300-V input voltage and 80-A load ($V_{IN} = 300V$, $V_{IN} = 400 V$).

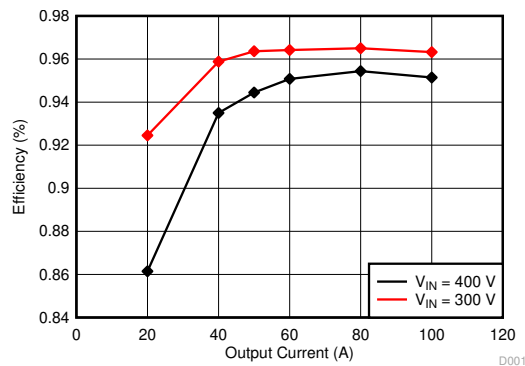


Figure 3-11. Measured Efficiency Under Input Voltages of 300 V, 400 V

3.2.2.5 Load Regulation ($V_{IN} = 250\text{ V}$, $V_{IN} = 400\text{ V}$)

Load regulation measurements show the % deviation from nominal output voltage as a function of output current. The experiment setup is the same as that of the efficiency measurement, as shown in [Figure 3-10](#). The measured results with 48-V and 60-V input voltages are shown in [Figure 3-12](#).

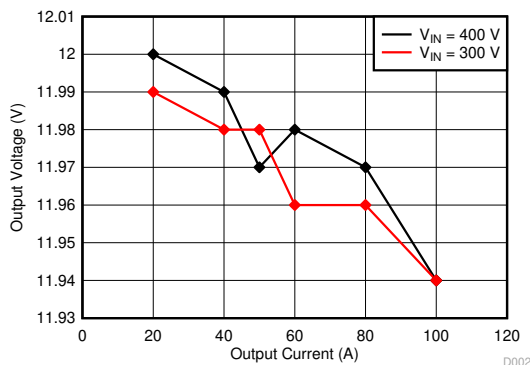


Figure 3-12. Load Regulation With $V_{IN} = 300\text{ V}$ and $V_{IN} = 400\text{ V}$

3.2.2.6 Load Transient Response

Load transient response presents how well a power supply copes with the changes in the load current demand. [Figure 3-13](#) shows the load transient response of TIDA-020031. The load is switching from 16.5 A to 33 A with a period of 5 ms and 50% duty cycle. The input voltage is set to 60 V.

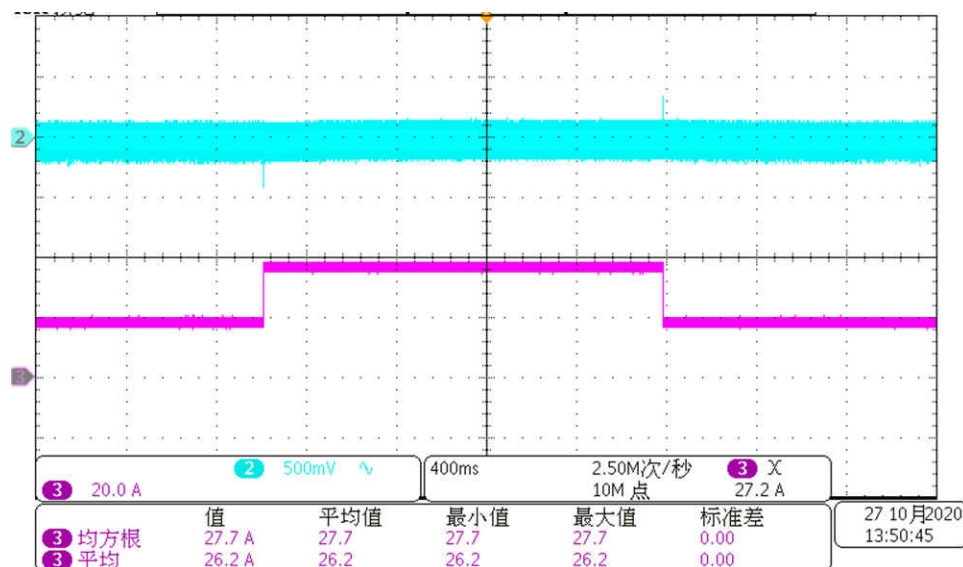


Figure 3-13. Load Transient Response Under $V_{IN} = 400$ V and I_{OUT} Switching Between 50 A and 100 A

3.2.2.7 Thermal Images

Thermal image of the design board is measured under the full load conditions. The circuit runs at the room temperature for 15 minutes. A 48 V nominal voltage is applied. The converter is loaded with 100 A and output power is 1.2 kW. [Figure 3-16](#) shows the temperature of thermal image of the inductor and circuit breaker MOSFETs on the secondary side.

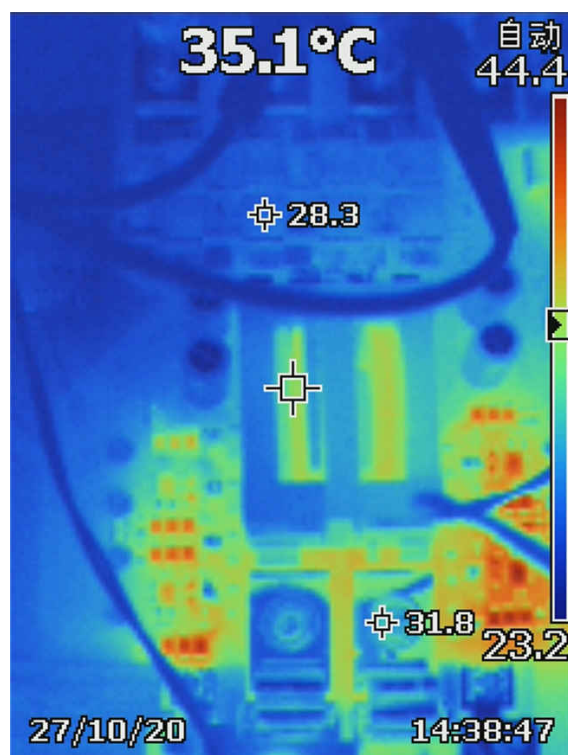


Figure 3-14. Thermal Image of the Inductor

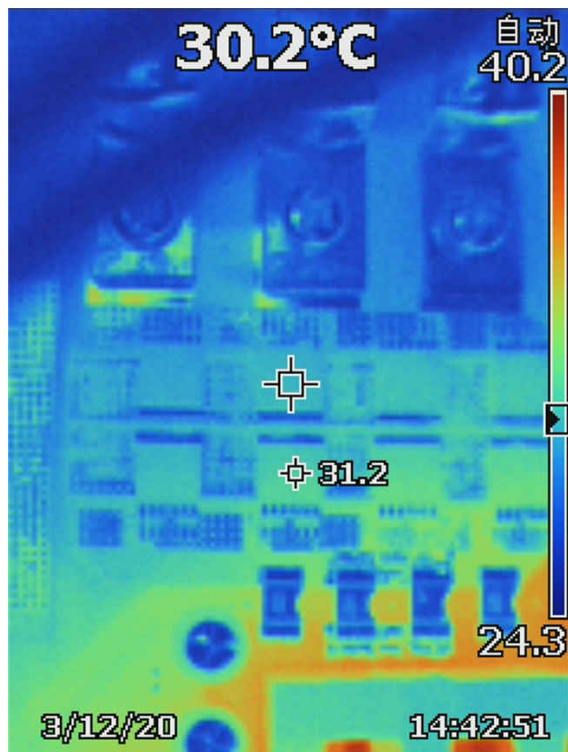


Figure 3-15. Circuit Breaker MOSFETs on the Secondary Side

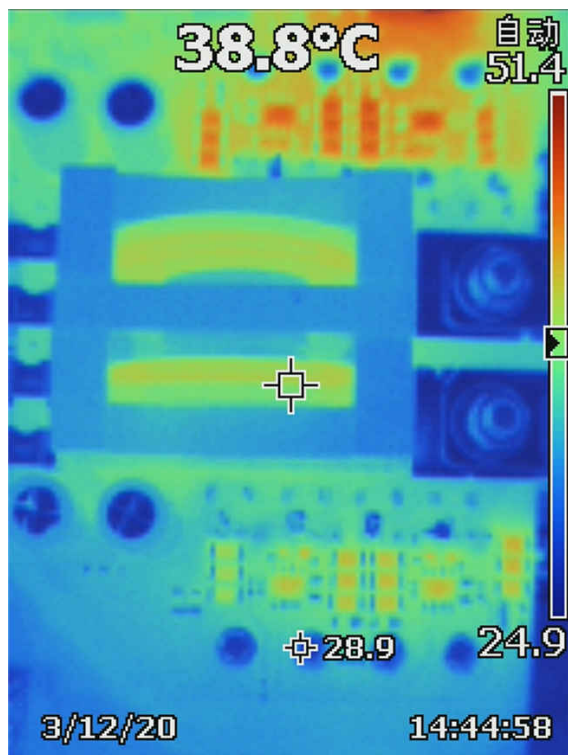


Figure 3-16. Thermal Image of Coupled Inductor at Secondary Side

4 Design Files

4.1 Schematics

To download the schematics, see the design files at [TIDA-020031](#).

4.2 BOM

To download the bill of materials (BOM), see the design files at [TIDA-020031](#).

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the Layout Prints for each board, see the design files at [TIDA-020031](#).

4.4 Altium Project

To download the Altium project files for each board, see the design CAD files at [TIDA-020031](#).

4.5 Gerber Files

To download the Gerber Files for each board, see the design files at [TIDA-020031](#).

4.6 Assembly Drawings

To download the Assembly Drawings for each board, see the design files at [TIDA-020031](#).

4.7 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 Related Documentation

1. Texas Instruments, [Automotive Wide Vin Front-End Power Reference Design w/Cold Crank Operation and Transient Protection - TIDA-01179](#)
2. Texas Instruments, [A Design Review of a Full-Featured 350-W Offline Power Converter User Guide](#)
3. Texas Instruments, [UCC28950 600-W, Phase-Shifted, Full Bridge Application Report](#)
4. Texas Instruments, [Modeling, Analysis and Compensation of the Current-Mode Converter Application Report](#)

6 Terminology

AFE	Analog Front End
AEC	Automotive Electronics Council
ESR	Equivalent Series Resistance
EMI	Electromagnetic Interference
EMC	Electromagnetic Compatibility
DM	Differential Mode
CM	Common Mode
DCM	Discontinuous Conduction Mode
CCM	Continuous Conduction Mode
UVLO	Under Voltage Lockout
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CISPR	International Special Committee on Radio Interference
PE	Protective Earth
RMS	Root Mean Square
BOM	Bill of Material
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
HEV	Hybrid Electric Vehicle
EV	Electric Vehicle

7 About the Author

Jason Cao is an Automotive Systems Engineer in HEV/EV and powertrain team, where he is responsible for developing reference design solutions, including on-board-charger, DCDC converter, Traction Inverter as well as the powertrain integration solutions. He is experienced in Wide-Bandgap-Device applications such as GaN in achieving high efficient, high power density system designs. Besides, he is a Certified Functional Safety Engineer from ISO26262 TUV SUED.

Xun Gong is an Automotive Systems Manager at Texas Instruments, where he is responsible for leading system engineering team for the automotive segment focusing on HEV/EV Power Train system applications. Xun brings to this role expertise in the field of Traction Inverter, Onboard Charger, EMI and EMC, and DC-DC converters. Xun achieved his Ph.D. in Electrical Engineering from Delft University of Technology in Delft, Netherlands.

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