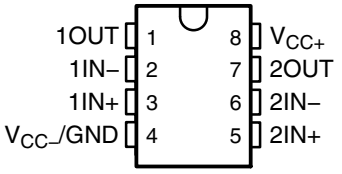
SLOS200G – OCTOBER 1997 – REVISED JULY 2003

- **Wide Gain-Bandwidth Product . . . 4 MHz**
- **High Slew Rate . . . 13 V/μs**
- **Fast Settling Time . . . 1.1 μs to 0.1%**
- **Wide-Range Single-Supply Operation . . . 4 V to 36 V**
- **Wide Input Common-Mode Range Includes Ground (V_{CC-})**
- **Low Total Harmonic Distortion . . . 0.02%**
- **Large-Capacitance Drive Capability . . . 10,000 pF**
- **Output Short-Circuit Protection**

D OR P PACKAGE
(TOP VIEW)



description/ordering information

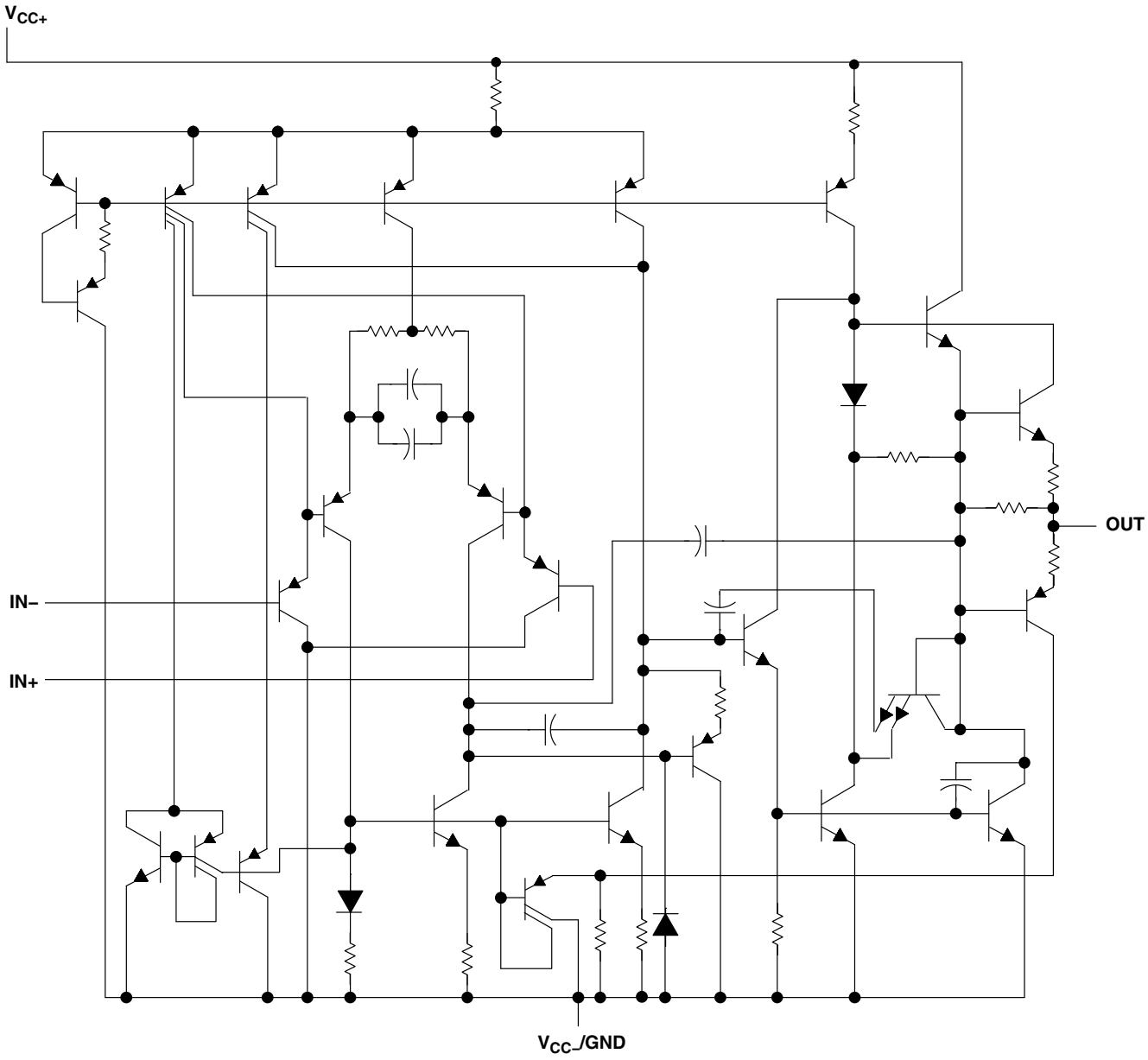
Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3472 operational amplifier. This device offers 4 MHz of gain-bandwidth product, 13-V/μs slew rate, and fast settling time, without the use of JFET device technology. Although the TL3472 can be operated from split supplies, it is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential (V_{CC-}). With a Darlington transistor input stage, this device exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 25	TL3472CP	TL3472CP
	SOIC (D)	Tube of 50	TL3472CD	3472C
		Reel of 2500	TL3472CDR	
–40°C to 105°C	PDIP (P)	Tube of 25	TL3472IP	TL3472IP
	SOIC (D)	Tube of 50	TL3472ID	Z3472
		Reel of 2500	TL3472IDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC+} . . . . . 18 V
V_{CC-} . . . . . –18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±36 V
Input voltage, V_I (any input) . . . . . $V_{CC±}$
Input current, I_I (each input) . . . . . ±1 mA
Output current, I_O . . . . . ±80 mA
Total current into V_{CC+} . . . . . 80 mA
Total current out of V_{CC-} . . . . . 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package . . . . . 97°C/W
P package . . . . . 85°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive input current can flow when the input is less than V_{CC-} – 0.3 V.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
4. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
$V_{CC±}$	Supply voltage		4	36	V
V_{IC}	Common-mode input voltage	V_{CC} = 5 V	0	2.8	V
		$V_{CC±}$ = ±15 V	–15	12.8	
T_A	Operating free-air temperature	TL3472C	0	70	°C
		TL3472I	–40	105	

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω	V_{CC} = 5 V		25°C		1.5	10	mV
			V_{CC} = ±15 V		25°C		1.0	10	
					Full range‡			12	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage		V_{CC} = ±15 V		Full range‡		10		μV/°C
I_{IO}	Input offset current		V_{CC} = ±15 V		25°C		6	75	nA
					Full range‡			300	
I_{IB}	Input bias current		V_{CC} = ±15 V		25°C		100	500	nA
					Full range‡			700	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω			25°C		–15 to 12.8		V
					Full range‡		–15 to 12.8		
V_{OH}	High-level output voltage	V_{CC+} = 5 V,	V_{CC-} = 0,	R_L = 2 kΩ	25°C	3.7	4		V
		R_L = 10 kΩ			25°C	13.6	14		
		R_L = 2 kΩ			Full range‡	13.4			
V_{OL}	Low-level output voltage	V_{CC+} = 5 V,	V_{CC-} = 0,	R_L = 2 kΩ	25°C		0.1	0.3	V
		R_L = 10 kΩ			25°C		–14.7	–14.3	
		R_L = 2 kΩ			Full range‡			–13.5	
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L = 2 kΩ		25°C	25	100		V/mV
					Full range‡	20			
I_{OS}	Short-circuit output current	Source: V_{ID} = 1 V,	V_O = 0		25°C	–10	–34		mA
		Sink: V_{ID} = –1 V,	V_O = 0			20	27		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}(min),	R_S = 50 Ω		25°C	65	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±13.5 V to ±16.5 V,		R_S = 100 Ω	25°C	70	97		dB
I_{CC}	Supply current (per channel)	V_O = 0,	No load		25°C		3.5	4.5	mA
					Full range‡		4.5	5.5	
		V_{CC+} = 5 V, V_O = 2.5 V, V_{CC-} = 0, No load			25°C		3.5	4.5	

† All typical values are at T_A = 25°C.
‡ Full range is 0°C to 70°C for the TL3472C device and –40°C to 105°C for the TL3472I device.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+	Positive slew rate	V_I = –10 V to 10 V, R_L = 2 kΩ, C_L = 300 pF	A_V = 1	8	10		V/μs
SR–	Negative slew rate		A_V = –1		13		V/μs
t_s	Settling time	A_{VD} = –1, 10-V step	To 0.1%		1.1		μs
			To 0.01%		2.2		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 100 Ω		49		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz			0.22		pA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V to 20 V, R_L = 2 kΩ, A_{VD} = 10, f = 10 kHz			0.02		%
GBW	Gain-bandwidth product	f =100 kHz		3	4		MHz
BW	Power bandwidth	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 1, THD = 5.0%			160		kHz
ϕ_m	Phase margin	R_L = 2 kΩ	C_L = 0		70		deg
			C_L = 300 pF		50		
	Gain margin	R_L = 2 kΩ	C_L = 0		12		dB
			C_L = 300 pF		4		
r_i	Differential input resistance	V_{IC} = 0			150		MΩ
C_i	Input capacitance	V_{IC} = 0			2.5		pF
	Channel separation	f = 10 kHz			101		dB
z_o	Open-loop output impedance	f = 1 MHz,	A_V = 1		20		Ω

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL3472CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3472C
TL3472CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3472CP
TL3472IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3472
TL3472IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3472IP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TL3472 :

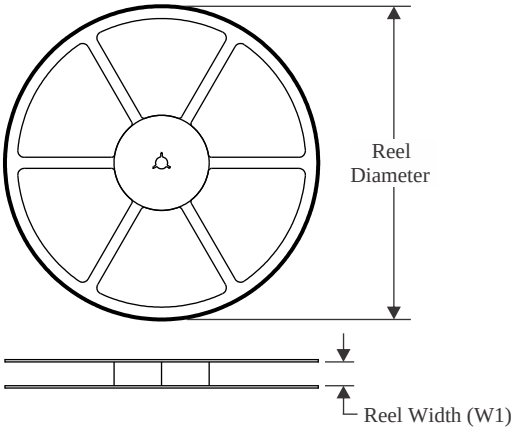
- Automotive : TL3472-Q1

NOTE: Qualified Version Definitions:

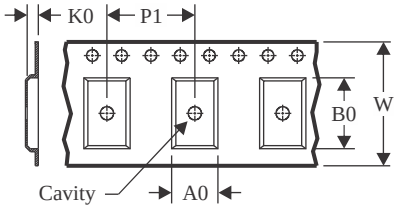
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

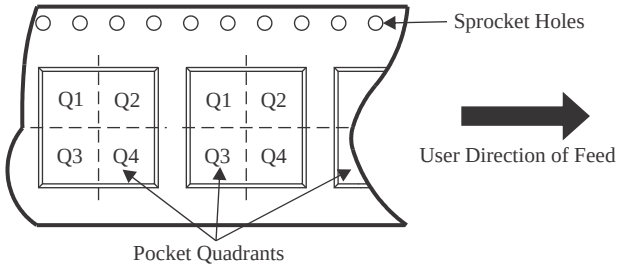


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

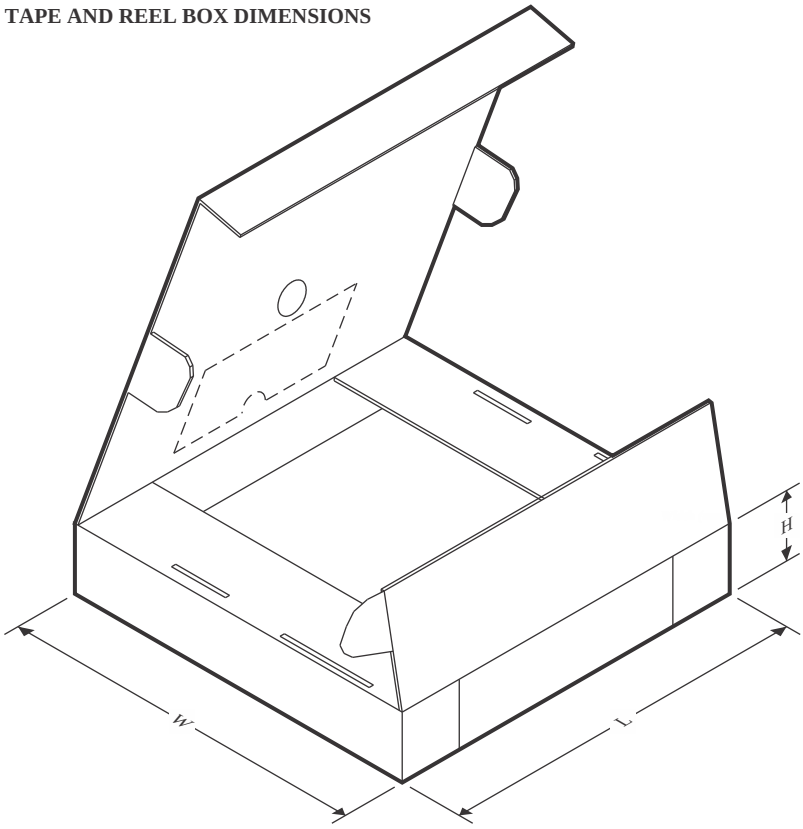
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3472CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3472CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3472IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3472IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

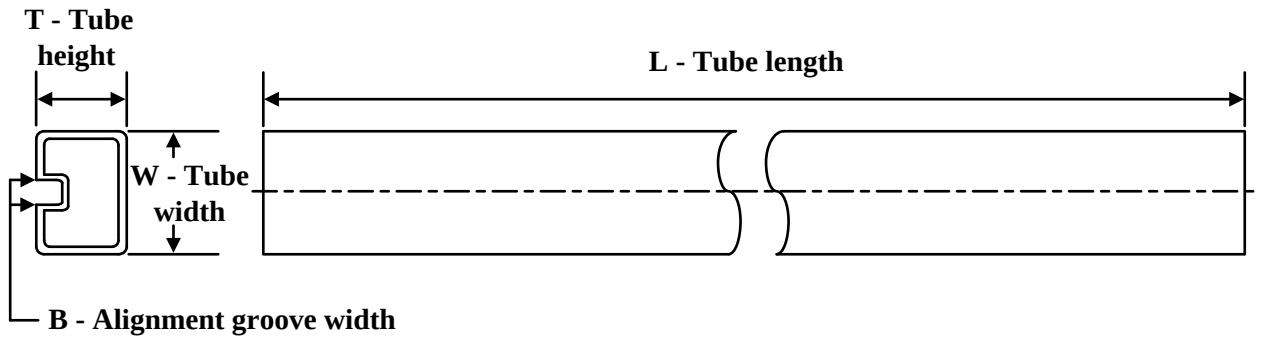
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

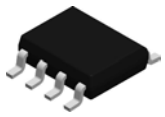
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3472CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL3472CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL3472IDR	SOIC	D	8	2500	356.0	356.0	35.0
TL3472IDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL3472CP	P	PDIP	8	50	506	13.97	11230	4.32
TL3472IP	P	PDIP	8	50	506	13.97	11230	4.32

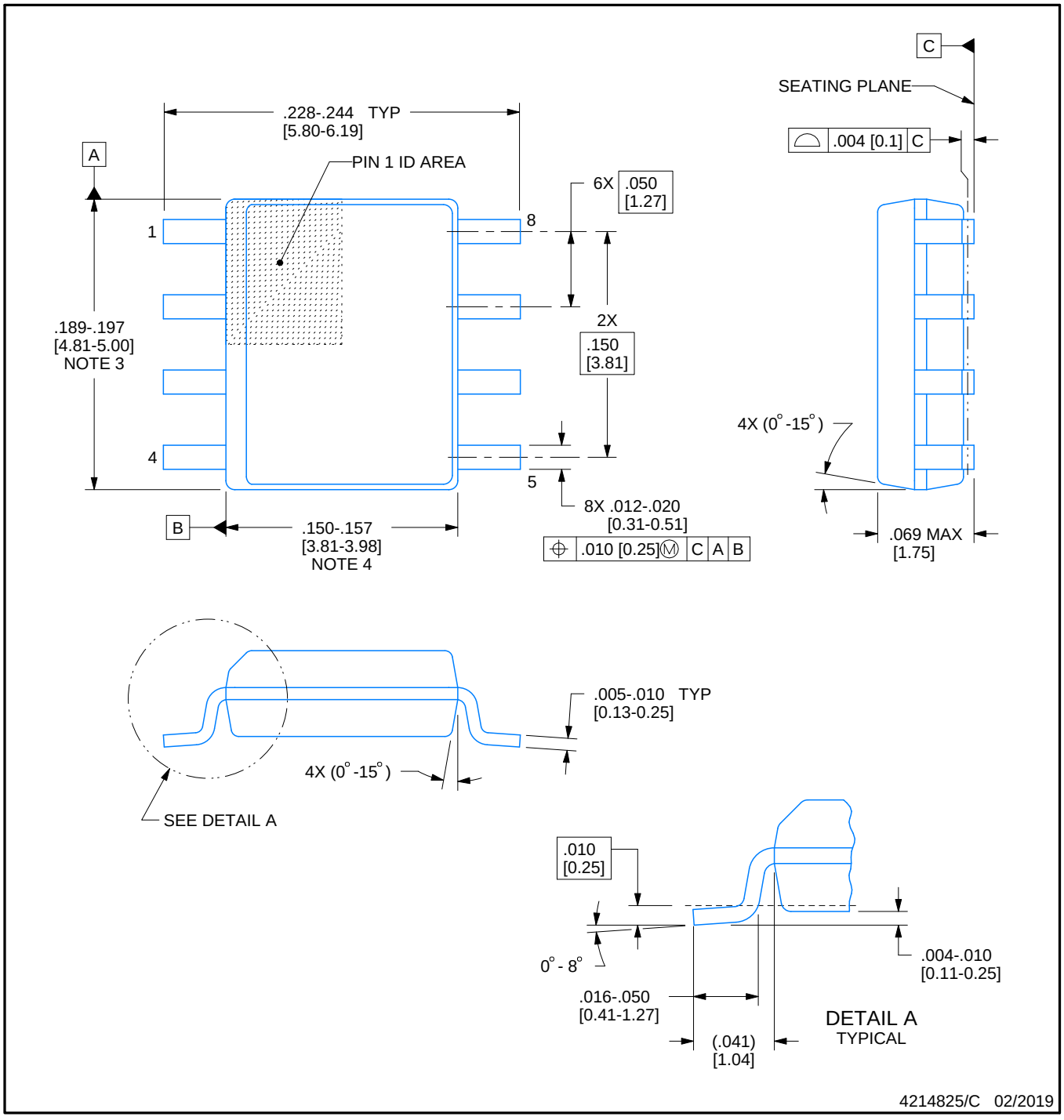


PACKAGE OUTLINE

D0008A

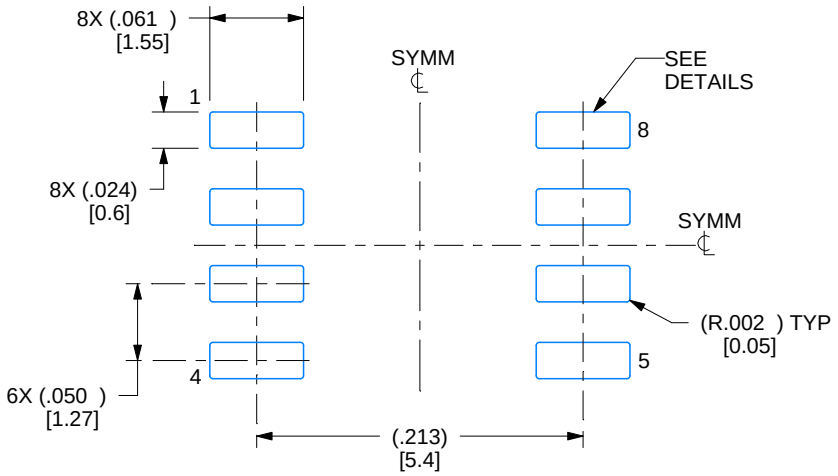
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

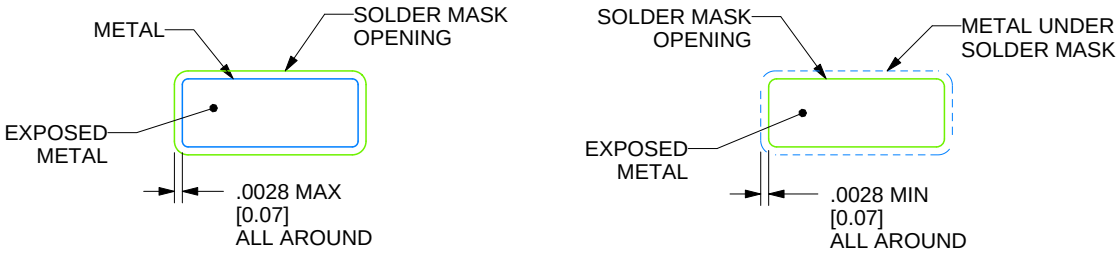


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

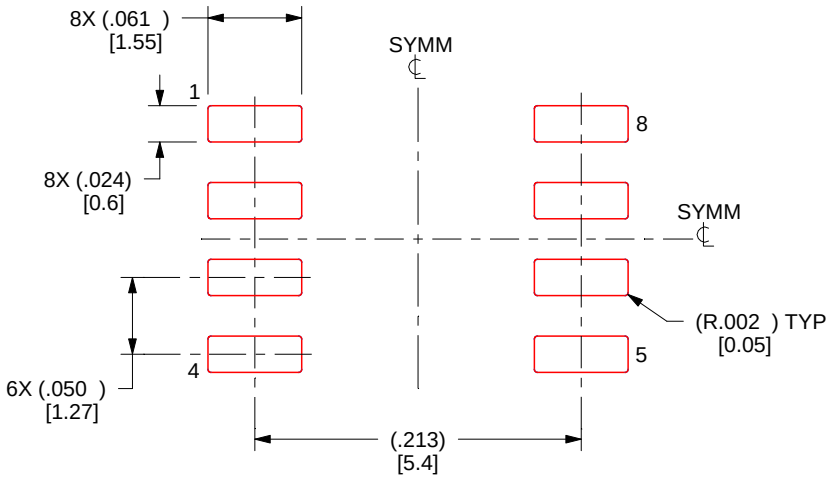
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



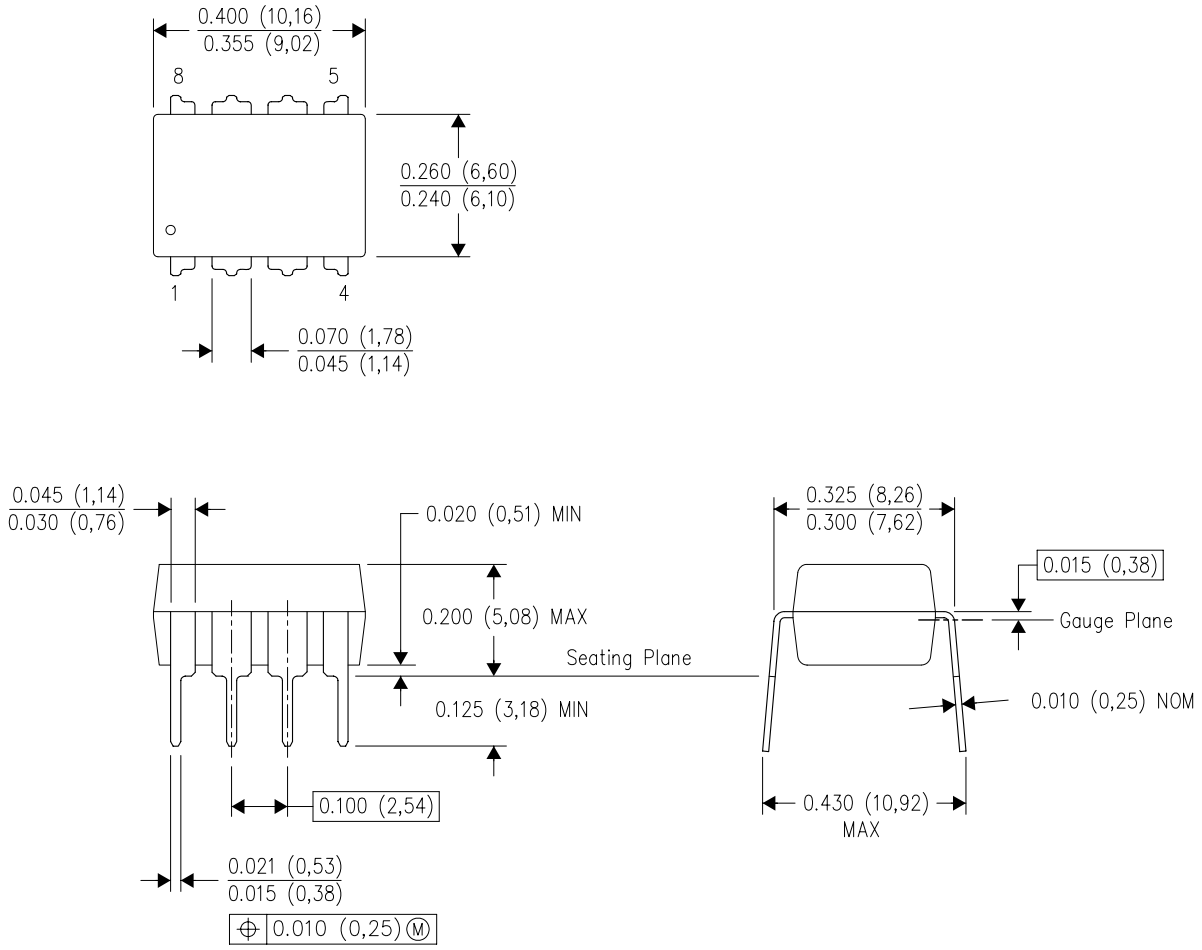
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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