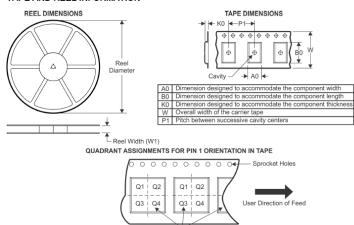
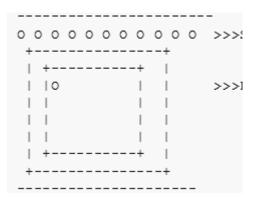
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)		B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63810YFFR	DSBGA	YFF	15	3000	180.0	8.4	1.5	2.42	0.75	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63810YFFR	DSBGA	YFF	15	3000	182.0	182.0	20.0

TAPE AND REEL INFORMATION



Pocket Quadrants



Marking picture	vendor Name	Part No.	Marking Rule
TI YMLLLLS TPS63810	ТΙ	TPS63810YFFR	the marking "TPS63810" represents the device name, by identifying units marking TPS63810 correctly to determine device

TI Part	Component	Homogeneous Material Name.	Substance Name	*CAS No.	Substance Mass. (mg)	Content Rate(%)
		Other Inorganic Materials	Silica	7631-86-9	0.115439	55.066926
	Back Side Coating	Other Plastics and Rubber	Carbon Black	1333-86-4	0.003547	1.691997
		Other Plastics and Rubber	Imidazole Derivative	288-32-4	0.000788	0.375893
		Thermoplastics	Epoxy	85954-11-6	0.08986	42.86518
TPS63810YFFR	Solder Bump	Copper and Its Alloys	Copper	7440-50-8	0.005481	0.599965
		Other Nonferrous Metals and Alloys	Tin	7440-31-5	0.872444	95.499992
		Precious Metals	Silver	7440-22-4	0.035629	3.900043
	Semiconductor Device	Ceramics / Glass	Doped Silicon	7440-21-3	2.352423	100

Basic Information	Result
Supplier Name	TI
Device Part Number	TPS63810YFFR
Wafer fab information, process type and node	RFAB / DMOS6
Wafer process was or not qualified and released to production.	Mature
Is there any part from the same wafer process family have been used in customer? If yes, please list the part number.	YES
Wafer Process Capability(SPC)	Meet SPC spec
Is there any wafer process CPK<1.33? If yes, please list it and provide the improvement plan.	NO
Do you have chip ID or die ID for this device?	NO
Assembly Factory, Package type	CDAT WCSP
Package Size (Length*Width*Height)	1.5x2.0x0.625mm
Ball/Lead pitch	0.4MM

		7	
Is there any part from the same package family yes, please list the part number.	YES		
Assembly Process Capability(SPC)	Meet SPC spec		
Is there any assembly process CPK<1.33? If yes, improvement plan.	NO		
Range of Operation Temperature (Ta, Tj or To)	-40~85C	
Storage Temperature range		-65 ~ 150C	
Storage limit		1years at customer side	
Max.Junctioin Temperature		-40~125C	
IFR, Intrinsic Failure Rate, FIT	0.4FIT@60%CL		
MSL, Moisture Sensitive Level	MSL 1		
	Оја	80.5°C/W	
Thata is is and in	Ѳјс	0.6°C/W	
Theta ja, jc and jb	Θjb	20.5°C/W	
	НВМ	2000	
ESD (HBM、CDM, for all pin)	CDM	500	
Latch-Up (At max. Ambient Temperature)		Meet qual test requirement	
If the chip is new process or new design, And so or beyond JEDEC standard) had been down. Ple result details.		NO	
Wafer reliability Qualification Report, including SM .etc	: TDDB, HCI, NBTI, PBTI, EM,	YES	
Package Qualification Report, including: PC, TH DT, Bend, PDT, PVT .etc	See Tl.com qual report		
Device Qualification Report, including: ELFR, HT ESD-CDM, LU .etc	See Tl.com qual report		
The device should be done reliability monitorin Reliability Monitoring Report, including: PC, TH HTOL .etc		ORT test is based on package	
Characterization report, follow JESD86		Can't provide	
		1	

Component information		Investigation Result		
Ball Compositions and ratio		SAC405		
Ball Diameter(µm) before b	all attachment	0.25MM		
Back side laminate		Yes		
Is there RDL layer in WLCSP	?	Yes		
Package standard		JEDEC		
Weight of component (g)		3.5mg		
Weight/ available P&P areas	<0.06g/mm2	Yes		
Is there polarity point on the		Yes		
Is the polarity point sole?		Yes		
Is there any specific location component specification?	n number of terminals in	Yes		
Component orientation can	be identified by AOI?	Yes		
Are matters RoHS complian	t and lead free?	Yes		
Are matters are Halogen-fre	ee	Yes		
	Relative humidity (%)	≥20%&≤70%		
	Temperature (°¢	≥-10C&≤35C		
Storage Condition	Maximum storage time (month)	12 at customer side		
Packaging type		Tape and real		
Position of component pin 1	L in packing	Q1		
Packaging height(K0)		0.75mm		
Packaging width(W)		8mm		
component pitch:P1		4mm		
ESD packaging		Yes		
Rollover rate ≤0.05% in pacl	king	Yes		
tray packing Baking condition	ons: 125°@24h	Yes		

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reel tape packing Baking conditions: 40°@192h	Yes
Can reel tape packing meet EIA-481 standard?	EIA
MSL	1
MSL>=2,moisture sensitive protection must include: moisture sensitive indicator card, desiccant, moisture sensitive grade logo	Yes
Baking requirement meet J-STD-033b if moisture	Yes
Maximum soldering times ≥3	Yes
Can heat resistance of SMT components meet JSTD020D. (should focus on the classification of temperature and reflow profiles, that is table 4-1, 4-2 and 5-2, please refer to sheet6 J-STD-020D in this file)	Yes
Maximum pick-and-place pressure (N)	Yes
Whether the welding process and design requirements of component have all written to the component specifications	Yes
Whether Pad & stencil design as Mandatory requirements in component spec?	recommended
Whether the device has special requirements for the reflow temperature ramp-up rata and ramp-down rata? Customer follow J-STD-002 standard	No
Are there other mandatory requirements in component spec?	No
Solder ability shall be tested per J-STD-002D and the report must be offered,	Yes

Qualification summary for:	TPS63810YFFR
Report date:	06/17/2020

Stress	Reference	Min lot qty	SS / lot	Condition	Duration	Result
HTOL	JESD22-A108	3	77	Life test, 125C	1000 hours	Pass
HTSL	JESD22-A103	3	25	High temp storage ba ke 150C	1000 hours	Pass
AC/UHAST	JESD22-A102/JESD2 2-A118	3	25	Autoclave 121C or un biased HAST 130C / 8 5% RH	96 hours	Pass
THB/HAST	JESD22-A101/JESD2 2-A110	3	25	THB 85C/85%RH or H AST 130C/110C/85% RH	1000 hours or 96 hours	Pass
TC	JESD22-A104	3	25	Temperature cycle -6 5/150C	500 cycles	Pass
SD	J-STD-002	1	15	Per specification	>95% lead coverage	Pass
НВМ	JS-001	1	3	ESD - HBM	Classification	See data sheet
CDM	JESD22-C101	1	3	ESD - CDM	Classification	See data sheet
LU	JESD78	1	3	Latch-up	Per JESD78	Pass
MSL	J-STD-020	_	_	Per J-STD-020	Classification	See data sheet