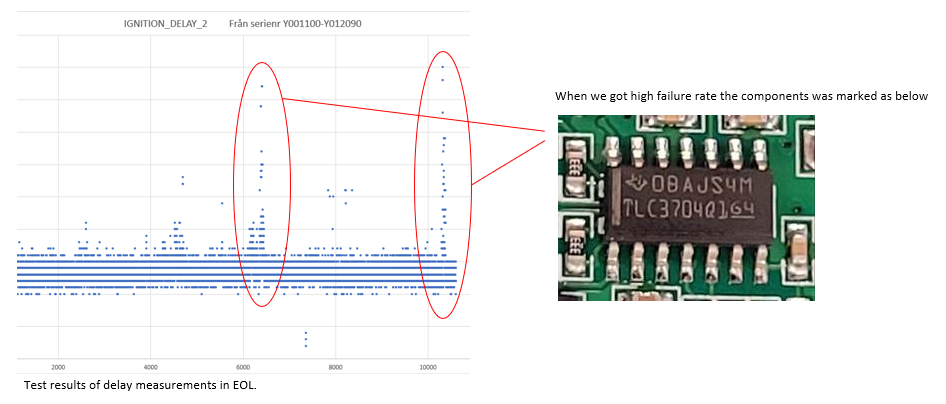
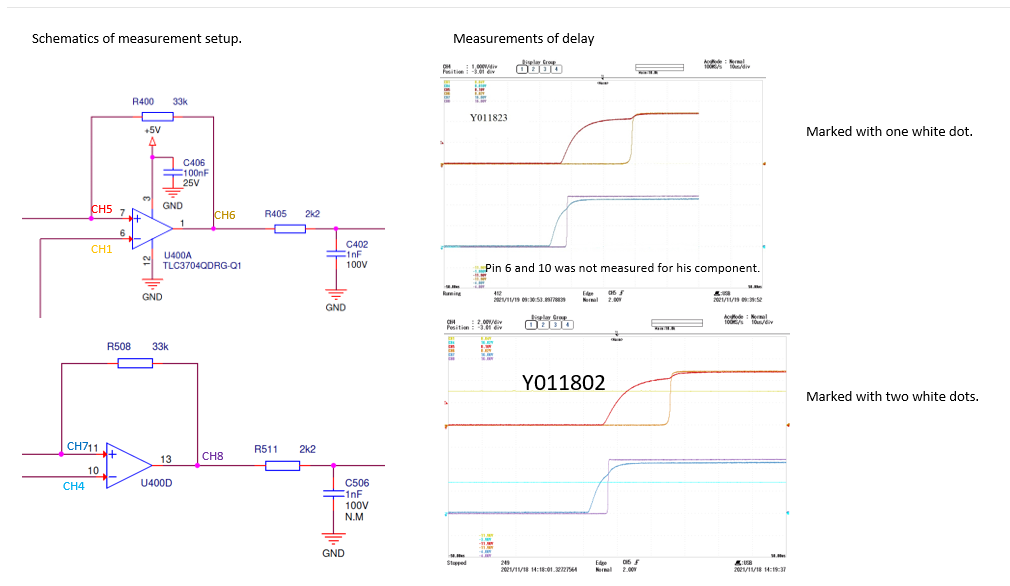
BACKGROUND

In our EOL testing we measure the delay from input to output. When we use components marked as the picture below, we get a high failure rate. The delay time is too high.





We expect some jitter, a few µs, on the delay as described in ”TLC3702 TLC3704 Family Application Note”.

Some of the components has a much longer delay, 10’s of µs.

Are the components from the mentioned batch safe to use if they pass our testing?

Or do we need to recall modules from field?

