Transcimpedance Amplifier

Circuit Design Consideration

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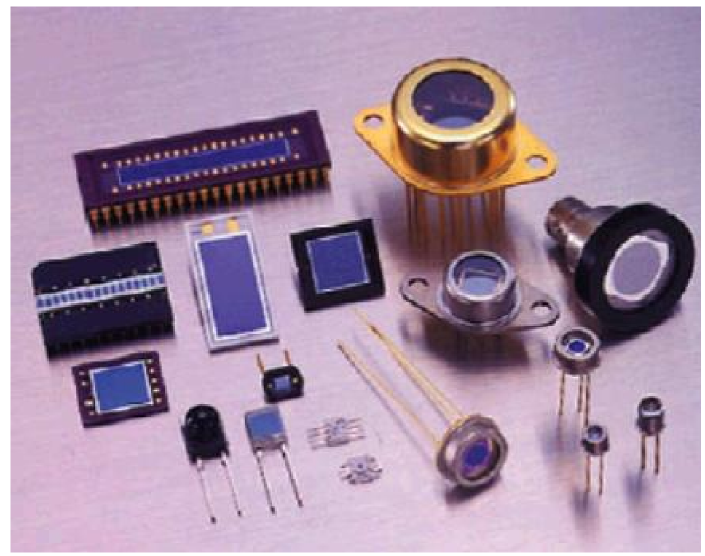
Photodiode Basic

Photodiode Basic

- **Introduction**

  Photodiodes are semiconductor light sensors that generate a current or voltage when the P-N junction in the semiconductor is illuminated by light. The term photodiode can be broadly defined to include even solar batteries, but it usually refers to sensors used to detect the intensity of light.



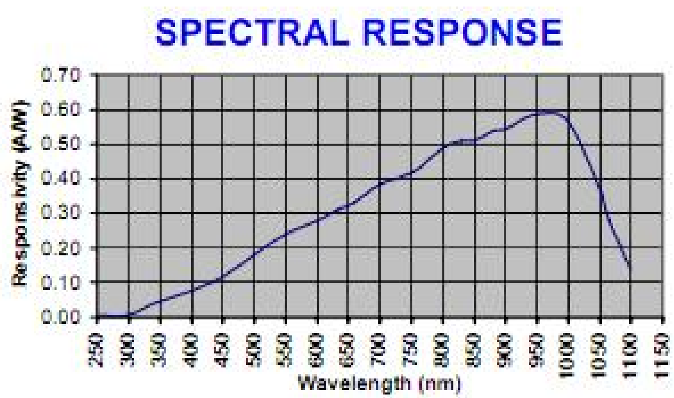
- **Photodiode type**

  PN photodiode

  PIN photodiode

  Schotty type photodiode

  APD (Avalanche photodiode)



Photodiode Basic

Principle of Operation:

. - The P-layer material at the active surface and the N material at the substrate form a PN junction which operates as a photoelectric converter.

- When light strikes a photodiode, the electron within the crystal structure becomes stimulated. If the light energy is greater than the band gap energy Eg, the electrons are pulled up into the conduction band, leaving holes in their place in the valence band.

- These electron-hole pairs occur throughout the P-layer, depletion layer and N-layer materials. In the depletion layer the electric field accelerates these electrons toward the N-layer and the holes toward the P-layer.

- This results in a positive charge in the P-layer and a negative charge in the N-layer. If an external circuit is connected between the P- and N-layers, electrons will flow away from the N-layer, and holes will flow away from the P-layer toward the opposite respective electrodes.

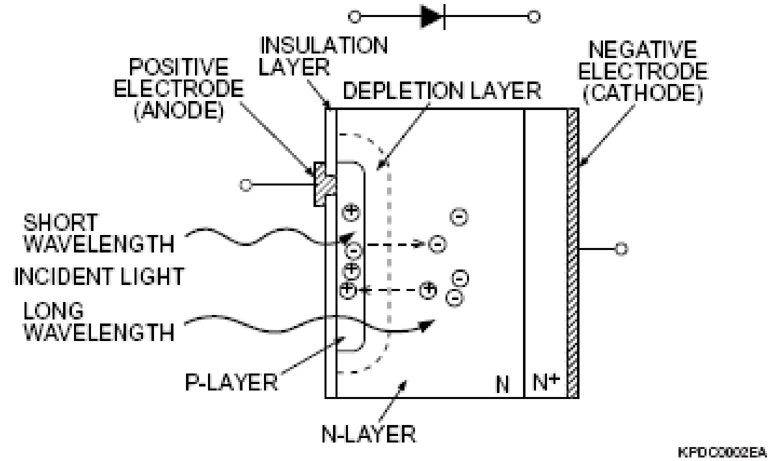


Figure1.1 Photodiode cross section

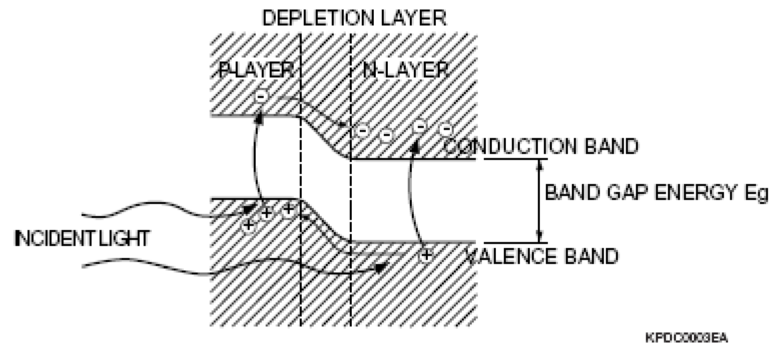


Figure1.2 PN junction State

Photodiode Basic

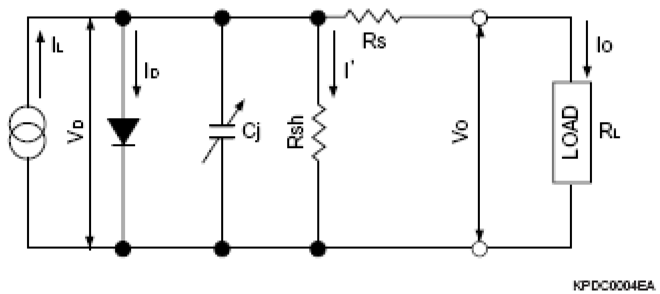


Figure1.3 Photodiode Equivalent Circuit

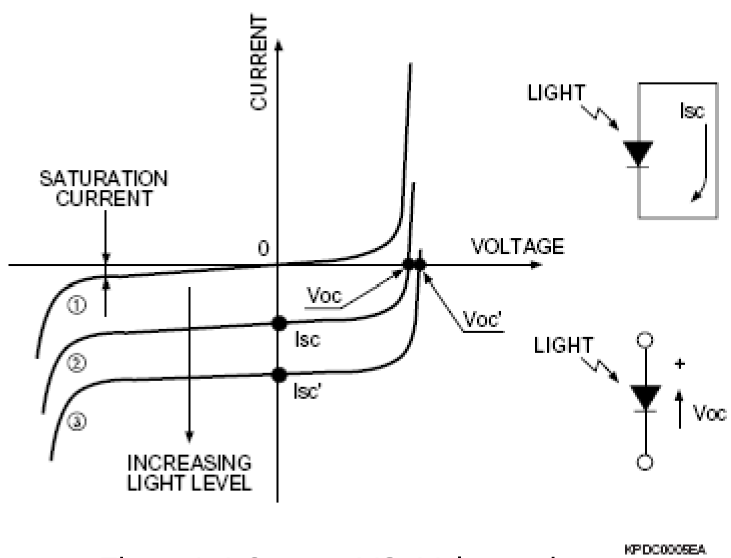


Figure1.4 Current VS. Voltage characters

I_L : Current generated by the incident light

$$I_L := r_\phi \phi_e$$

r_ϕ is the diode's flux responsivity

ϕ_e is the radiant flux energy in watts

I_D : Diode Current

C_j : Junction capacitance

$$C_j := \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{\phi_B}}}$$

C_{j0} is the photodiode capacitance at zero bias

ϕ_e is the built-in voltage of the diode junction

V_R is the reverse vias voltage

R_{sh} : Shunt resistance

R_s : Series resistance

I' : Shunt resitance current

V_D : Output current

I_o : Output current

V_o : Output voltage

Photodiode Basic

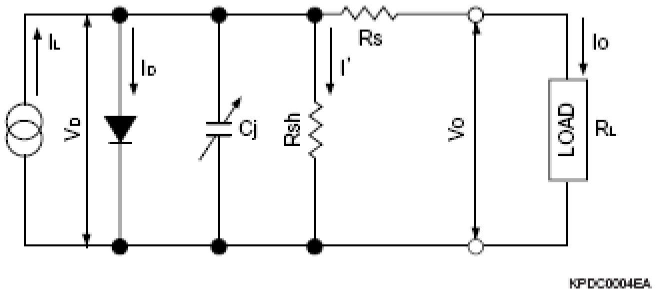


Figure1.4 Photodiode Equivalent Circuit

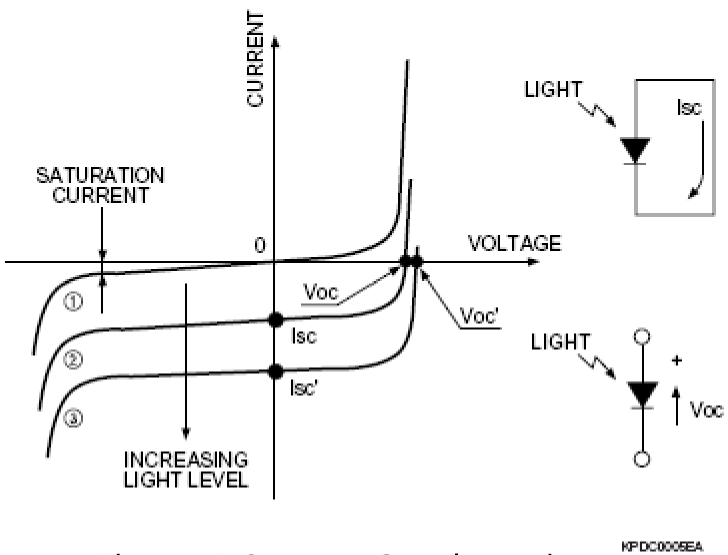


Figure1.5 Current VS. Voltage characters

Use left equivalent circuit, the output current is given as :

$$I_o := I_L - I_D - I' = I_L - I_S\left(e^{\frac{eV_D}{kT}} - 1\right) - I'$$

I_S : Photodiode reverse saturation current

e: electron charge

k: Boltzmann's constant

T: Absolute temperature of the photodiode

The open circuit voltage V_{oc} is the output voltage when I_o equals 0. Thus Voc becomes:

$$V_{oc} := \frac{kT}{c}\ln\left(\frac{I_L - I'}{I_S} + 1\right)$$

If I' is negligible, since Is increases exponentially with respect to ambient temperature, V_{oc} is inversely proportional to the ambient temperature and proportional to the log of I_L. However, this relationship does not hold for very low light levels.

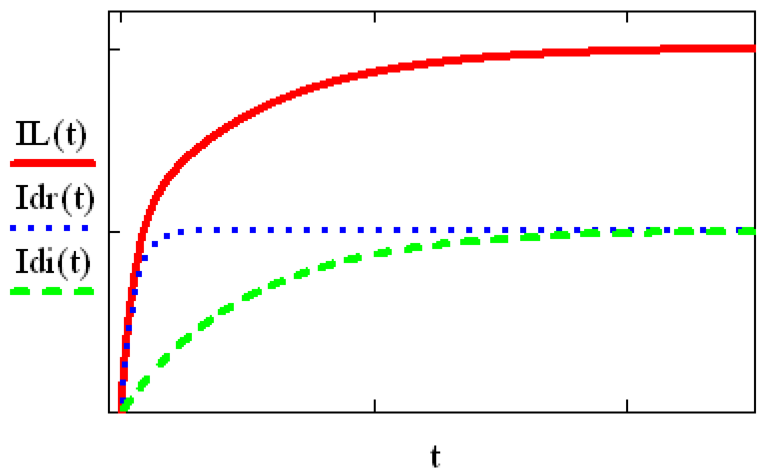
Current response

Photodiode Basic

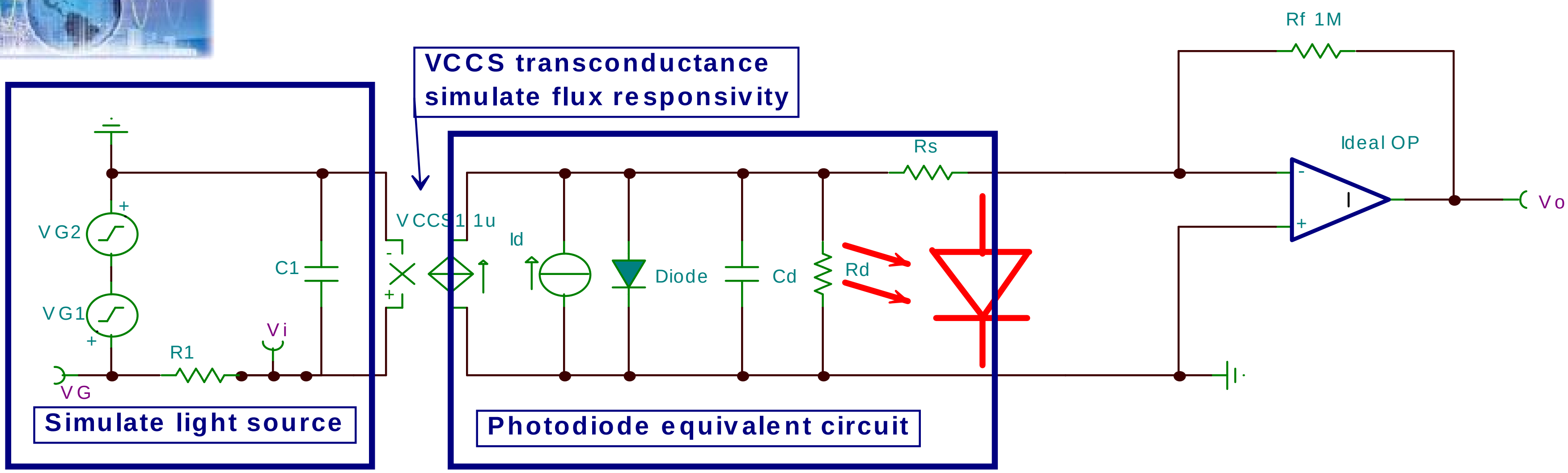
- The ac response of I_L displays a dual time constant due to the two carries travel mechanisms that account for photodiode current. Carries generated both within and outside the depletion region travel under the accelerating influence of the region's electric field and proceed rapidly to the diode's terminals. This produces a fast or drift component of I_L, I_{dr} as controlled by the drift time of the depletion region.
- The carries generated outside the region initially travel slower. So the interim diffusion time produces a slow component of I_L, I_{di}.
- The combination of the two components produces a time domain current of I_L.

$$I_L(t) = I_L(\infty)\left(1 - \alpha_{dr}\, e^{\frac{-t}{\tau_{dr}}} - \alpha_{di}\, e^{\frac{-t}{\tau_{di}}}\right)$$

α_{dr} and α_{di} represent the fractions of I_L supplied by the drift and diffusion components.



Photodiode and Control Source TINA model



Light exciting source:

1) Use VG1 and VG2 voltage sources to simulate light power wave.

2) Use R1 and C1 to control voltage signal's rise edge and fall edge, to simulate photo diode's current response. The time constant τ equals to R1*C1, change R1 and C1 can set different rise/fall edge times. Usually we need select a very small R1 to prevent voltage attenuation.

3) The signal is converted to current by Voltage Control Current Source (VCCS1), we control the transconductance to simulate photodiode 's sensitivity.

photodiode equivalent circuit:

1), Current Source Id simulate Dark current

2), Diode is a ideal diode

3), Cd and Rd simulate photodiode's junction capacitor and dark Resistance.

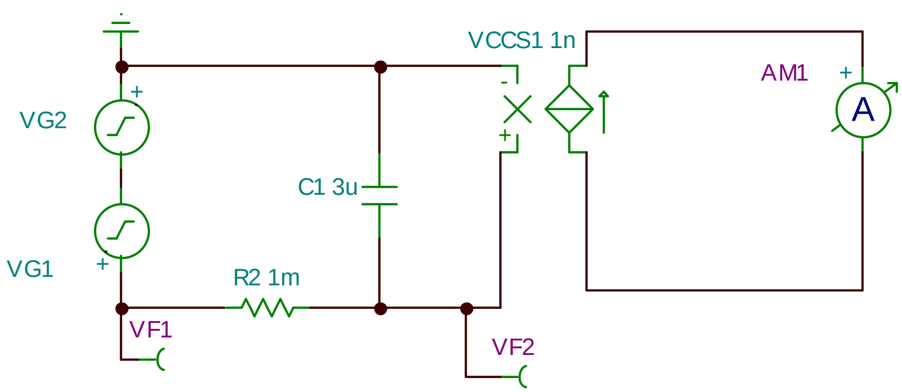
4), Rs is series resistor, which is far smaller than Rd.

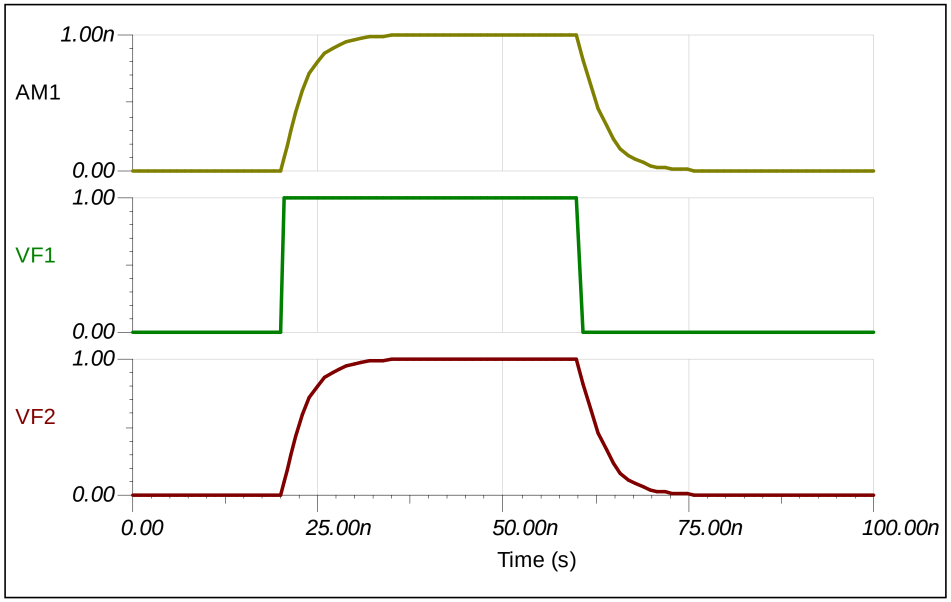
Photodiode TINA model- Exciting Source

If we need a 1nA peak, 40ns width, 5ns rise/fall time photodiode output current.

1), Set VG1 and VG2 as 1V, unit step with 20ns and 60ns delay.
2), Set VCCS1 trans conductance equals to 1u
3), Set R1=1mΩ, C1=3uF.
4), Time constant equals to R1*C1=3ns

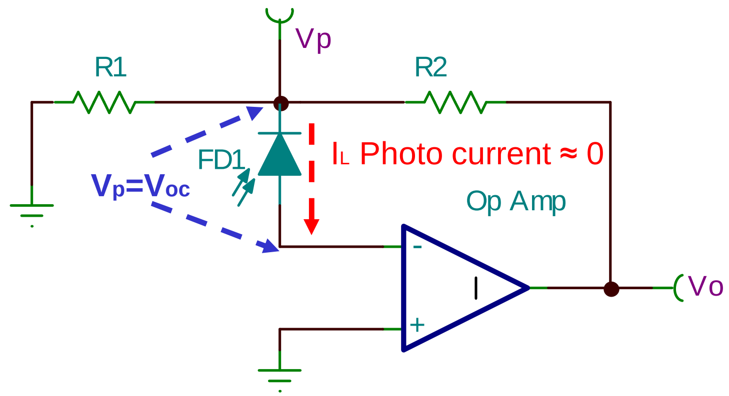
Rise/Fall time ≈ R1*C1*1.6=4.8ns;





The basic amplifier

Voltage Monitor Mode



Vo=-(1+R2/R1)Vp

In voltage monitor mode the diode is placed in series with an op amp input to avoid impedance loading but results in a nonlinear response and large dc offset. The nonlinearity results primarily from the logarithmic current-voltage characteristic of the diode junction. Photodiode operated in the voltage output mode produces a voltage described by:

$$V_{oc} := \frac{kT}{c} \ln\left(\frac{I_L - I'}{I_S} + 1\right)$$

In the photovoltaic mode shown, the photodiode's own output voltage modulates the junction voltage to further increase nonlinearity. This circuit also produces a large dc offset due the flow of the op amp's input bias current I_{b-} through the high resistance of the photodiode.

Current Mode – Resistor Load

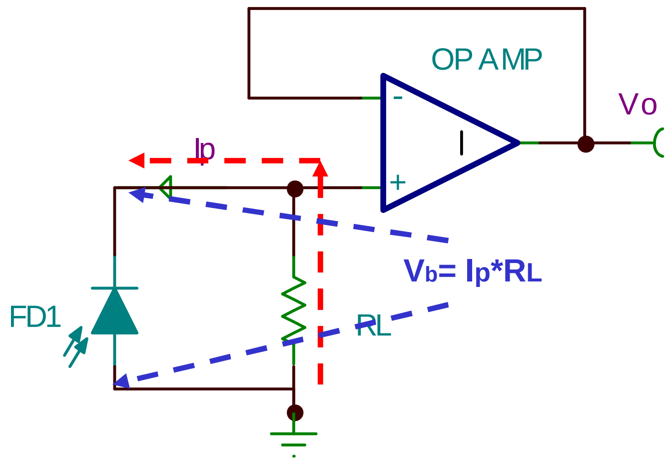


Figure (a)

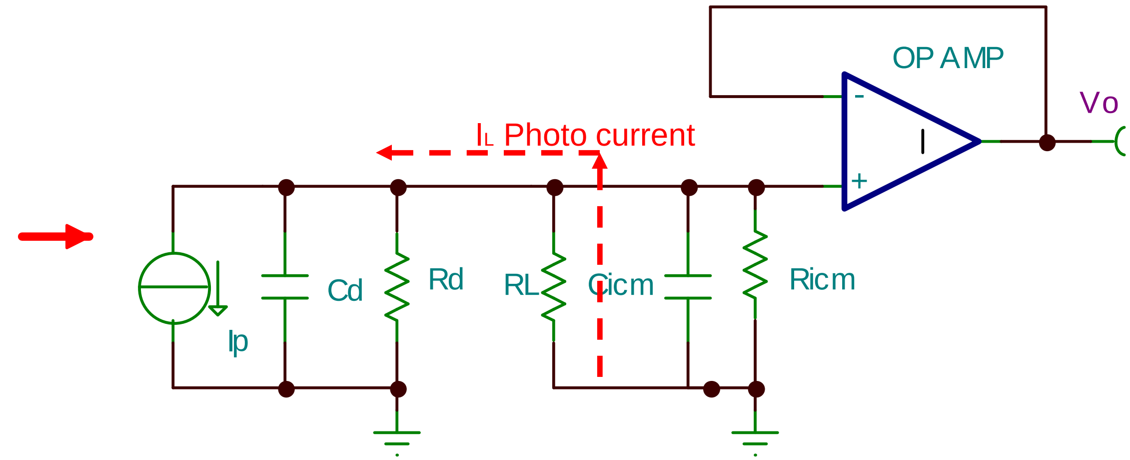
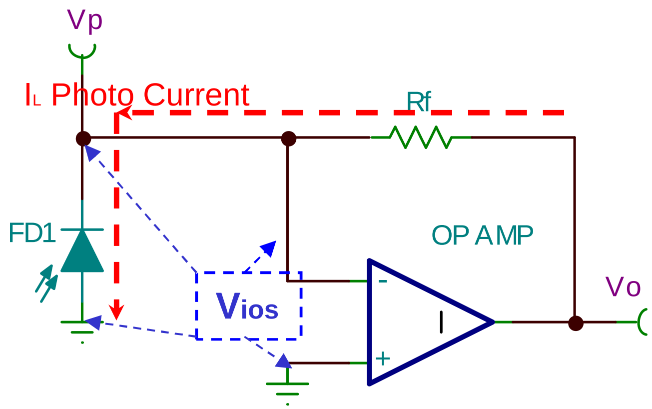


Figure (b)

- We can connect the photodiode as figure (a), so the photocurrent flow to R_L converting current to voltage. The op amp follower isolates RL from any impedance loading error at the circuit output.
- However, this simple circuit also develops the full signal voltage V_o across the photodiode and its capacitance. The resulting signal current in this capacitance shunts the diode current at high frequency, producing a bandwidth limit.

Current Mode



Vo=Ip·Rf

Figure (c)

Current Mode connection as figure (c). This circuit removed photodiode voltage and op-amp bias current I_{b-} from it's capacitance and dark resistor .This alternative virtually eliminates V_p and the resulting nonlinearity, but only transfers I_{b-} to a smaller resistance.

Current monitoring requires that the monitor circuit present zero load impedance to the diode. Then the monitor absorbs the diode's current without producing a voltage across diode.

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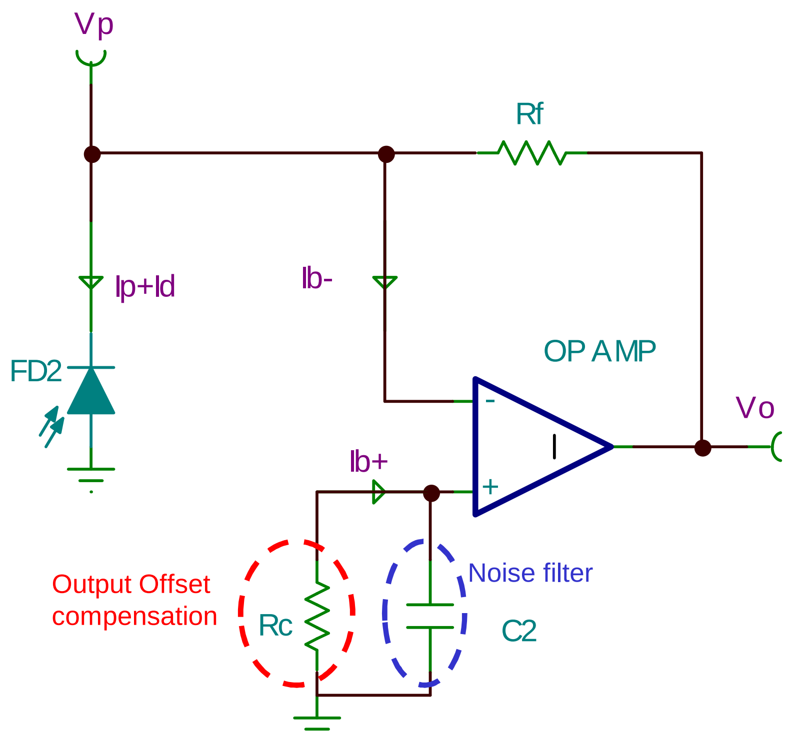
Current Mode – Compensation resistor



In real application, op-amp is not ideal and photodiode also have dark current, op amp need bias current at both inverting and non-inverting inputs. The bias current I_{b-} and dark current I_d will produce a Op amp output offset V_{oso}:

$$Voso = Rf*(Id+Ib-)$$

Id and Ib- multiplied by large resistor Rf will produce a large offset output. In order to reduce the offset, we can use a compensation resistor Rc, so the Voso will be:

$$Voso = Rf*(Id+Ib-)-Rc*Ib+$$

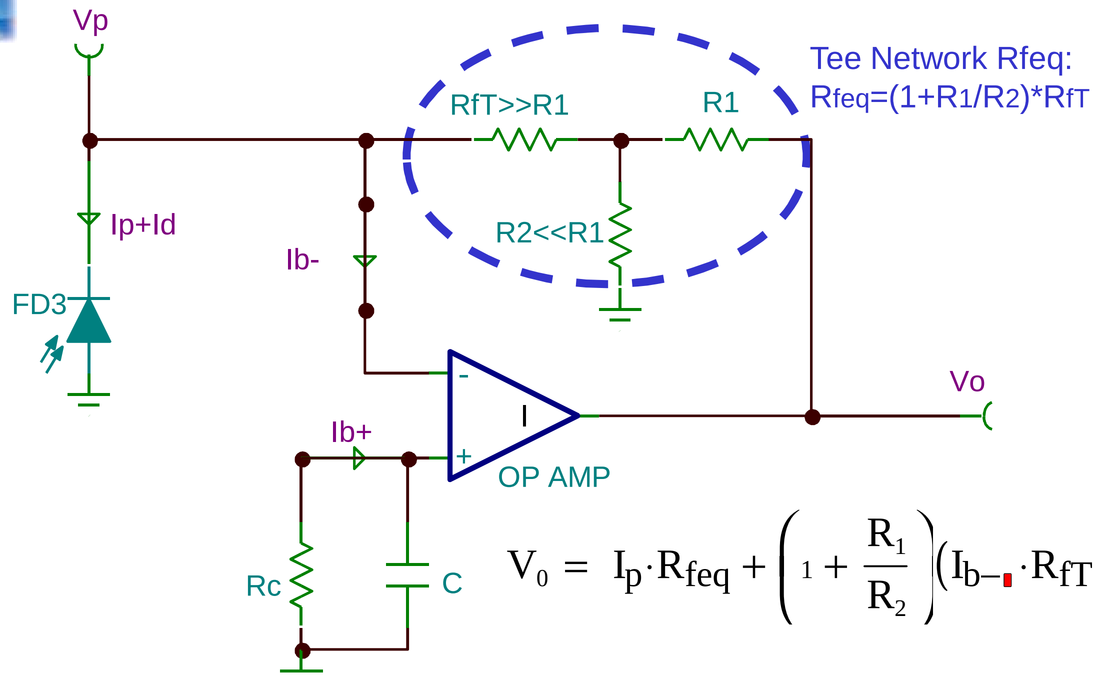
Usually we set Rc=Rf to compensate the offset produced by Ib-. This reduced output offset a factor of 5 to 10 improvement over the initial offset and drift produced by the amplifier's input current.

Adding Rc also develops a voltage across the photodiode. The compensating voltage drop across Rc, Rc*Ib+, also drops across the photodiode and produce the diode's leakage current IL(Id).

High sensitivity photodiodes require much larger junction areas than the typical op amp input FET and potentially larger leakage currents.

This requires evaluation of specific application conditions before adding Rc.

Current Mode – Tee Network



$$V_0 = I_p \cdot R_{feq} + \left(1 + \frac{R_1}{R_2}\right)\left(I_{b-} \cdot R_{fT} - I_{b+} \cdot R_C + I_d \cdot R_{fT} + V_{os}\right)$$

-Replacing Rf with a resistor tee **greatly reduce offset error** through reduced resistance levels.

-Reduced resistances **decrease** the Rc*Ib+ **voltage** impressed **upon the photodiode**, and reduced the resistance matching error of Rc to Rf.

-The tee also amplifiers the op amp's input offset voltage Vos and input noise voltage by factor 1+R1/R2.

Bandwidth and Stability

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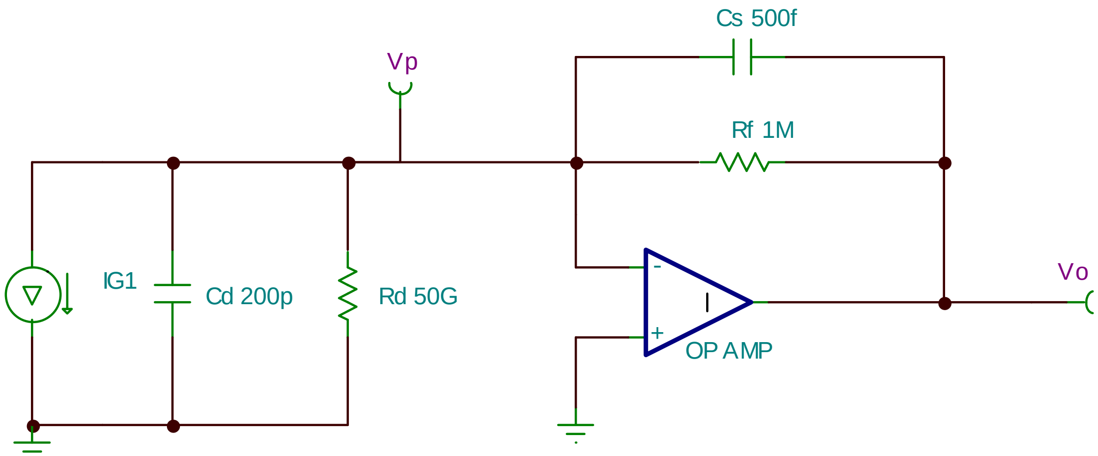
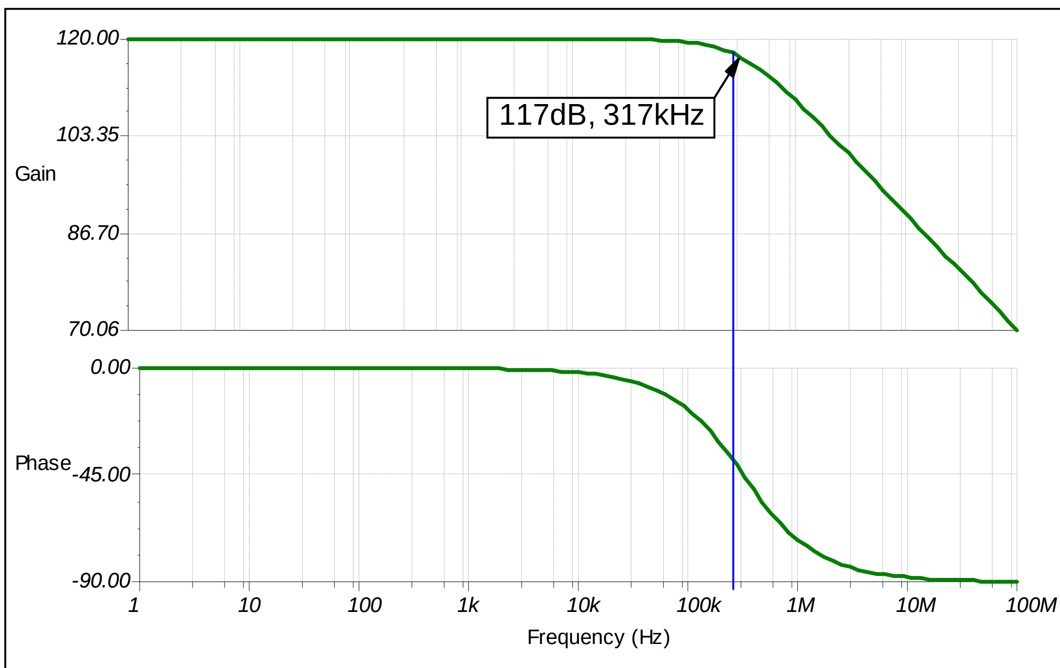
Parasitic Capacitance limit the bandwidth





Higher feedback resistor value potentially make parasitic capacitance bypass dominate the photodiode amplifier's response and set the circuit bandwidth.

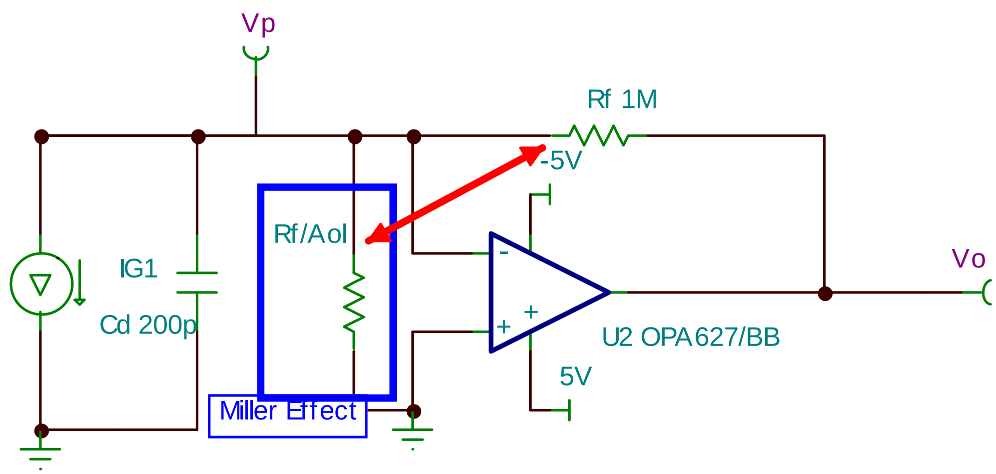
Good construction parasitic limit Cs around 0.5pF.

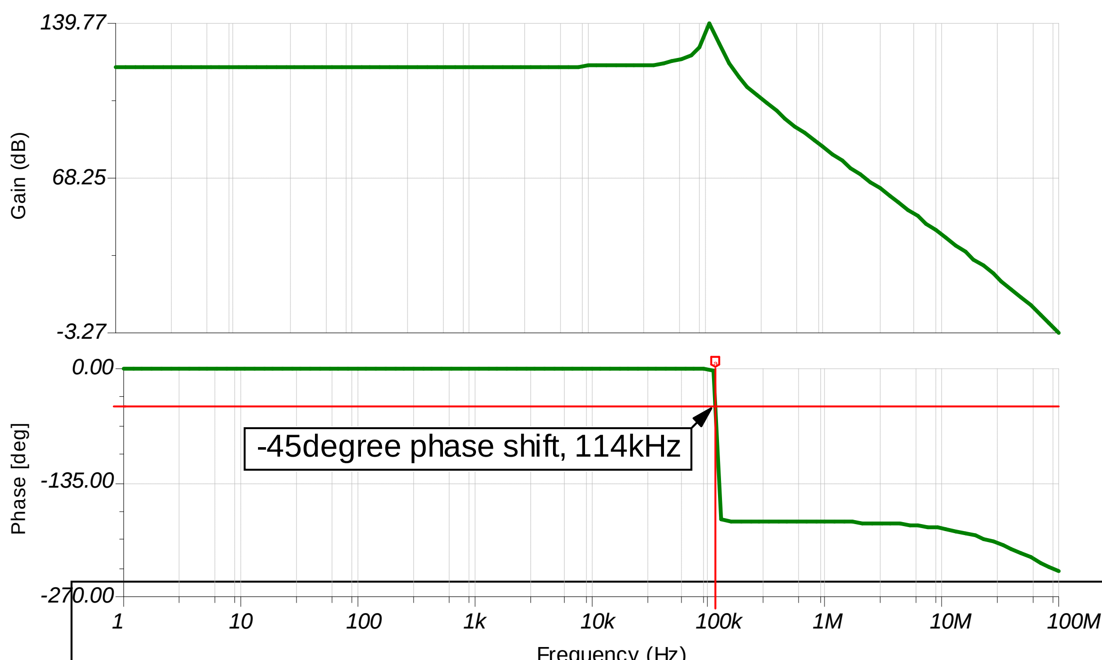
The parasitic capacitance and feedback resistance produce a gain pole at:

$$f_p = \frac{1}{2p\,R_f C_s} = 318kHz$$

It is the same as simulation

Amplifier GBW limit bandwidth





Because of miller effect, op amp's input resistor $R_i' = R_f / A_{ol}$, which will produce another pole to limit circuit's bandwidth. The pole frequency f_p is:

$$f_{pf} = \frac{A_{ol}}{2p\, R_f C_i} \qquad , A_{ol} = \frac{f_c}{f}$$

$$f_{pf} = \frac{f_c}{2p\, R_f C_i f_{pf}}$$

$$f_{pf} = \sqrt{\frac{f_c}{2p\, R_f C_i}}$$

fc is unity gain bandwidth

Ci=Cd+Cid+Cicm

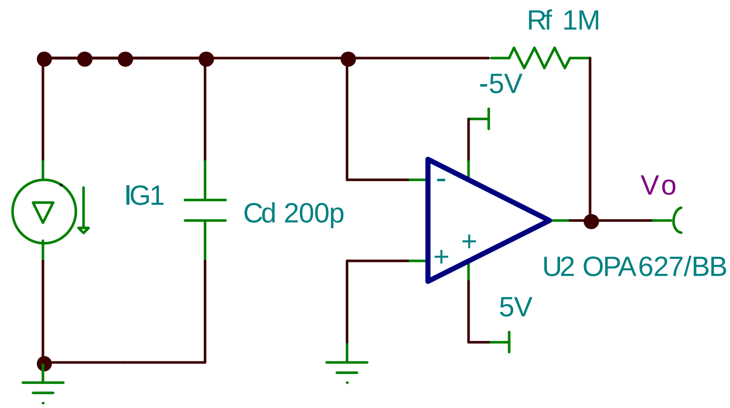
We select OPA627 to simulate:

OPA627, f_c=16MHz, C_{id}=8pf, C_{icm}=7pf

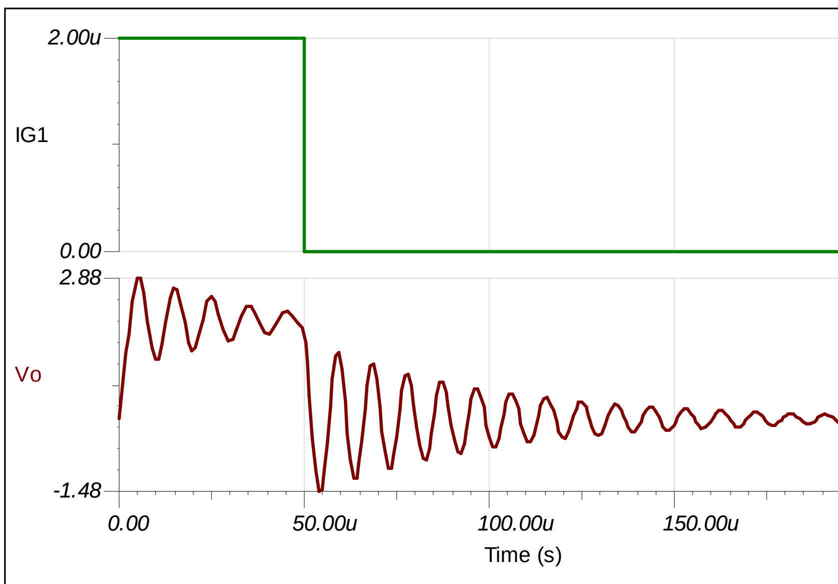
Calculation : f_{pf}=109KHz

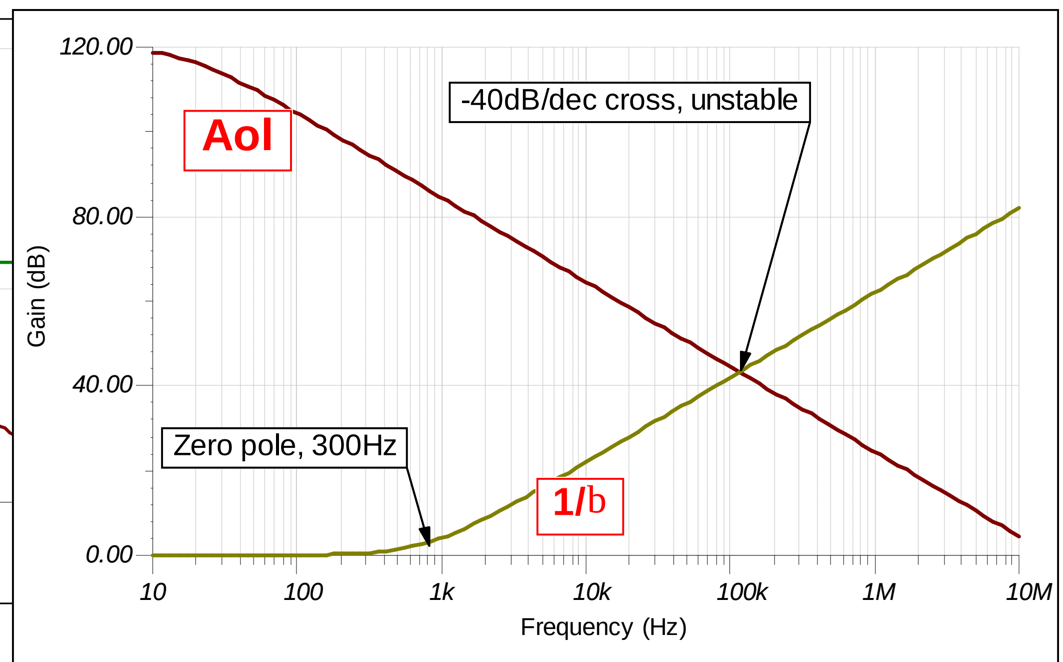
Simulation : f_{pf}=114KHz

Phase compensation limit bandwidth

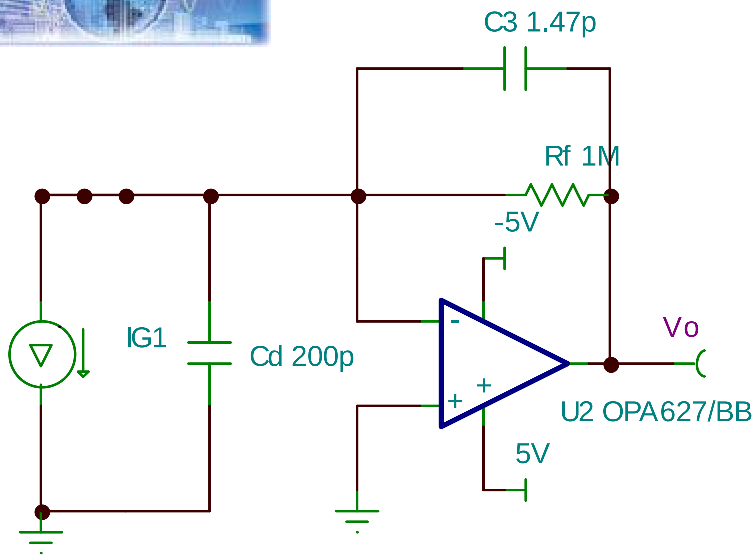


Rf and Cd will produce a zero at 1/β curve , and it will cross with Aol curve at 20dB/dec, it make Acl closure in -40dB/dec, the circuit is unstable. As the simulation, the output is ringing.
In order to stabilize the circuit, we need add a capacitor parallel with Rf to produce a zero at Acl for phase compensation





Phase compensation limit bandwidth



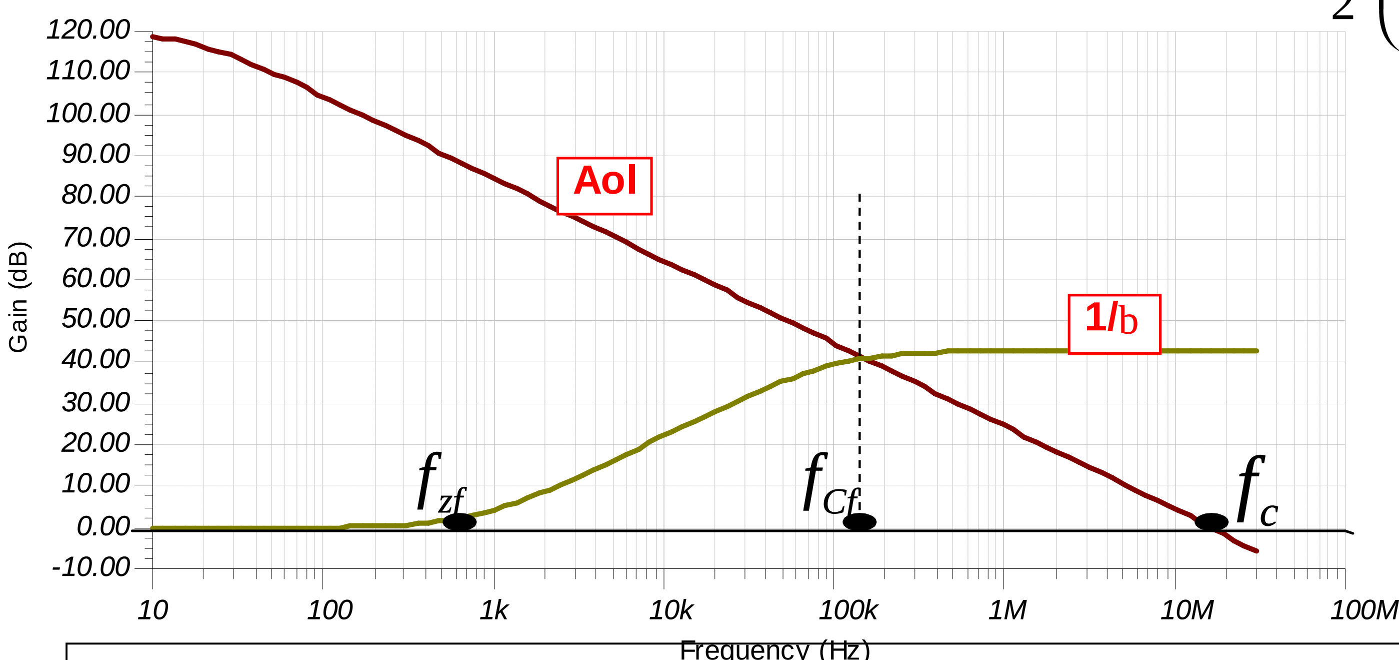
$$BW = 1.4 f_i \qquad f_i = \sqrt{f_{zf} \; f_c}$$

$$f_{zf} = 1/2\pi R_f (C_i + C_f)$$

$$C_c = 1/2\pi R_f f_c$$

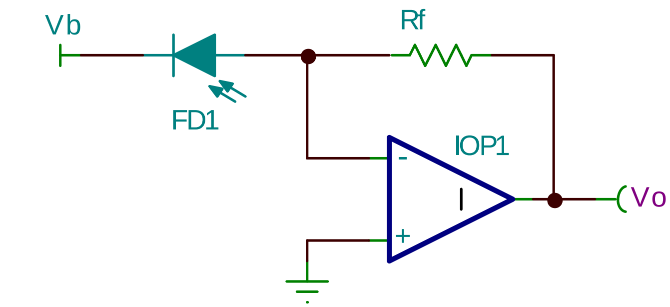
$$C_f = \sqrt{\frac{C_i}{2\pi R_f f_c}}$$

$$C_f = \frac{C_c}{2}\left(1 + \sqrt{1 + \frac{4C_i}{C_c}}\right)$$

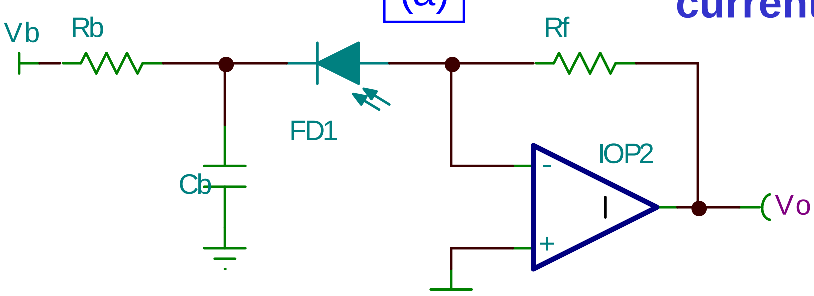


Wideband photodiode Amplifier

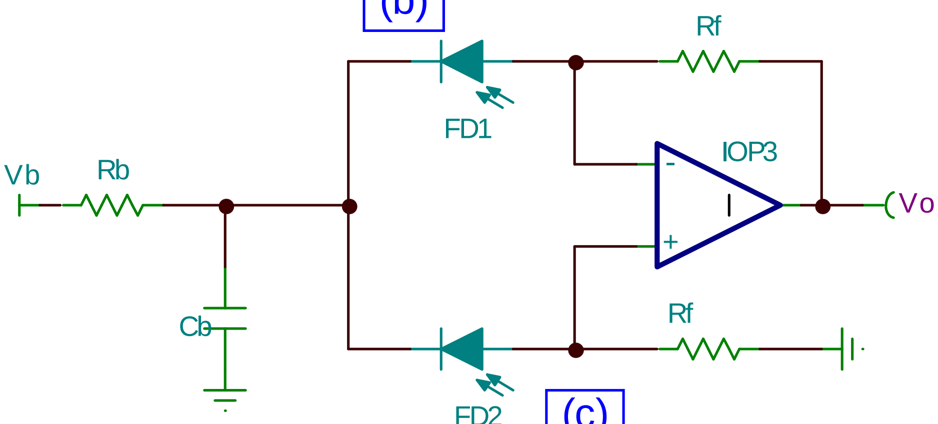
Biasing



(a)



(b)



(c)

(a), **The bias voltage can decrease photo diode capacitor**, for a given amplifier, if we decrease photodiode capacitor, we can increase 1/β curve zero frequency which make us may use a smaller compensation capacitance so that can increase circuit bandwidth. It will also reduce noise gain region.

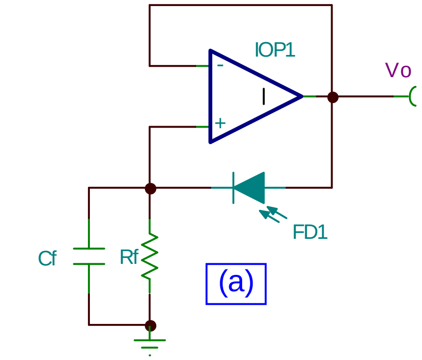
It can still introduce bias noise and increase leak current, which will make output a larger noise and offset.

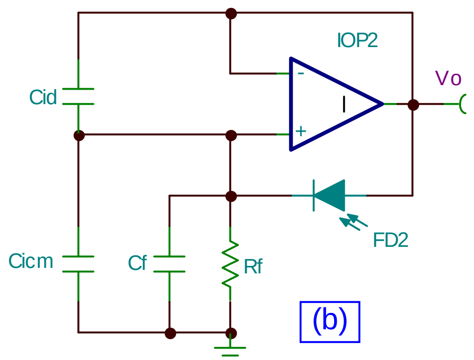
(b) We can **use RC filter to limit bias voltage noise** pass to circuit output. Also, photodiode operating current can also pass Rb also, which produce AC modulation on Vb', it will reintroduce some nonlinearity to output. We need set Rb<<Rf, Cb>>Cd. The bias noise gain could be:

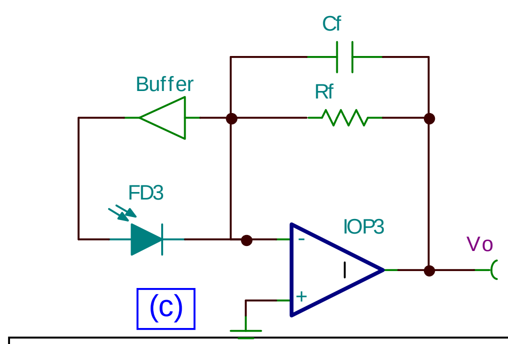
$$A_n = \frac{R_f C_D}{R_B C_B}$$

(c) We still can not remove leak offset on output in the (b) circuit. We can use (c) circuit to both remove leak offset and bias noise. We use same two photodiode to set up differential input. Let one operating and let another one in dark just provide cancellation leak current.

Bootstrapping







Bias circuit can decrease photodiode capacitor but it also more or less introduced noise , offset and nonlinearity to output. We can setup bootstrapping circuit as left (a), in bootstrapping mode, it removes signal voltage on photodiode, this void photodiode absorb diode's signal current at high frequencies.

$$BW = 1.4 f_i \qquad f_i = \sqrt{f_{zf} \; f_c}$$

$$f_{zf} = \frac{1}{2\pi R_f (C_D + C_{id} + C_{icm} + C_f)}$$

$$C_c = 1/2\pi R_f f_c$$

$$C_f = \frac{C_c}{2}\sqrt{1 + \frac{4C_i}{C_c}} - C_{icm}$$

$$C_i = C_D + C_{id}$$

Bootstrapping circuit actually use amplifier's differential input capacitance as part of compensation capacitance, so we can use a smaller value Cf. Obviously bootstrapping circuit improves bandwidth through a decrease in Cf that increase fzf in the bandwidth expression. It can only benefits the small capacitance case.

If we combine current monitor mode and bootstrapping mode, it has greater bandwidth improvement. The buffer amplifier need to be low input capacitance, low output noise, low output impedance and wideband.

This combination best serves larger photodiodes with high capacitances.

Noise

Photodiode noise

The lower limits of light detection for photodiodes are determined by the noise characteristics of the device. The photodiode noise in is the sum of the thermal noise (or Johnson noise) i_j of a resistor which approximates the shunt resistance and the shot noise i_{sD} and i_{sL} resulting from the dark current and the photocurrent.

$$i_n = \sqrt{{i_j}^2 + {i_{sD}}^2 + {i_{sL}}^2}$$

$$i_j = \sqrt{4 \cdot k \cdot T \cdot BW / R_{sh}}$$

$$i_{sD} = \sqrt{2 \cdot q \cdot I_D \cdot BW}$$

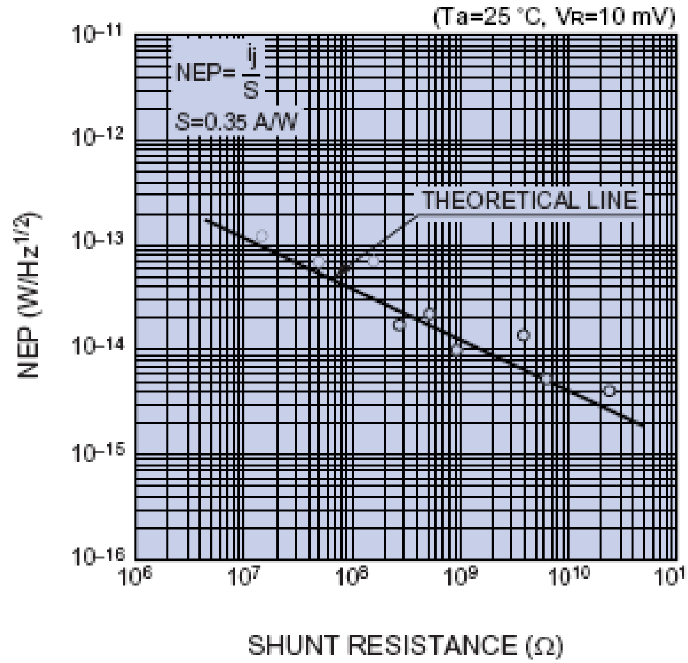
$$i_{sL} = \sqrt{2 \cdot q \cdot I_L \cdot BW}$$

K: Boltzmann's constant
T: Absolute temperature of the element
B: Noise bandwidth
q: Electron charge
I_D: Dark current (Leak current)
I_L: Photocurrent

If IL >> 0.026/Rsh or IL >> ID, the shot noise becomes predominant. The lower limit of light detection for a photodiode is usually expressed as the intensity of incident light required to generate a current equal to the noise current . Essentially this is the noise equivalent power (NEP).

$$NEP = \frac{i_n}{S} [W / Hz^{1/2}]$$

In: noise current (A/√Hz)
S: Photo Sensitivity (A/W)



Circuit Noise

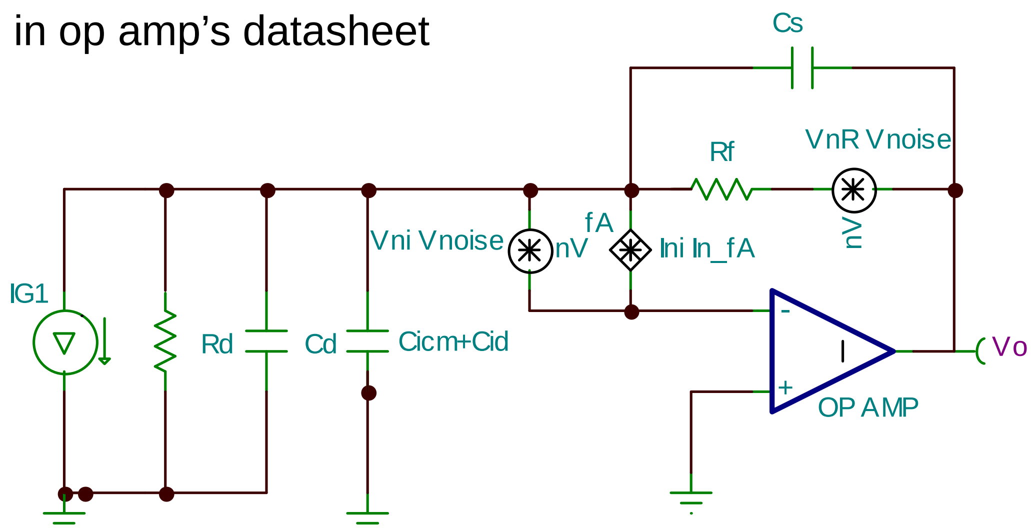
Exclude photodiode noise, there are three kinds of circuit noise: Input voltage noise (V_{ni}), Input current noise (I_{ni}) and feedback resistor noise (V_{nR}).

Different noise has different noise gain amplifying input noise to output.

$$e_{no} = \sqrt{(e_{noR})^2 + (e_{noi})^2 + (e_{noe})^2}$$

$$A_{en} = \frac{e_{no}}{e_{ni}} = \frac{1 + sR_f C_i}{1 + sR_f C_S} \quad , \quad A_{in} = \frac{e_{ino}}{i_{ini}} = R_f \quad , \quad A_{e_{nR}} = \frac{e_{nR}}{e_{nR}} = 1$$

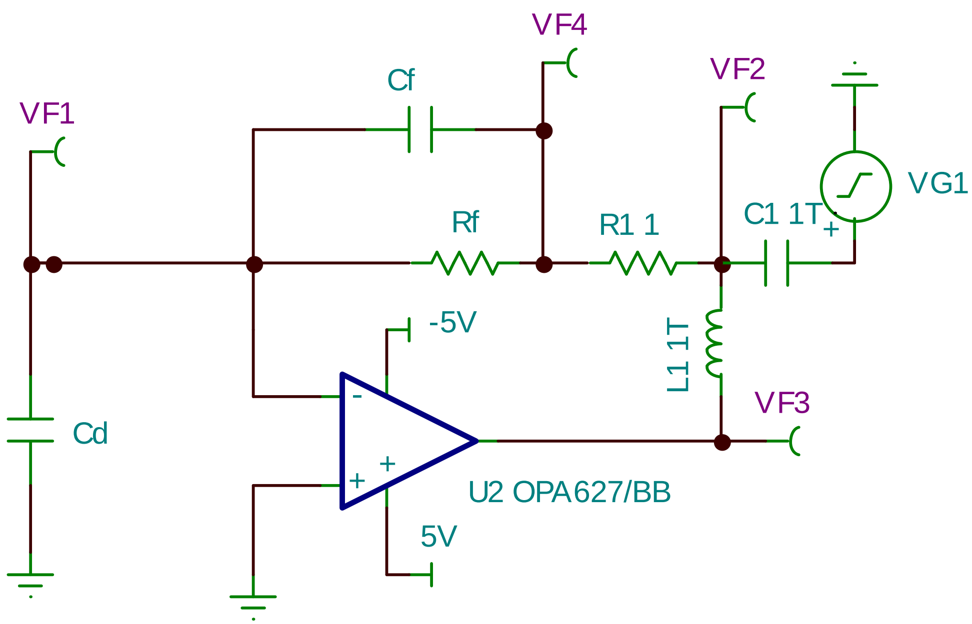
$e_{noR} = \sqrt{4kTRf}$, e_{ni} and i_{ni} can find in op amp's datasheet



Noise gain and noise bandwidth

We setup below simulation circuit:

In order to simulate I-V gain, we need add 1ohm resistor series with Rf and Cf. The voltage between 1ohm resistor present the current flow Rf and Cf. The voltage drop on Cf and Rf divide current to calculate amplifier's trans impedance. Amplifier's trans impedance is not exactly equals to I-V gain. But at low frequency, they are almost the same.

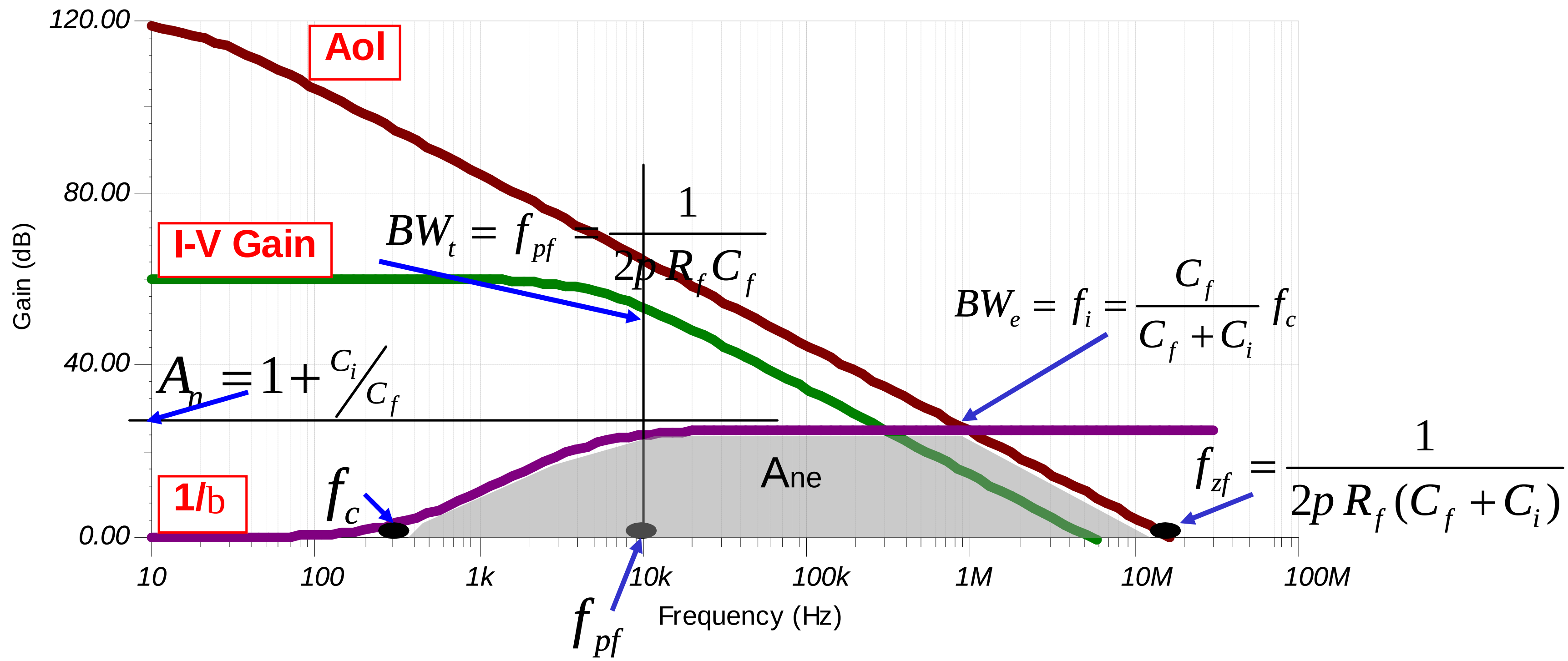


$$A_{ol} = -\frac{VF3}{VF1}$$

$$1/b = \frac{VF4}{VF1}$$

$$I-V_{gain} = \frac{VF4-VF1}{VF2-VF4}$$

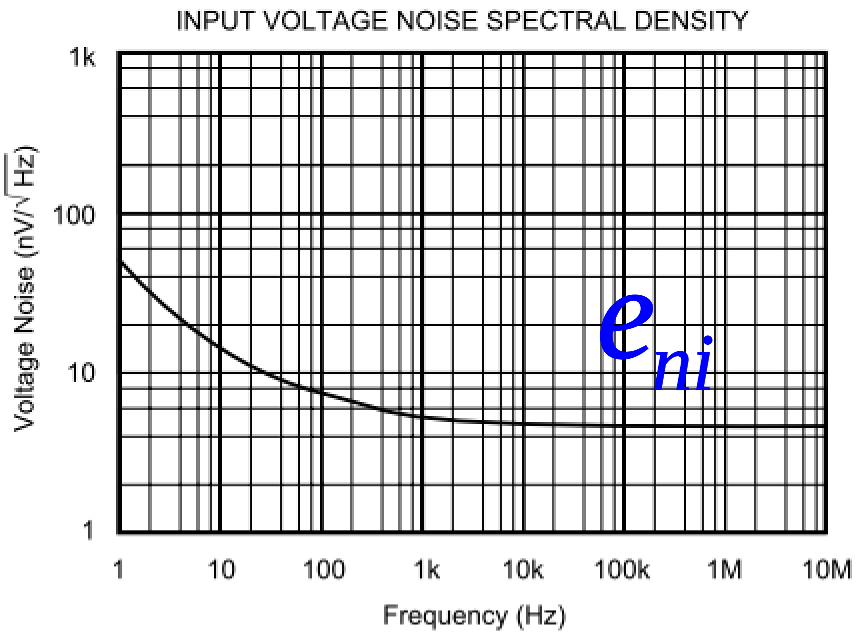
Noise gain and noise bandwidth

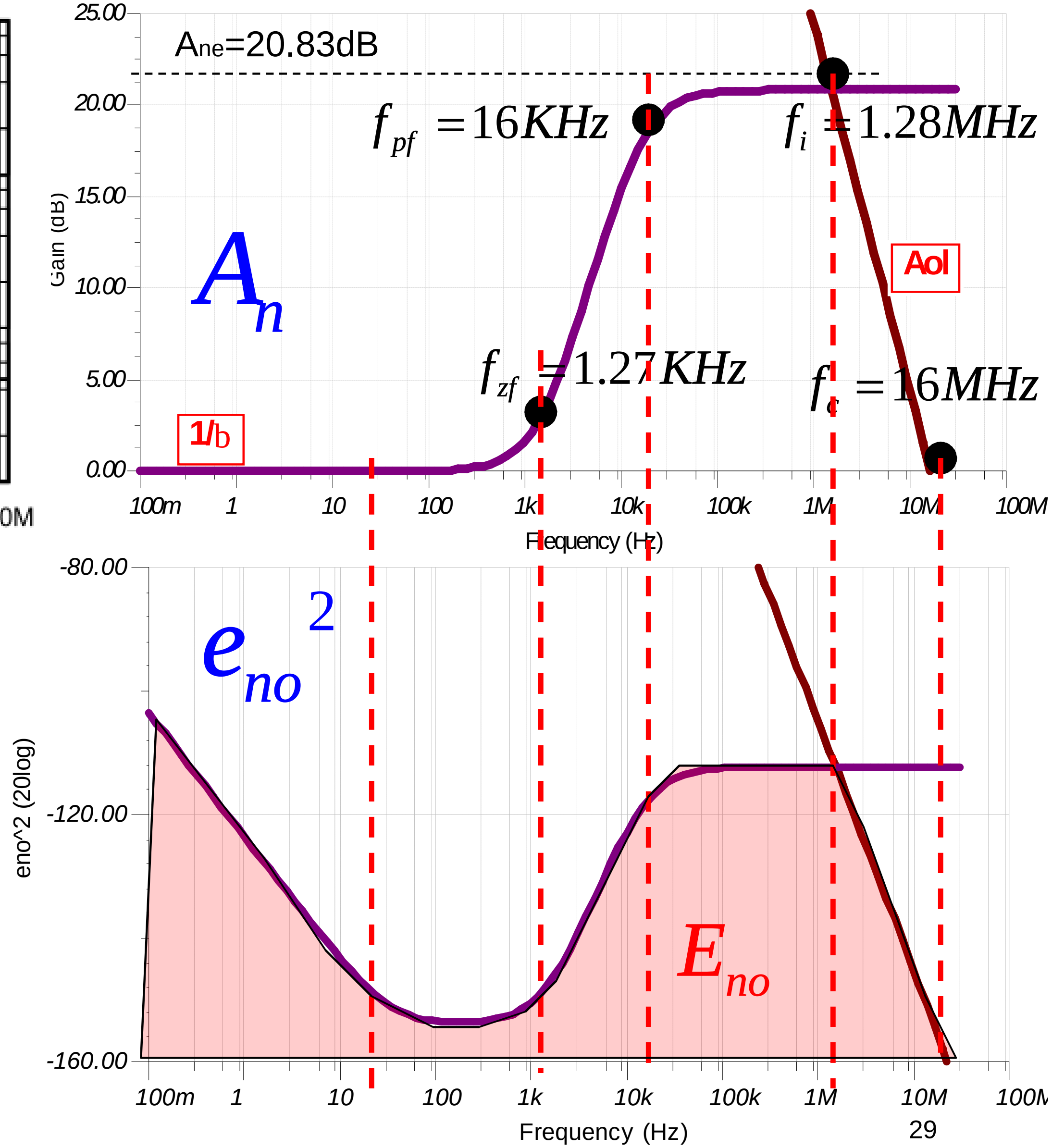


Photodiode parasitic capacitance and amplifier's input capacitance make circuit noise gain increase with frequency until leveled by compensation or stray capacitance and finally rolled off by the amplifier open-loop response.

From figure we can see the bandwidth of current noise, voltage noise are different. current noise and feedback resistor noise we should use BW_t in calculation while using f_{zf} in voltage noise calculation.

Voltage Noise e_{ni} , e_{no} and E_{no}

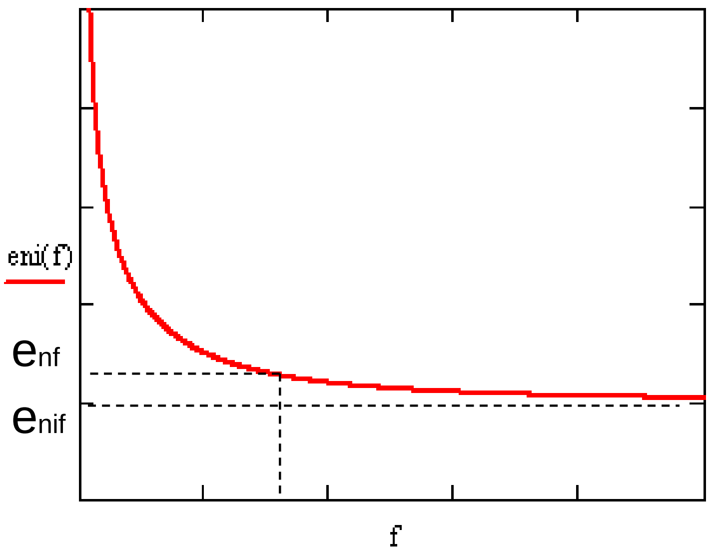




$$e_{no} = A_n \; e_{ni}$$

$$E_{no} = \int_0^\infty e_{no}{}^2 d_f = \int_0^\infty A_n{}^2 \; e_{ni}{}^2 d_f$$

Voltage Noise e_{ni} , e_{no} and E_{no}



Voltage noise expression is:

$$e_{ni} = e_{nif} \sqrt{1 + \frac{w_f}{s}}$$

$$w_f = 2p\, f_f$$

f_f is corner frequency where noise density is √2 times of flat value

The magnitude response is: $e_{ni} = e_{nif} \sqrt[4]{1 + \left(\frac{f_f}{f}\right)^2}$

In the trans impedance amplifier circuit, Ci+Cf and Rf create a zero, Cf and Rf create a pole, at fc*β there is another pole. So the noise gain can expressed as:

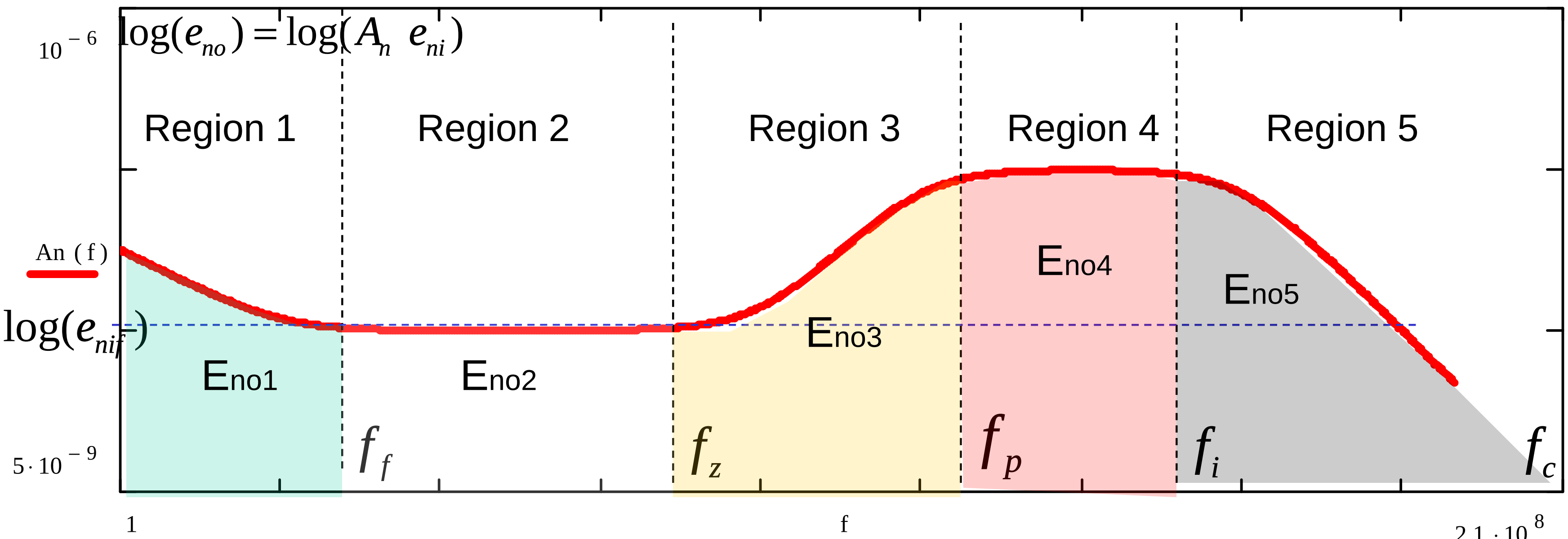
$$A_n = \frac{1 + \frac{s}{w_{zf}}}{\left(1 + \frac{s}{w_p}\right)\left(1 + \frac{s}{w_i}\right)}$$

Voltage Noise e_{ni} , e_{no} and E_{no}

From An and e_{ni} expression we can express e_{no} as below:

$$e_{no} = A_n\ e_{ni} = \frac{\left(1+\frac{s}{w_{zf}}\right)\sqrt{1+\frac{w_f}{s}}}{(1+\frac{s}{w_p})\left(1+\frac{s}{w_i}\right)}\ e_{nif}$$

Output noise density as below figure. Total output noise is integration of e_{no}. We separate the noise density into five regions for easy calculation.



TEXAS INSTRUMENTS

Voltage Noise e_{ni} , e_{no} and E_{no}

Region 1 noise: $$E_{noe1}^{\;2} = \int_{f_L}^{f_f} \frac{e_{nif}^{\;2} \cdot f_f}{f} d_f = e_{nif}^{\;2} f_f \ln \frac{f_f}{f_L}$$

Region 2 noise: $$E_{noe2}^{\;2} = \int_{f_f}^{f_z} e_{nif}^{\;2} d_f = e_{nif}^{\;2} \left(f_z - f_f \right)$$

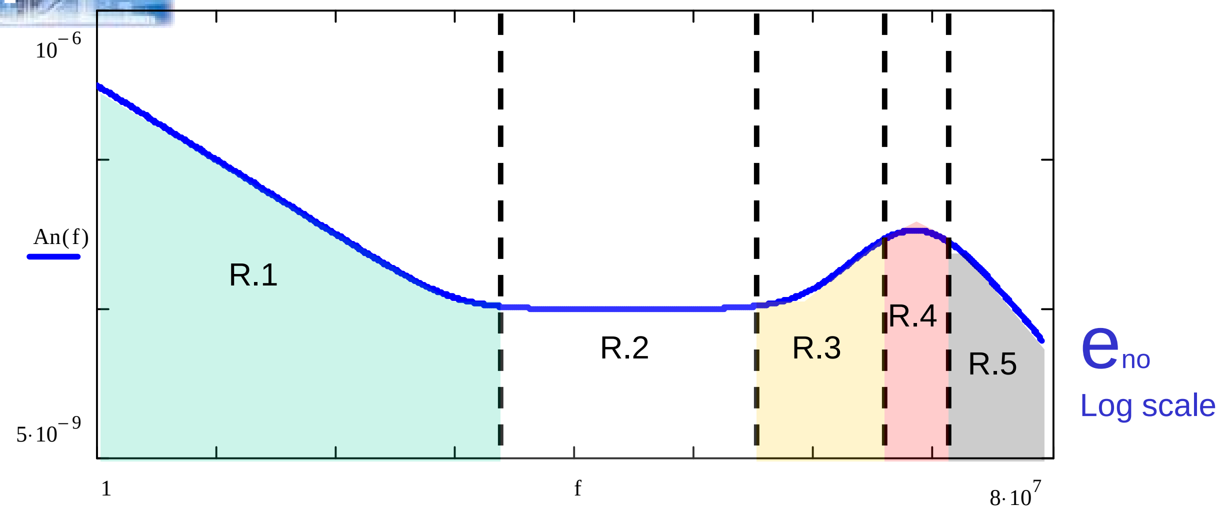
Region 3 noise: $$E_{noe3}^{\;2} = \int_{f_z}^{f_p} \frac{e_{nif}^{\;2} \cdot f^2}{f_z^{\;2}} d_f = \left(\frac{e_{nif}}{f_z} \right)^2 \frac{f_p^{\;3} - f_z^{\;3}}{3}$$

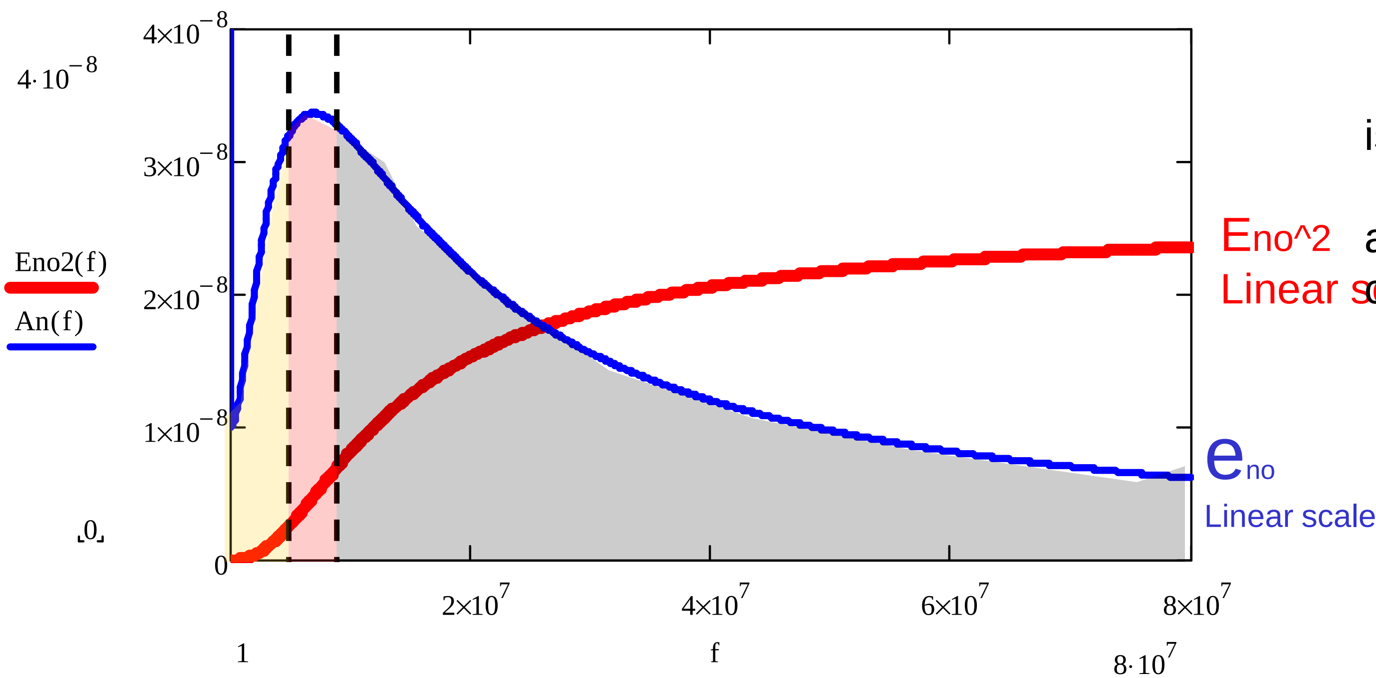
Region 4 noise: $$E_{noe4}^{\;2} = \int_{f_p}^{f_i} \left(\frac{e_{nif}}{b} \right)^2 d_f = \left(e_{nif} \cdot \frac{C_i + C_f}{C_f} \right)^2 \left(f_i - f_p \right)$$

Region 5 noise: $$E_{noe5}^{\;2} = \int_{f_i}^{\infty} \left(\frac{e_{nif} f_c}{f} \right)^2 d_f = \frac{\left(e_{nif} f_c \right)^2}{f_i}$$

Total voltage noise: $$E_{noe}^{\;2} = E_{noe1}^{\;2} + E_{noe2}^{\;2} + E_{noe3}^{\;2} + E_{noe4}^{\;2} + E_{noe5}^{\;2}$$

Voltage Noise e_{ni} , e_{no} and E_{no}

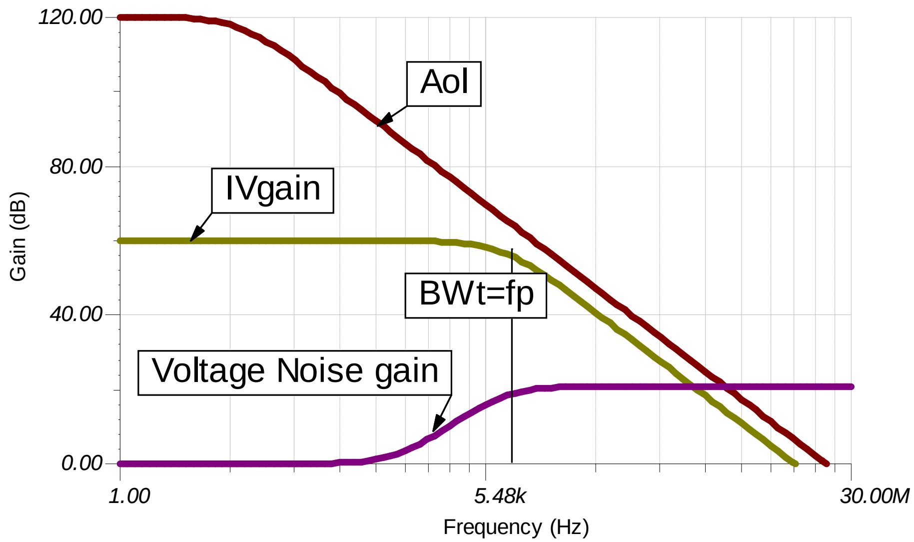




Two left figures obviously present: although 1/f noise density is very large in noise density, but noise gain and bandwidth make region (3,4,5) contribute to output noise (E_{no}) most.

Noise gain effect region is controlled by Ci,Cf,Rf,fc. Compensation design and op amp selection is critical for noise characters.

Resistor Noise and Current Noise



Current noise and resistor noise are pass trans impedance. IV frequency curve is LP filter.

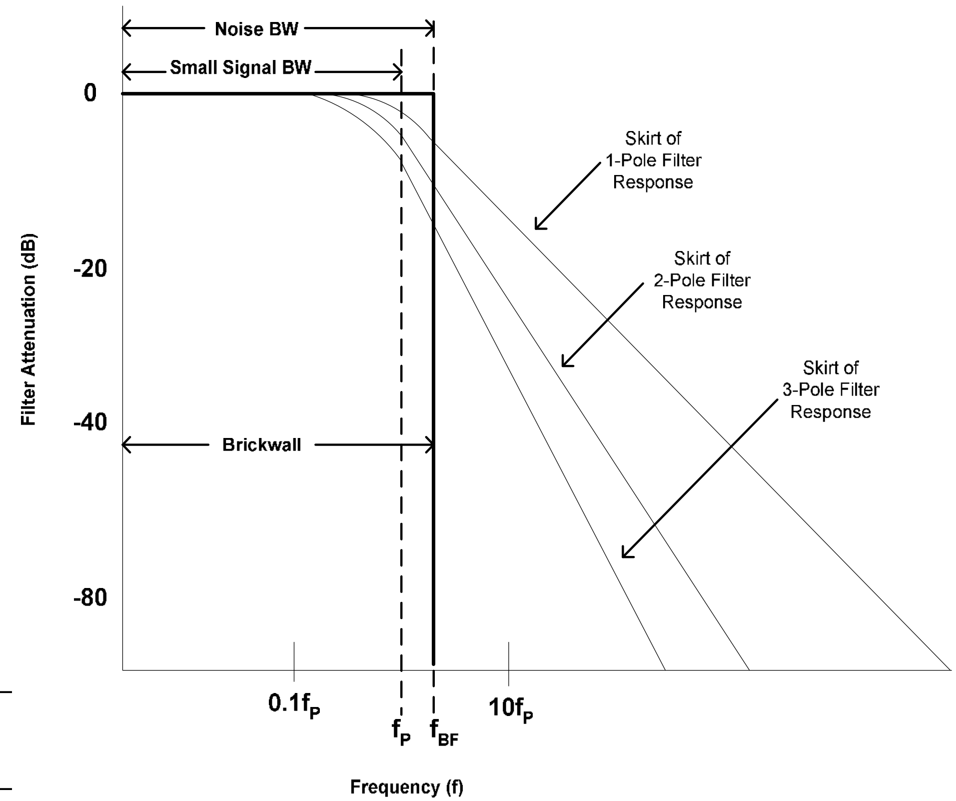
$BW_n = (f_H)(K_n)$ Effective Noise Bandwidth

Poles	Kn
1	π/2=1.57
2	1.22
3	1.16

$$E_{noR} = \sqrt{4KTR_f BW_n} = \sqrt{2p\, KTR_f\, f_p}$$

$$E_{noI} = i_{ni} R_f \sqrt{\frac{p}{2} f_p}$$

i_{ni} is current noise density

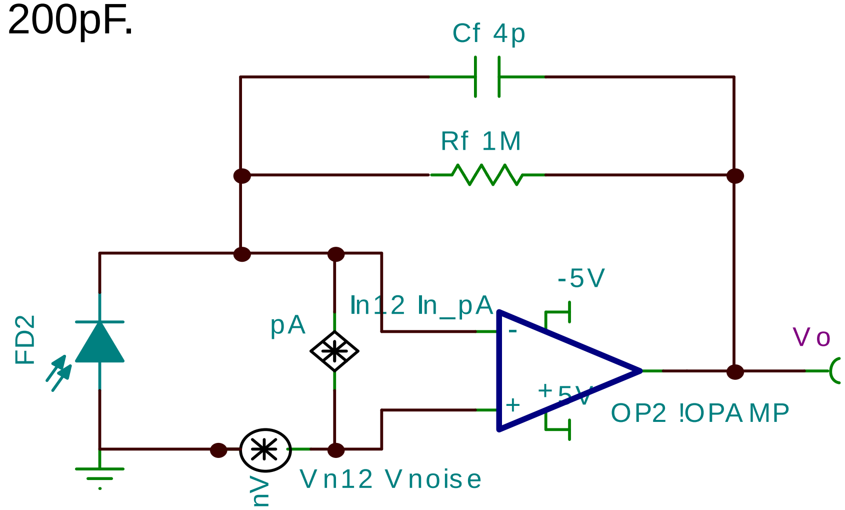


Noise Hands calculation

We have a amplifier with 500Mhz GBW, 120dB open loop gain, noise specific as below:

NOISE								
Input Voltage Noise								
Noise Density: f = 10Hz			15	40		20		nV/√Hz
f = 100Hz			8	20		10		nV/√Hz
f = 1kHz			5.2	8		5.6		nV/√Hz
f = 10kHz			4.5	6		4.8		nV/√Hz
Voltage Noise, BW = 0.1Hz to 10Hz			0.6	1.6		0.8		µVp-p
Input Bias Current Noise								
Noise Density, f = 100Hz			1.6	2.5		2.5		fA/√Hz
Current Noise, BW = 0.1Hz to 10Hz			30	60		48		fAp-p
INPUT IMPEDANCE								
Differential			10^{13} || 8			*		Ω || pF
Common-Mode			10^{13} || 7			*		Ω || pF

The circuit total input capacitor is 200pF.



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Noise Hands calculation

$$C_i = 200pF, C_f = 4pF, f_f = 100Hz, R_f = 1M\Omega, b = \frac{C_f}{C_i + C_f} = \frac{4}{200+4} = 0.02, e_{nif} = 4.5\frac{nV}{\sqrt{Hz}}$$

$$f_z = \frac{1}{2\pi R_f (C_i + C_f)} = 780Hz, f_p = \frac{1}{2\pi R_f C_f} = 40KHz, f_i = b f_c = 9.8MHz$$

$$E_{noe1} = \sqrt{e_{nif}{}^2 f_f \ln\frac{f_f}{f_L}} = 118.3nV \qquad E_{noe2} = \sqrt{e_{nif}{}^2 \left(f_z - f_f\right)} = 117.4nV$$

$$E_{noe3} = \sqrt{\left(\frac{e_{nif}}{f_z}\right)^2 \frac{f_p{}^3 - f_z{}^3}{3}} = 26.43mV \qquad E_{noe4} = \sqrt{\left(e_{nif} \cdot \frac{C_i + C_f}{C_f}\right)^2 \left(f_i - f_p\right)} = 717.1mV$$

$$E_{noe5} = \sqrt{\frac{\left(e_{nif} f_c\right)^2}{f_i}} = 718.6mV$$

Noise Hands calculation

Output voltage noise, resistor noise and current noise are:

$$E_{noe} = \sqrt{E_{no1}{}^2 + E_{no2}{}^2 + E_{no3}{}^2 + E_{no4}{}^2 + E_{no5}{}^2} = 1.016mV$$

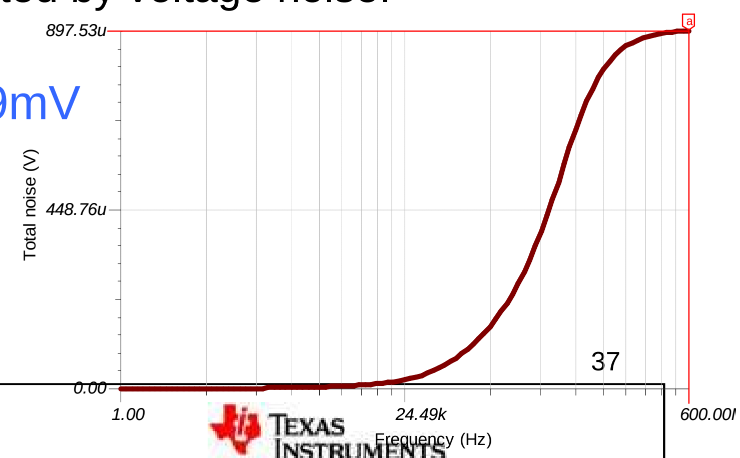
$$E_{noR} = \sqrt{2p\,KTR_f\, f_p} = 32.17mV$$

$$E_{noI} = i_{ni} R_f \sqrt{\frac{p}{2} f_p} = 0.4mV$$

Total output noise is: $$E_{no} = \sqrt{(E_{noR})^2 + (E_{noi})^2 + (E_{noe})^2} = 1.016mV$$

We can see in this circuit, output noise is mainly contributed by voltage noise.

Tina Simulation Result: Total output noise E_{no}=0.9mV



Calculation Accuracy

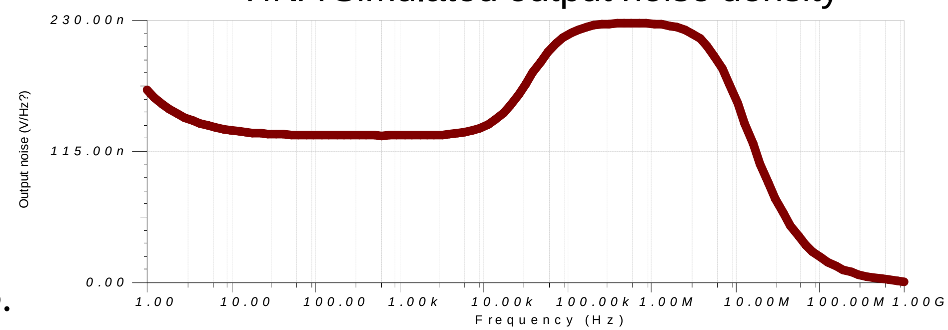
There are 0.1 mV error in hands calculation and TINA simulation. As Noise is mainly contributed by voltage noise, we compared TINA simulation output noise density and Our noise model density as below:

Unit : nV/√Hz	1Hz	260Hz	600KHz	16MHz	70MHz	140MHz	200MHz
TINA	137.2	128.88	227.5	121.71	31.89	15.82	10.86
Calculation Model	45	4.91	228.6	119.9	31.83	16.03	11.24

At high frequency two curve values are very close to each other, At low frequency the noise density is different on resistor and current noise. Resistor noise density is 128nV/√Hz.

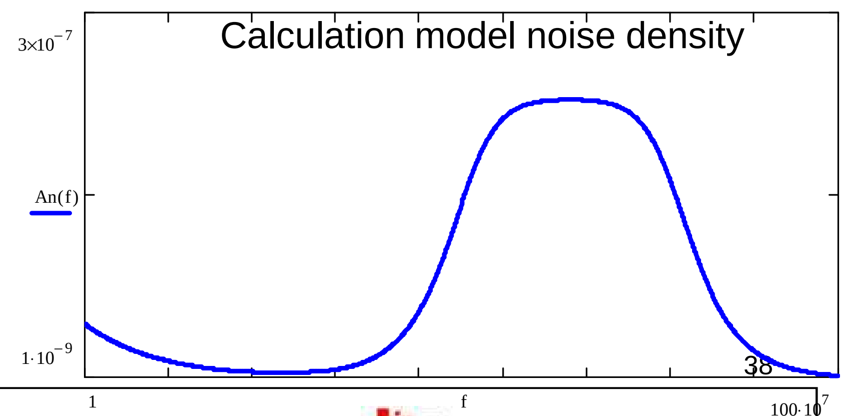
Integrate the calculation mode from 0.1Hz to ∞.

TINA Simulated output noise density



$$E_{oe}' = \sqrt{\int_{0.1Hz}^{\infty} \left| \frac{\left(1+\frac{s}{w_{zf}}\right)\sqrt{1+\frac{w_f}{s}}}{\left(1+\frac{s}{w_p}\right)\left(1+\frac{s}{w_i}\right)} e_{nif} \right| d_f} = 0.8947mV$$

$$s = jw$$



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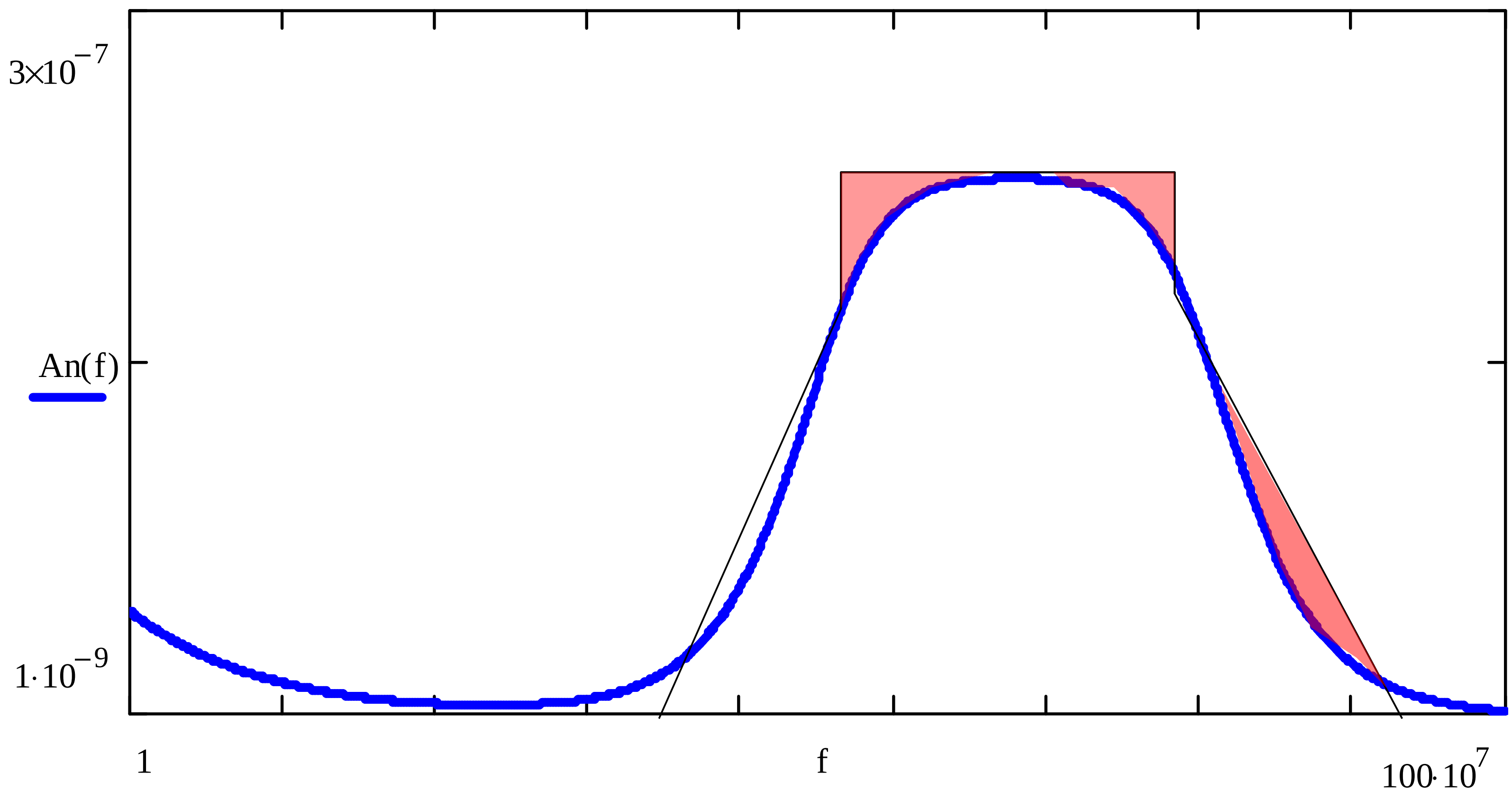
Calculation Accuracy

Integration value is very close to TINA simulation value, which illustrate the calculation noise expression model is accurate. We simplified the curve especially corner frequency's 3dB attenuation.

In low noise gain and wide fp-fz circuit, the error will be more significant



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Calculation Accuracy

Five different region's hand calculation errors as below. Obviously, the error is mainly comes from Region4 and Rgeion5

$$E_{noe1}=\sqrt{e_{nif}{}^{2} f_f \ln\frac{f_f}{f_L}-\int_{f_L}^{f_f}\left(A_n e_{ni}\right)^2 d_f}=65nV$$

$$E_{noe2}=\sqrt{e_{nif}{}^{2}\left(f_z-f_f\right)-\int_{f_f}^{f_z}\left(A_n e_{ni}\right)^2 d_f}=78nV$$

$$E_{noe3}=\sqrt{\left(\frac{e_{nif}}{f_z}\right)^2\frac{f_p{}^{3}-f_z{}^{3}}{3}-\int_{f_z}^{f_p}\left(A_n e_{ni}\right)^2 d_f}=16mV$$

$$E_{noe4}=\sqrt{\left(e_{nif}\cdot\frac{C_i+C_f}{C_f}\right)^2\left(f_i-f_p\right)-\int_{f_p}^{f_i}\left(A_n e_{ni}\right)^2 d_f}=0.335mV$$

$$E_{noe5}=\sqrt{\frac{\left(e_{nif}\,f_c\right)^2}{f_i}-\int_{f_i}^{\infty}\left(A_n e_{ni}\right)^2 d_f}=0.26mV$$

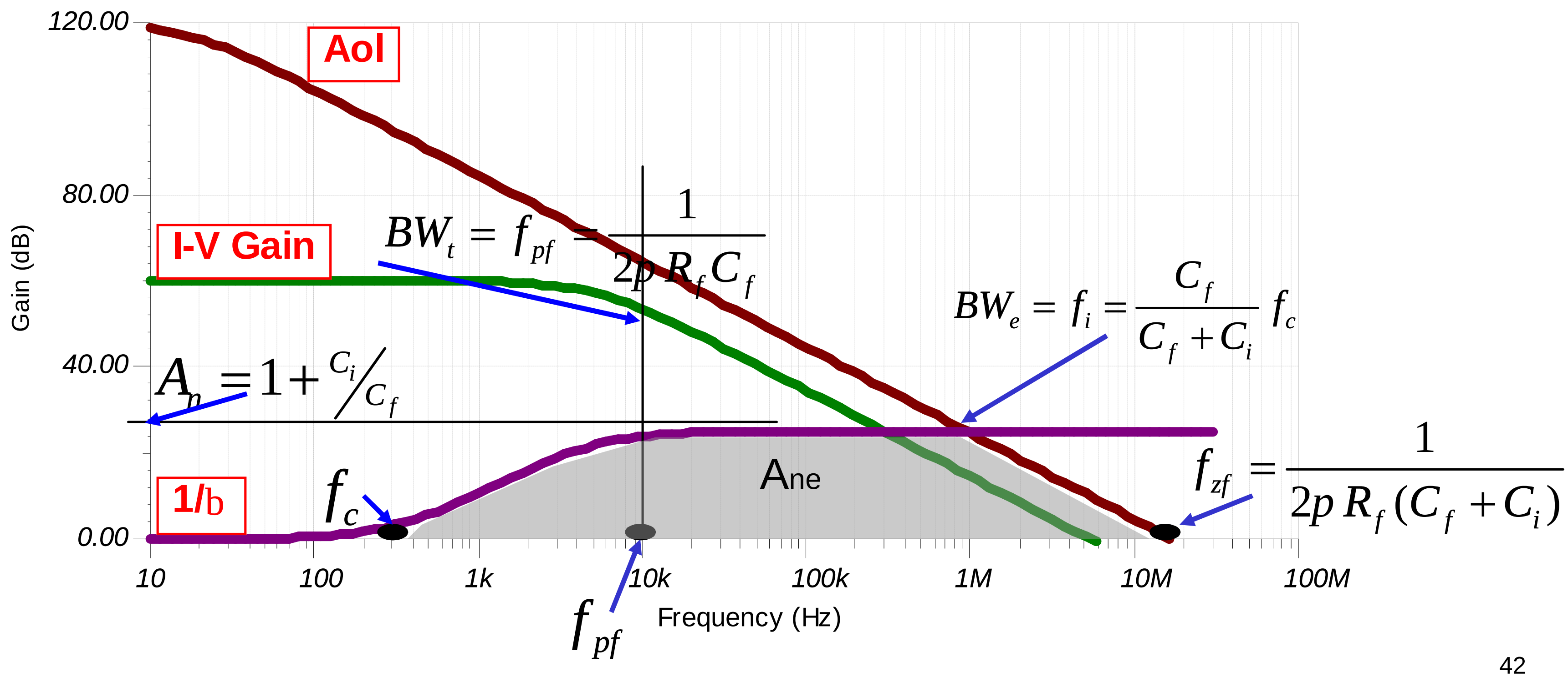
Noise Reduction

Noise Reduction

As analyzed, trans impedance amplifier's noise mainly comes from Region 3,4,5 especially region 4 and 5. We have two guide line to reduce noise:

-Reduce noise gain

-Reduce noise bandwidth

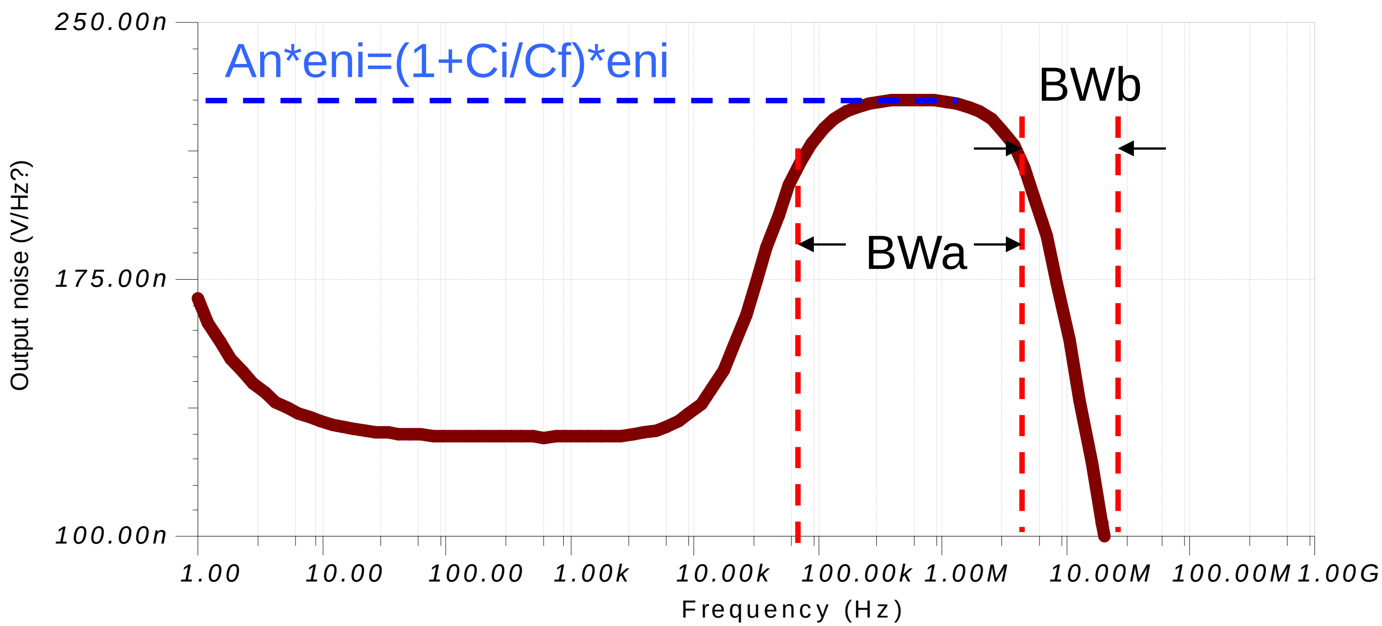


Noise Reduction

As analyzed, trans impedance amplifier's noise mainly comes from Region 3,4,5 especially region 4 and 5. We have two guide lines to reduce noise:

- Reduce noise gain
- Reduce noise bandwidth

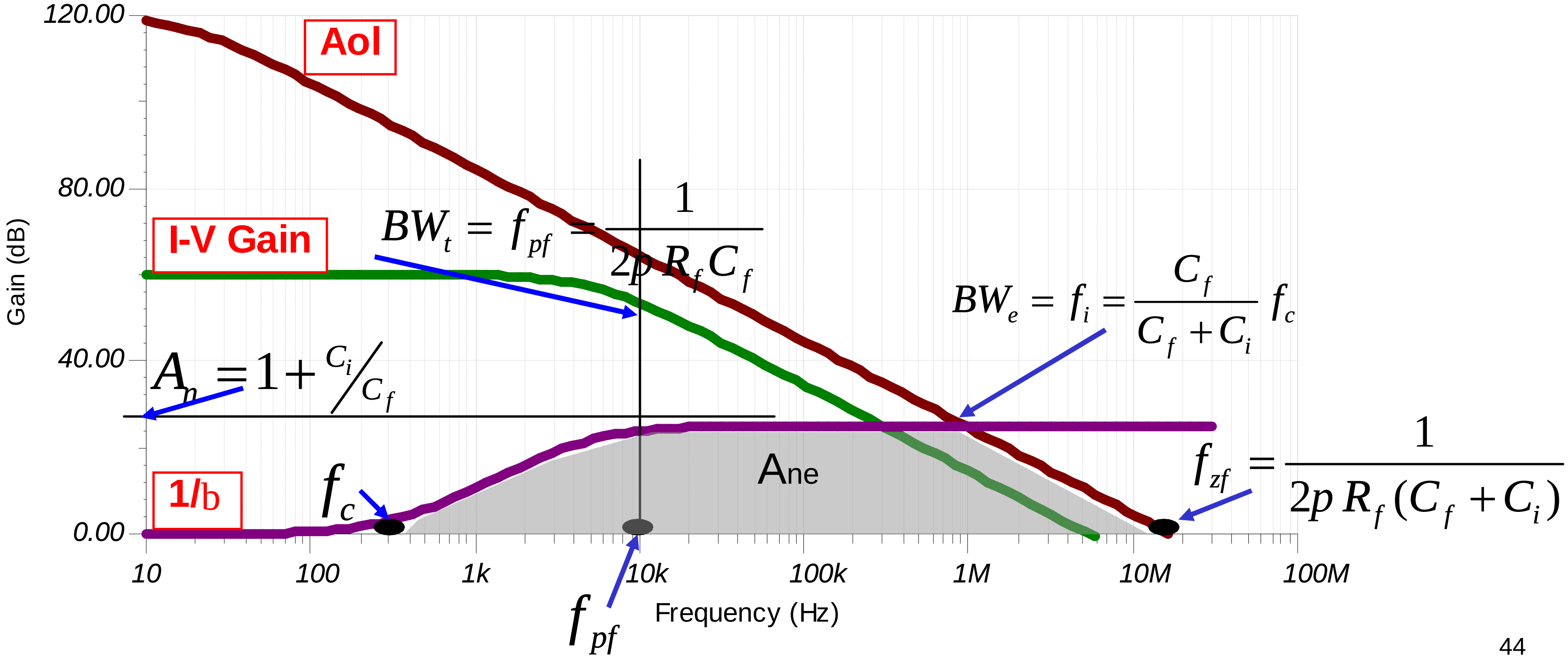
In trans impedance amplifier, peak noise gain equals to 1+Ci/Cf. We select a larger feedback capacitor can effective reduce noise.



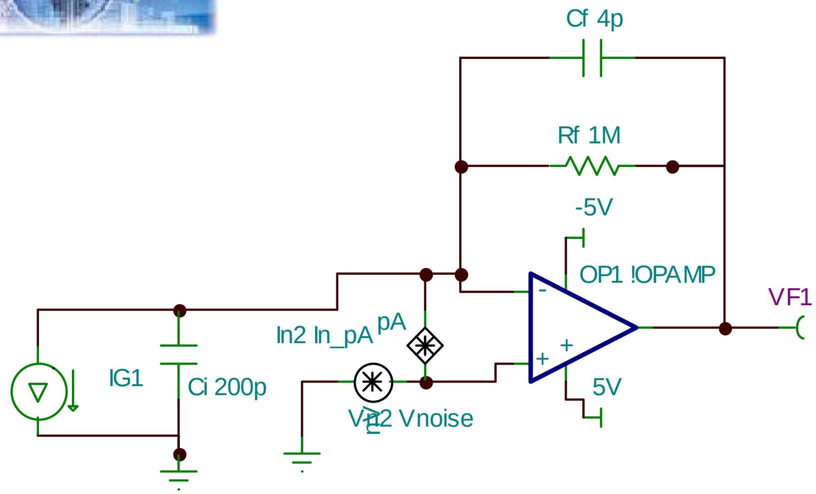
Noise Reduction

Signal bandwidth BWt=1/(2πRfCf), when we increase feedback capacitor signal bandwidth BWt also decreased, noise bandwidth BWa increase. We need synthetically consider whether the total noise is effective redudced or not.

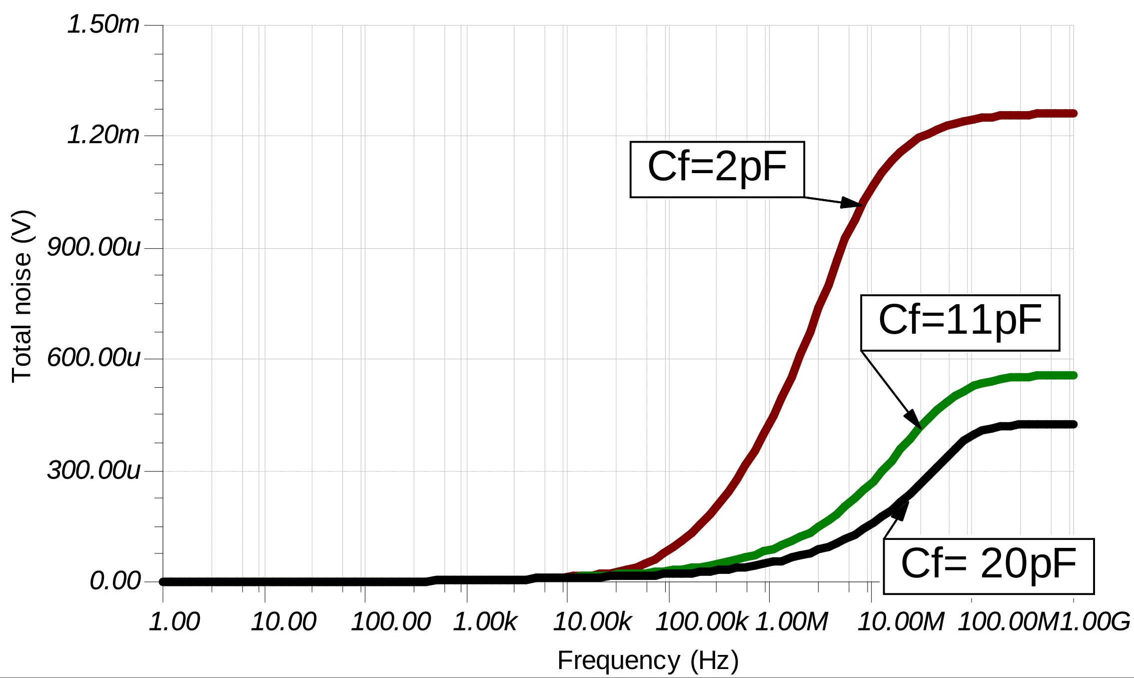
However, as long as bandwidth requirements permit, use a suitable capacitor offers the simplest method to reduce noise.



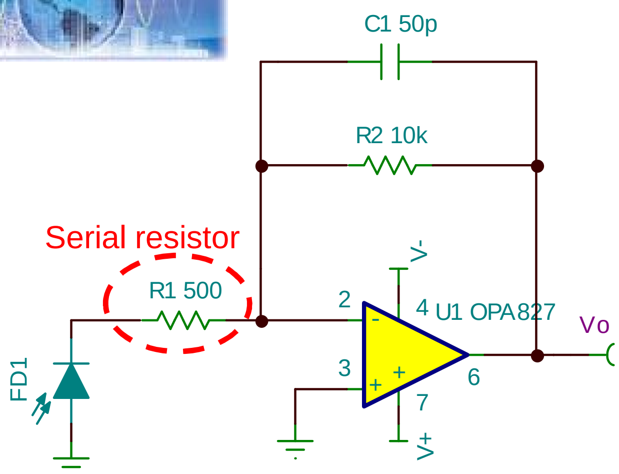
Noise Reduction

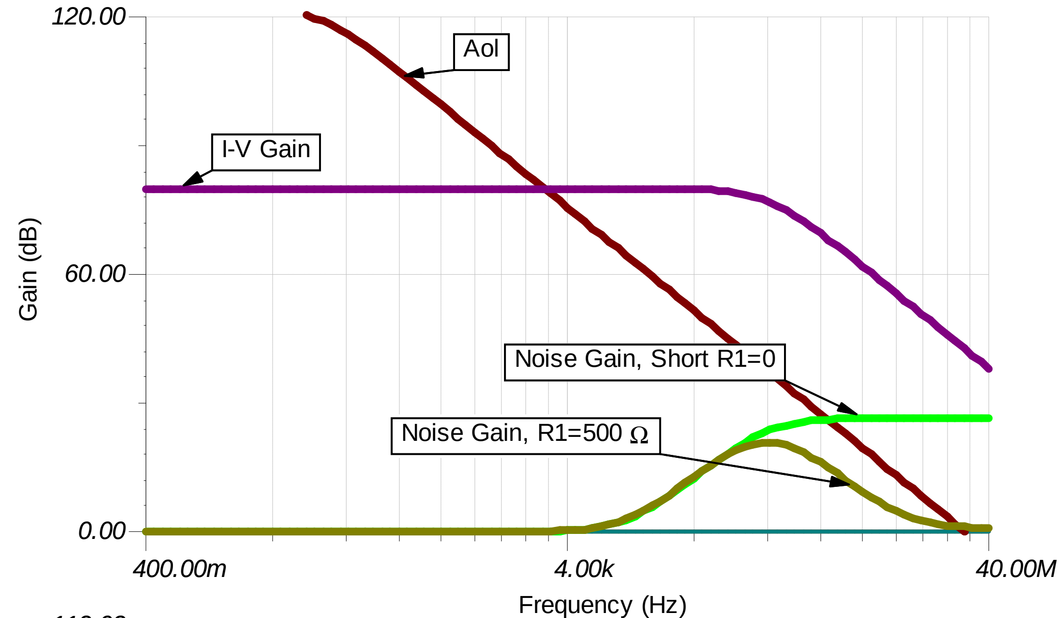


Using the op amp we just analyzed, the simulation circuit as left. We select three feedback capacitor value2pF, 11pF, 20pF. Output noise is obviously decrease with feedback capacitance value increase.



Noise Reduction, Serial Resistor

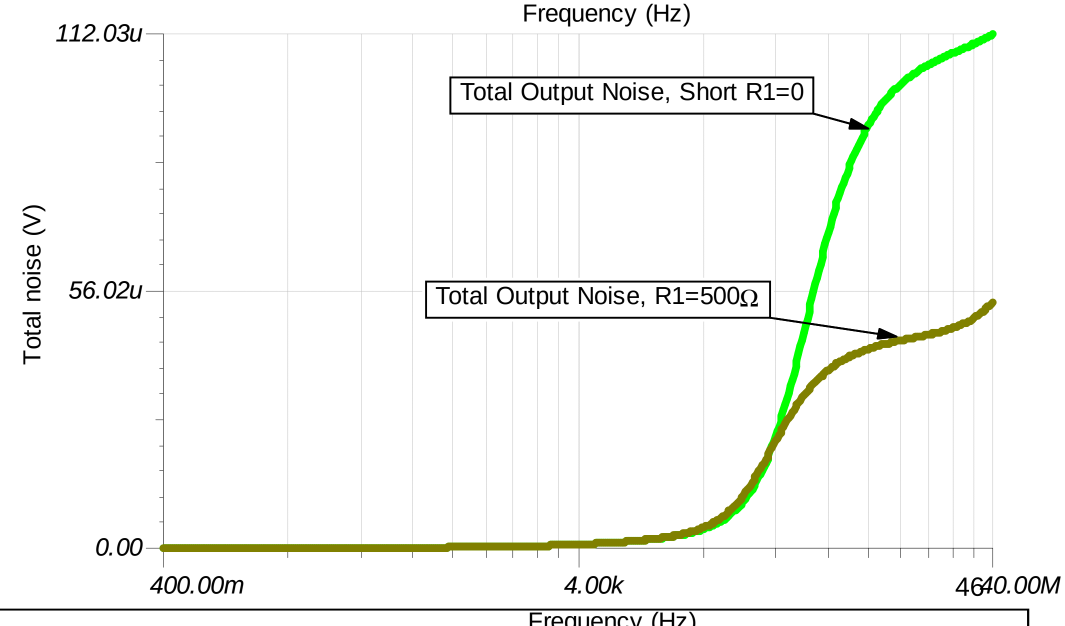




Use a resistor R1 serial with photodiode as figure (a), The noise gain is changed by the serial resistor R1. A noise gain curve pole will produced by the serial resistor and photodiode capacitor C3 at 1/(2pi*R2*C3), as figure (b). The total output noise is apparently reduced.

But when current flow R1 will also modulate non-inverting bias voltage across photodiode which will increase dark current and affect AC specifics like linearity.

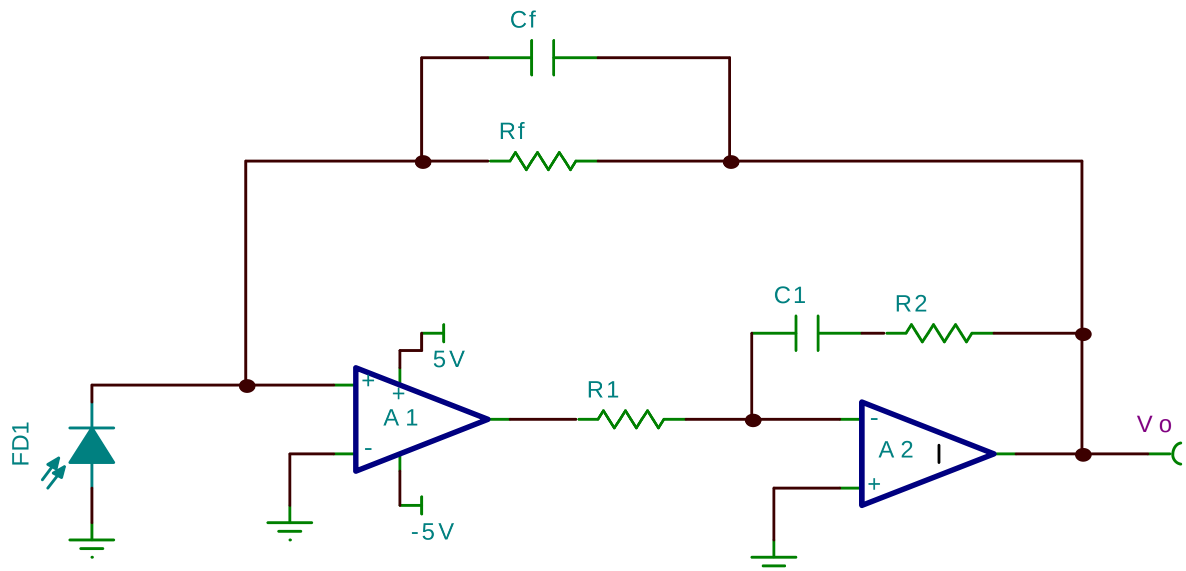
So a the resistance need to be small. This requires evaluation of specific application conditions before adding Rc.



Noise Reduction

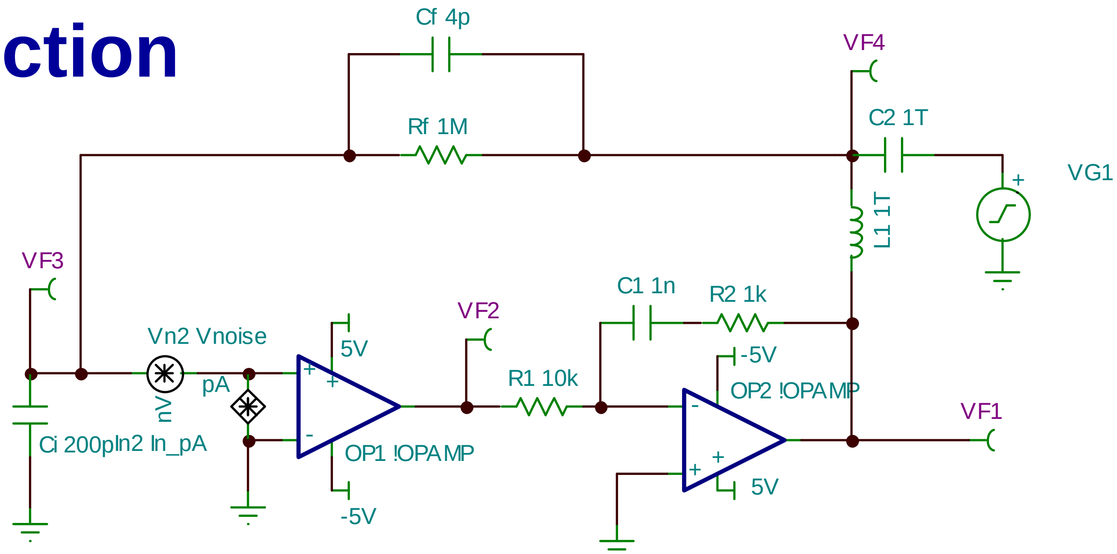
Another way to reduce noise in reduce noise bandwidth. Below circuit can reduce noise bandwidth while not change signal bandwidth. It uses two amplifier to built up a composite op amp which has modified Aol curve. We can modify the Aol curve by adjusting R1, R2 and C2.

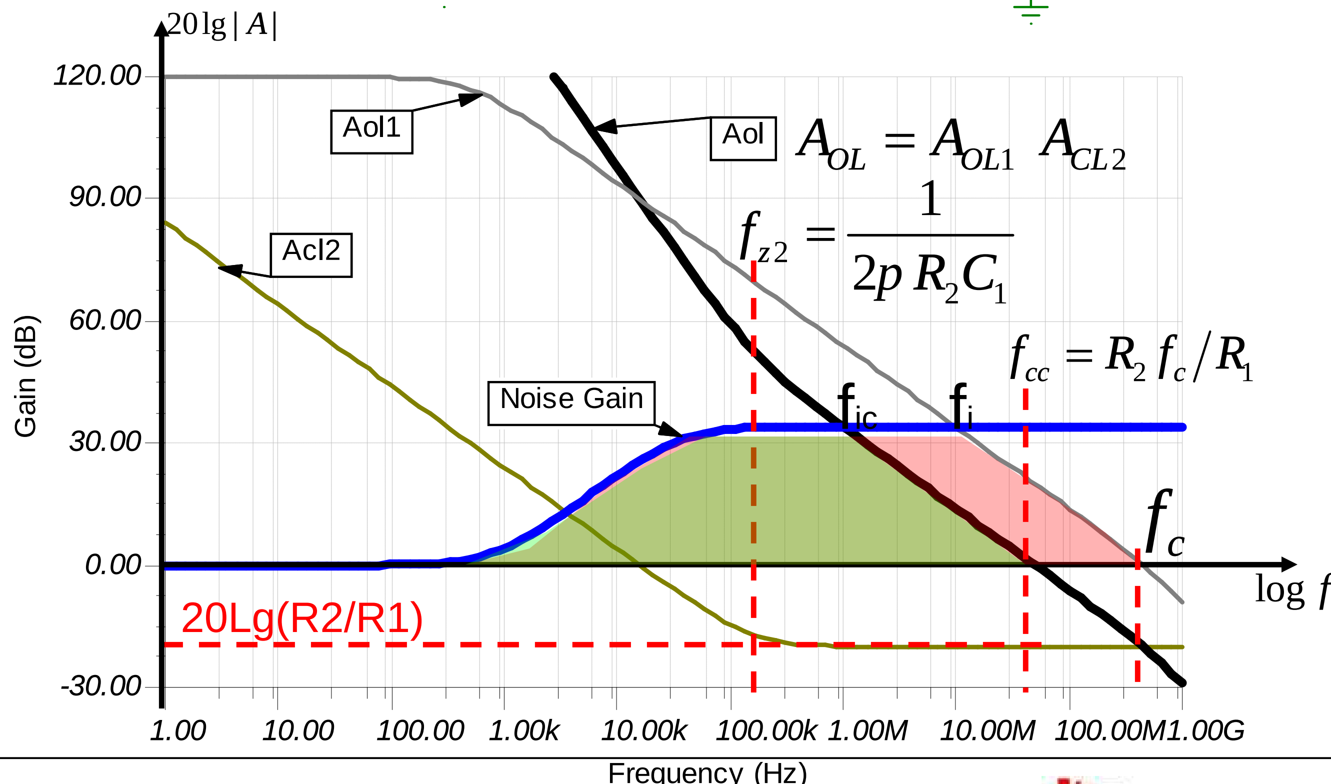
At low frequencies, C1 blocks A2's local feedback, and this amplifier contributes its full open loop gain to composite feedback. At intermediate frequencies, the integrator feedback formed by R1 and C1 reduces the A2 gain support in a transition to the attenuator mode. At high frequencies, C1 becomes short circuit, A2 circuit's gain stable at –R2/R1. Make R2>R1to produce desired high-frequency attenuation.



Noise Reduction

Using the circuit on right for TINA simulation. the noise bandwidth has been changed smaller. We set R1, R2 and C1 to realize Aol modify.





Noise Reduction

How to optimize R1, R2 and C1?

R2/R1 factor produces a compromise between noise and signal bandwidths through placement of fic. Decrease R2/R1 factor will move Aol curve left, expending the shaded area removed from the noise response. However, this move also brings a new signal bandwidth limit into significance. In compromise, setting fic=fpf makes the two limits coincident for the maximum possible noise reduction with out a major reduction of signal bandwidth.

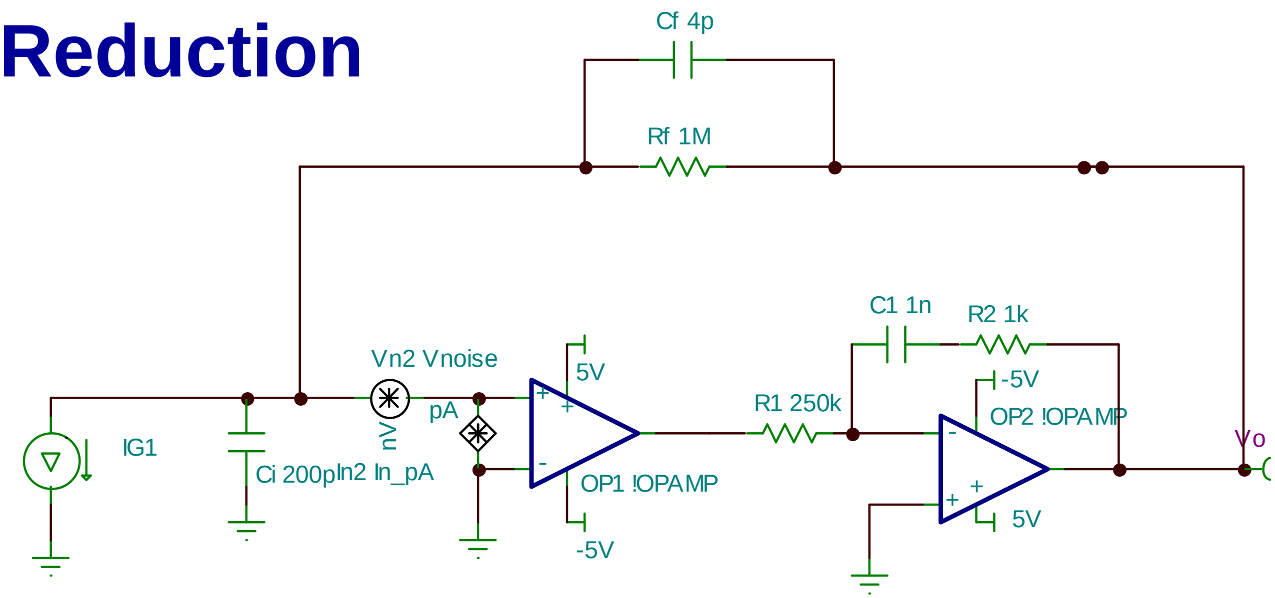
The optimized value is: $\frac{R_2}{R_1} = \frac{f_{pf}}{b\ f_{cf}}$ $\qquad C_1 = \frac{10R_f}{R_2}$

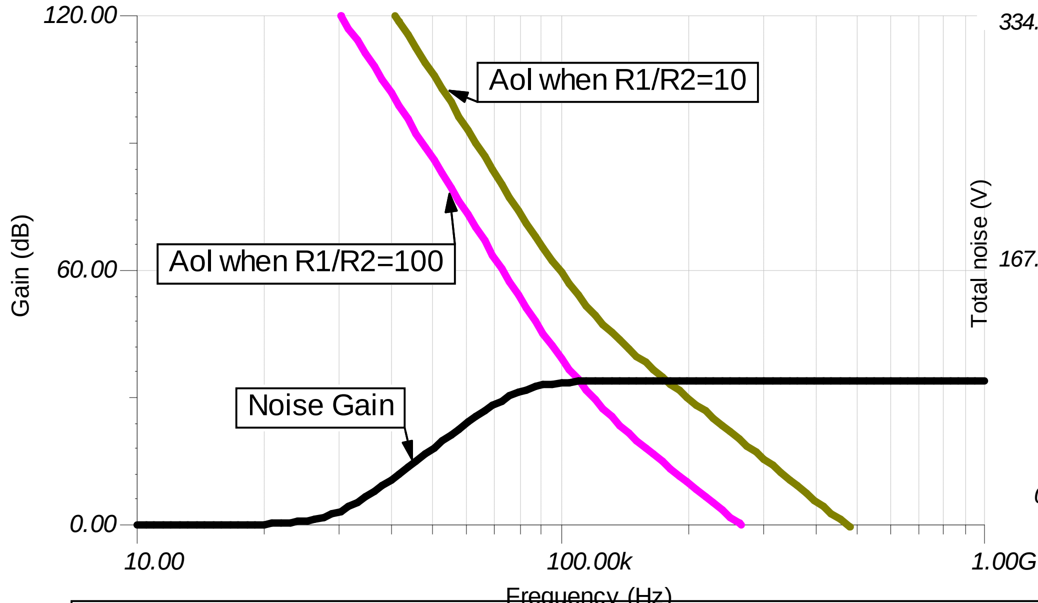
We can also use a active filter following trans impedance opamp for noise filtering and composite noise Aol modify, but added op amp also added it's noise in to the circuit. Composite solution attenuated op2's noise by op1's Aol, but series filter op amp added it's noise in to signal chain directly.

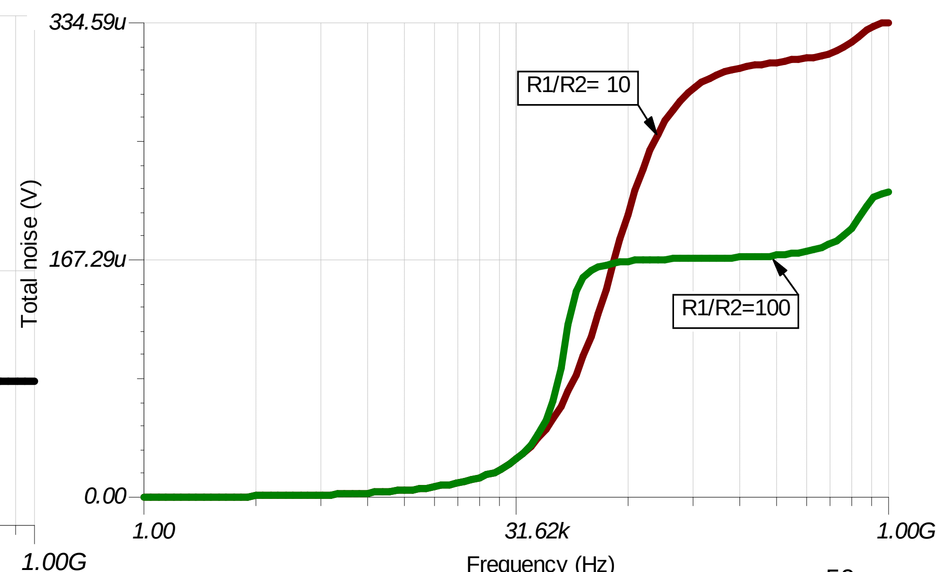
Noise Reduction

Use right circuit for noise simulation. Stepping R1 as 10K and 100K, the total output noise obviously different.

Decrease R2/R1 factor will move Aol curve left, expending the shaded area removed from the noise response





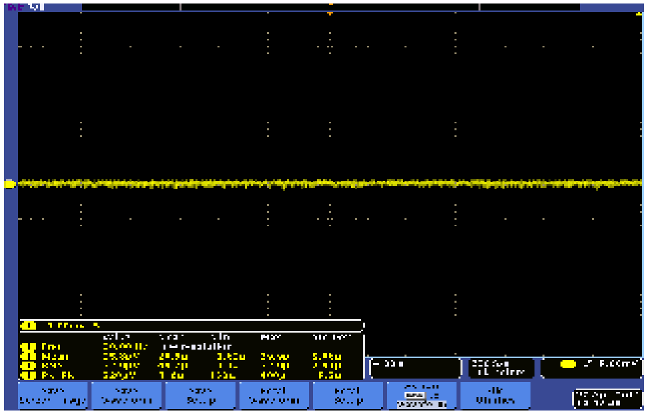


Transimpedance amplifier Noise Test, Calculation and Simulation

Test Equipment

- Tektronix DPO 4034 Oscilloscope
- Hewlett Packard 3458A Digital Multimeter
- Agilent 35670A dynamic Signal Analyzer
- Agilent 4395A Spectrum Analyzer

Tektronix DPO 4034 Oscilloscope



STDEV: 48uV
P-P: 6.6*STDEV=319uV
40s P-P: 320uV

1) Set DC couple, 20MHz bandwidth limits;
2) Use BNC short Cap to short input channel at panel to measure background noise;
3) Use BNC wire to connect board and scope;

Hewlett Packard 3458A Digital Multimeter

1) True RMS Meter;
2) SETACV RNDM mode;
3) 20~10MHz Bandwidth;
4) 0.1% accuracy;
5) Maximum Resolution 1uV

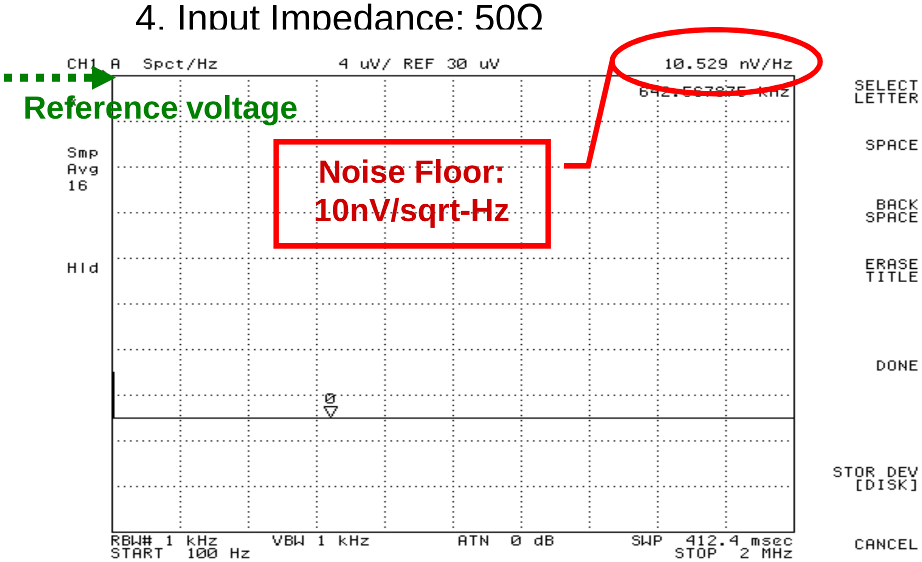
Spectrum Analyzer

Agilent 35670A dynamic Signal Analyzer

1, Frequency Range: 122uHz~102.4KHz;
2, Noise floor: 20nV/sqrt-Hz
3, 90dB Dynamic range
4, Input Impedance: 1MΩ

Agilent 4395A spectrum analyzer

1, Frequency Range: 10Hz~500MHz;
2, Noise floor: 10nV/sqrt-Hz, but min reference voltage is about 2uV, so it can only present more than hundreds nano density
4. Input Impedance: 50Ω



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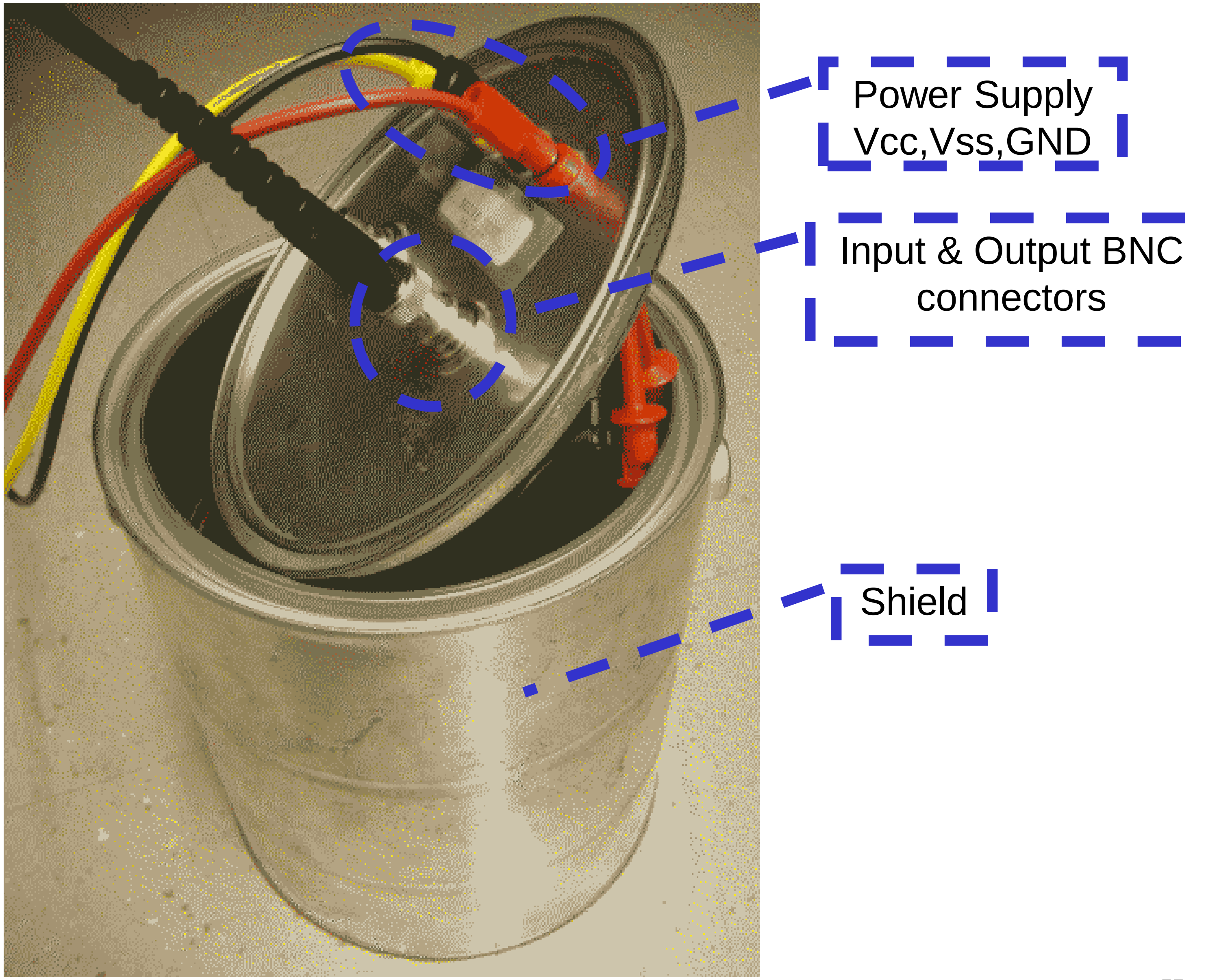
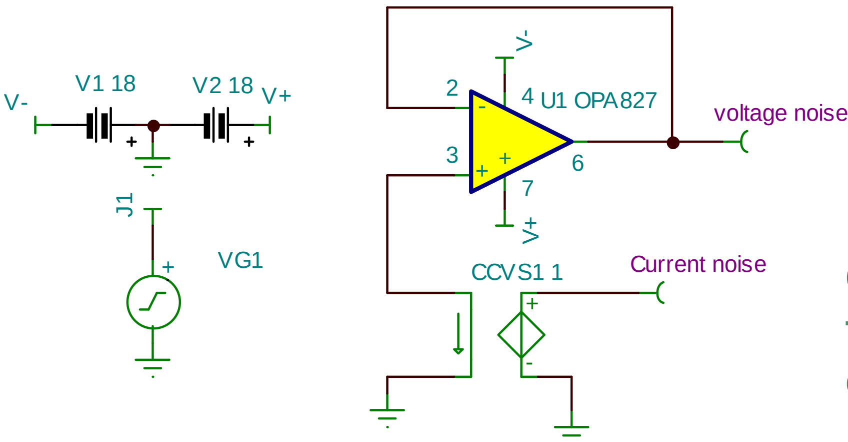
Test in Can


Power Supply
Vcc,Vss,GND
Input & Output BNC
connectors
Shield

Post Amplifier

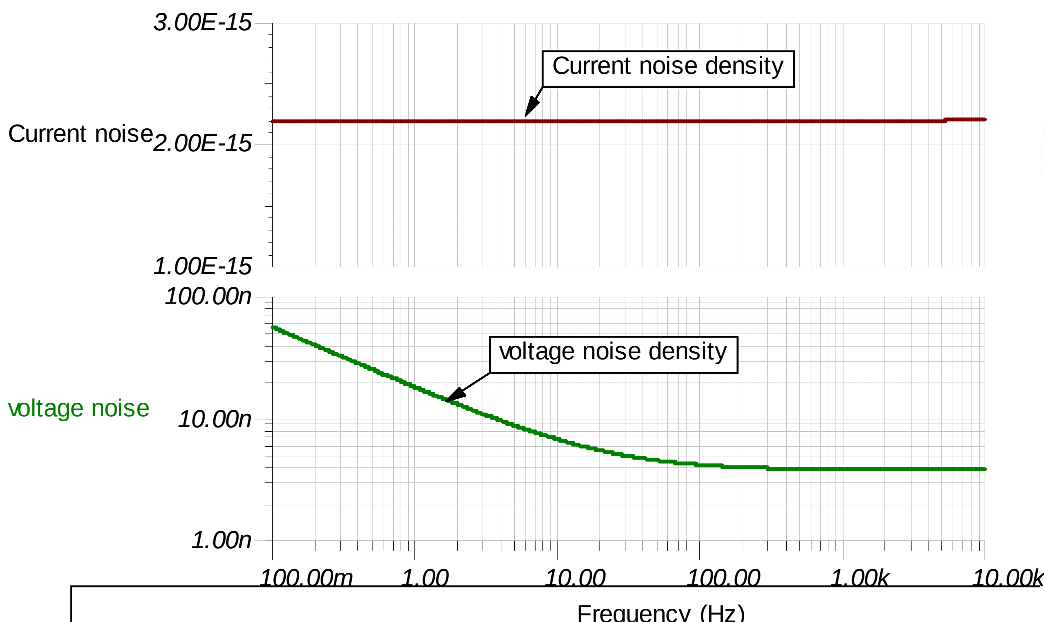
OPA827

- Low Noise Voltage: 4nV/√Hz at 1kHz
- Low Offset Voltage: 150µV max
- JFET Input: I_B= 15pA typ
- Wide Bandwidth: 22MHz



In most transimpedance circuit, amplifier GBW determines noise bandwidth. If we need test the opa827 transimpedance amplifier circuit, we must ensure signal chain BW is not less than 22MHz.

The noise performance is the same as datasheet.



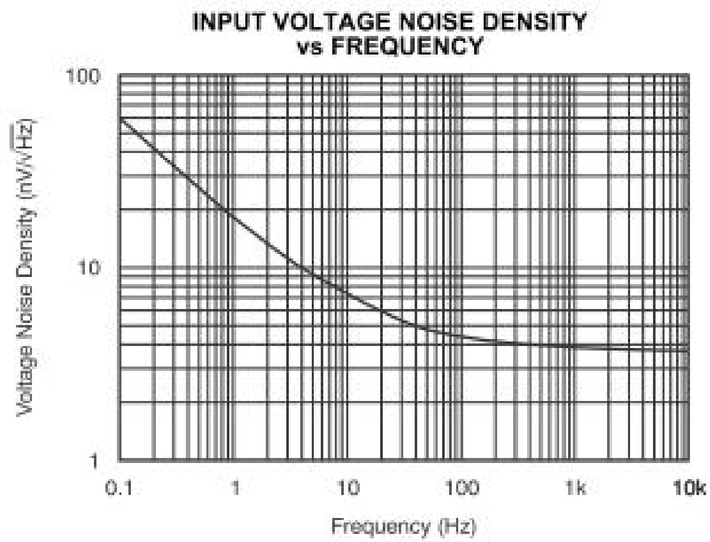
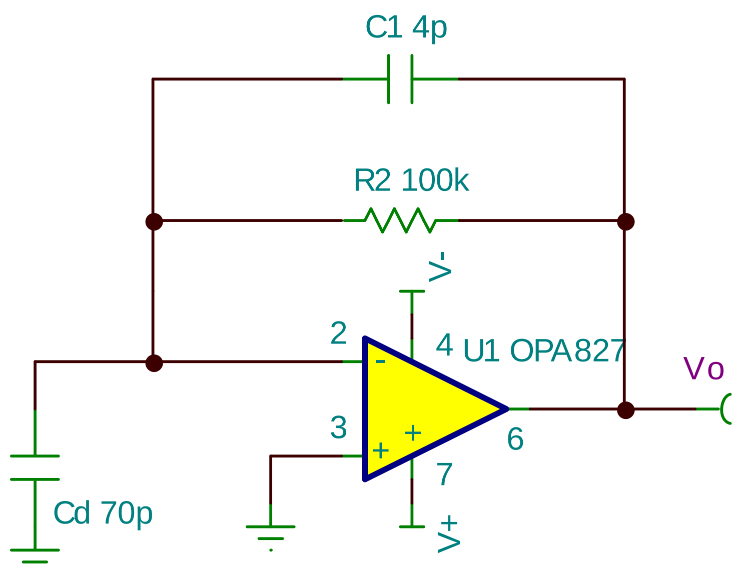
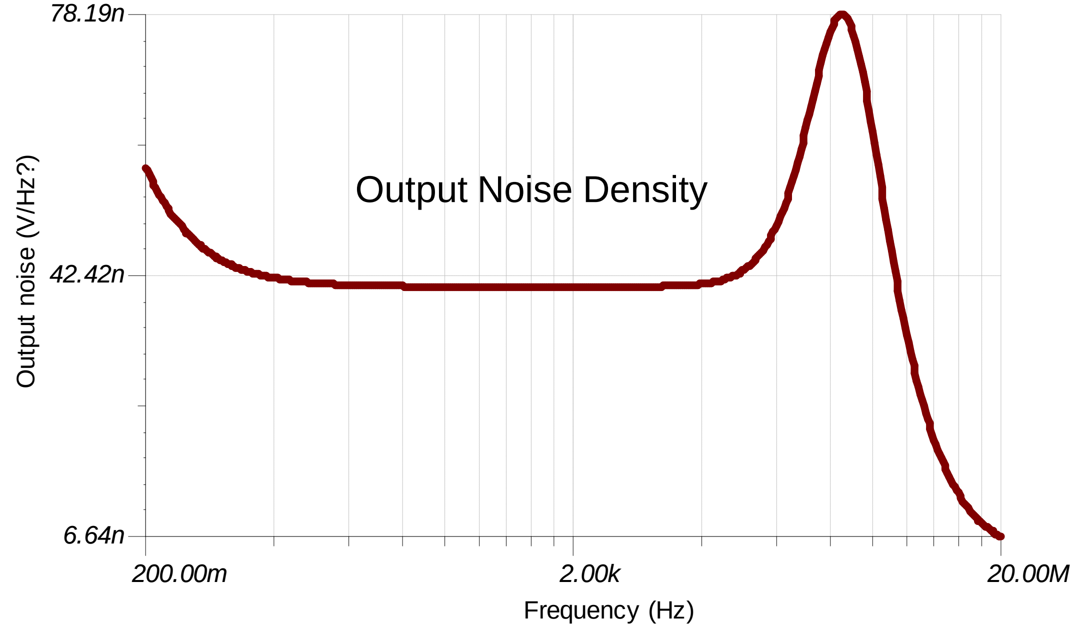
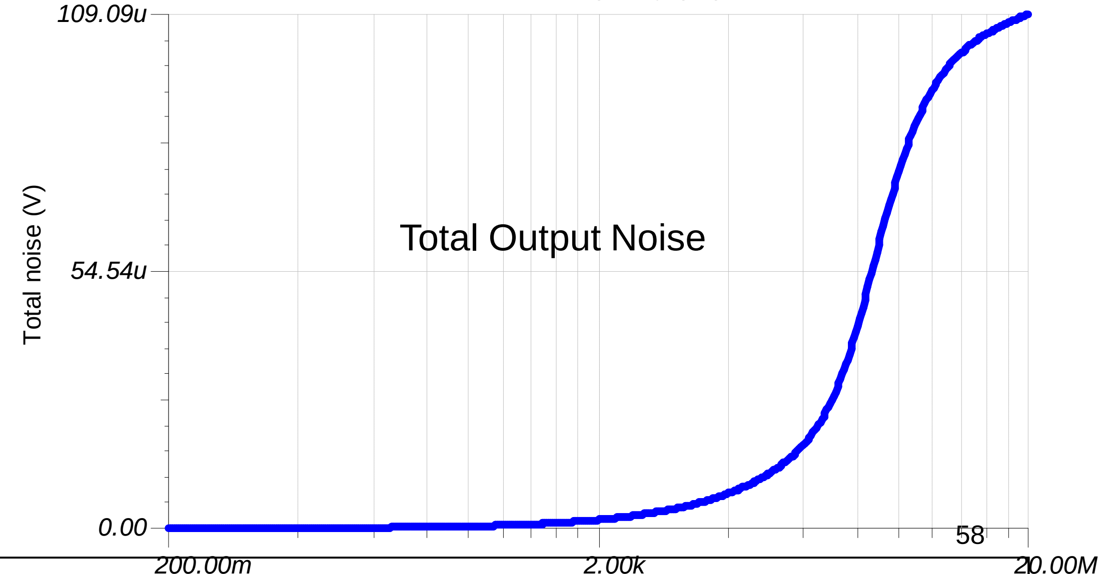


Figure 1.

Current Monitor mode







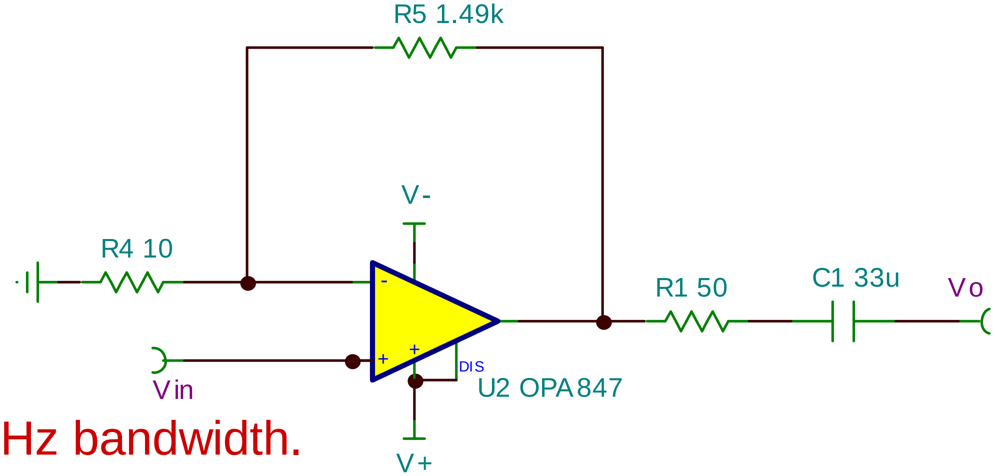
Very small noise, will be flood in test equipments noise. We need post amplifier with high gain to zoom out noise so that we can check it in test equipments.

Use OPA847 as post amplifier

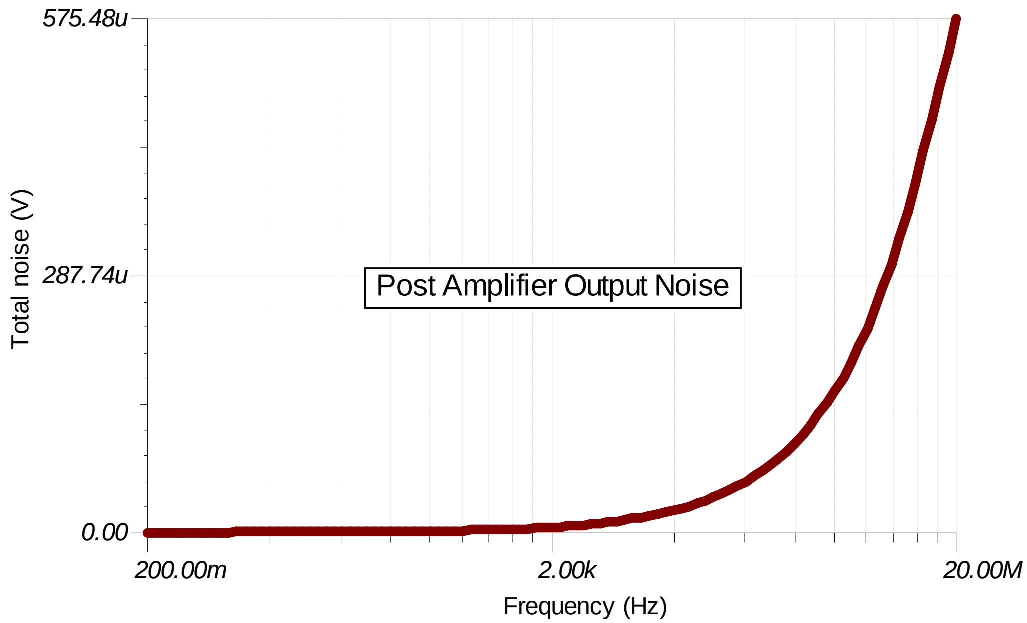
Wideband, Ultra-Low Noise, Voltage Feedback, Operational Amplifier

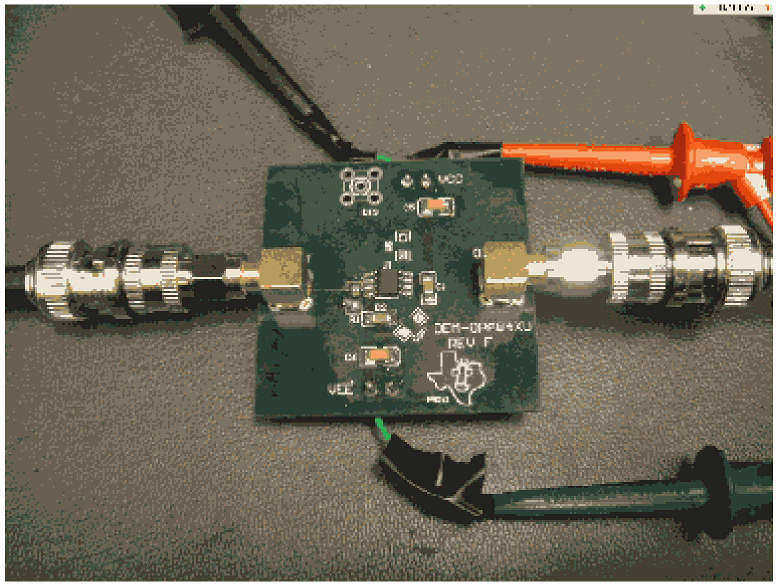
- **350MHz Bandwidth (Gain of +20)**
- **3900Mhz Gain Bandwidth Product**
- **0.85nV/ÖHz Input Voltage Noise**
- **2.5pA/ÖHz Input Current Noise**
- **± 100uV Input Offset Voltage (Typical))**

At the gain of 150, the bandwidth is 26Mhz

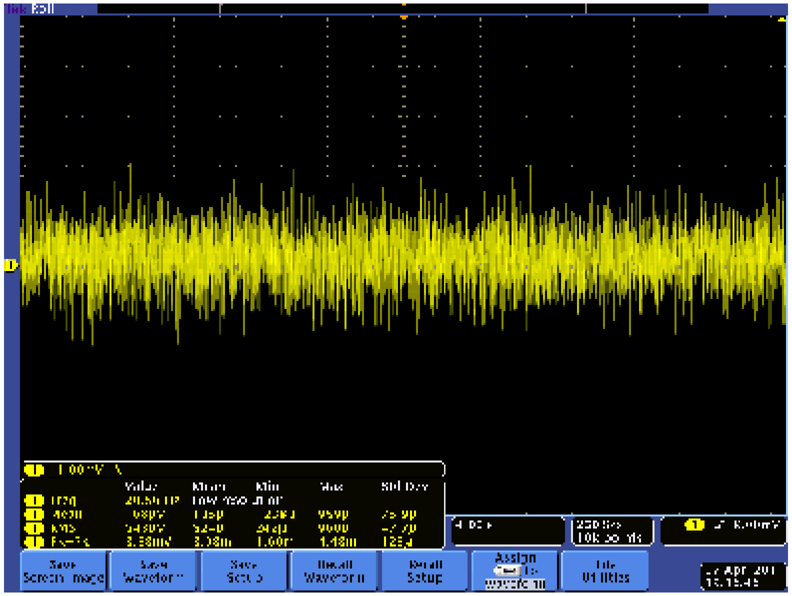


575uVrms post amplifier noise in 20MHz bandwidth.





Post amplifier noise in oscilloscope



STDEV: 518uV
P-P: 6.6*STDEV=3.4mV
40s P-P: 3.88mV

Tested Post Amplfier Noise is:

$$\sqrt{518^2 - 48^2} = 515.771 \text{ uV}$$

Test Result is very close with simulation result 575uV. The difference may come from:

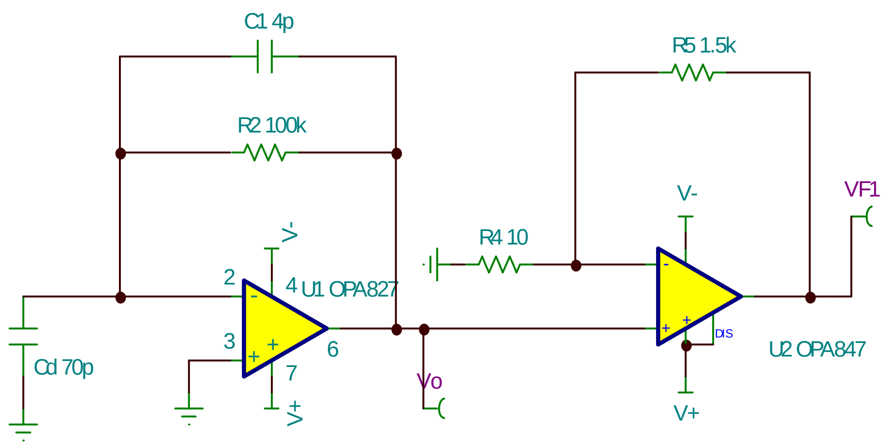
(1) 20MHz Oscilloscope's 20MHz bandwidth limit will also reduce some noise in 20Mhz;

(2) Component value accuracy and variation;

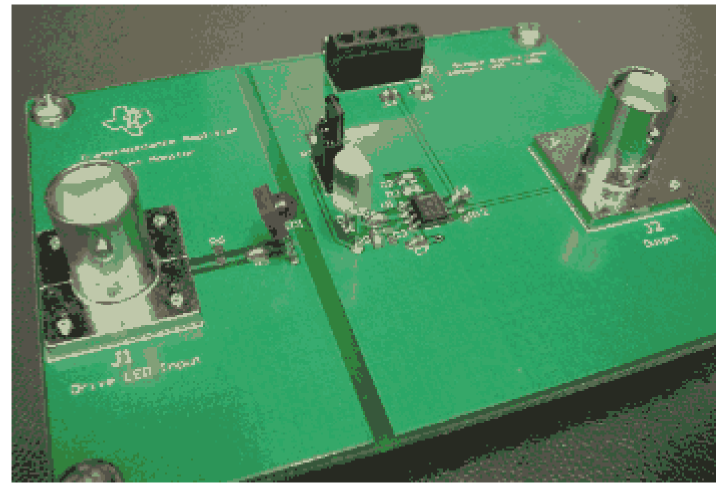
(3) Board parasitic parameter affect.

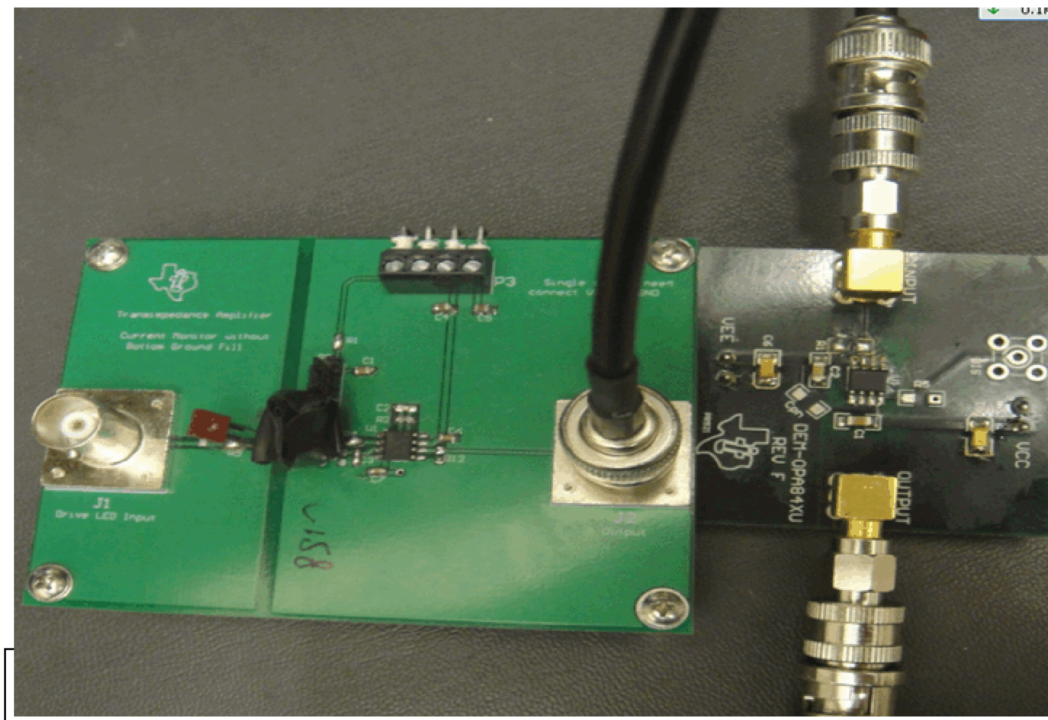
Current Monitor Mode

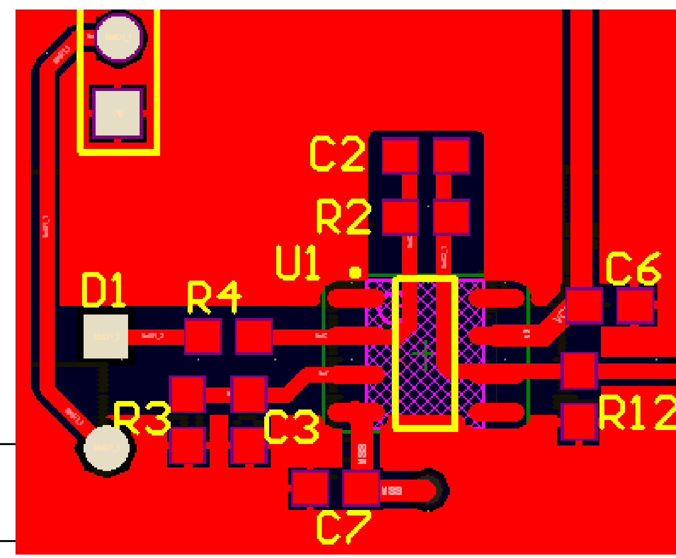
Current monitor



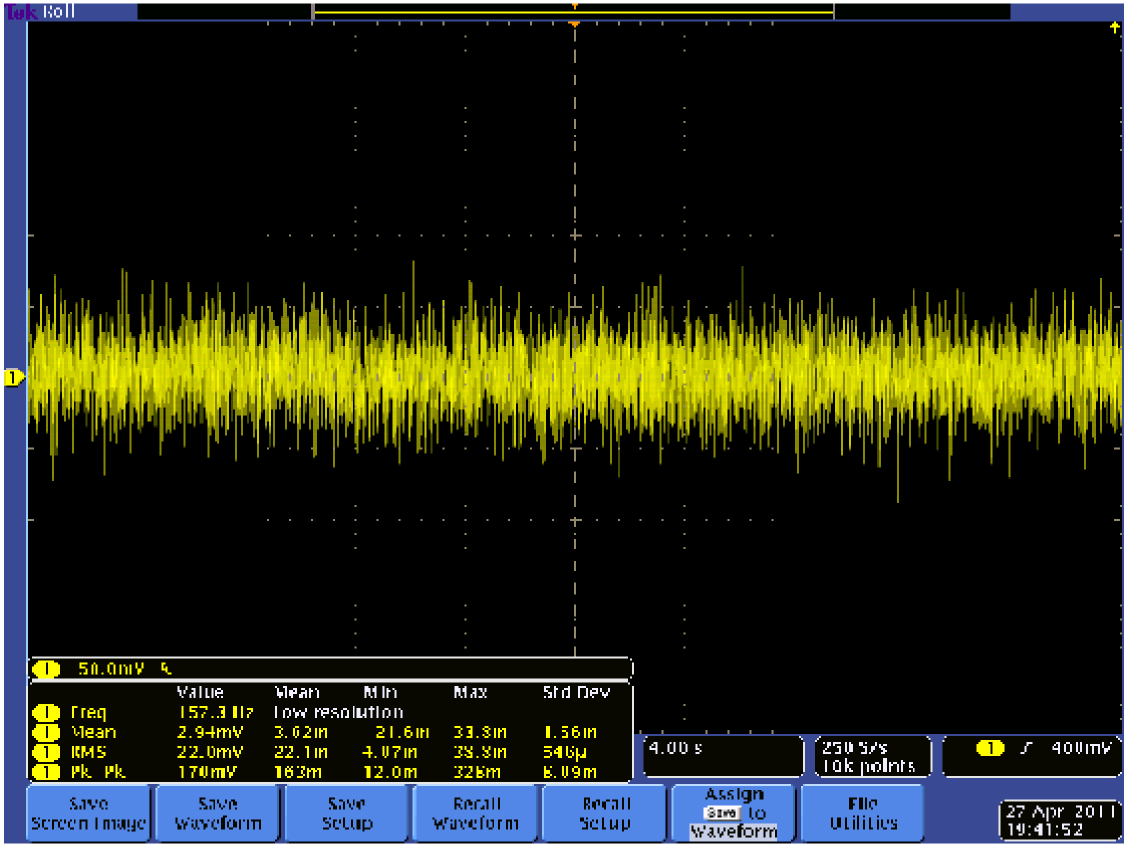
1, Use PDB-C158-ND photodiode, 70pF junction capacitance at Vr=0 V;
2, 100dB C-V gain;
3, 4pF compensation capacitor;
4, ± 5V power supply.







Tested Total output Noise



Tested:

STDEV: 21.7mV

P-P: 6.6*STDEV=143mV

40s P-P: 170mV

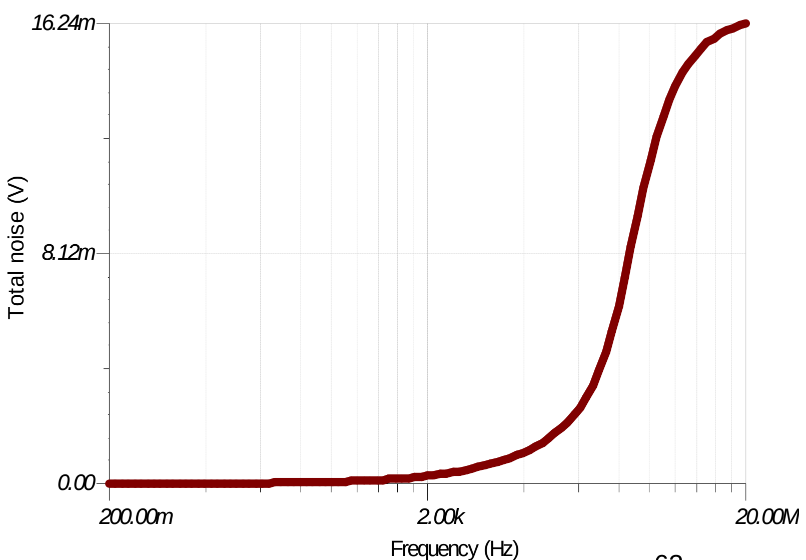
TA output noise:

$$\frac{21.7}{150} = 0.145 \text{ mV} = 145\text{uV}$$

Simulation:

Total output noise: 16.24mV

TA Output noise: 110uV



Noise Hand calculation

Feedback resistor: $R := 100 \cdot 10^{3}$

Compensation Cap: $C1 := 4 \cdot 10^{-12}$ F

Photodiode Junction Cap: $C2 := 70 \cdot 10^{-12}$ F

Amplifier Input Cap: $Copa := 18 \cdot 10^{-12}$ F

Total Cap: $CT := C1 + C2 + Copa = 9.2 \times 10^{-11}$ F

Required bandwidth: $BW_0 := 400 \times 10^{3}$ Hz

Voltage Noise density at 1Hz: $en1 := 10.5 \cdot 10^{-9}$ V/sqrt(Hz)

Voltage wideband noise density: $en := 5.1 \cdot 10^{-9}$ V/sqrt(Hz)

Low frequency noise (1/f) Low frequency: $fL := 0.1$ Hz

Lower frequency noise (1/f) High frequency: $fH := 100$ Hz

Zero Frequency: $fz := \frac{1}{2\pi \cdot R \cdot CT} = 1.73 \times 10^{4}$ Hz

Pole Frequency: $fp := \frac{1}{2\pi \cdot R \cdot C1} = 3.979 \times 10^{5}$ Hz

Amplifier GBW: $fc := 11 \times 10^{6}$ Hz

1/¦Â and Aol cross point frequency: $fi := \frac{C1}{CT} \cdot fc = 4.783 \times 10^{5}$ Hz

Noise Hand calculation

Region 1 Noise: $\mathbf{Een1} := \sqrt{\mathbf{en1}^2 \ln\left(\frac{\mathbf{fH}}{\mathbf{fL}}\right)} = \mathbf{2.76 \times 10^{-8}}$ V

Region 2 Noise: $\mathbf{Een2} := \sqrt{\mathbf{en}^2 \cdot (\mathbf{fz} - \mathbf{fH})} = \mathbf{6.688 \times 10^{-7}}$ V

Region 3 Noise: $\mathbf{Een3} := \sqrt{\frac{\mathbf{en}^2}{\mathbf{fz}^2} \cdot \frac{\left(\mathbf{fp}^3 - \mathbf{fz}^3\right)}{3}} = \mathbf{4.272 \times 10^{-5}}$ V

Region 4 Noise: $\mathbf{Een4} := \sqrt{\left(\mathbf{en} \cdot \frac{\mathbf{CT}}{\mathbf{C1}}\right)^2 \cdot (\mathbf{fi} - \mathbf{fp})} = \mathbf{3.325 \times 10^{-5}}$ V

Region 5 Noise: $\mathbf{Een5} := \sqrt{(\mathbf{en} \cdot \mathbf{fc})^2 \cdot \left(\frac{1}{\mathbf{fi}} - \frac{1}{\mathbf{fc}}\right)} = \mathbf{7.934 \times 10^{-5}}$ V

Voltage output noise:

$$\mathbf{Veo} := \sqrt{\mathbf{Een1}^2 + \mathbf{Een2}^2 + \mathbf{Een3}^2 + \mathbf{Een4}^2 + \mathbf{Een5}^2} = \mathbf{9.605 \times 10^{-5}} \text{ V}$$

Noise Hand calculation

Photodiode current noise: $\mathbf{in1} := 4.5 \cdot 10^{-15}$ fA/sqrt(Hz)

Amplifier input current noise is: $\mathbf{in2} := 0.8 \cdot 10^{-15}$ fA/sqrt(Hz)

Current noise contribute in noise volatge at circuit output is:

$$\mathbf{Vi} := \sqrt{R^2 \cdot \left(in1^2 + in2^2\right)} = 4.571 \times 10^{-10} \text{ V}$$

Resistor Thermal Noise is:

Bolzmann constant $\mathbf{K} := 1.38 \cdot 10^{-23}$ J/K

Temperature: $\mathbf{T} := 300$ K

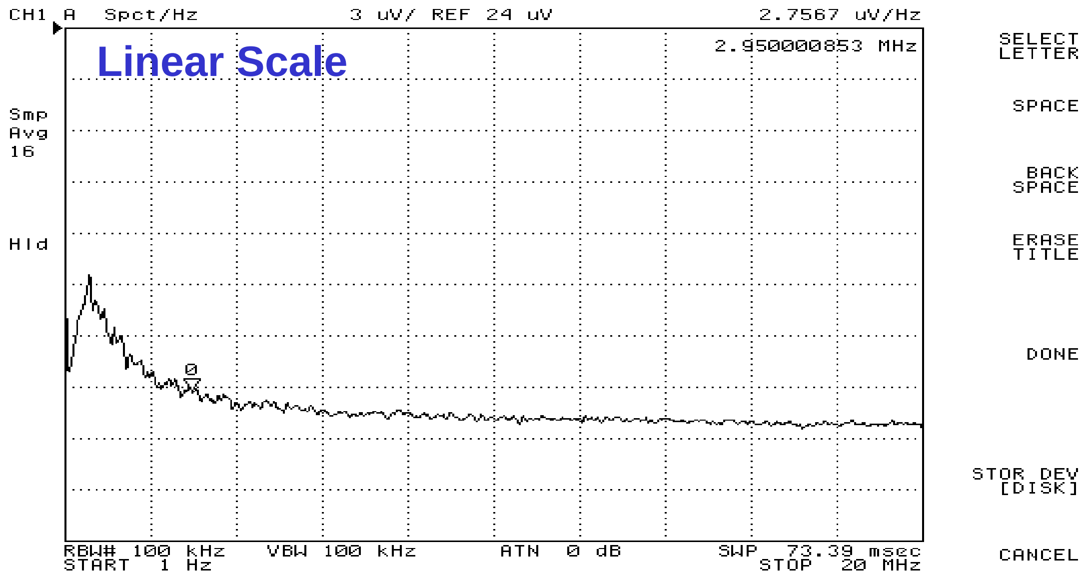
$$\mathbf{Vr} := \sqrt{4K \cdot T \cdot R \cdot fp} = 2.567 \times 10^{-5}$$

Total Output Noise:

$$\mathbf{Vn} := \sqrt{Veo^2 + Vr^2 + Vi^2} = 9.942 \times 10^{-5}$$

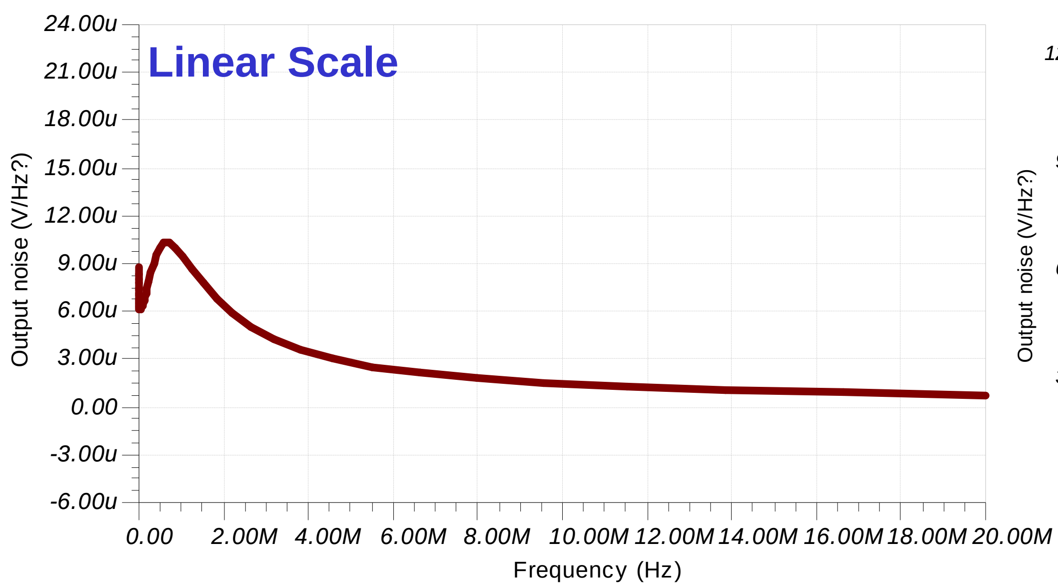
Simulation	Calculation	Test
110uV	99.4uV	145uV

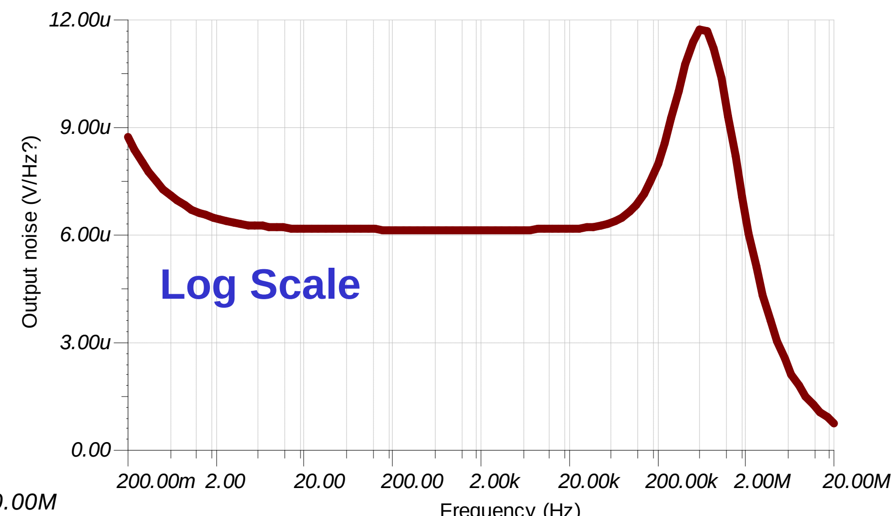
Noise Density



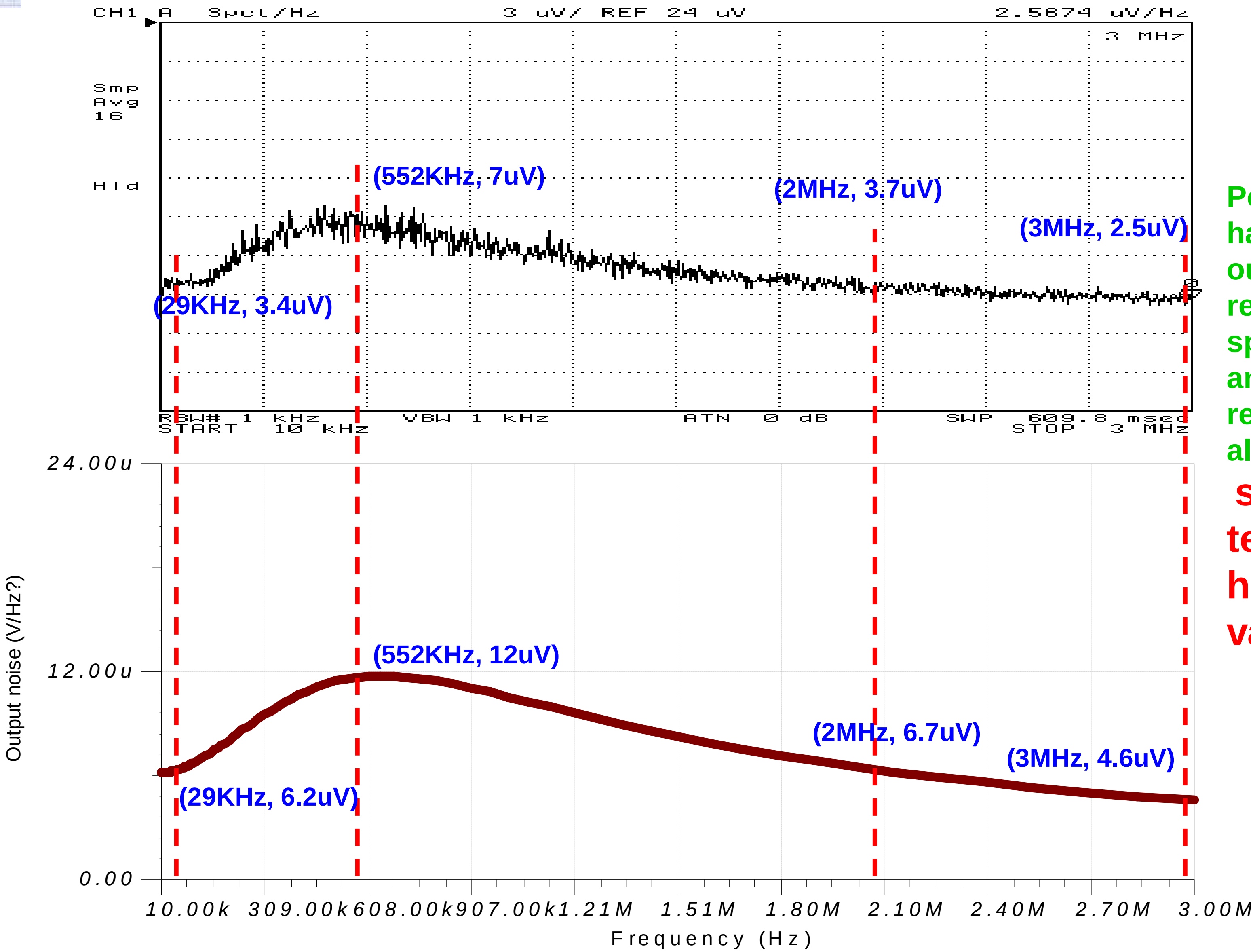
1, Agilent 4395A spectrum Analyzer test 1Hz~20MHz span, 3uV/div, REF=24uV.

2, The tested noise density curve shape is the same as simulation.





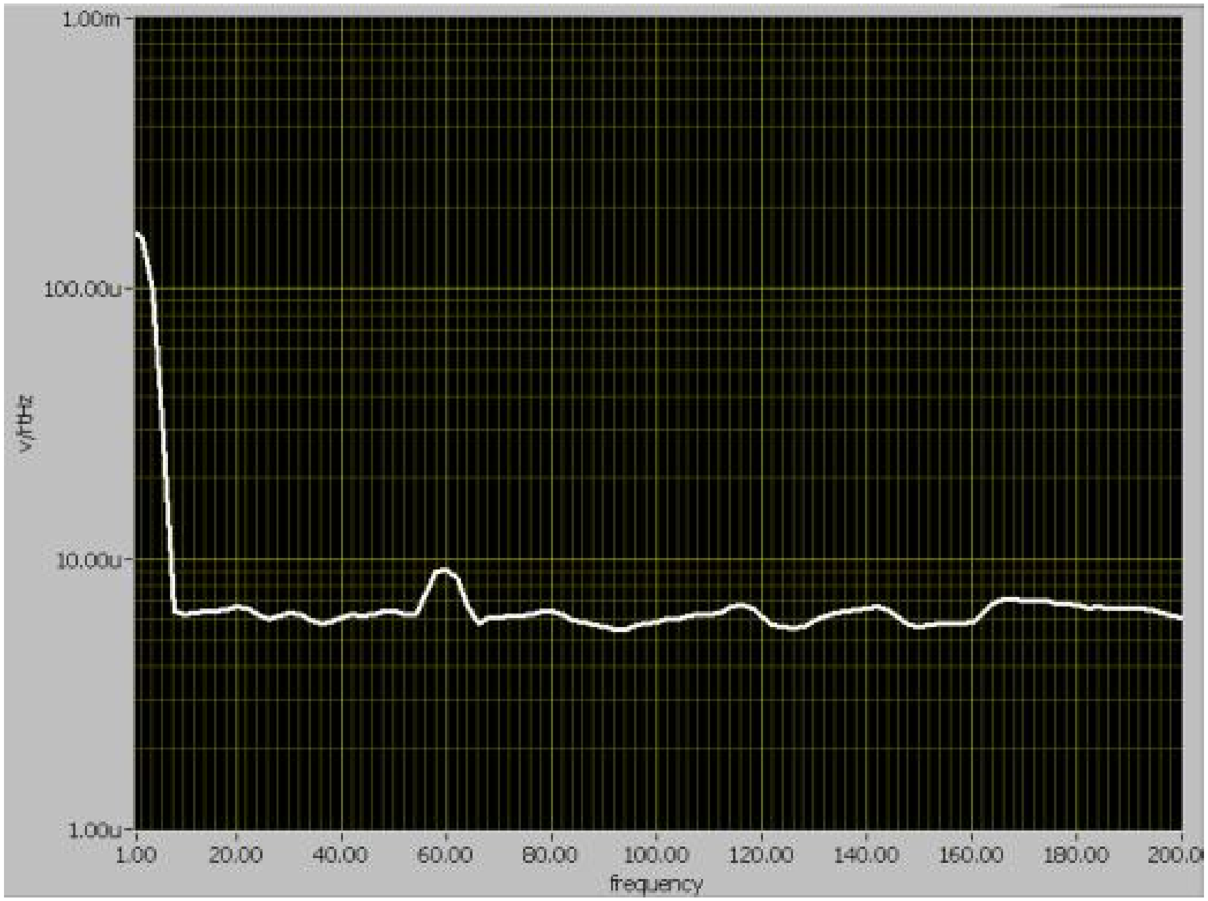
Noise Density



Post amplifier has 50ohm output resistance, spectrum analyzer's input resistance is also 50 ohm,

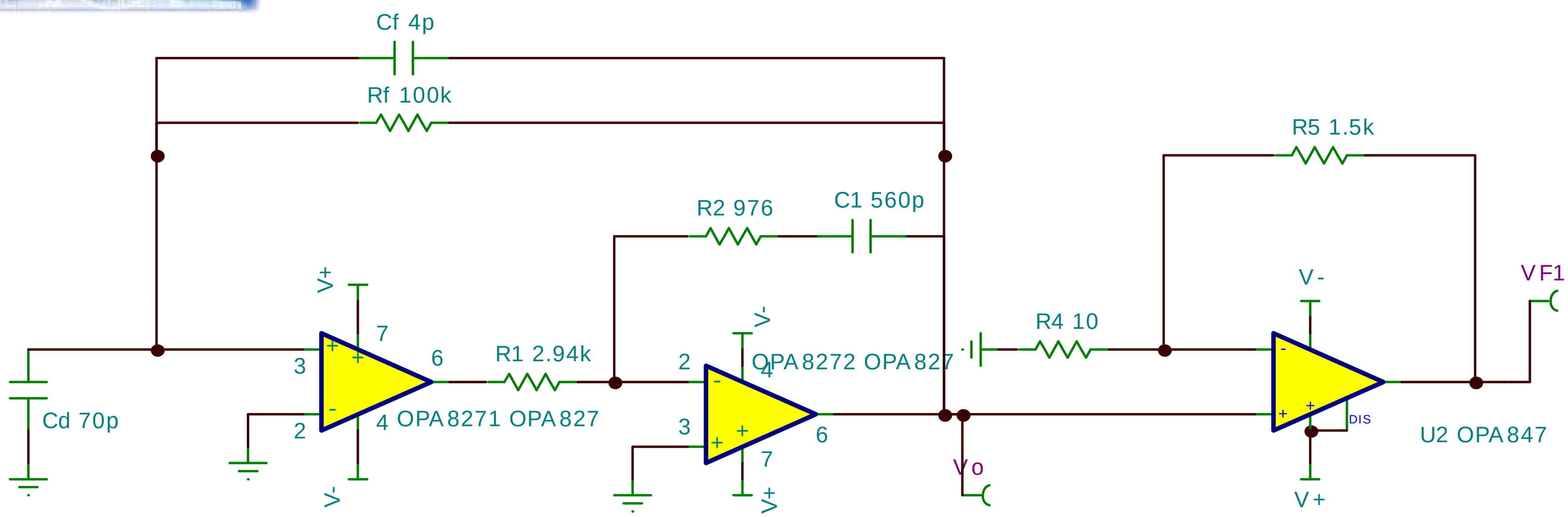
so 4395A test value is half of real value.

Agilent 35670A, 1MΩInput impedance

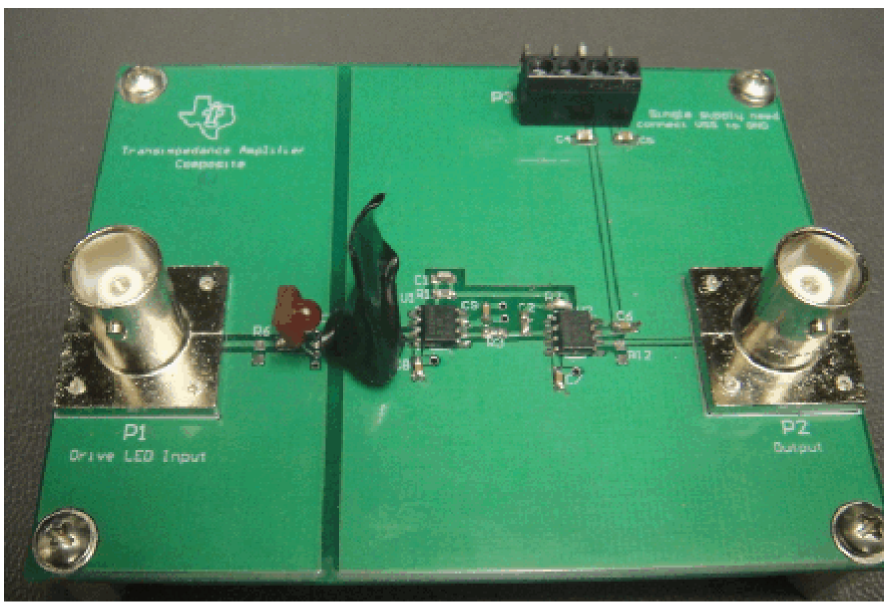


Agilent 35670A Dynamic signal analyzer's input impedance is 1Mohm, From 1Hz to 200Hz, Noise floor is about 6.3uV, almost the same as simulation value.

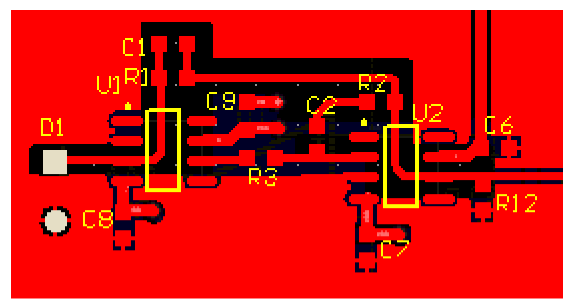
Composite



Cf 4p
Rf 100k
R5 1.5k
R2 976
C1 560p
V+
V-
VF1
7
6
3
2
4
R1 2.94k
R4 10
OPA8271 OPA827
OPA8272 OPA827
U2 OPA847
Cd 70p
Vo
DIS

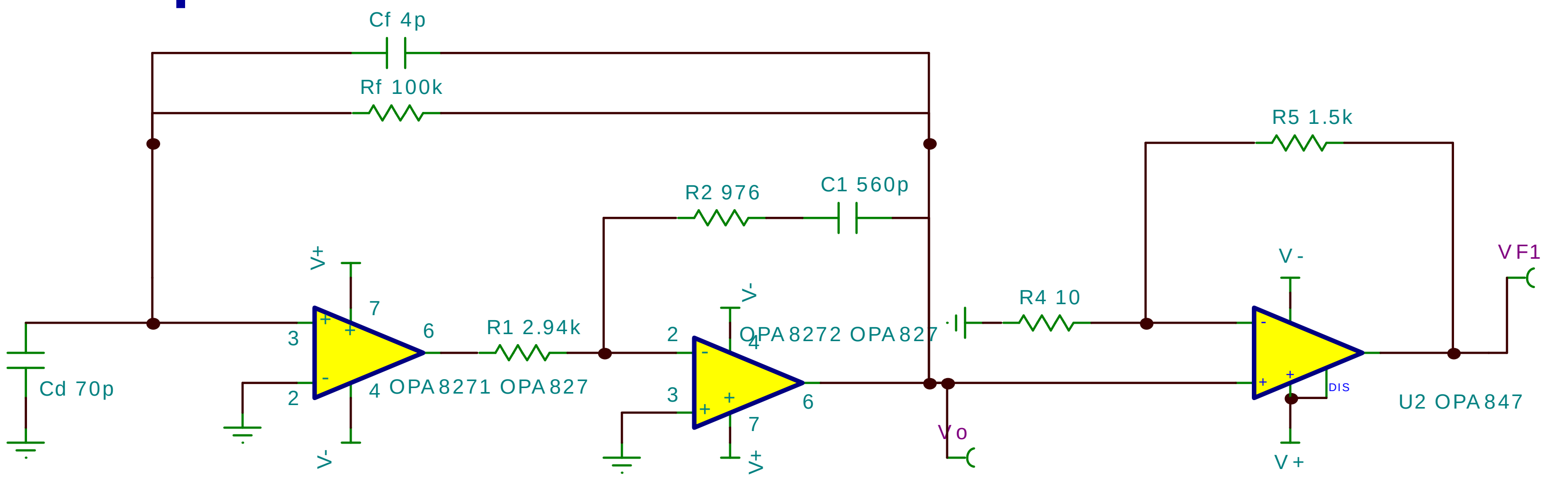


P3
P1
Drive LED Input
P2

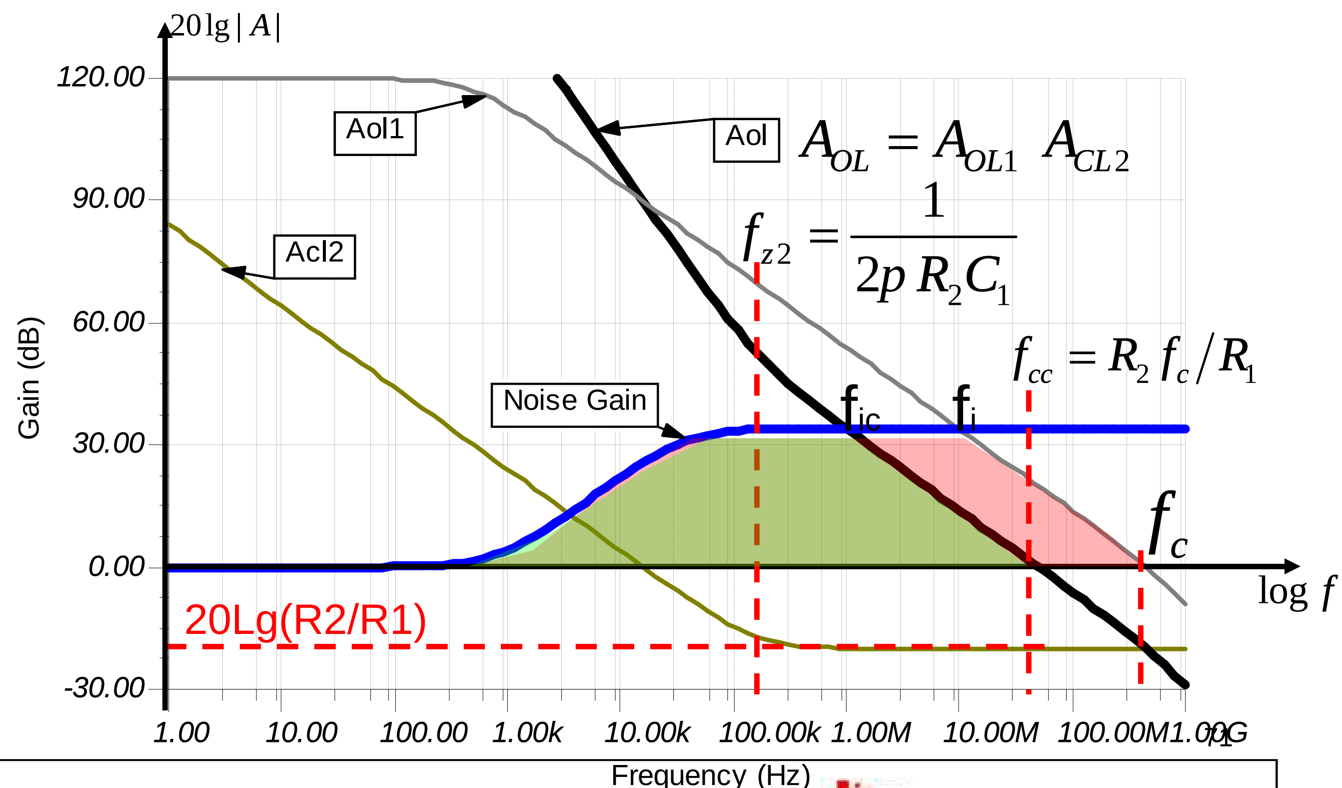


C1
U1
R1
D1
C9
C2
R2
U2
C6
R3
C8
R12
C7

Composite



Using the circuit on right for TINA simulation. the noise bandwidth has been changed smaller. We set R1, R2 and C1 to realize Aol modify.



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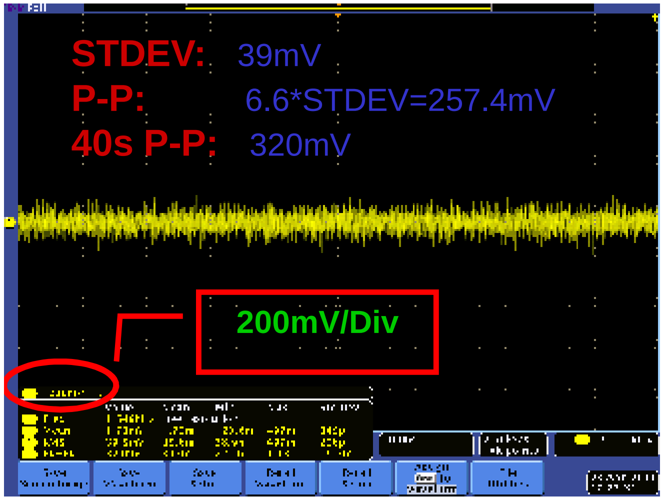
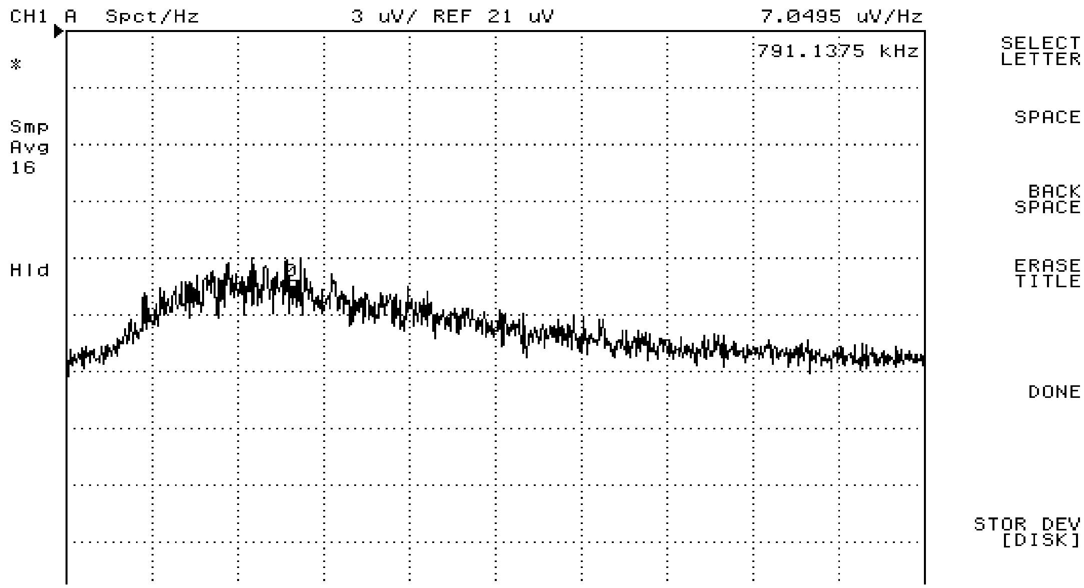
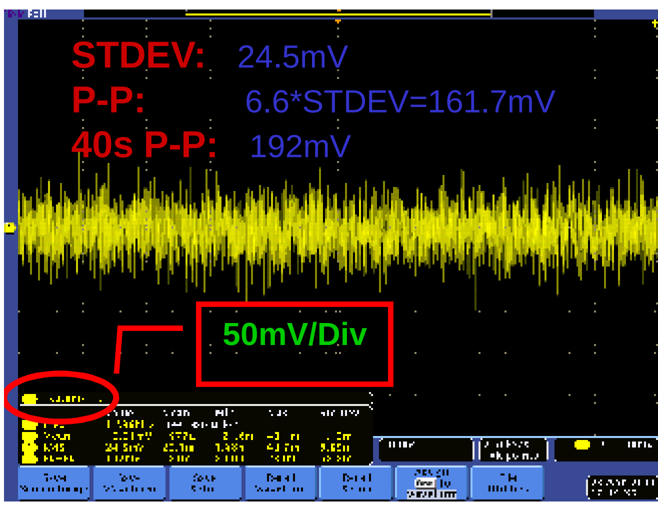
Composite amplifier Noise

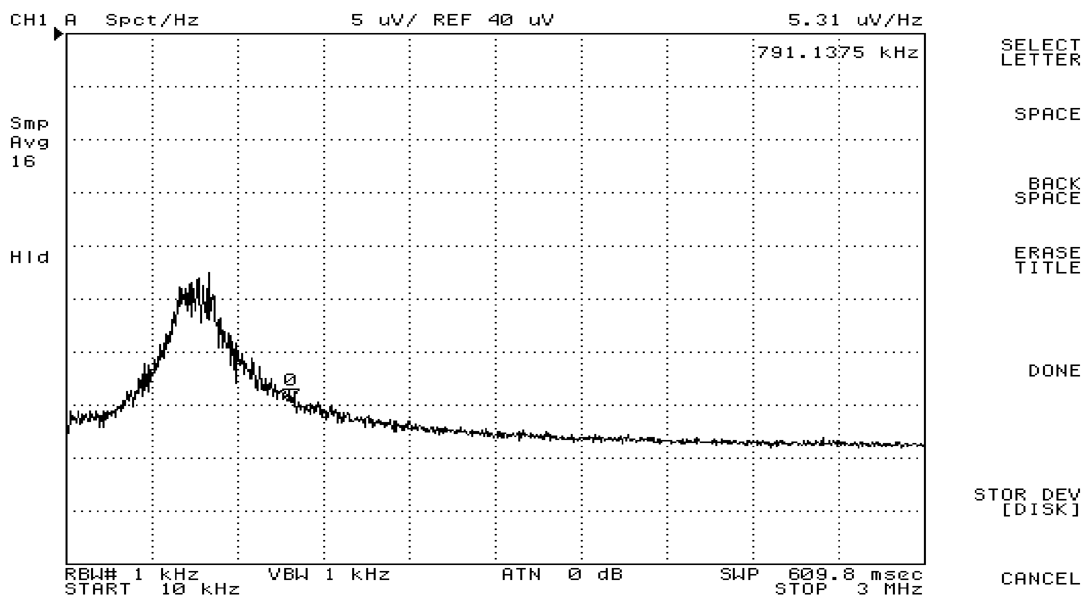
R1=2.9K, R3=2.9K, C2 short



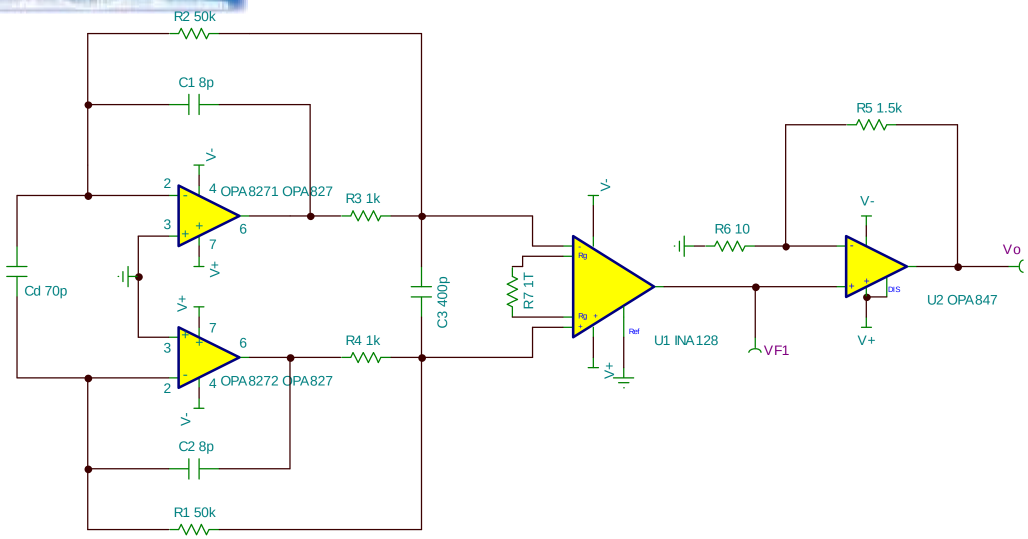


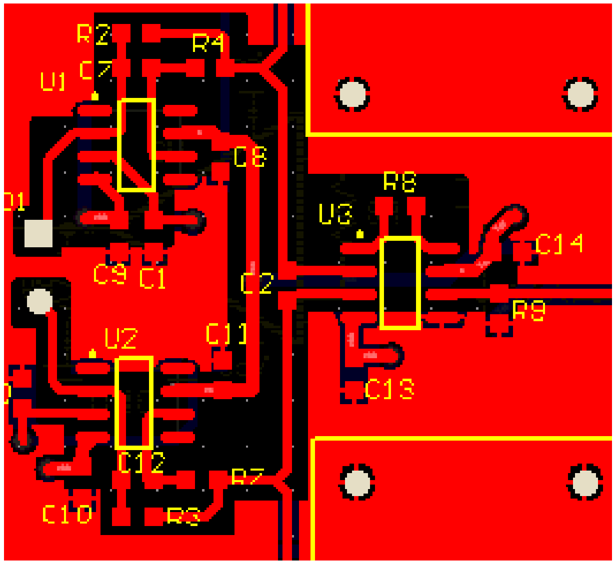
R1=2.9K, R2=K, C1=560pF

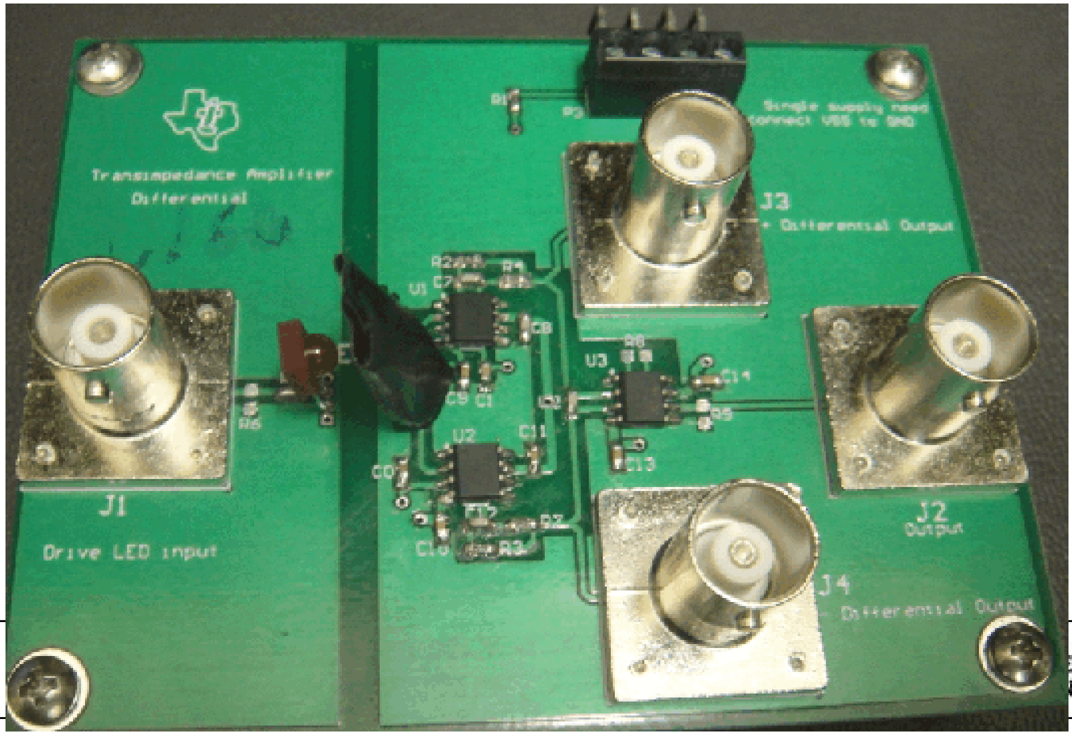




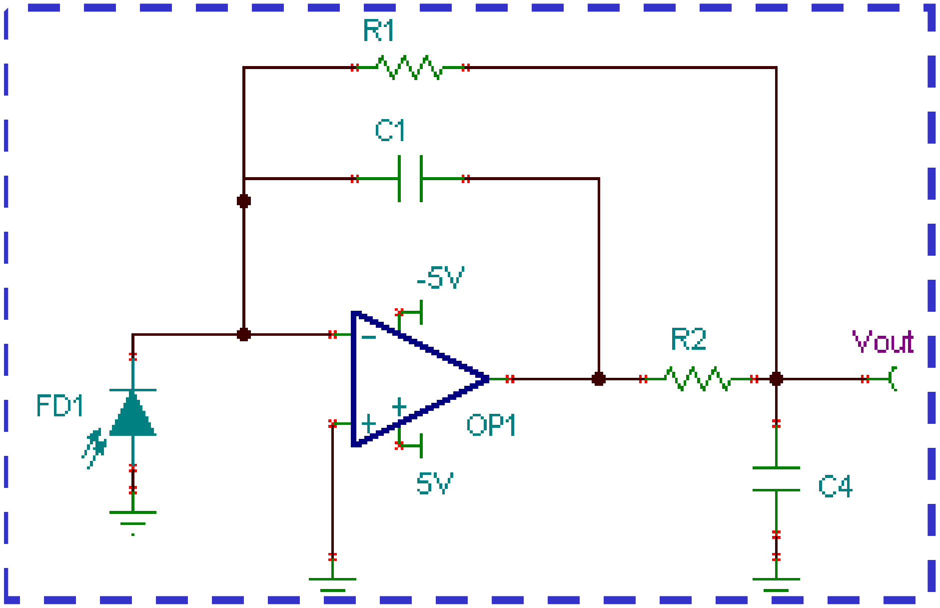
Differential

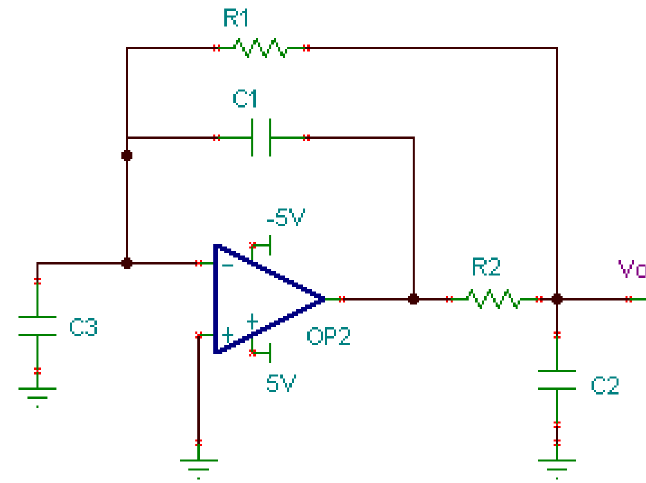






How to Analyze?

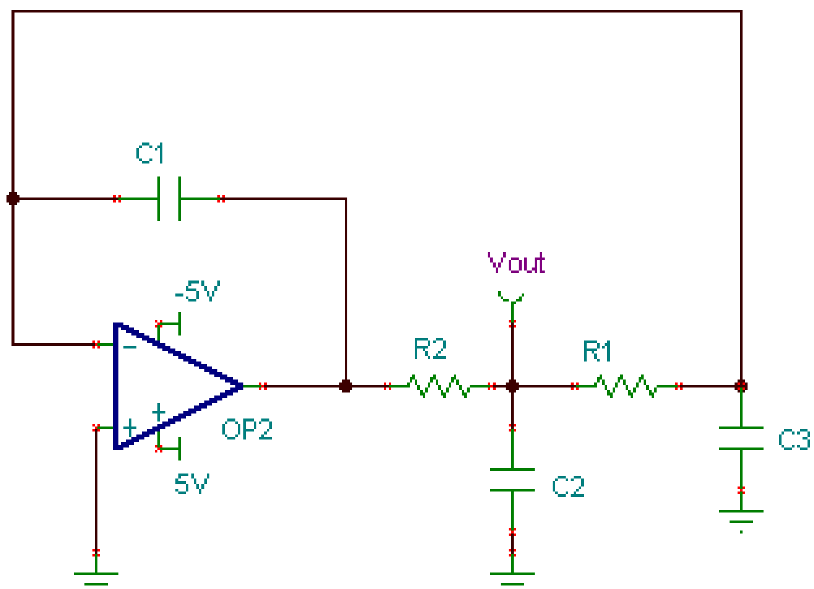




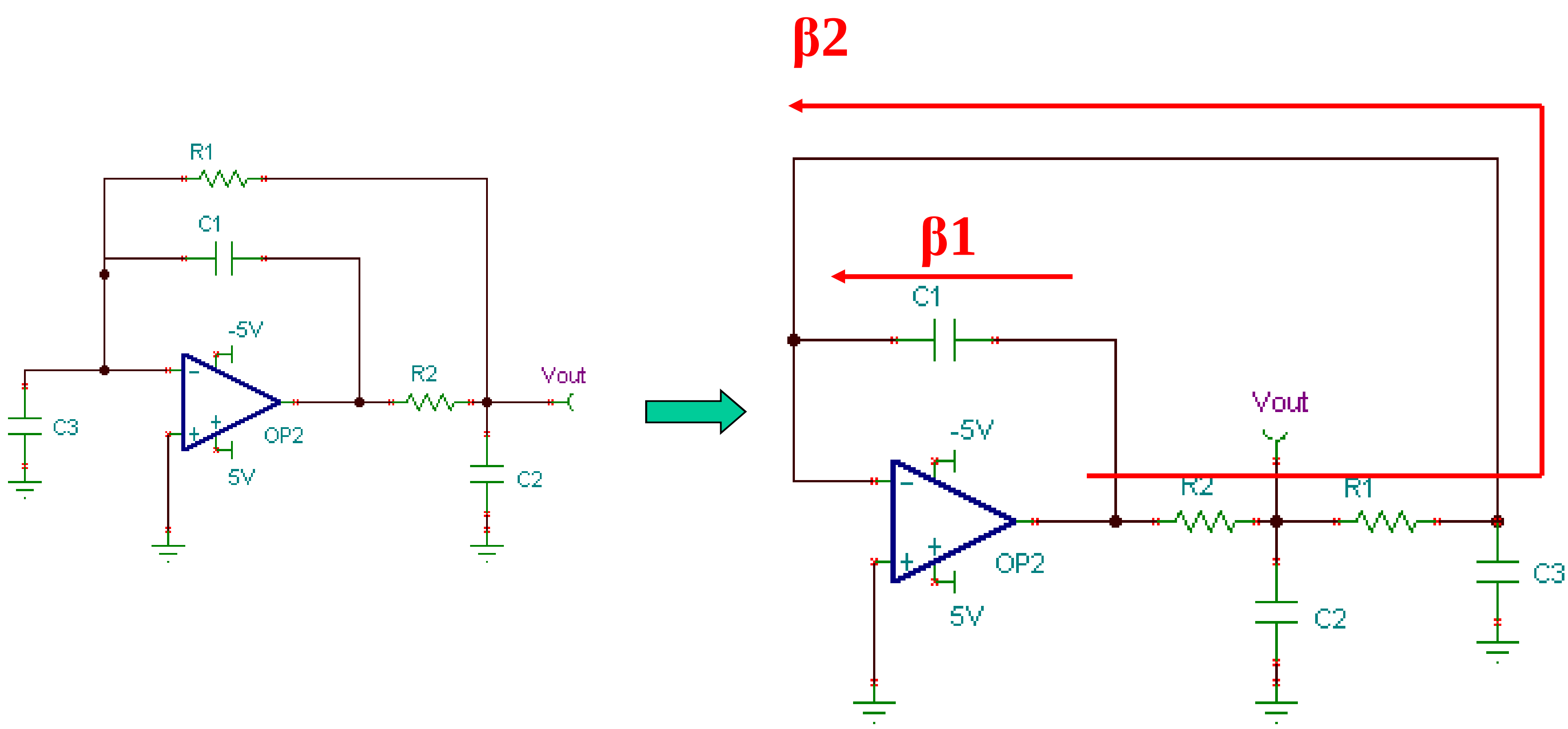
1, Dual feedback circuit usually used in High Cap load application.

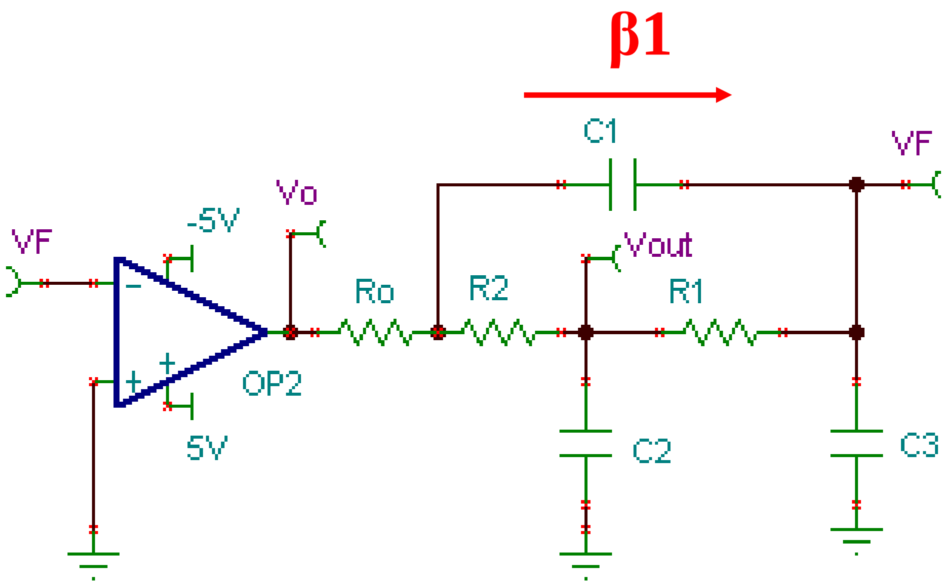
2, Dual feedback is used to compensate close loop phase margin to make circuit stable.

3, But in photo current amplifier application, circuit has very large input capacitance. The circuit is different to normal use.



Dual feedback circuit in PD application





In 1/ β1 Curve:

1), At Low frequency, Vo/VF=1
2), At low frequency, VF is mainly contributed by current from R1. Signal pass R0, R2, R1 C3 to ground, there is a zero created by R0, R2 and R1:

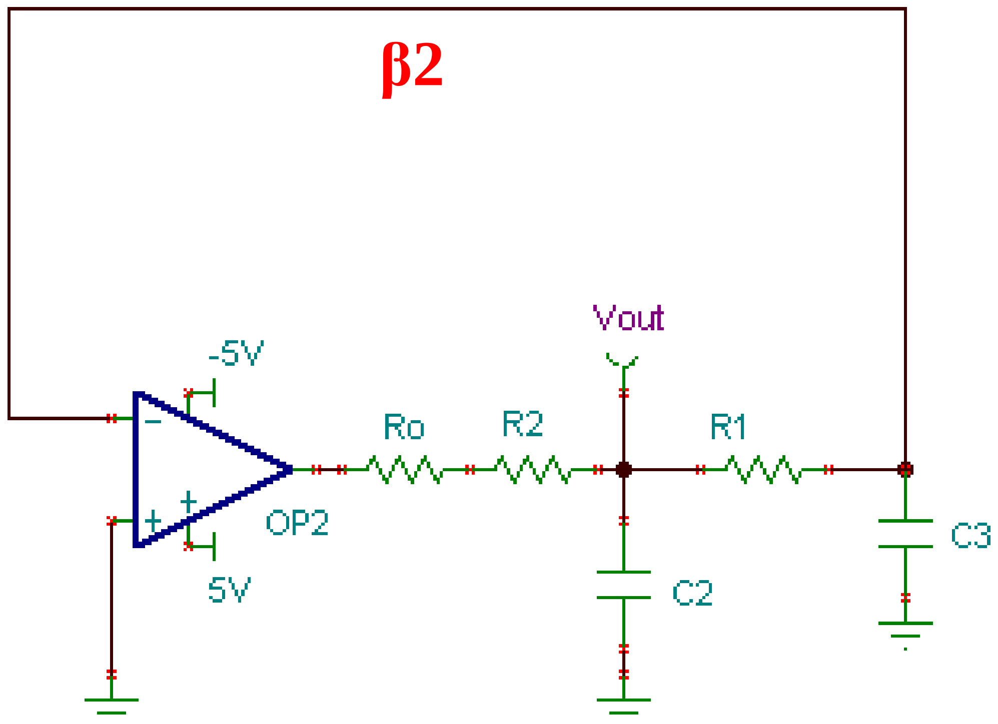
fz=1/[2*pi*(R0+R1+R2)*C3]≈1/ /[2*pi*R1*C3]

3), At higher frequency, C1's impedance decrease, VF is contributed by currents from both C1 and R1. When frequency is higher enough, most current comes from C1, the Vo/VF=(C1+C3)/C1

Pole frequency is:

fp=1/ /[2*pi*R1*C1]

Dual feedback circuit in PD application

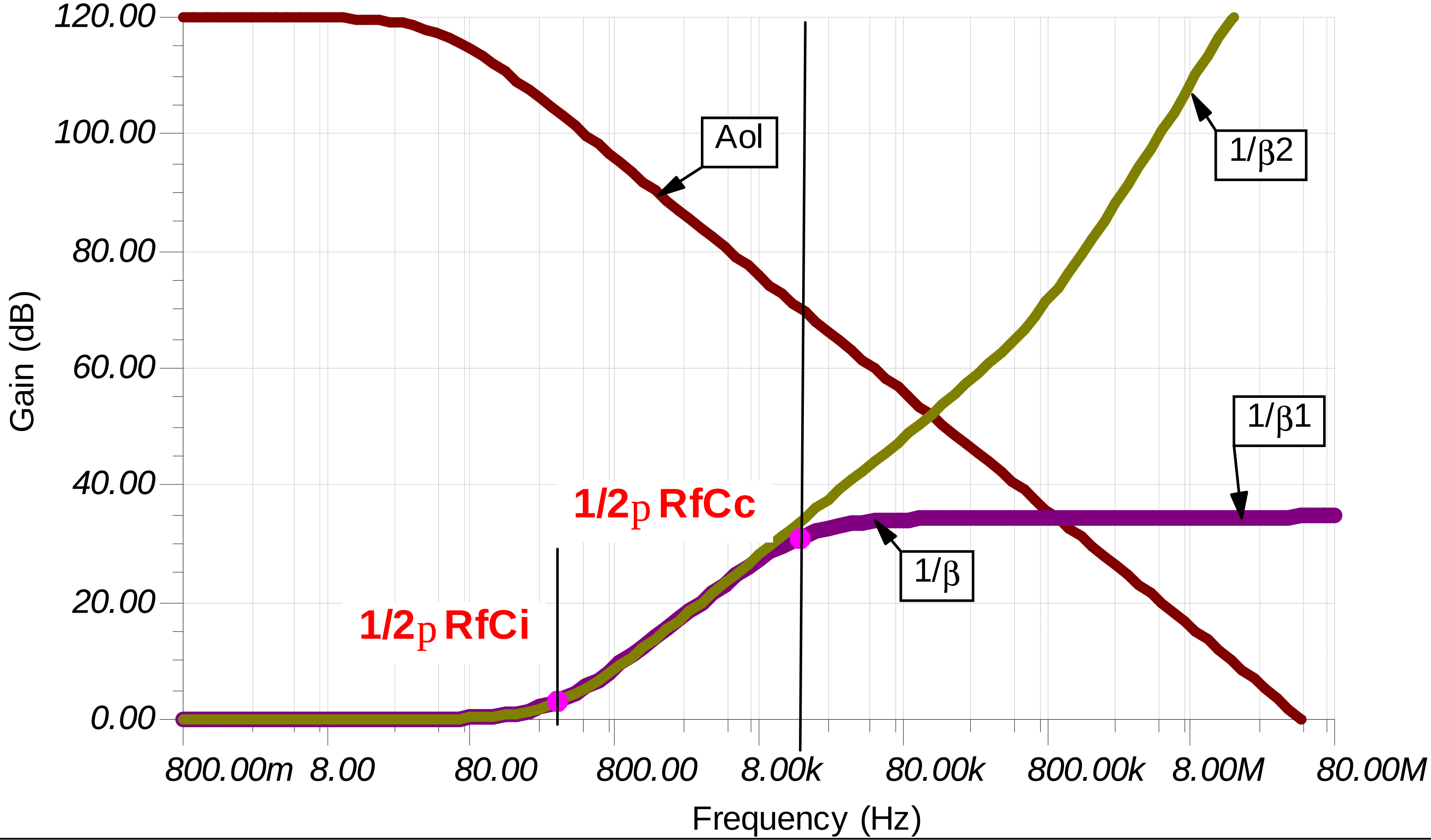


In 1/ β2 Curve

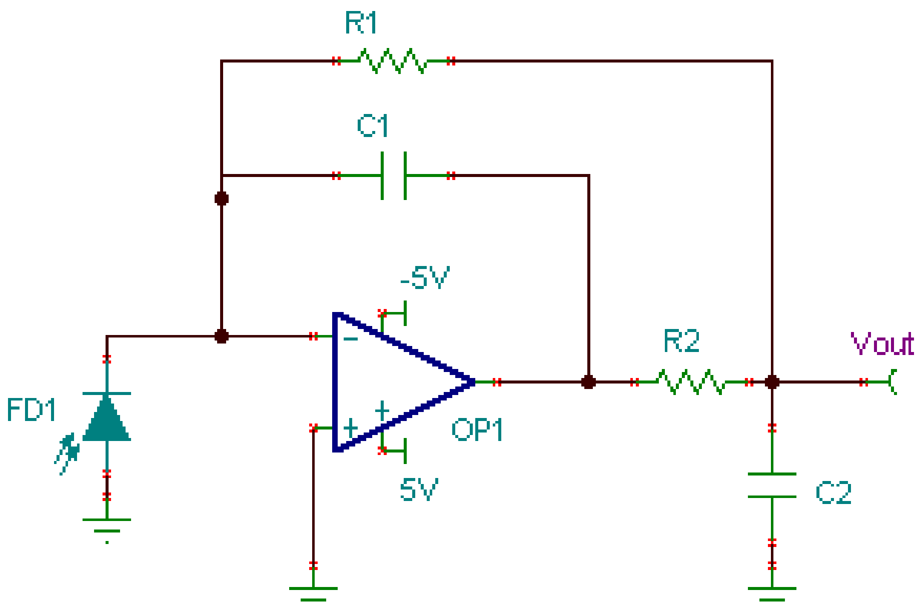
1), Will Create First zero at 1/[2*pi*R1*C3]

2), Will Create Second zero at 1/[2*pi*(R0+R2)*C2]

Dual Feedback, Superposition : The largest β (smallest 1/β) will dominate!

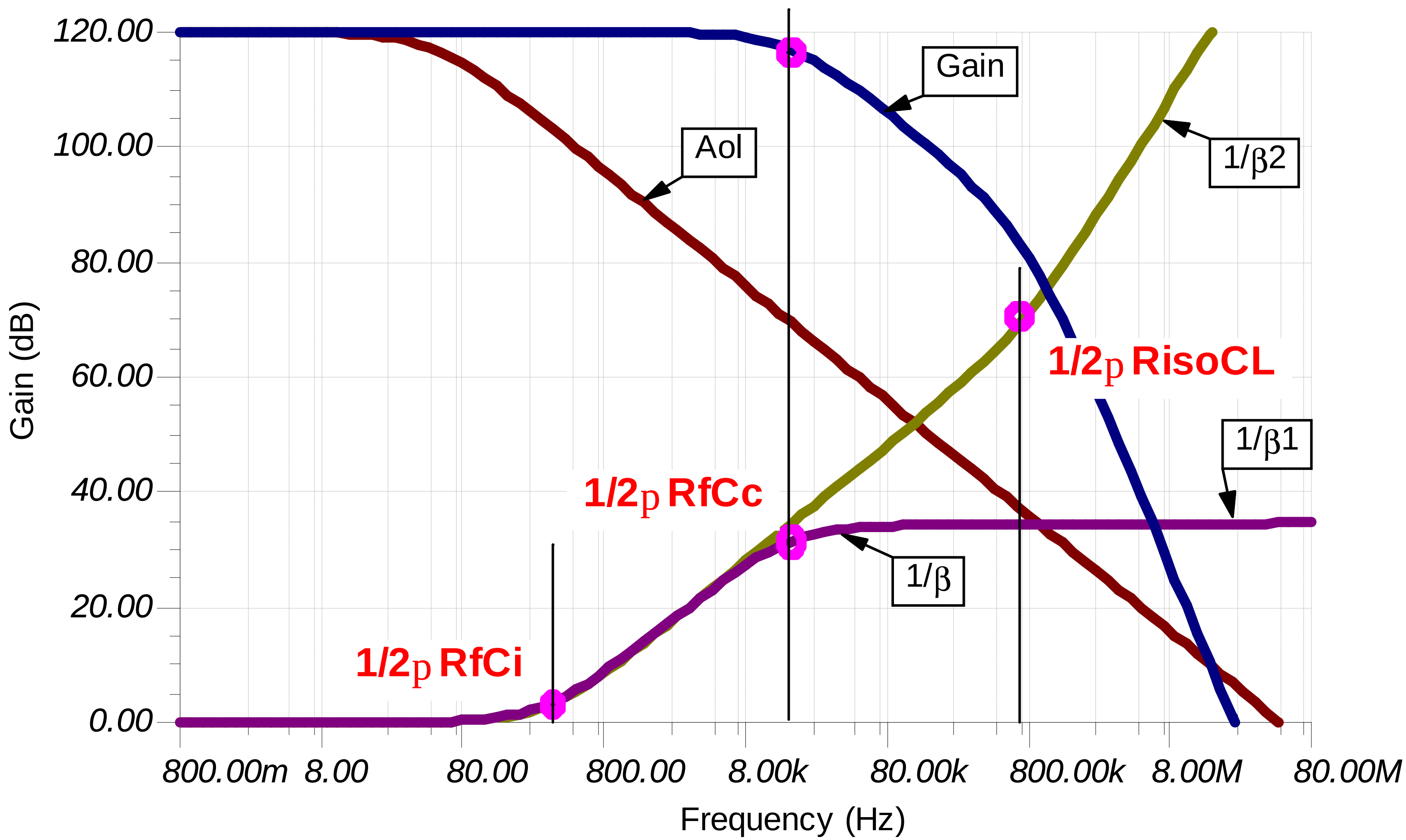


How about Signal Bandwidth?

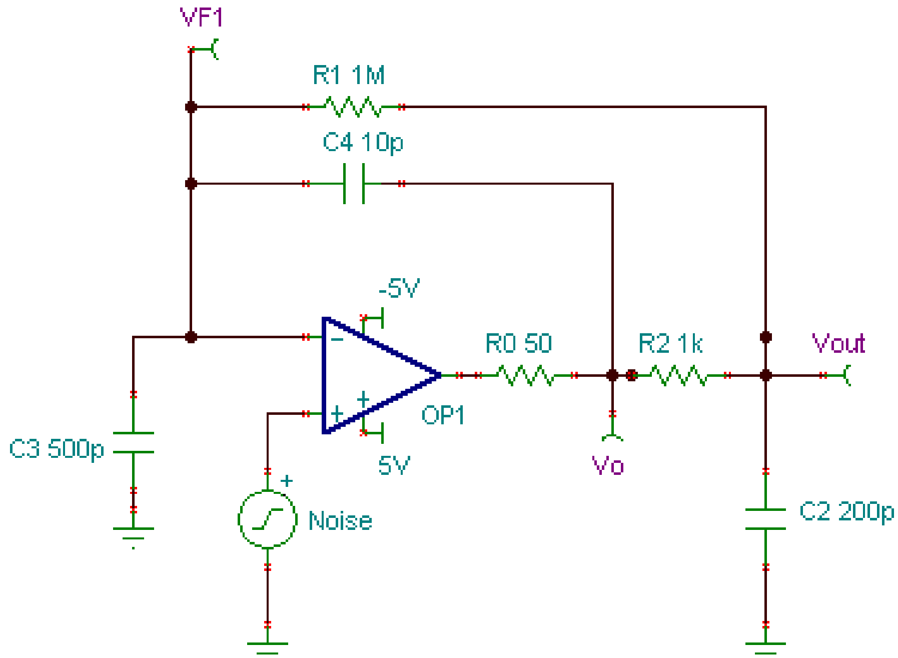


(1) At low frequency, the photo current mainly pass through R1, R1 will dominate the gain.
(2) When frequency goes high, C1 will split more current, so R1 and C1 will create a gain curve pole at:
    fp1=1/(2*pi*R1*C1)

The signal bandwidth is set by R1 and C1


120.00
100.00
80.00
60.00
40.00
20.00
0.00
Gain (dB)
800.00m
8.00
80.00
800.00
8.00k
80.00k
800.00k
8.00M
80.00M
Frequency (Hz)
Gain
Aol
1/β2
1/2p RisoCL
1/β1
1/2p RfCc
1/β
1/2p RfCi

How about Output Noise Gain?

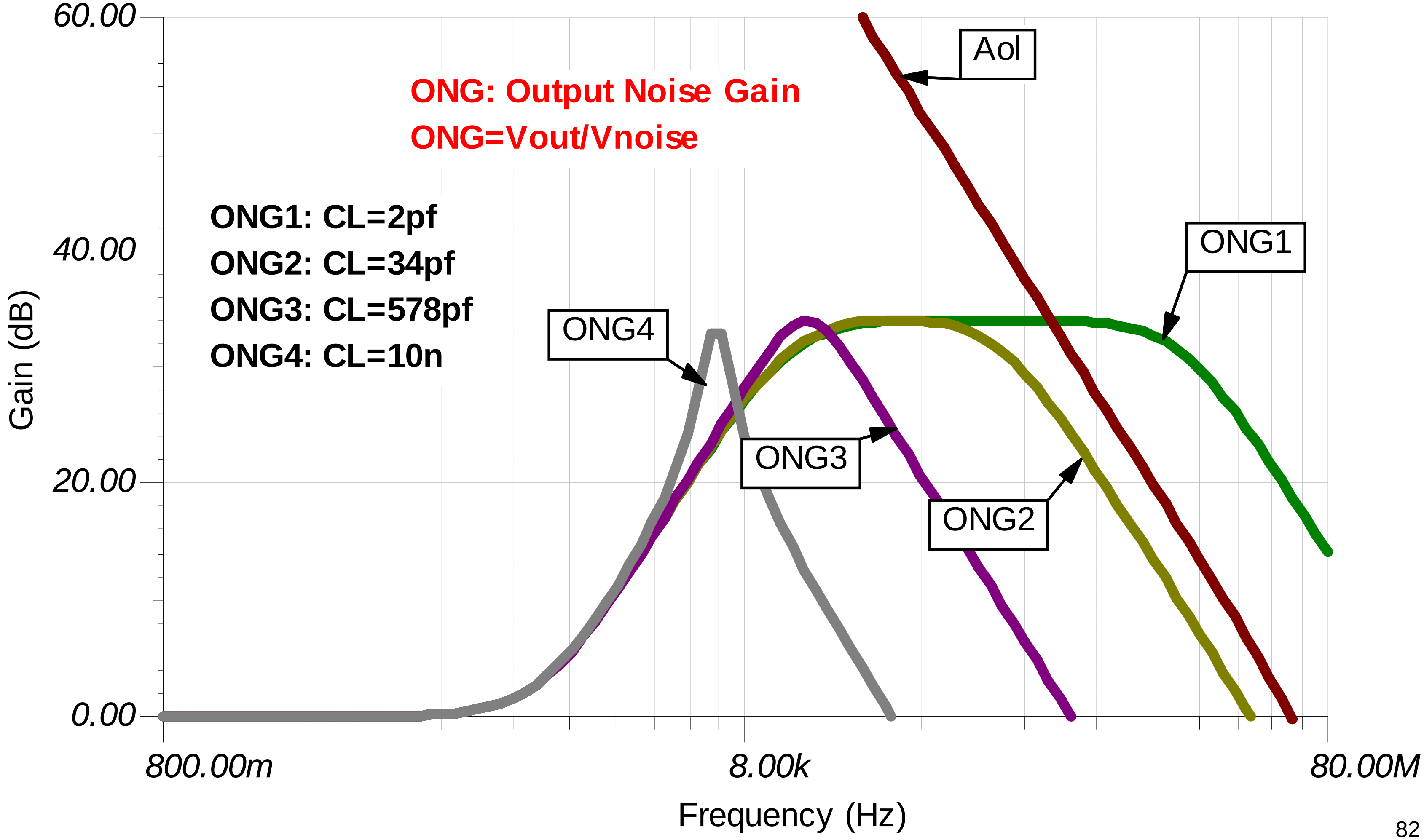


(1) At low frequency, C2 impedance is much larger than R2, the voltage difference between Vo and Vout is small, so the noise gain at vout is restricted by 1/β Curve.

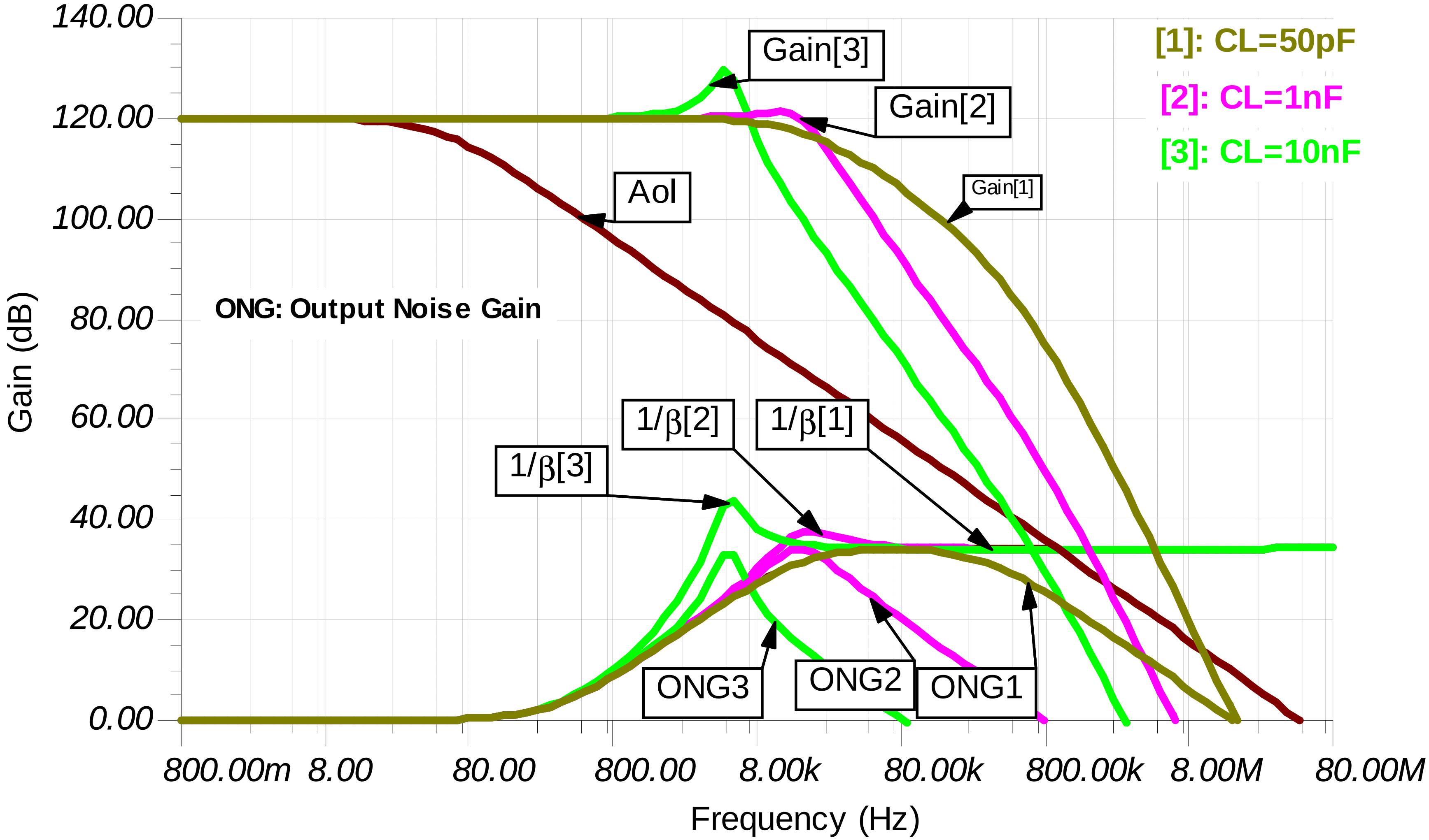
(2) At high frequency, R2 and C2 is a filter which can reduce the noise at -20dB/dec.

(3) The output noise gain curve will **not** be restricted by Aol.

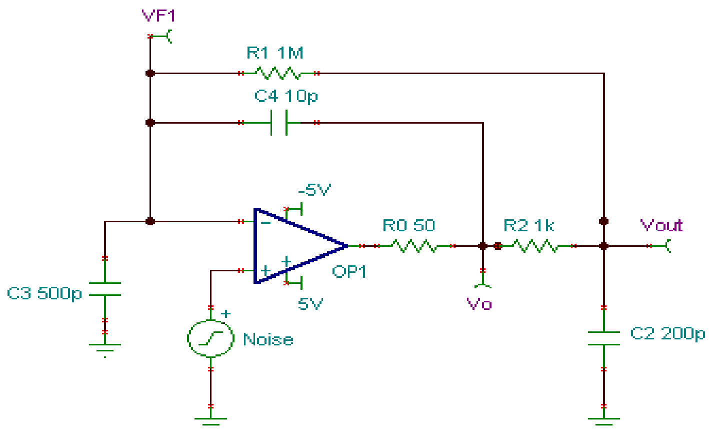
Output Noise Gain



CL vs Gain , 1/β and ONG



How to optimize Riso and CL?

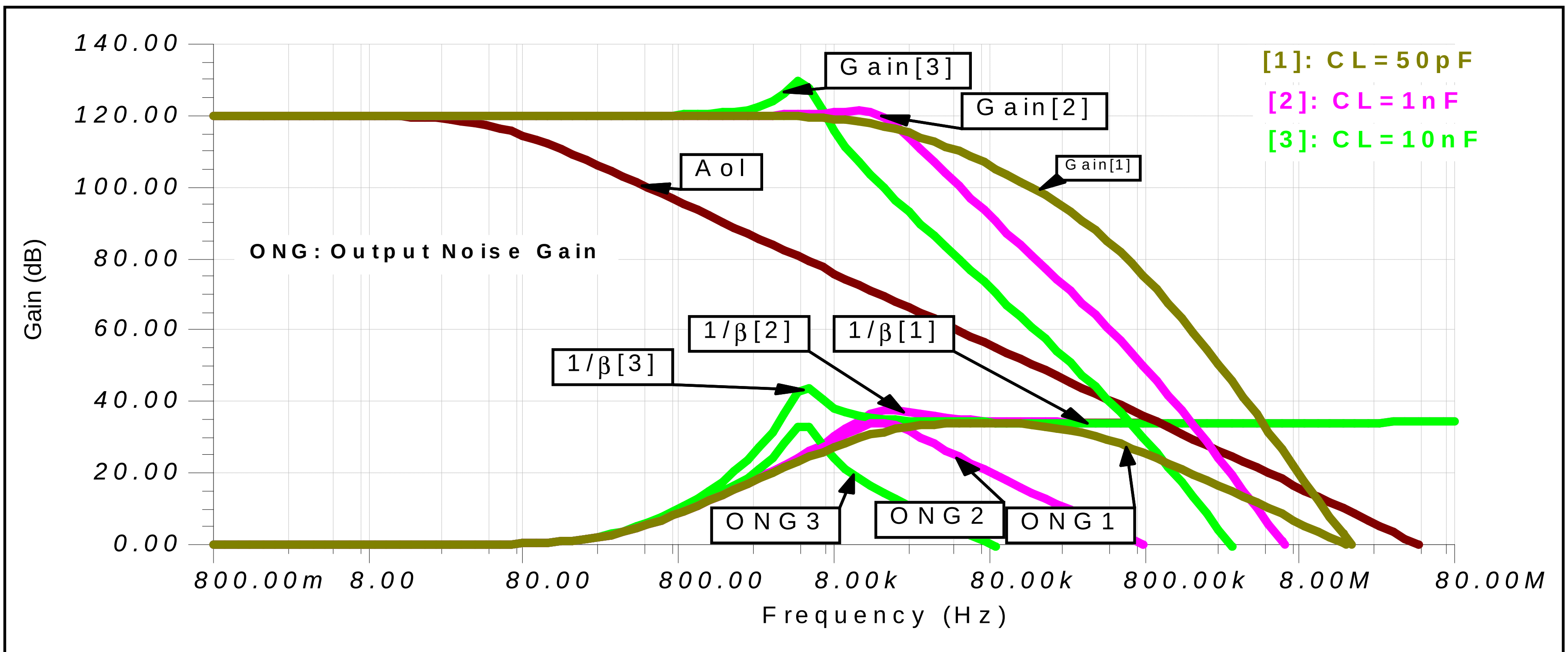


We need Riso and CL as filter in differential circuit to strict noise bandwidth.

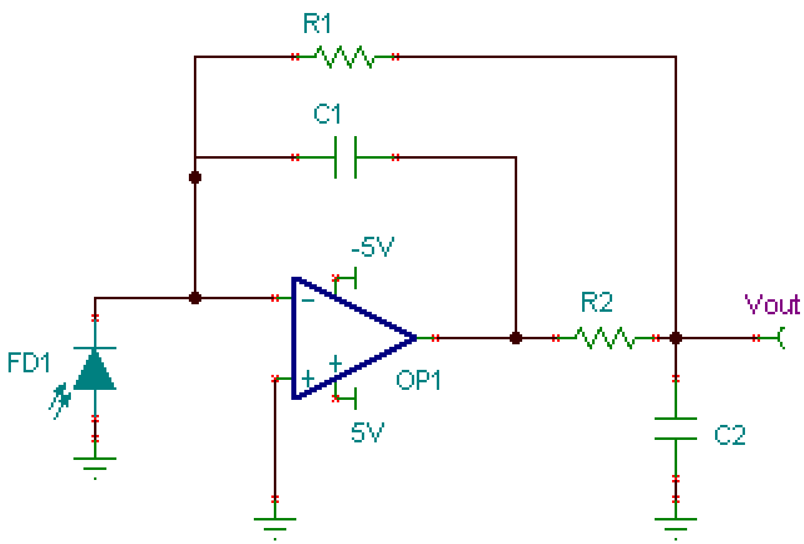
.From simulation we can see, filter ‘s bandwidth can affect signal bandwidth.

In order not to decrease signal bandwidth. we can select:

Riso*CL=Rf*Cc

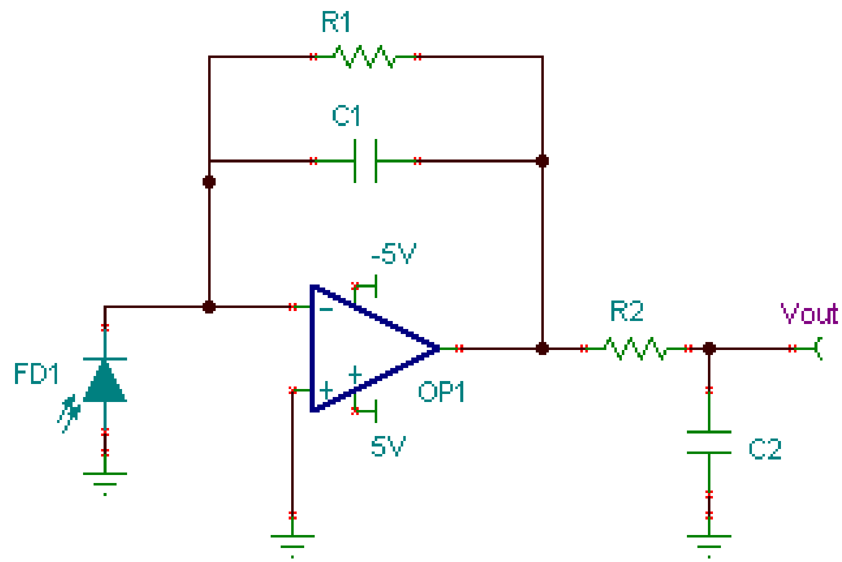


Different?



Dual Feedback

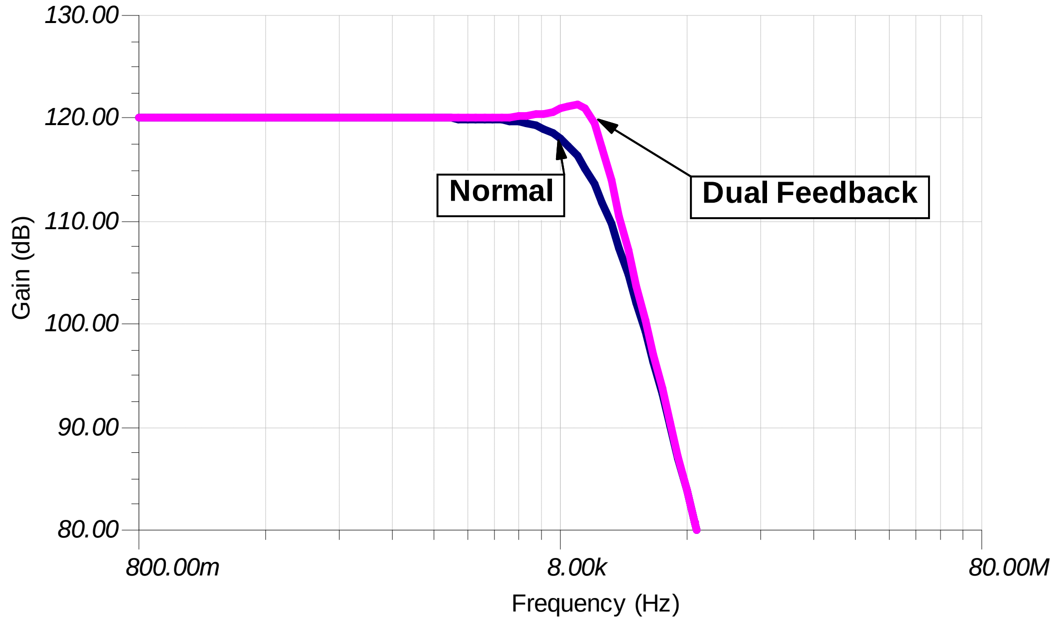
VS



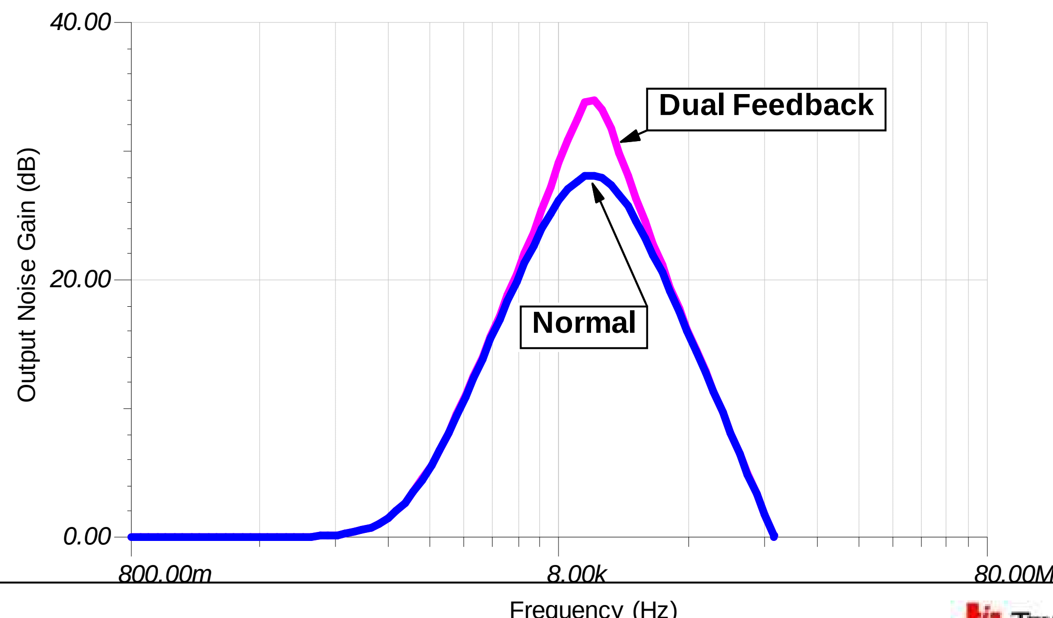
Normal

If R2<<R1, these tow circuits are almost the same.

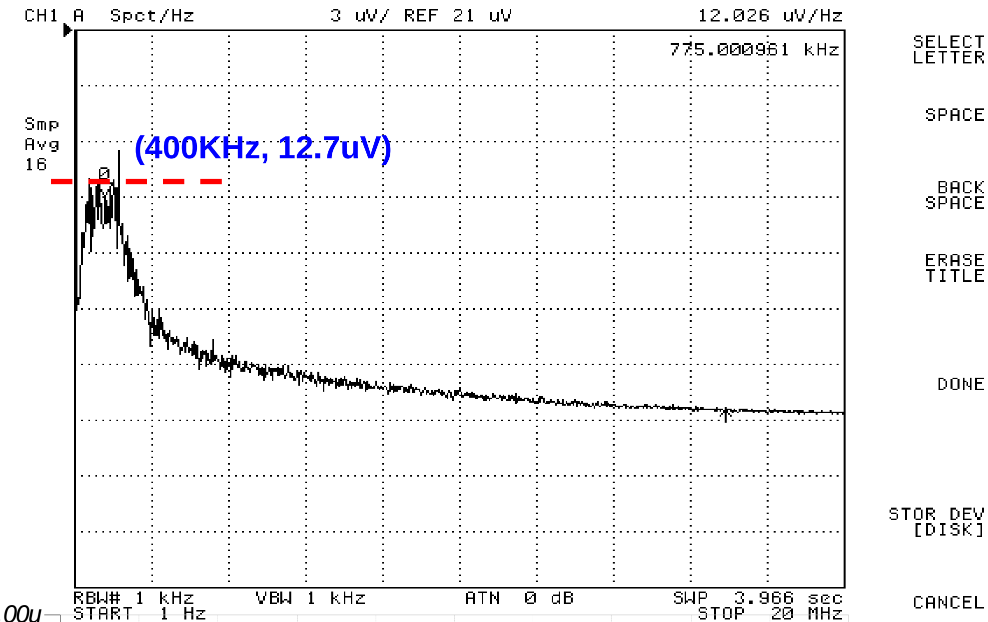
Signal Gain

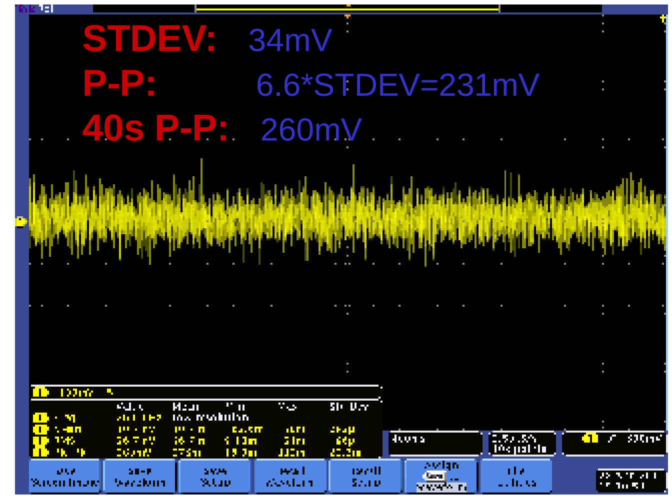


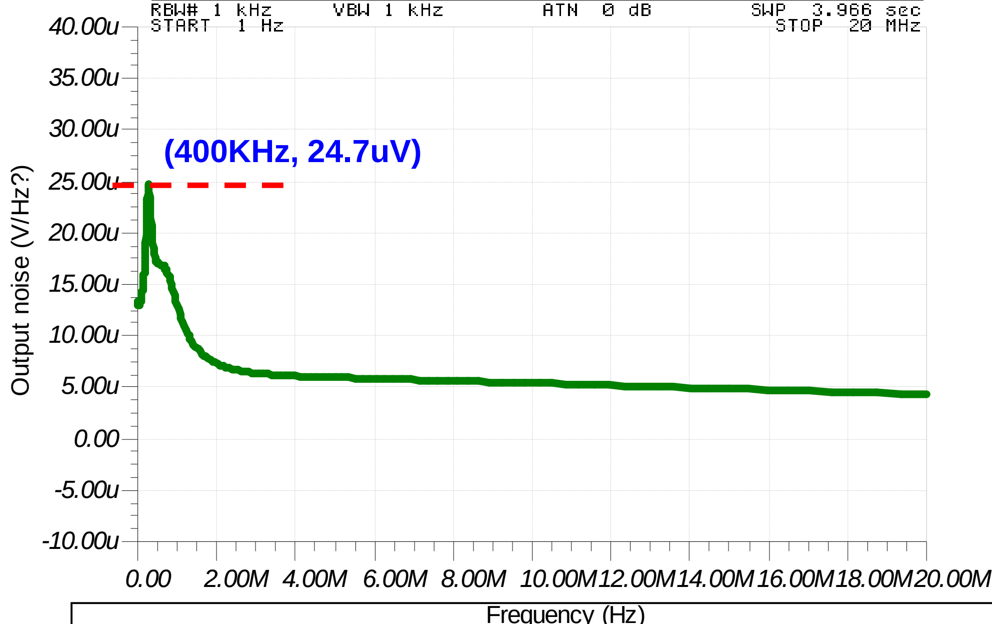
Output Noise Gain



Total Output Noise







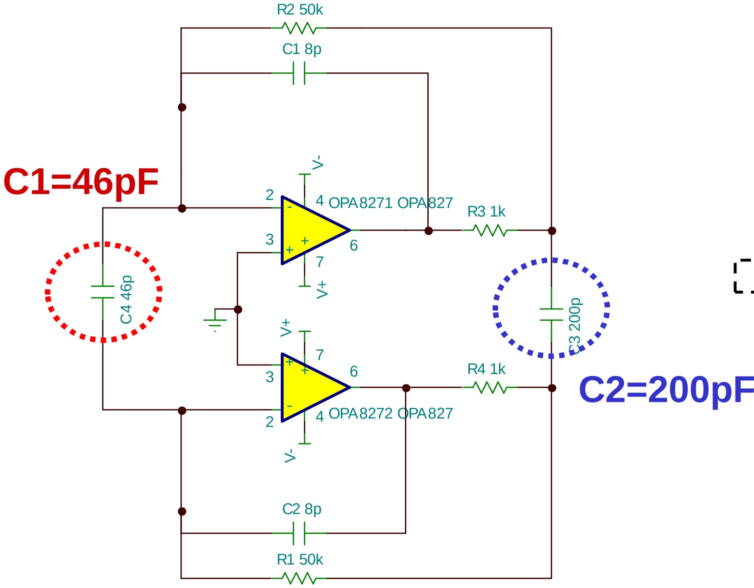
Noise calculation:

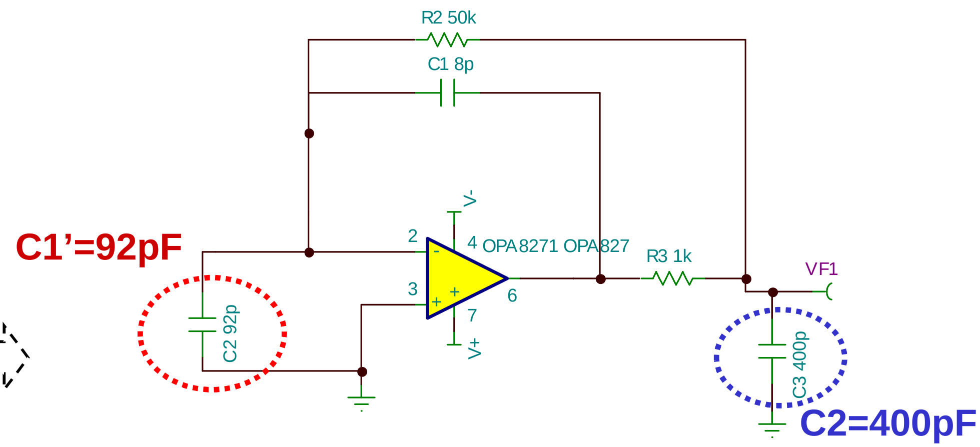
In tina simulation, from 1Hz~20MHz INA128 output noise is: 207uV;

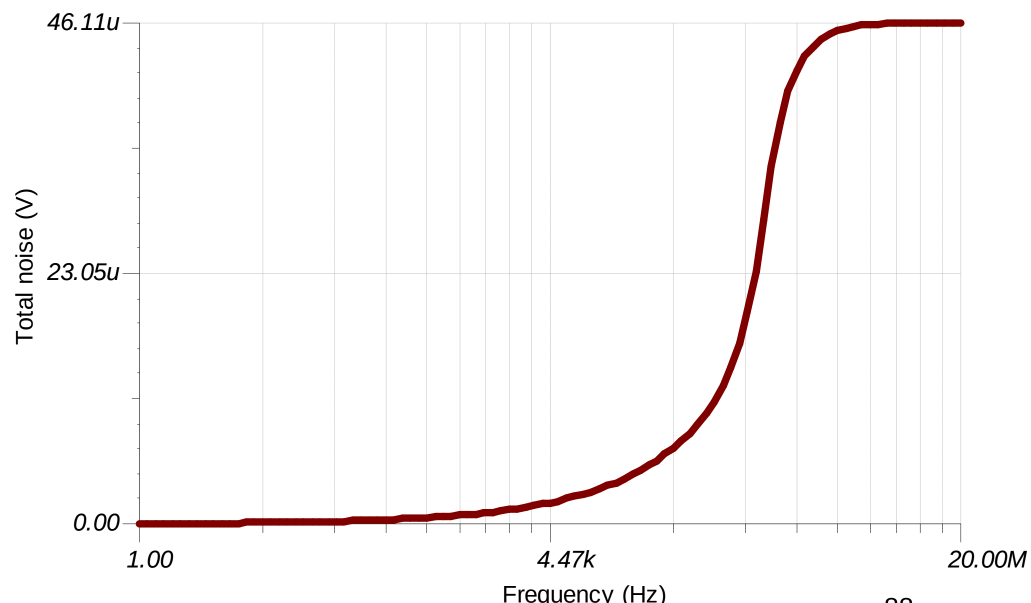
Each differential transimpedance amplifier output noise is:

$$\frac{\sqrt{\left(\frac{34000}{150}\right)^2 - 207^2}}{\sqrt{2}} = 65.302\ \text{uV}$$

Noise simulation







Simulation value: 46uV

Calculation value: 65uV

The difference comes from photo diode junction capacitance value, in simulation we use 46uF, but photo diode junction capacitance will vary with temperature, frequency, bias voltage….

Texas Instruments

References

- Jerald Graeme <Photodiode Amplifiers>
- Art Kay < Op-Amp Noise Calculation and Measurement >
- HAMAMATSU <Photodiode Technical Information>
- Tim Green <Operational amp stability>
- …