



VESA®

VSIS™ Standard

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Video Signal Standard

Version 1, Rev. 1

March 29, 2000

Purpose

To establish the standard analog video signal characteristics of today's graphics cards and display monitors.

Summary

To date, the graphics controller output signals that drive the display monitor have not been well-defined. H and V sync signals are defined only as TTL. The display side has the same problem, as each design may have been optimized to correct for certain signal deficiencies from particular graphics controllers. This document will lay the groundwork that both graphics controller and monitor designers can use to achieve compatible designs.

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Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

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Revision History

Version 1.0 -- September 1999

Initial release of the standard

Version 1, Rev. 1 -- March 2000

1. Removed pre-shoot definitions from Figure 3
2. Added definition of overshoot and undershoot
3. Redrew Figure 3 to eliminate pre-shoot
4. Removed Fig 8.
5. Fig 5 Note: Vmax missing could not add
6. Fig 5. Note: Vmin missing could not add
7. Note (d) added--see figs. 2 and 3.
8. Added to note (a) section 2.3 Min/max Luminance taken at Steady state values Fig 3.
9. 2.4 Test circuits VSWR correct to 1:2:1.
10. 2.6 Jitter measurement Definition : add at end "see fig. 6 also".
11. 2.7 Added definitions for INL and DNL Reference to table 2.
12. Table 2 took out Gamma.
13. Fig 3 pre-shoot: Note (a) redefined as undershoot.
14. Fig.3 (i) corrected overshoot to read undershoot.
15. Fig3. Define (j) as V min steady state.
16. Fig 3. Note (h) Add reference to undershoot.
17. Table 1: add clarity on Jitter spikes
18. Reference fig 7 in 2.3 note (c).
19. Definition of monotonic.

Section 2.1 Eliminated and placed under section 2.2 and 2.3

Section 2.3 added comments as follows:

Input Data =(FFFh)

Input Data =(000h)

Added notes Letters in the comment sections of the Table where appropriate

Add new notes: (d), (e), (f), (g)

Added clarification to note (a)

Changed Note (b) section 2.4 to section 2.5

Changed the Video Injection Noise ratio from 5% to +/- 2.5%

Changed the Paragraph in 2.6 Jitter Measurement Definition for simplicity.

Acknowledgments

The VESA Video Signal Standard is the result of expert input from many sources. VESA acknowledges and thanks the Display Committee members who contributed to and combined the industry expertise that resulted in this standard. In particular the following individuals and their companies contributed significant time and effort.

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1 Introduction

Display - graphics controller technology has leapt forward in the last 10 years at a break-neck pace. Displays have gone from VGA to 1600 x 1200@85Hz and beyond. Graphics controllers have increased performance up to fast 3D imagery with 32-bit pixel depth. However, the signal path between the graphics controller and display monitor has remained the same for 10 years. With new graphics ASICs running at 2.5 volts, there is no longer any margin left in the TTL synchronization circuits. With current high bandwidth designs, display signals have little margin left, resulting in monitor jitter and poor front of screen definition. Consequently, there have often been last minute patches by both display vendors and graphics card companies just to get products to work.

This document will give monitor/graphics vendors a starting point from which to address these issues. By using these specifications as a guideline, industry designers will be able to master the art of good signal integrity. This will benefit the industry as a whole, as well as the end user.

1.1 Compliance with standard

If a supplier does not wish to specify compliance of the standard to the minimum pixel clock period, then the supplier may alternately specify a longer pixel clock than minimum clock pixel period for compliance with the standard.

Related VESA documents

VESA Display Specifications and Test Procedures (DSTP) Version 1.0 Rev 1.0 - Oct. 3, 1996

VESA Display Data Channel Standard (DDC) Version 3 - Dec.15, 1997

VESA Enhanced Display Data Channel Standard (E-DDC) Version 1.0 - Sept. 2, 1999

2 VESA Video Signal Definition

2.1 Specifications

2.2 Synchronization (Hsync and Vsync) Signal Specification

All measurements are made at the interface between the System Unit connector and Signal Cable connector to the Display Device, unless otherwise noted. See Figure 1 for Sync terminations.

	Min	Max
Driver Logic Level "1"	2.4 Volts	5.5 Volts
Driver Logic Level "0"	0.0 Volts	0.5 Volts
Driver High Level Output Current	-8ma	
Driver Low Level Output Current	+8ma	
Receiver Logic Level "1"	2.0 Volts	
Receiver Logic Level "0"		0.8 Volts
Fall Time Max		80% of minimum pixel clock period
Rise Time Max		80% of minimum pixel clock period
Monotonic Rise/Fall Voltage range	0.5-2.4 Volts	
Overshoot/Undershoot		30% of high level signal voltage range No excursions allowed in the 0.5-2.4 volt voltage range
Jitter (Measured between Hsyncs). Voltage spikes are not allowed during Hsync level transitions.		Over the frequency spectrum: 15% of peak-to-peak or 6 sigma minimum pixel clock period, from 0Hz to max. horizontal refresh rate at all image formats, worst-case screen patterns. Minimum of 100,000 samples. (also refer to Section 2.6 Jitter Definition)

Table 1

See Section 2.4 for signal definition

2.3 Analog Video Outputs

All measurements are made at the interface between the System Unit connector and Signal Cable connector to the Display Device, unless otherwise noted. See Figure 2 for RGB terminations.

	Value	Comment
Max Luminance Voltage Input Data = (FFFh)	0.700 Volts +0.07 volts / -0.035 volts	DC Measurement. See note (a) and (d).
Min Luminance voltage Input Data = (000h)	0.000 Volts	DC Measurement. See note (a) and (d).
Video Channel Rise/Fall Time Max	50% of minimum pixel clock period	See notes (b), (e) and (g).
		See notes (b), (e) and (g).
Video Channel Rise/Fall Time Min	10% of minimum pixel clock period	
Settling Time Max after overshoot/undershoot	30% of minimum pixel clock period averaged over 100 waveforms to 5% final full-scale value.	See notes (b).
Monotonic	Yes	Definition in section 2.7
Resolution	1 LSB	
Integral Linearity Error	+/- 1 LSB	Definition in section 2.7
Differential Linearity Error	+/- 1 LSB	Definition in section 2.7
Video Channel to Video Channel Mismatch	6% of any video output voltage over the full voltage range	See notes (f).
Video Noise injection ratio	+/- 2.5 % of Max Luminance Voltage	See note (c) and (e).
Video Channel to Video Channel Output Skew	25% of minimum pixel clock period	See notes (f).
Overshoot/Undershoot	+/-12% of step function voltage level over the full voltage range	1.5 X the rise time duration

Table 2

(a) With respect to Analog Channel RTN pin in the connector, where Analog Channel RTN denotes the RED return, Green return and Blue return signals as shown in Figure 2. Measurement taken at Steady state Values in Fig 3.

(b) See Section 2.5 for Signal Definition, Definition of Terms.

(c) Use minimum 500MHz bandwidth differential probe or FET Probes using difference method (A B). Measurement technique 100K samples or 2 seconds measurement time. See Fig. 7.

(d) All other voltage amplitude values (with exception of Min Luminance voltage) are ratiometric from this reading. Measure the final or settled white level over 100k samples or 2 seconds measurement time. Reference Figs. 2 and 3.

(e) Measurement level is calculated based on the Max. Luminance Voltage value.

(f) Video matching compares the levels between: Red video output compared to green video output, green video output compared to blue video output, and blue video output compared to red video output.

(g) Rise and fall time measurement test pattern can use an alternating pattern of 100 pixels black and 100 pixels white per scan line.

2.4 Test Circuits

	Transmitter	Receiver
Sync Signals (See Fig 1)	Max of 2.2K Ohms to voltage equivalent source of +Vcc at display adapter	2.2K Ohms to GND at the monitor.
Analog Video Impedance (See Fig 2)	75 Ohms	75 Ohms DC $\pm$ 1.5 Ohms 1 Hz to $\frac{1}{4}$ pixel clock $\pm$ 7.5 Ohms $\frac{1}{4}$ pixel clock frequency to $\frac{1}{2}$ plus 10% (+60%) pixel clock frequency $\pm$ 15 Ohms
VSWR (for 75 Ohms Load)	Less than 1.2:1 For pixel frequencies between 140MHz and 1GHz	

Table 3

Typical H and V sync. monitor termination

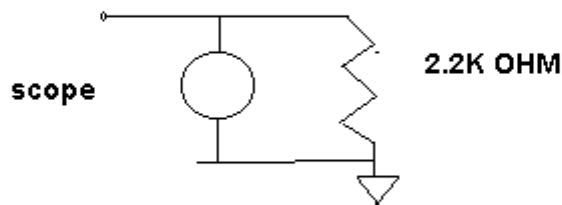
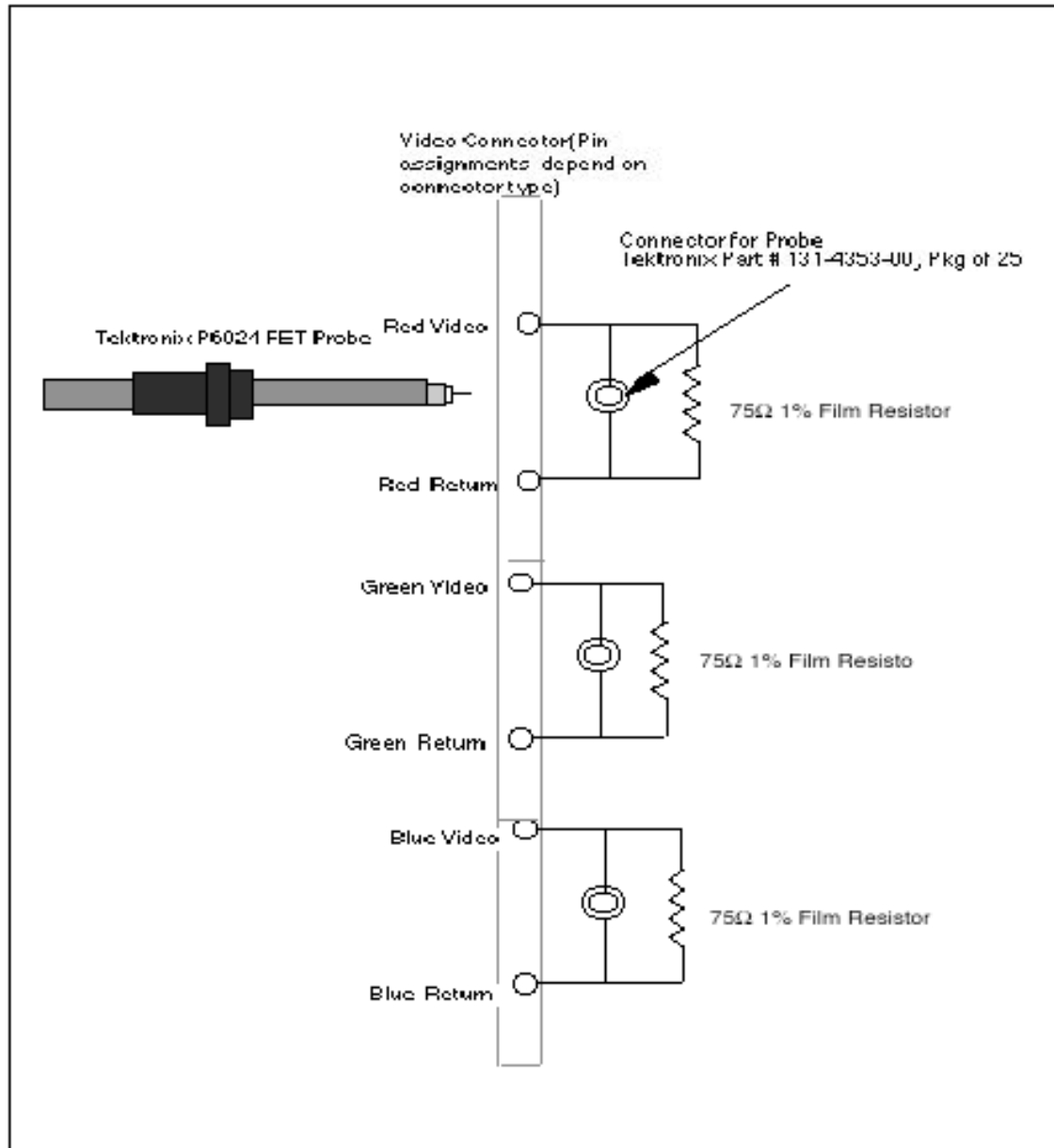


Figure 1

Fig 2. Video terminated measurement fixture.

Probes used are for example only. Equivalent probes and equipment may be used.



2.5 Definition of Terms

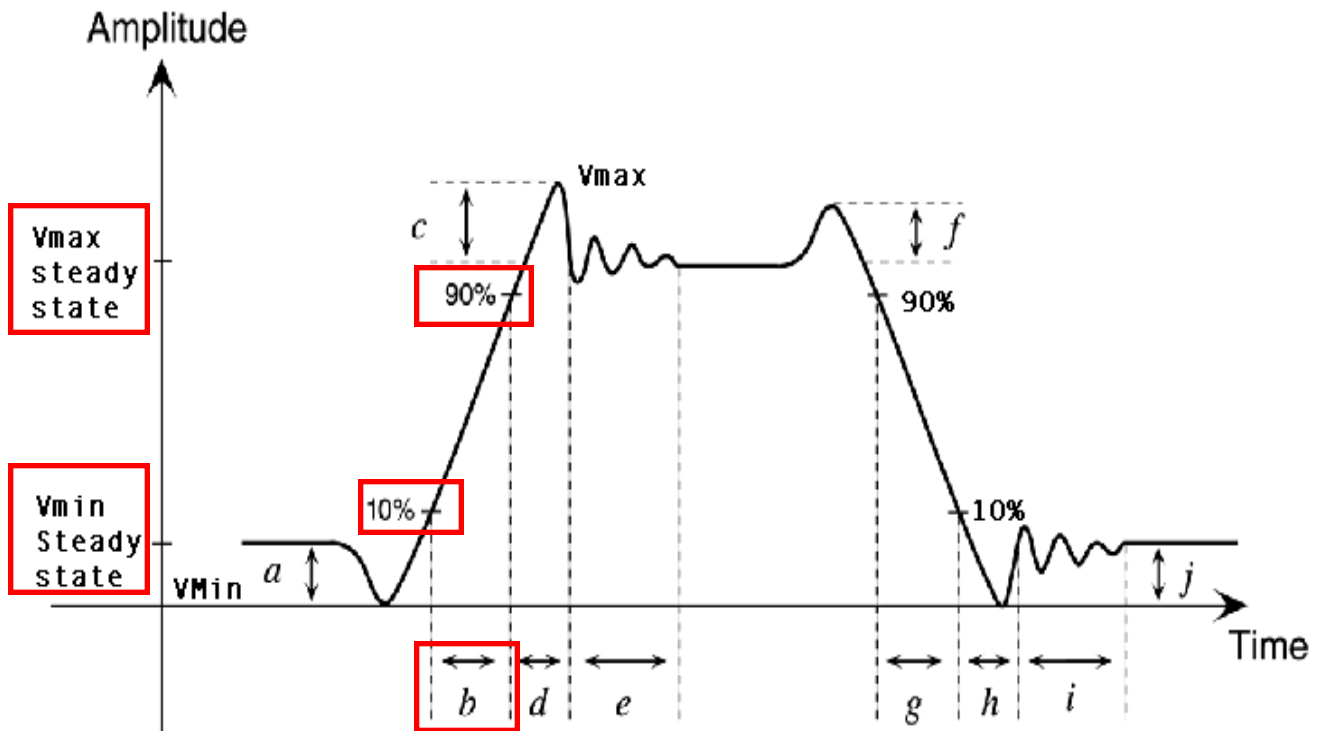


Figure 3. Video Signal Definitions

a) V_{min} steady state Amplitude before transition

b) Video Rise Time Delta (t), (measured from the 10% to 90% points of V_{minSS} to V_{maxSS})

c) Overshoot Amplitude

d) Undefined

e) Settling Time - Measured from the end of the overshoot to the point where the amplitude of the video ringing is down to $\pm 5\%$ of the final steady state value

f) Undefined

g) Video Fall Time Delta (t), (measured from the 10% to 90% points of V_{minSS} to V_{maxSS})

h) Undefined here, Note: Undershoot is within this period and with Amplitude of (j)

i) Settling Time - Measured from the end of the undershoot to the point where the amplitude of the video ringing is down to $\pm 5\%$ of the final steady state value

j) V_{min} steady state Amplitude after transition

2.6 Jitter Measurement Definition

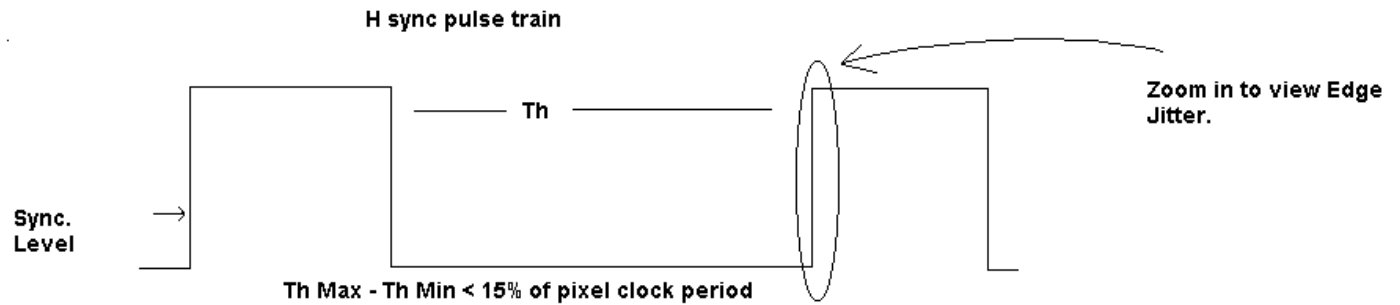


Figure 4. Jitter Measurement Definition

Trigger scope at 1.5 volts on the rising or falling edge of the Hsyncs. Measure the next Hsyncs edge, the edge has to be the same that was triggered on, and accumulate the data for least 100,000 edges. The peak-to-peak measurement subtracts the minimum Hsyncs period from the maximum Hsync period, then divide by 2 to get result. A six sigma result uses all 100,000 samples to determine the six sigma period deviation. See Fig 6 also.

2.7 Glossary of Terms

LSB Least Significant Bit

Monotonic 1. The property of either never increasing or never decreasing in reference to the slope of a Transient response. 2. A constant slope value containing no inflection points.

Sync Synchronization Signals

TTL Transistor - Transistor Logic

VSWR Voltage Standing Wave Ratio

$$LSBc = (V_{out}(255) - V_{out}(0)) / 255$$

where $V_{out}(255)$ is the full scale current for a 8 bit DAC and $V_{out}(0)$ is the zero level for the DAC. $LSBc$ is the ideal least significant bit.

$$INL \text{ (Integral Linearity Error)} = (V(n) - LSBc * n) / LSBc$$

where $V(n)$ is the DAC output voltage level measured at the nth step and $LSBc * n$ is the ideal DAC level measured at the nth step. INL is thus the actual nth value compared to the ideal nth value and normalized to the ideal LSB.

$$DNL \text{ (Differential Linearity Error)} = (V(n) - V(n-1)) / LSBc$$

DNL is the difference between the DAC output voltage measured at the nth value and the previous n-1 value. DNL is normalized to the ideal LSB.

Overshoot/Undershoot

Overshoot is defined as a positive going pulse during a transition time.
Undershoot is defined as a negative going pulse during the transition time.

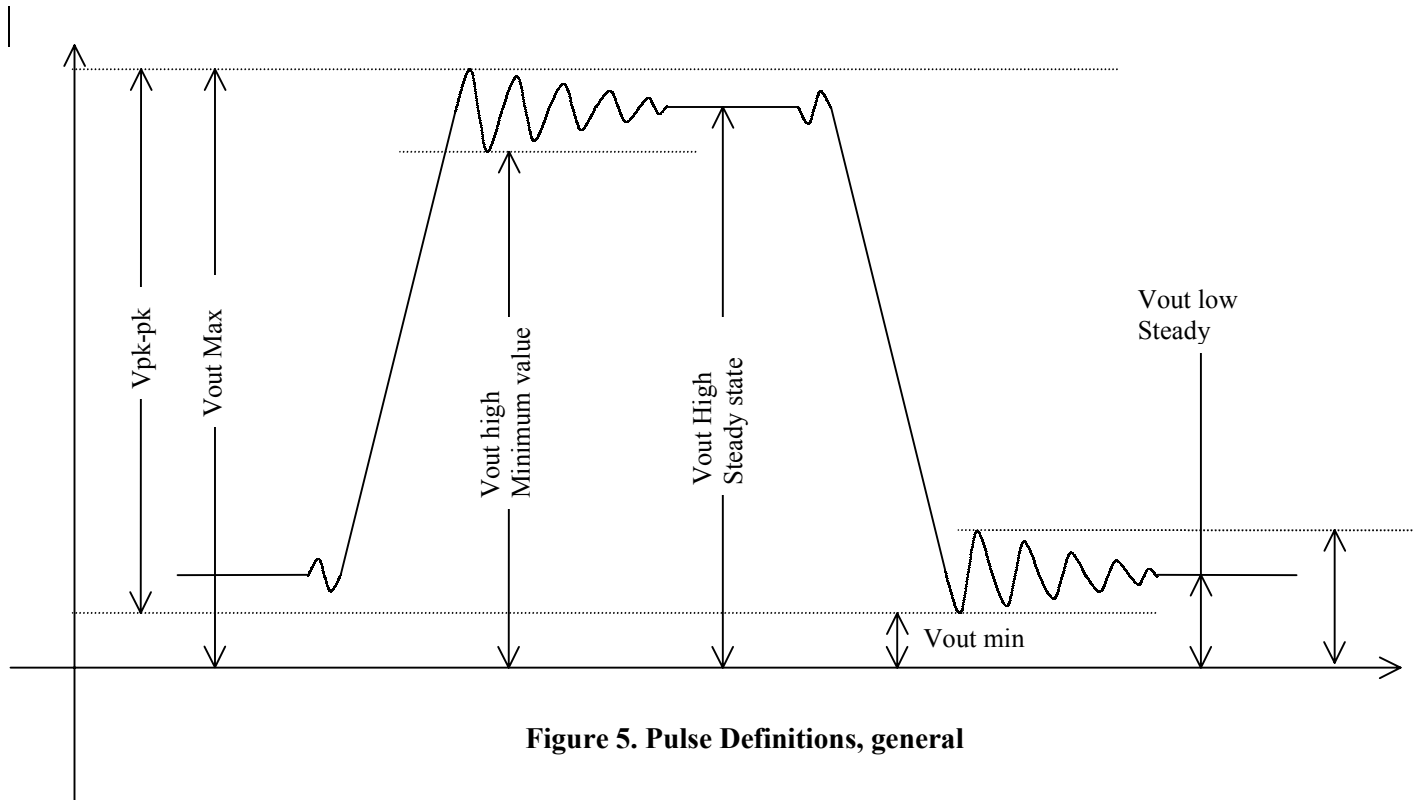
2.8 References

IBM Personal System/2 Hardware Interface Technical Reference - Common Interfaces, 84F9809 S84F-9809-00, pp 106-113.

IBM Personal System/2 Hardware Interface Technical Reference - Common Interfaces, 84F9809 S84F-9809-00, pp 105.

High Speed Digital Design (A Handbook of Black Magic), Johnson, H. and Graham, M., Prentice Hall, ISBN 0-13-395724-1, pp 108-110

3 Appendix A - Wave Form Diagrams



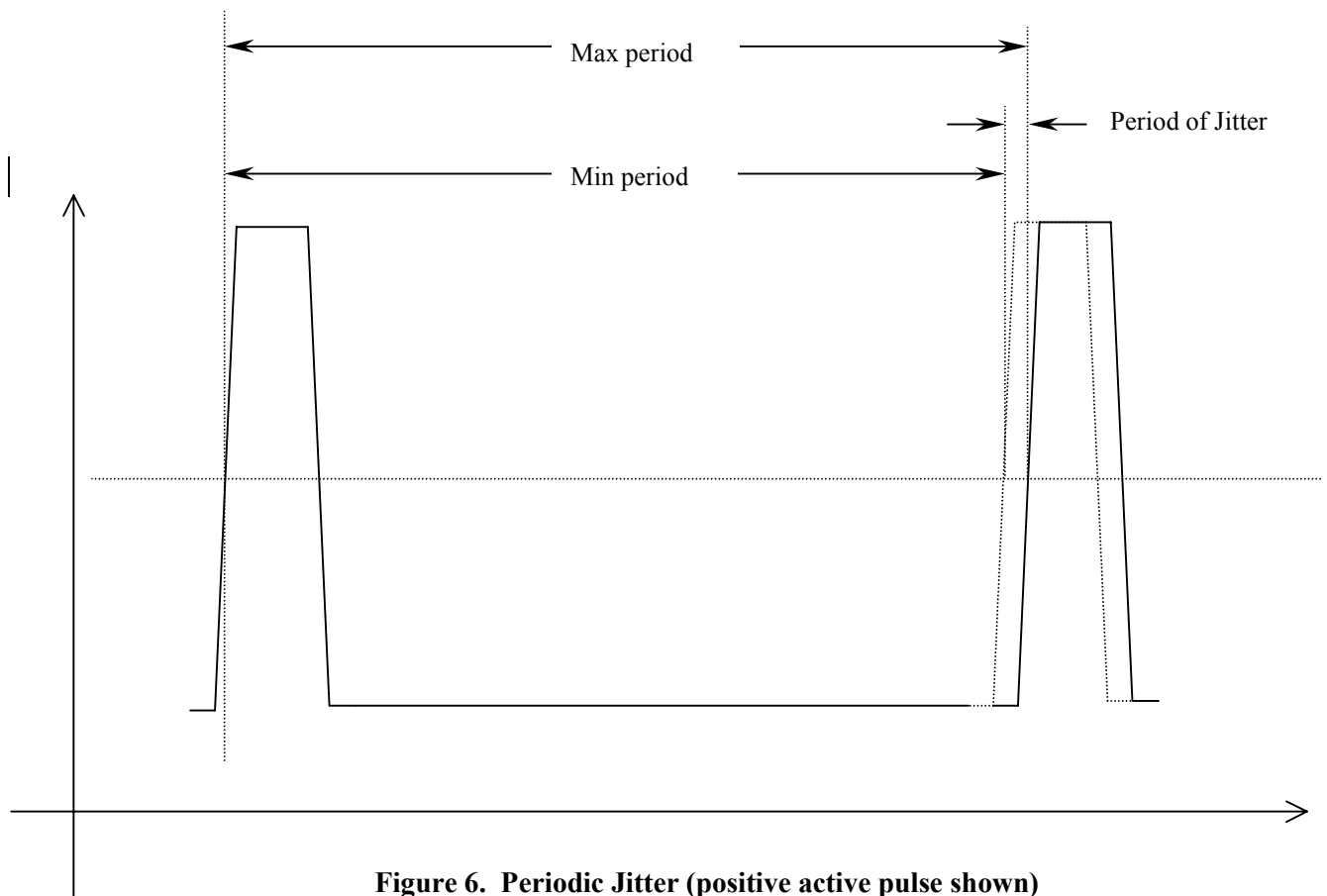


Figure 6. Periodic Jitter (positive active pulse shown)

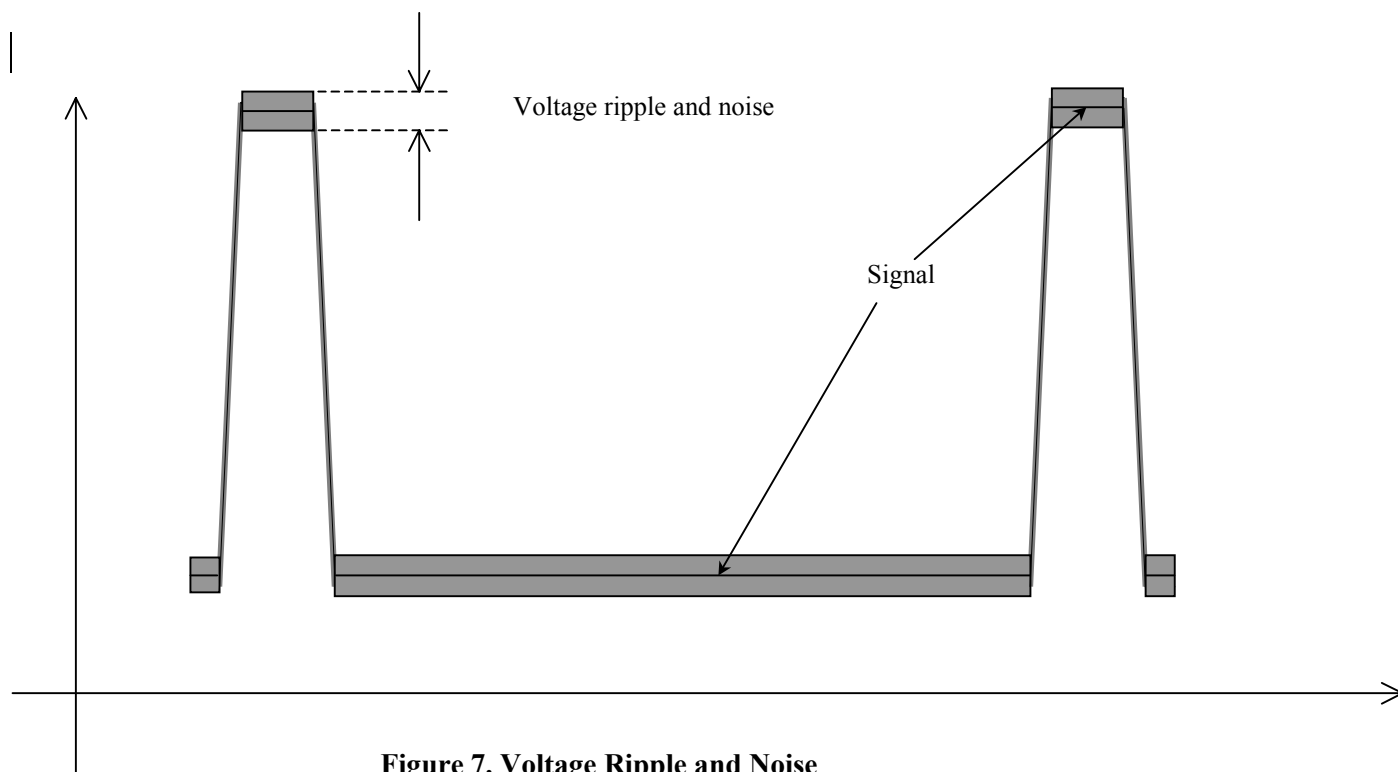


Figure 7. Voltage Ripple and Noise