The Input Offset Voltage Internal Calibration – Auto-zero vs Chopper Amplifiers

by Marek Lis

Some devices offer internal calibration of the input offset voltage and drift. These features are called autocalibration, zero-drift, or Self-Cal™. Texas Instruments zero-drift op amps are implemented using auto-zero or chopper-stabilized techniques. They both have an internal control loop that nulls out the input offset voltage that is caused by change in temperature, supply voltage, input common-mode or output voltage. For this reason, zero-drift amplifiers not only achieve single digit uV offset and tens of nV/C drift but also extremely high AOL, CMRR, PSRR (above 140dB) and no 1/f noise (it's removed together with dc offset).

In case of auto-zero a main amplifier, A1, and the nulling amplifier, A2, each have an associated input offset voltage that is stored during sample phase on C1 and C2, respectively – see Figure 1. In the auto-zero phase the charge from both caps is being transfer to null the total offset. The internal high-order filters are used to minimize switching noise. Some of the first Texas Instruments auto-zero op amps are OPA335 and OPA735 with maximum offset of +/-5uV and maximum drift of +/-0.05uV/C.

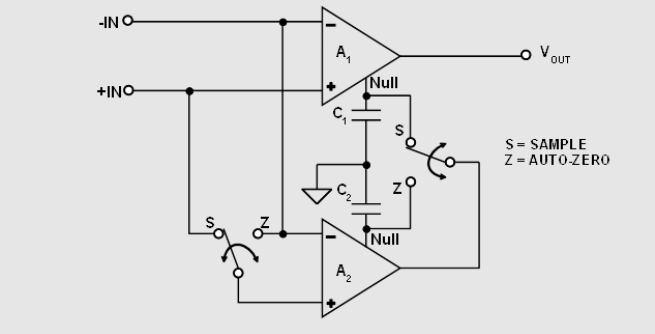

Figure 1. Auto-zero amplifier

Figure 2 shows the input stage of a chopper op amp. The amplifier is a conventional transconductance stage with differential input and differential output current. Chopping is accomplished with commutating switches on the input and output that synchronously reverse the polarity. The offset voltage of the transconductance stage is inside the input switching network, thus its contribution to output is periodically reversed by the output switches. The output current caused by offset voltage causes the voltage on C1 to ramp up and down at an equal rate. The internal logic assures equal up and down ramp times so the average output voltage on C1 is zero. Since both differential input and output

stages are reversed simultaneously, the net effect on the output capacitor, C1, is in-phase signal and zero average offset voltage.

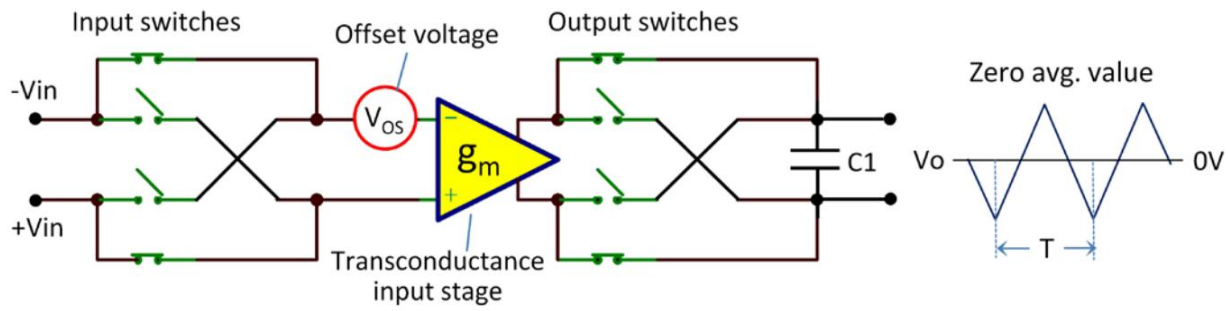

Figure 2. Chopper-stabilized amplifier

New-generation choppers are dramatically quieter, incorporating a switched-capacitor filter with multiple notches aligned with the chopping frequency and its odd harmonics. This is accomplished by integrating a charge on C1 for a full cycle before transferring its charge to the next stage of the op amp. Integrated over a full up-down cycle, its net value is zero – perfectly averaged. In the frequency domain, this creates a sinc(x) or sin(x)/x filter response with nulls that precisely align with the fundamental and all harmonics of the triangle wave. Since 1/f (flicker) noise is merely a slow time-varying offset voltage, choppers virtually eliminate this increased noise-spectral density in the low-frequency range. The chopping shifts the baseband signal to the chopping frequency, beyond the input stage's 1/f region. Thus, the low-frequency signal range of the chopper has a noise-spectral density equal to that of the amplifier's broadband range.

Some of the most recent high voltage chopper amplifiers, like OPA182, achieve maximum offset voltage of +/4uV and maximum drift of +/-12nV/C with typical AOL, CMRR and PSRR at or above 166dB. TI low voltage choppers like OPA387 maximum offset and drift are +/-2uV and 12nV/C, respectively, while its typical CMRR, PSRR and AOL are all above 145dB. Having said that, the input bias current is affected by the charge and discharge current glitches of the input zero-drift circuitry. This effectively creates a repetitive current pulse in 100's of pA. For this reason, the zero-drift amplifiers are not recommended for applications with high source impedances. The amount of current sunk or sourced from the input stage is dependent on the combination of input impedance (resistance and capacitance), as well as the balance and matching of these impedances across the two inputs. These positive and negative input current pulses, integrated by the input capacitance, may cause a shift in the apparent "average bias current" that leads to offset shift. Since the input bias current is dependent on the input impedance, it is difficult to estimate what the actual input bias current is without knowing the end circuit and associated capacitive strays. For this reason, in order to minimize the offset voltage shift caused by

unequal positive and negative IB, it is important to match input impedances between the two input terminals.