Voltage-to-Current (V-to-I) Circuit Design for Current Control in Inductive Loads

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Welcome to the Texas Instruments presentation of Voltage-to-Current Circuit Design for Current Control in Inductive Loads. We will focus on a few of the most popular circuit configurations used to drive constant current into inductive loads. The techniques and tools provided will allow one to stabilize any configuration of V to I (Voltage-to-Current) circuits driving inductive loads. Use of power op amps will require external protection and thermal considerations, due to internal power dissipation, that will be covered at the end of this presentation.

About Presenter – Tim Green, SMTS

Applications Manager – Precision Amps, Tucson, Arizona USA

Background

THE UNIVERSITY OF ARIZONA

- ***BSEE, University of Arizona, 1981***
- ***37 years of Analog and Mixed Signal Experience***
  - *17 years in Board/System Level Design:*
    Brushless Motor Control, Jet Engine Control, Missile Systems, Data Acquisition Systems, CCD Cameras
  - *20 years in Analog/Mixed Signal Semiconductor:*
    Power Op Amps, Instrumentation Amplifiers, 4-20mA, PGAs Difference Amplifiers, Small Signal Op Amps

AKA:
"Wizard of Zo"

Expertise

- Op Amp Stability & SPICE Op Amp Macro-modeling
- Publishing definition-by-example articles on op amp stability
- Troubleshooting complex board/system level problems
- SAR ADC Input and Reference Pin SPICE model and drive

Prologue

- Focus on the concepts presented for V-I Circuits driving Inductive loads
- Detailed definition by example circuits contain formulae for re-use
- We will be focusing on the *key* points of these designs
- Presentation is available to refer back to for detailed design help
- If you remember only one thing → where to go look for V-I Op Amp Circuits!

Where and Why are V-to-I circuits used?

For Motor Control Torque ∝ Current
So Current Control → Torque Control

Linear Torque Motors

Linear Actuators

Linear Valves

Current Sources for Test Equipment

Voltage Controlled Current Source

Voltage-to-current circuits are used to control current in Linear torque motors, linear actuators, and linear valves. Torque is proportional to current in a motor and so by controlling current you are controlling torque, which is often preferred in many servo systems. In addition there are many test equipment applications requiring V-to-I circuits for device under test applications.

Agenda

- **Op Amp Critical Stability Tools Review**
- **V-I Floating Load (Non-Inverting)**
- **V-I Grounded Load (Difference Amplifier)**
- **V-I Grounded Load (Improved Howland Current Pump)**
- **V-I Floating Load (Improved Howland Single Supply Bridge)**
- **Power Op Amp Protection**
- **Power Op Amp Power Dissipation**
- **Precision Amplifiers – Popular Power Op Amps**
- **Appendix**

This section will populate your analysis toolbox with all of the tools needed to effectively stabilize V to I circuits driving inductive loads. Key op amp stability concepts will be reviewed to enable ease of analysis in the follow-on V to I circuits.

Review: Gain in Linear vs. Decibel

Linear (V/V) to Decibels (dB)

$$G_{dB} = 20 \times \log(G_{V/V})$$

Example: Convert the closed-loop gain (G_{CL}) of an op amp circuit from 100V/V to decibels

Solution:

$$G_{CL(dB)} = 20 \times \log\left(100 \frac{V}{V}\right) = 40dB$$

Decibels (dB) to Linear (V/V)

$$G_{V/V} = 10^{\left(\frac{G_{dB}}{20}\right)}$$

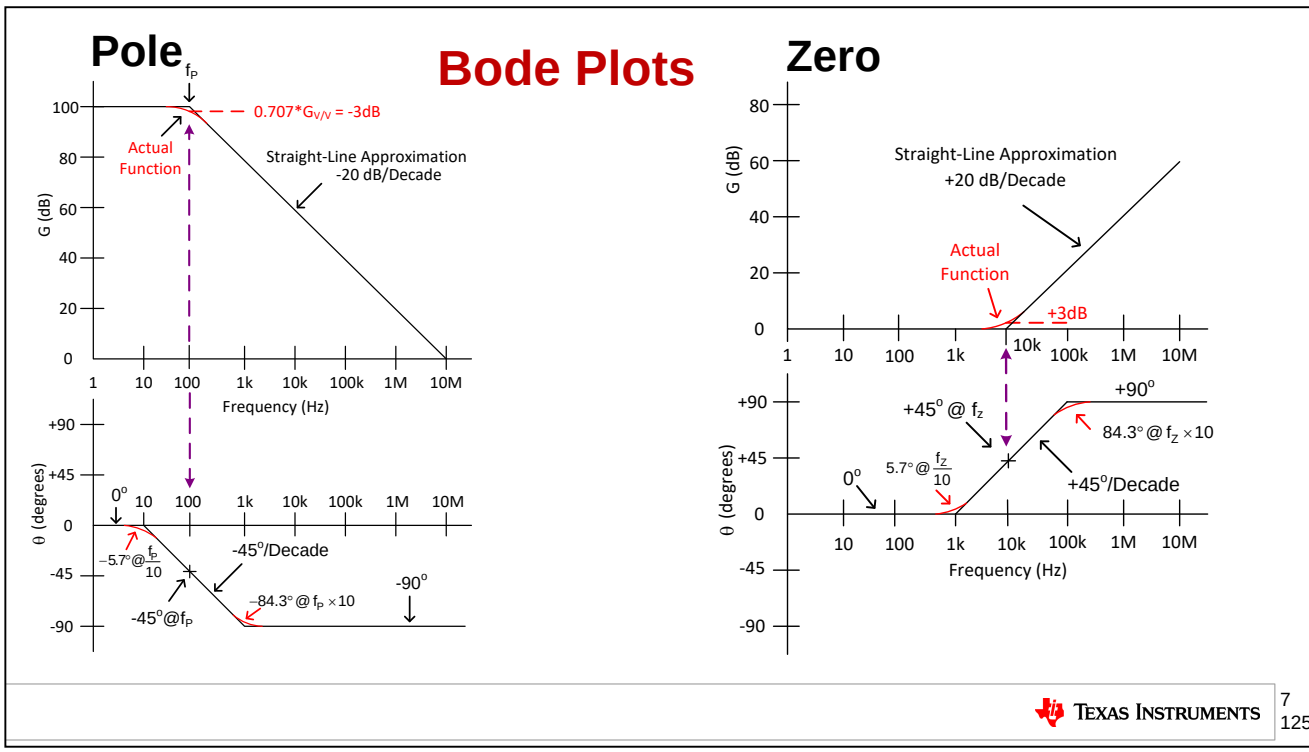
Example: Convert the open-loop gain (A_{OL}) range of the OPA188, 130dB, to V/V

Solution:

$$G_{A_{OL}@1Hz} = 10^{\left(\frac{130\,dB}{20}\right)} = 3{,}162{,}277 \frac{V}{V}$$

$$G_{A_{OL}@2MHz} = 10^{\left(\frac{0dB}{20}\right)} = 1 \frac{V}{V}$$

Important gain factors we will be working with will be plotted on a dB gain scale vs a frequency logarithmic scale. As seen here we will need to convert from linear gain (V/V) to dB and from dB back to linear gain (V/V). Gain in dB is simply the log to the base 10 of the linear gain in V/V multiplied by 20. To convert gain in dB back to linear gain (V/V) we use the base 10 and raise it to the power of gain in dB divided by 20.



Our Gain (dB) vs Frequency (Logarithmic scale) plots will contain regions indicative of poles and zeros.

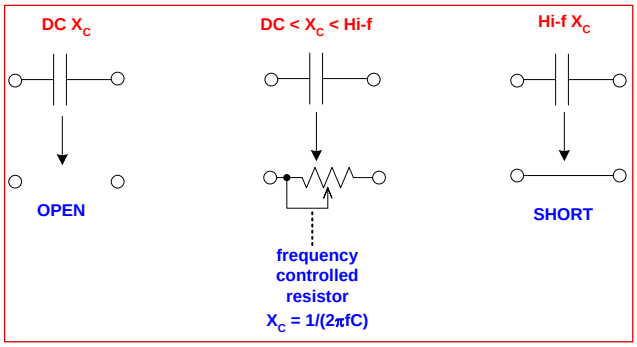
A pole, shown on the left has a -20dB per decade magnitude slope, as frequency increases, beginning at the location of the pole. The phase shift due to a pole is -45 degrees at the location of the pole, with a -45 degree/decade slope flattening out to 0 degrees, one decade to the left of the pole location's frequency, and flattening out to -90 degrees, one decade above the pole location's frequency.

A zero, shown on the right has a +20dB per decade magnitude slope, as frequency increases, beginning at the location of the zero. The phase shift due to a zero is +45 degrees at the location of the zero, with a +45 degree/decade slope flattening out to 0 degrees, one decade to the left of the zero location's frequency, and flattening out to +90 degrees, one decade above the zero location's frequency.

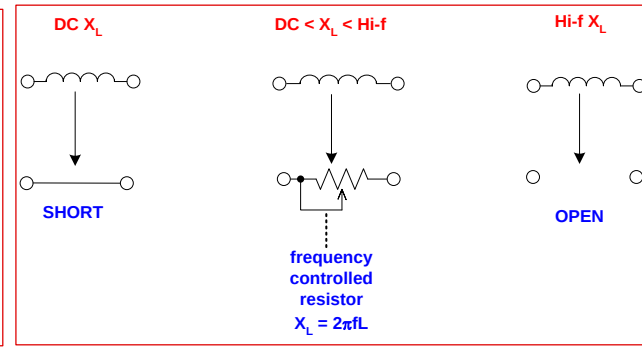
Note both poles and zeros have an effective one decade below and one decade above influence, from their frequency location.

Capacitor & Inductor – Intuitive Impedance Model

Capacitor - Intuitive Model

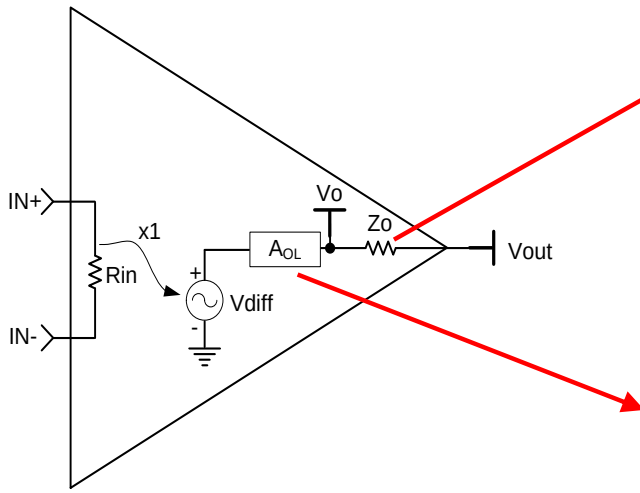


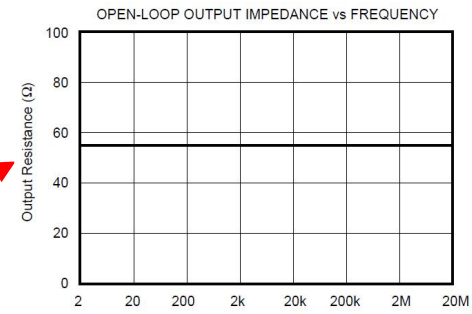
Inductor - Intuitive Model

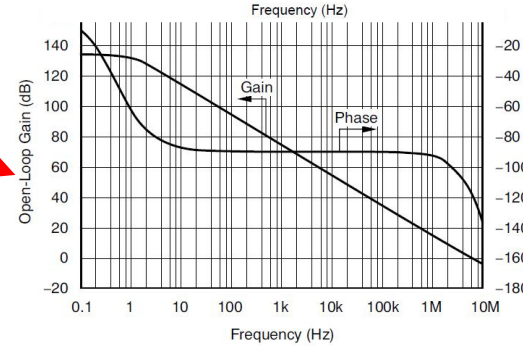


Two reactive elements that will be involved in our circuit analysis are the inductor and the capacitor. We will use a simplified model of each to expedite our analysis. On the left we see a simplified model for a capacitor. At DC the capacitor's impedance looks like an open. And at high frequency it will become a short. In between DC and high frequency the capacitor looks like a frequency dependent impedance, XC=1/(2*pi*f*C). On the right we see a simplified model for an inductor. At DC the inductor's impedance looks like a short. And at high frequency it will become an open. In between DC and high frequency the inductor looks like a frequency dependent impedance, XL=2*pi*f*L.

Op Amp Open Loop Model







It is helpful to use an intuitive model for the op amp when performing ac stability analysis because of the complexity of modern op amps. In this simplified “stability” model, the differential input voltage applied to the inputs is passed to the amplifier output stage where it passes through the amplifier open-loop gain, followed by the open-loop output impedance before it reaches the output terminal.

The open-loop gain, or Aol, of an op amp represents the maximum gain that can be applied over frequency to the differential voltage applied between the inputs of the device. Aol for an ideal amplifier is infinite and is not limited by frequency. Modern op amps can have open loop gains in excess of 1 million volts per volt, or 120dB at low frequencies and unity-gain bandwidths from 10’s of kHz up to several GHz.

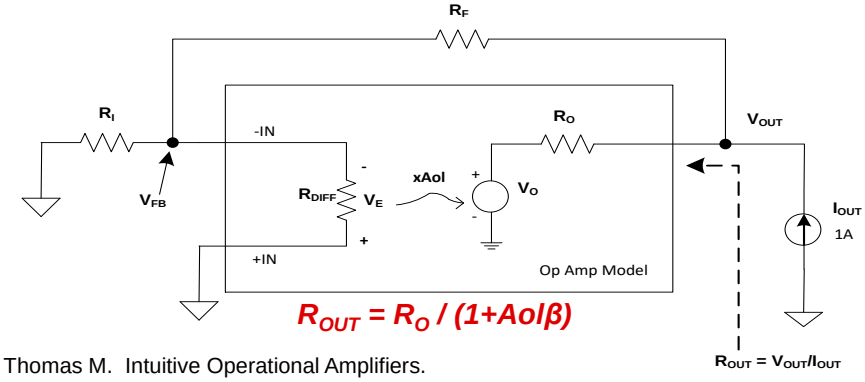
The open-loop output impedance, Zo, is a measure of the impedance of the open-loop output stage of the op amp. Zo should not be confused with the amplifier’s closed-loop output impedance, Zout, which depends on Zo, Aol, and the circuit configuration. To keep the stability analysis focused on the basic concepts for this series, the behavior of the Zo will be viewed as a resistor over all frequencies of interest. In truth Zo can vary widely over frequency for newer rail-to-rail output stages making stability analysis more difficult. We can rely on accurate op amp macromodels that match the datasheet to simplify analysis.

Op amp impedance: Output resistance

Definition of Terms:

$\mathbf{R_O}$ = Op Amp ***Open Loop*** Output Resistance

$\mathbf{R_{OUT}}$ = Op Amp ***Closed Loop*** Output Resistance



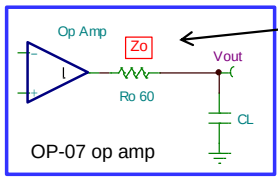
$R_{OUT} = R_O / (1+Aol\beta)$

From: Frederiksen, Thomas M. Intuitive Operational Amplifiers. McGraw-Hill Book Company. New York. Revised Edition. 1988.

There are two types of output resistance we can discuss when looking at an op amp. The first is $R_{O,}$ the open loop output resistance of an op amp. The second is R_{OUT} defined as the closed loop output resistance of an op amp.

R_O and R_{OUT} are intimately related as we can see in the relationship defined in this slide. R_{OUT} is R_O reduced by one plus the loop gain. If we consider the effects of feedback, then intuitively this makes sense. Imagine that we sat on the output and injected a current into the amplifier. This current would produce a corresponding change in voltage through the output resistance of the amplifier. As this happens, the output voltage would tend to increase. But the output voltage is set by the input voltage and the feedback network, and the amplifier wants to keep the two inputs at the same potential to maintain linear operation. To account for this, the op amp tries to adjust its internal Vo to maintain the same Vout, and this effectively causes the closed loop output resistance to appear much lower than the open loop resistance! Remember that we can think of loop gain as the op amp's ability to adjust its output to correct for errors, and this is exactly what our equation for Rout is telling us. The more loop gain we have, the lower the output impedance and consequently the lower the impact of a disturbance on the output.

Op amp impedance: Zo versus Zout



Assume Zo = 60Ω, resistive

$$\text{Zout} = \frac{Zo}{1 + Aol\beta}$$

If a unity gain follower then β=1

Assume Aol ≫ 1

$$\text{Zout} \approx \frac{Zo}{Aol}$$

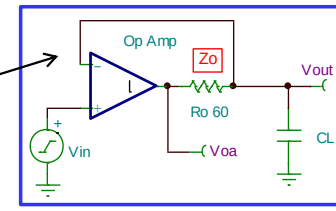
Frequency increase

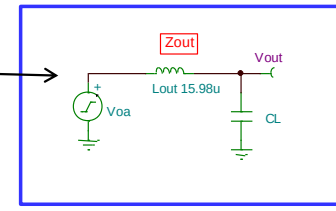
→ Aol decrease (−20dB/decade)

Frequency increase

→ Zout increase (+20dB/decade)

Zout at +20dB/decade → Inductor = 15.98uH

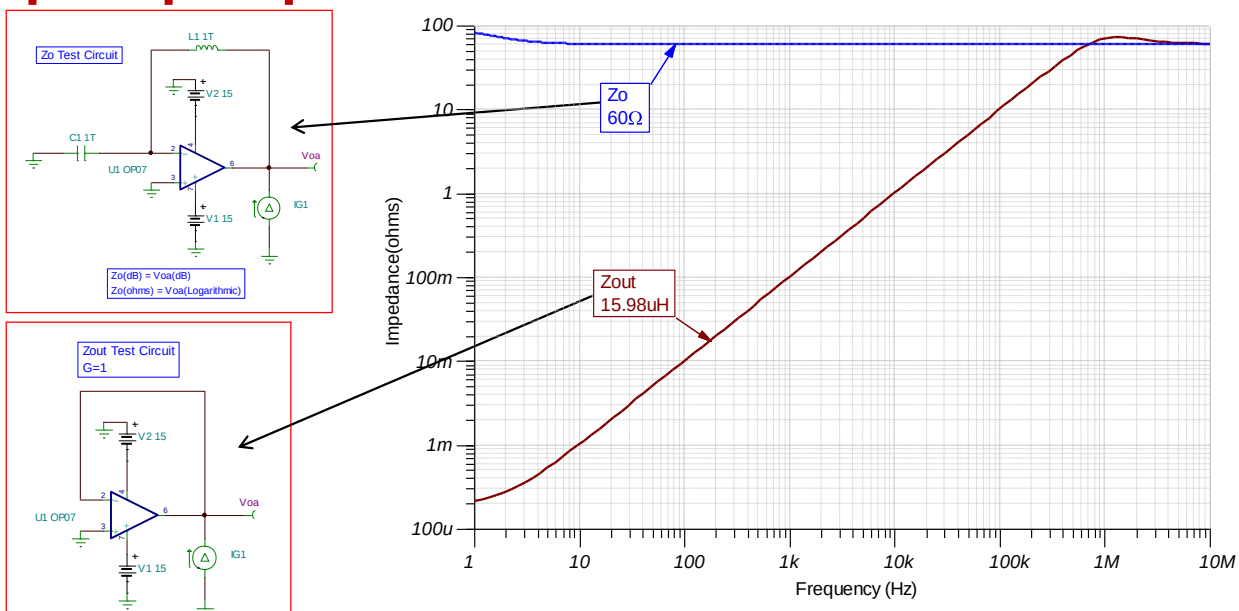




This is why, in general, without proper external compensation, you ***never put a capacitor on op amp output! → Makes an L-C resonant circuit!***

If we examine an op amp with a purely resistive open loop output impedance, Zo, we will find that it will look different when the op amp loop is closed. Using the example of a unity gain follower, G=+1, and the formula for Zout = Zo / (1+AolBeta) we can predict Zout. Since Beta = 1 for a unity gain follower and Aol >> 1 for most frequencies of interest then our Zout formula simplifies to Zout = Zo/Aol. As Aol decreases (-20dB/decade), with increasing frequency, the Zout must increase (+20dB/decade), implying Zout looks inductive. Here, for the chosen op amp of OP-07, with Zo = 60ohms we will find Zout = 15.98uH. This is also, in general, you never put a capacitor directly on an op amp output with external compensation because it can form a resonant L-C circuit!

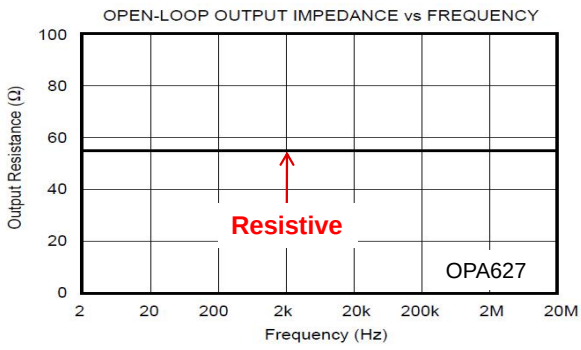
Op amp impedance: Zo versus Zout



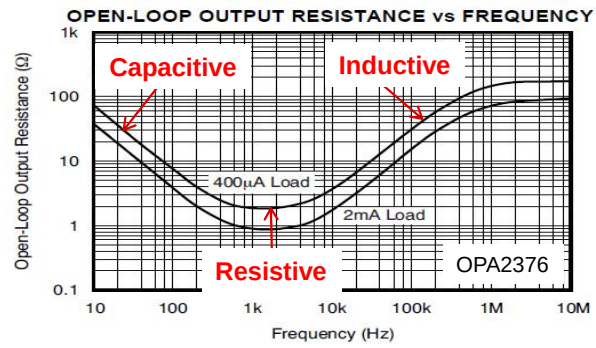
Our TINA-TI SPICE simulations for open loop output impedance, Zo, and closed loop output impedance, Zout, concur with our prediction of an inductive Zout for a resistive Zo and an Aol that decreases at -20dB/decade as frequency increases.

Op amp impedance: When R_O is really Z_O!

OPA627 has R_O



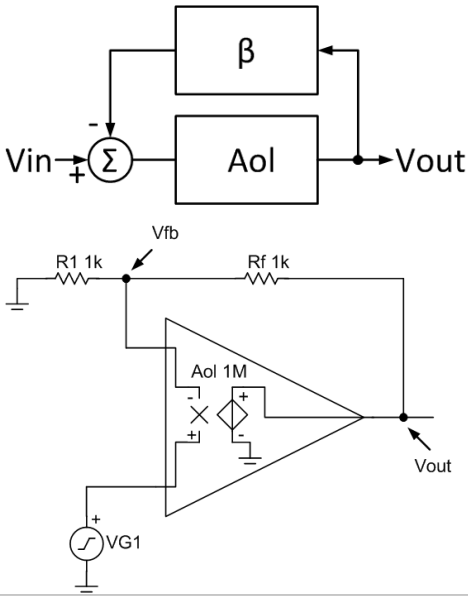
OPA2376 has Z_O



Note: **Some op amps have Z_O characteristics other than pure resistance, R_O.**
Consult data sheet for Z_O or Z_{OUT}.
Always "Trust But Verify" any SPICE op amp macromodel against the data sheet.

Most of the early op amp designs had purely resistive, low output impedances. While many devices today still retain this characteristic, it is becoming increasingly common for devices to have complex, reactive output impedances. In this example, the open loop output impedance of the OPA376 starts off capacitive, becomes resistive for a decade or so, and then becomes inductive over the remaining bandwidth of the device before it flattens out again. This can present additional design challenges that aren't encountered with resistive outputs. So what is responsible for this shift in output impedance and why would we want to design with devices that exhibit this behavior?

Op Amp Closed Loop Model



A_{ol} = Open loop Gain

β = Feedback Factor = $\frac{V_{fb}}{V_{out}} = \frac{R_1}{R_1 + R_f}$

A_{cl} = Closed Loop Gain = $\frac{A_{ol}}{1 + A_{ol}\beta}$

$A_{ol}\beta$ = Loop Gain

$A_{cl} = \lim_{A_{ol}\beta \to \infty} \left(\frac{A_{ol}}{1 + A_{ol}\beta}\right) = \frac{1}{\beta} = 1 + \frac{R_f}{R_1}$

To control the large open-loop gain of modern amplifiers, negative feedback is required between the output of the amplifier and the inverting input. This is referred to as “closing the loop.” In this circuit, the loop is closed with Rf and R1 which create a voltage divider, and therefore an attenuation, between the output and the inverting input. The ratio of the resistors determines the amount of the output that is fed back to the input which is defined as the feedback factor, or Beta, of the circuit.

Closing the loop results in a closed-loop gain, Acl, that is equal to Aol divided by 1 plus Aol multiplied by Beta. Aol multiplied by Beta is referred to as Loop-gain. When the loop-gain is large, the closed-loop gain formula can be simplified to equal 1/Beta. In this example 1/Beta equals 1+Rf/R1, which can be recognized as the gain of a non-inverting amplifier circuit.

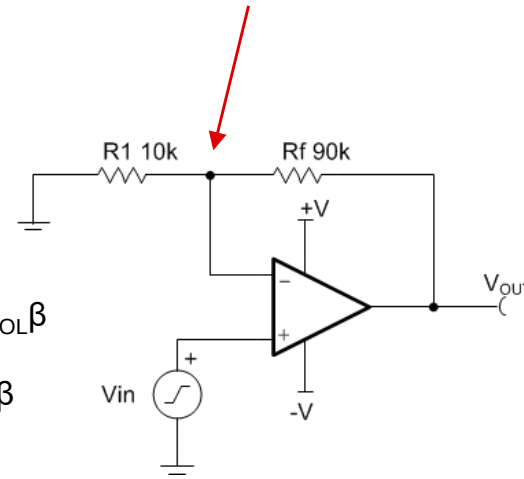
Closed-loop gain through negative feedback is a fundamental concept in amplifier circuit design and should be thoroughly understood. Let’s review it again quickly. The amplifier will adjust it’s output to equalize the two inputs establishing the virtual short between them. Therefore an attenuation from the output to the input, set by Beta, forces the output to be larger than the input by the inverse of Beta. This is how the ratio of the feedback resistors sets the closed-loop gain of the circuit.

When is an Amplifier Unstable?

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta}$$

- A circuit is unstable when $A_{OL}\beta = -1$
- $A_{OL}\beta = -1$ sets the denominator of $A_{CL} = 0$
- $A_{OL}\beta = -1$ when $A_{OL}\beta$(dB) = 0dB and phase shift($A_{OL}\beta$) = 180°
  - Phase shift is relative to the DC phase

$A_{OL}\beta = -1$ when the phase at V_{FB} has shifted 180º relative to Vin



Phase Margin (PM)

How close the system is to a 180° phase shift in $A_{OL}\beta$

- PM = Phase($A_{OL}\beta$) when Gain($A_{OL}\beta$) = 0dB
- Ex: 10° phase margin = 170° phase shift in $A_{OL}\beta$
- >45° phase margin for stable design

Let's now move on and define the conditions for stability using mathematical and graphical methods.

First, we must define when an amplifier is unstable. Looking back at the op amp closed-loop gain equation, we remember that Acl = Aol / 1+ AolB. Taking a closer look, we can see that if AolB, or the loop gain, equals -1, we get zero in the denominator and therefore Acl becomes undefined. This is the mathematical definition of instability.

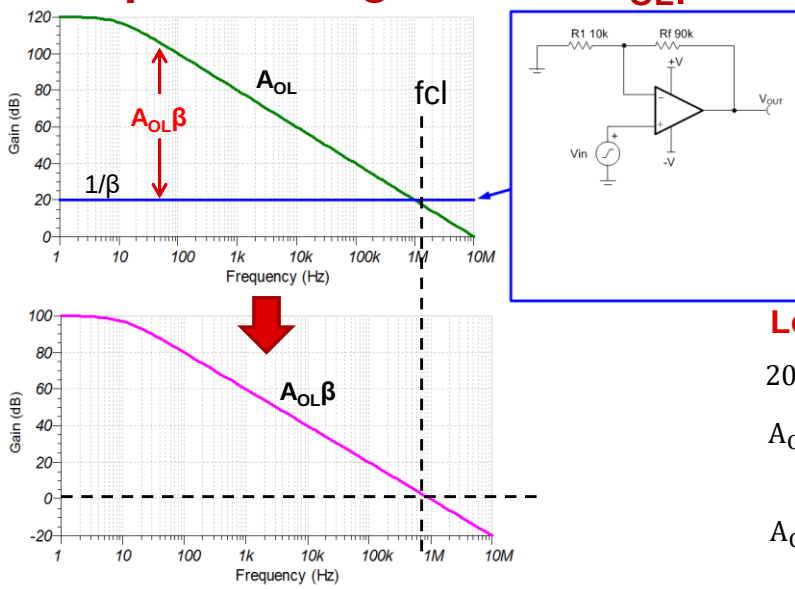
How can this happen in a real circuit?

Well, at some point in frequency AolB will equal 0dB, which is equal to 1V/V. If enough delay is introduced into the feedback path, the phase in the feedback network will shift 180 degrees relative to Vin. A 180 degree phase shift is equivalent to an inversion of the input, or -1. Therefore, when the gain of AolB = 0dB and the phase has shifted by 180 degrees, the result is AolB = -1.

The term "Phase Margin" is used to define how close a circuit is to this condition. Phase margin is simply the phase of AolB at the frequency where AolB = 0dB. For example, 10 degrees of phase margin means that AolB has shifted by 170 degrees at the point where AolB = 0dB.

As you can see, loop gain or AolB is a key component of stability analysis. How can we observe loop gain?

Loop Gain Magnitude – $A_{OL}\beta$



$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = \frac{R_F}{R_1} + 1 = 10\,V/V$$

$$\frac{1}{\beta}(dB) = 20\log(10) = 20dB$$

Loop gain in dB:

$$20\log(A_{OL}\beta) = 20\log(A_{OL}) - 20\log\left(\frac{1}{\beta}\right)$$

$$A_{OL}\beta(dB) = A_{OL}(dB) - \frac{1}{\beta}(dB)$$

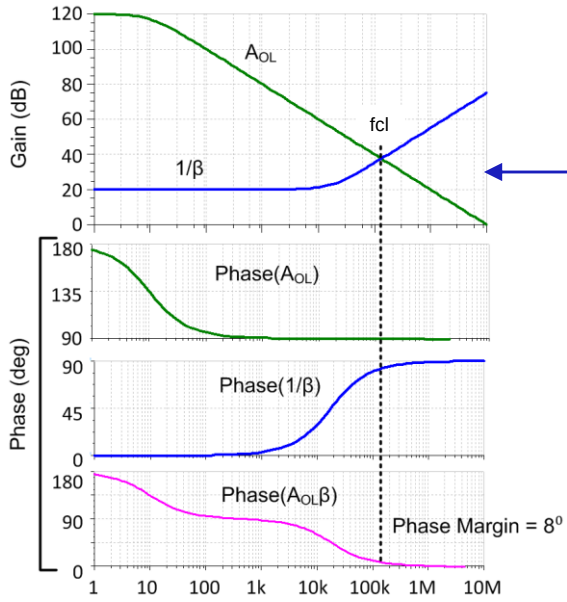
$$A_{OL}\beta(V/V) = \frac{A_{OL}\left(\frac{V}{V}\right)}{\frac{1}{\beta}\left(\frac{V}{V}\right)}$$

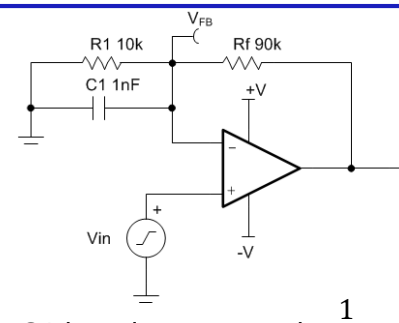
Note: $A_{OL}\beta(dB) = 0dB$ when A_{OL} and $\frac{1}{\beta}$ intersect

First we can consider the loop gain magnitude using a Bode plot. Using the same circuit as before, we have a gain of 10V/V, or 20dB, so 1/Βετα is a constant 20dB over frequency. The circuit's Aol is also shown. To find the magnitude of AolBeta, we can simply subtract 1/Beta from Aol. This might not seem intuitive, but the mathematical relationship shown on the right side of the slide proves this using the properties of logarithms.

Remember in the last slide we stated that the phase margin is the loop gain phase at the frequency where AolBeta = 0. This frequency is called "fcl" and defines where the loop is closed. This is also the frequency where Aol and 1/B intersect, which makes sense since the difference of two equal values is zero.

Loop Gain Phase – Phase ($A_{OL}\beta$)





C1 introduces a zero in $\frac{1}{\beta}$

$$\frac{1}{\beta} = \frac{Z_f}{Z_1} + 1$$

At DC the capacitor is open, so gain = 10V/V. At high frequency the capacitor causes Z_1 to decrease, so gain increases by +20dB/decade

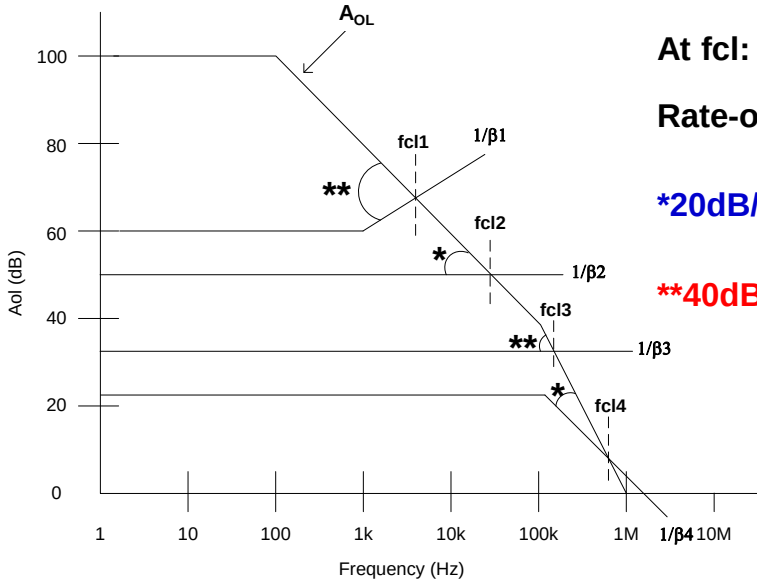
$\text{Phase}(A_{OL}\beta) = \text{Phase}(A_{OL}) - \text{Phase}(1/\beta)$

To measure the phase margin, we need to know the loop gain phase, or phase of AolBeta, over frequency. Using the same log properties as before, we can simply subtract the phase of 1/Beta from the phase of Aol to get the phase of AolBεtα.

In this example, a capacitor was added to the feedback network of the op amp circuit. At DC the capacitor is open, so the closed-loop gain is 10V/V like the previous circuit. At some higher frequency, the capacitor causes the impedance of the combination of R1 and C1 to decrease, so the gain of the circuit increases by +20dB/decade. This can be seen from the zero in the 1/Beta plot.

Looking at the phase, the 90° increase in the phase of 1/Beta creates a 90° decrease in the phase of AolB, so phase margin becomes very low at only 5°.

Rate of Closure: Stability using 1/β & A_{OL}



At fcl: Loop Gain ($A_{OL}\beta$) = 1 (0dB)

Rate-of-Closure @ fcl =
$|A_{OL}$ slope – 1/β slope|

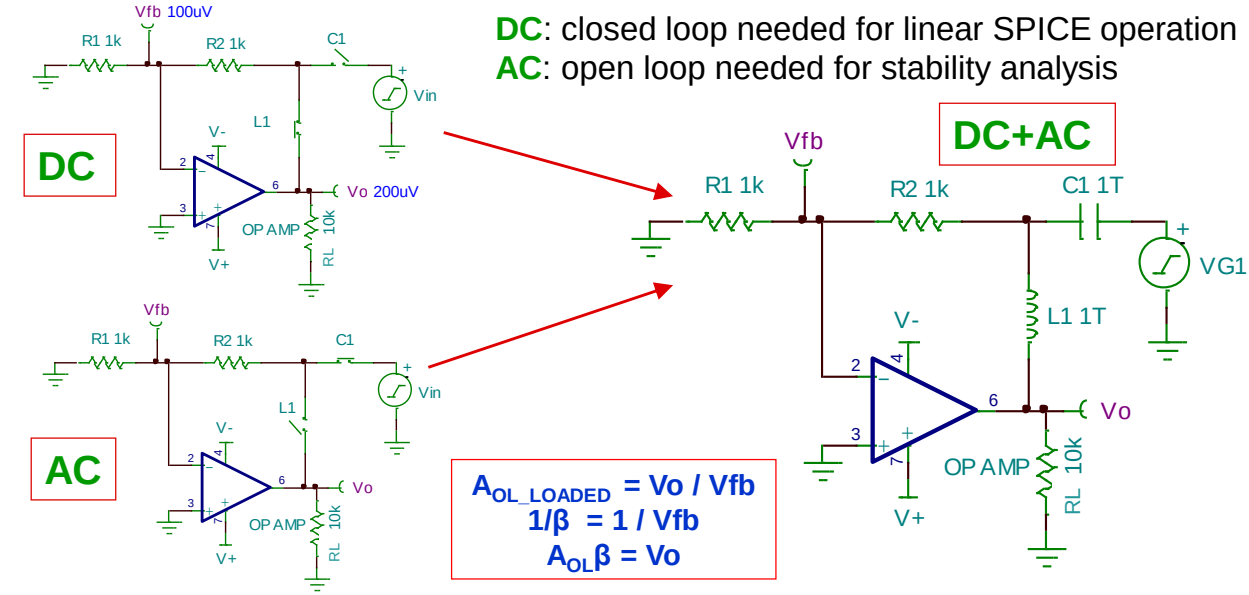
***20dB/decade Rate-of-Closure @ fcl =**
STABLE

****40dB/decade Rate-of-Closure@ fcl =**
UNSTABLE

First Order Stability Check → does not predict loop gain phase margin

We will use the information that a 1/Beta plot on an Aol curve will indicate Loop Gain (Aol*Beta). Remember that loop gain goes to 0dB where 1/Beta and Aol curves intersect each other at fcl. A quick first order stability check is easily determined by one observing the difference in the slopes of the 1/Beta and Aol curve at fcl. A 20dB per decade "rate-of-closure" is stable and a 40dB/decade "rate-of-closure" is not stable. Notice this does not tell us any detailed information about loop gain phase margin or degree of circuit stability. We will do an easy loop gain analysis to get these details. The power in 1/Beta plots on an Aol curve is that they will allow us to easily see how we can modify the 1/Beta curve to make unstable circuits stable.

Simulating Open-Loop Circuits for A_{OL}, $A_{OL}\beta$, $1/\beta$



AC Analysis only valid for DC Linear Operating Point → Check DC Analysis First!

To properly generate the open-loop curves in SPICE, the circuit being simulated must have a closed loop feedback path at dc while being open for all ac frequencies.

The circuit at the top left shows the desired dc circuit with the L1 switch closed and C1 switch open. A closed loop circuit at dc allows the output to be properly biased to a recommended dc operating point, commonly mid-supply.

The circuit at the bottom left shows the desired ac circuit with the L1 switch open and C1 switch closed. With the loop open for ac frequencies, the ac stimulus can be applied to generate the open-loop curves.

Thankfully, there's a straightforward way to create a circuit that meets both the dc and ac criteria using the ideal properties of SPICE components. Switch L1 is replaced with a 1Tera-Henry inductor, and switch C1 is replaced with a 1Tera-Farad capacitor.

At dc, L1 is a short and C1 is an open-circuit, providing a proper dc operating point. For all ac frequencies, L1 is an open-circuit and C1 is a short resulting in the proper open-loop ac connections.

Therefore, here is the recommended standard open-loop SPICE circuit configuration for op amp circuits. The feedback loop is broken between the op amp output and the feedback elements. The ac signal source is injected into the feedback network and measurements are taken at the output, Vo, and feedback node, Vfb.

With the feedback loop broken as shown, on the right, the equations for generating the desired curves are as follows:

Aol_loaded = Vo/Vfb

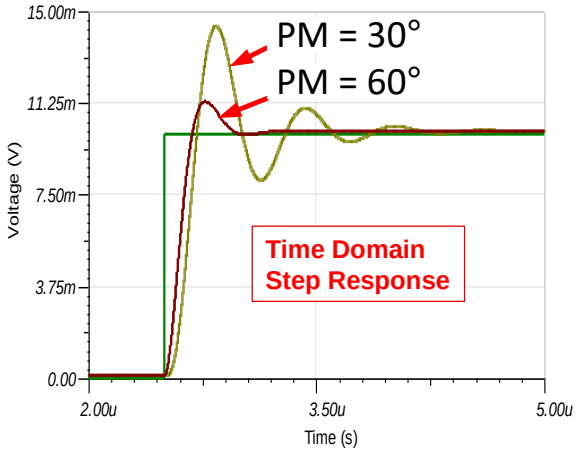
1/ß = 1/Vfb

Aol*ß = Vo

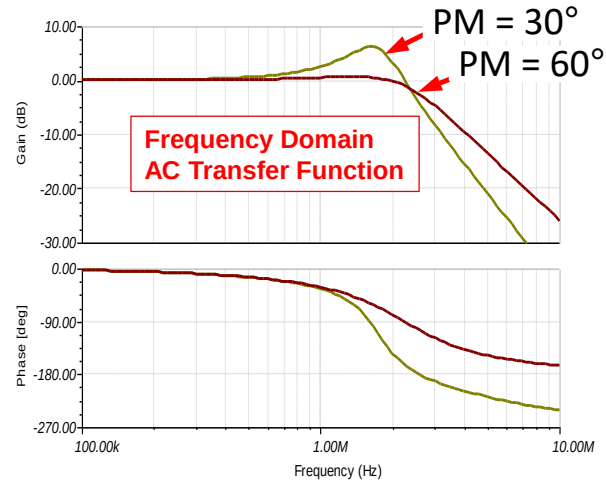
Indirect Loop Gain Phase Margin Measurements

1) **Phase Margin can be measured indirectly on closed-loop circuits!**
2) **Accurate for dominant 2-pole loop gain op amp circuits which many are.**

Time Domain → Percent Overshoot

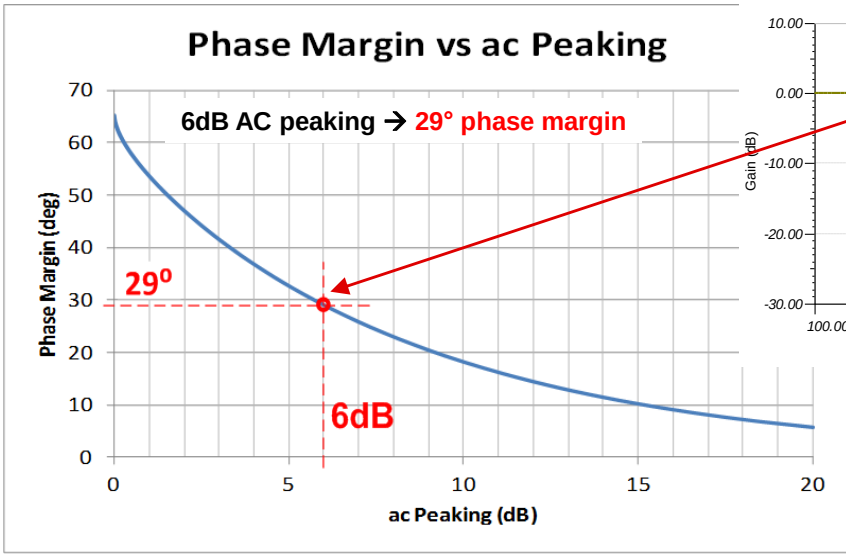


AC Gain/Phase → AC Peaking

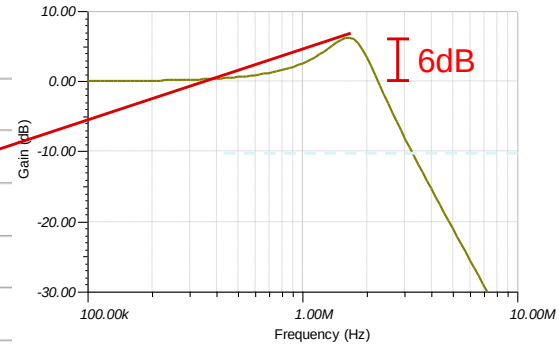


Phase Margin can also be indirectly measured on closed-loop circuits in the time domain and in ac gain/phase measurements. In the time domain, we can observe phase margin based on the overshoot of an op amp's output relative to a small-signal step input. In the frequency domain, we can observe phase margin based on the maximum AC peaking in the circuit's transfer function compared to the DC gain.

2nd Order Closed Loop Peaking in AC Frequency Sweep vs Phase Margin



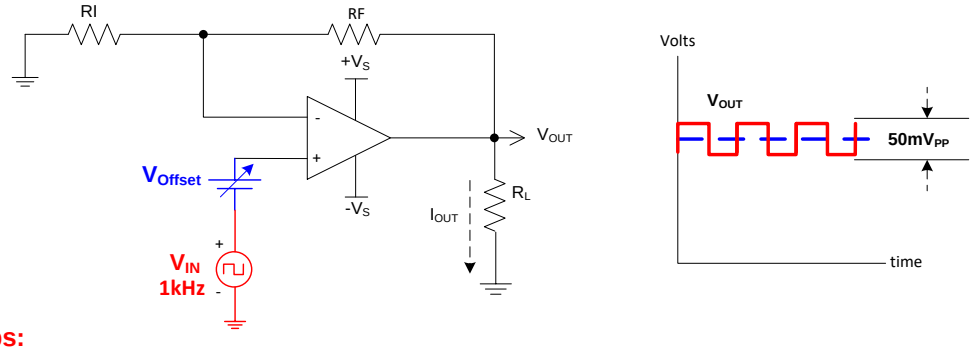
AC peaking = 6dB – 0dB = 6dB



1) **Phase Margin can be measured indirectly on closed-loop circuits!**
2) **Accurate for dominant 2-pole loop gain op amp circuits which many are.**

In AC Gain/Phase plots, the amount of ac peaking relative to the DC gain can be used to indirectly measure the phase margin of a circuit. In this example, the AC transfer function is peaking at 6dB, while the DC gain is 0dB. A total peaking of 6dB again results in 29 degrees of phase margin.

Transient Real World Stability Test

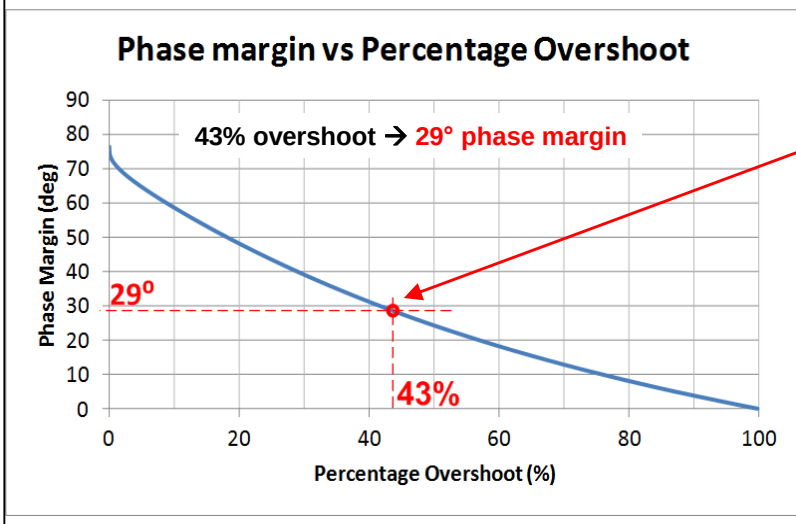


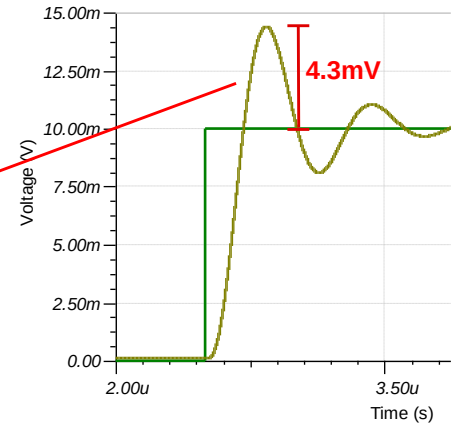
Test Tips:

- Choose test frequency << fcl → "Small Signal" AC Output Square Wave (1kHz usually works well)
- Adjust V_{IN} amplitude to yield output ≤50mVpp
- Worst case is usually when $V_{Offset} = 0$ → Largest Op Amp R_O ($I_{OUT} = 0$)
- Use V_{Offset} as desired to check all output operating points for stability
- Scope = AC Couple, expand vertical scale to look for amount of overshoot & ringing on V_{OUT}
- Use X1 Scope Probe on V_{OUT} for best resolution

This slide details the Transient Real World Stability Test. A small amplitude square wave is injected into the closed loop op amp circuit as the V_{IN} source. A frequency is chosen well within the loop gain bandwidth but also high enough to make triggering with an oscilloscope easy. 1kHz is a good test frequency for most applications. V_{IN} is adjusted such that V_{OUT} is 50mVpp or less. We are interested in the small signal AC behavior of the circuit to look for AC stability. To that end we do not want a large signal swing on the output which could also contain large signal limitations such as slew rate or output current limitations or output stage voltage saturation. V_{offset} provides a mechanism to move the output voltage up and down through its entire output voltage range to look for AC stability under all operating point conditions. For many circuits, especially those that drive capacitive loads, the worst case for stability is when the output is near zero (for a dual supply op amp application) and there is little or no DC load current since this results in the highest value of R_O, the op amp's open loop small signal resistance. Record the amount of overshoot and ringing on the square wave output and compare it to the 2nd Order Transient Curves in the Slide 75 to derive the phase margin for stability.

2nd Order Transient Curves



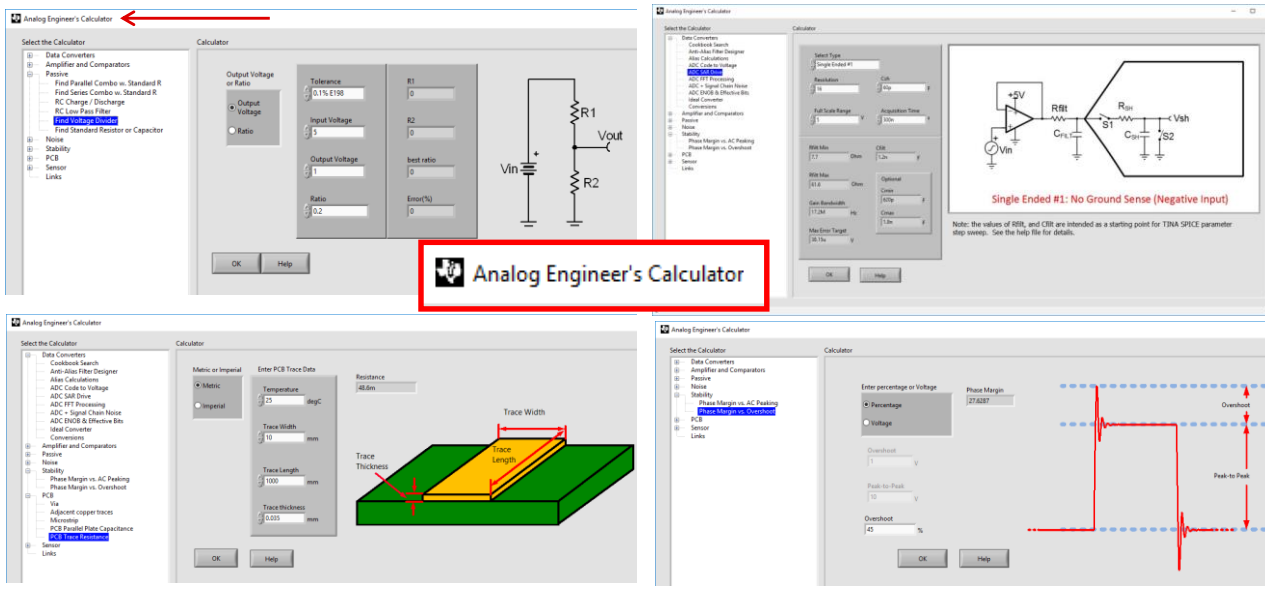


$$\%\text{Overshoot} = \left(\frac{14.3\text{mV} - 10\text{mV}}{10\text{mV}}\right) * 100\% = \mathbf{43\%}$$

1) **Phase Margin can be measured indirectly on closed-loop circuits!**
2) **Accurate for dominant 2-pole loop gain op amp circuits which many are.**

In the time domain the percent overshoot to a step input can be used to indirectly calculate the phase margin. In this example, a 10mV step was applied. The output overshoot reached 14.3mV, or 4.3mV above the intended output. This corresponds to a percent overshoot of 43%. Using the phase margin vs. percentage overshoot plot, we can see that 43% of overshoot results in only 29 degrees of phase margin.

Handy Engineering Calculator (Thanks – Art Kay)



http://www.ti.com/tool/ANALOG-ENGINEER-CALC

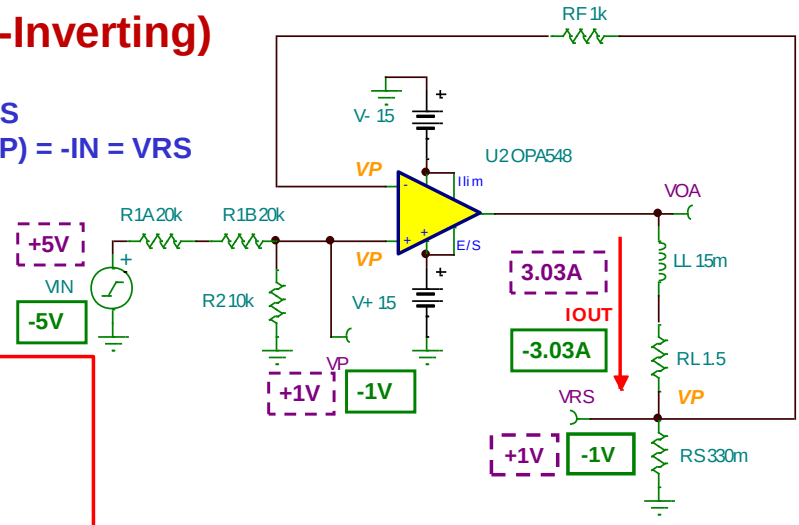
When we are designing our V to I circuits there will often be a need to accurately scale an input voltage down to accurately command current out of the V to I circuit. The “Analog Engineer’s Calculator” offers a handy way to accomplish this. Check back occasionally as this tool is often updated with additional powerful calculators for signal chain design.

Agenda

- Op Amp Critical Stability Tools Review
- V-I Floating Load (Non-Inverting)
- V-I Grounded Load (Difference Amplifier)
- V-I Grounded Load (Improved Howland Current Pump)
- V-I Floating Load (Improved Howland Single Supply Bridge)
- Power Op Amp Protection
- Power Op Amp Power Dissipation
- Precision Amplifiers – Popular Power Op Amps
- Appendix

V-I Floating Load (Non-Inverting)

Op Amp Point of Feedback is VRS
Op Amp Loop Gain forces +IN (VP) = -IN = VRS



Op Amp forces VRS = VP

$$IOUT = \frac{VP}{RS}$$

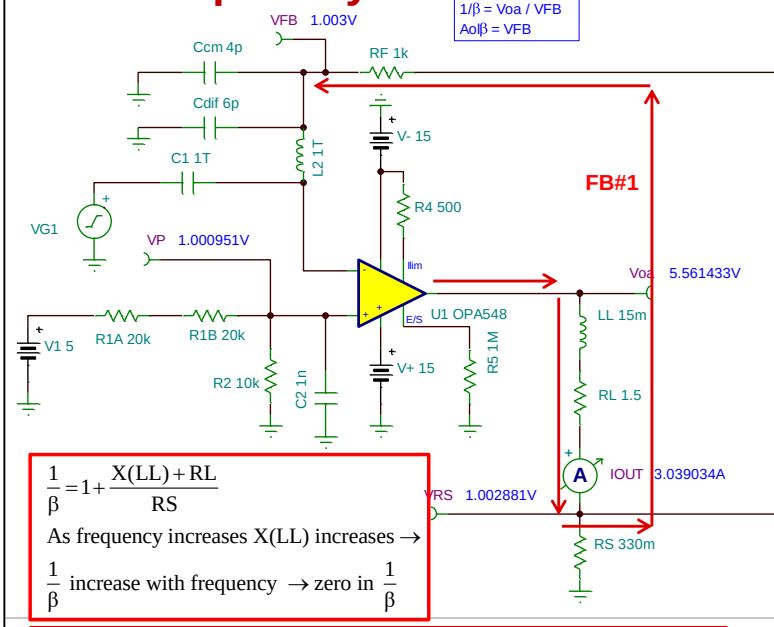
$$IOUT = \frac{VIN * R2}{(R1A + R1B + R2) * RS}$$

$$IOUT = \frac{VIN * 10k}{(20k + 20k + 10k) * 330m} = VIN * 0.606$$

Note:
Load (RL, LL) must float → Neither end tied to GND

The first V to I circuit we will analyze is the “V to I Floating Load (Non-Inverting)”. Non-Inverting because a positive input voltage creates a positive output current through the inductive load as show above. The input voltage is attenuated down to VP. VP appears at the +input of the op amp. The op amp’s loop gain will force the op amp –input to equal the +input. The –input is a feedback node connected to the top of resistor RS. The other end of RS is grounded. Notice the load must be allowed to “float” in this configuration. That means that neither end of the load is connected to ground or any other voltage potential. The voltage at VP will be held across Rs which will then cause the output current to flow based on VP/RS.
For this case +/-5V in will yield +/-3.03A out.

FB#1 Loop Analysis



$$\frac{1}{\beta} = 1 + \frac{X(LL) + RL}{RS}$$

As frequency increases X(LL) increases $\rightarrow$

$\frac{1}{\beta}$ increase with frequency $\rightarrow$ zero in $\frac{1}{\beta}$

FB#1 at DC:

LL = short at DC $\rightarrow 0\Omega$

$$\frac{1}{\beta}(dc) = 1 + \frac{RL}{RS} = 1 + \frac{1.5}{0.33} = 5.545 \rightarrow 14.88dB$$

FB#1 over Frequency:

Around fz, where X(LL) = RL+RS: $\frac{1}{\beta}$ will increase

One reactive element $\rightarrow$ 20dB/decade slope

$$fz = \frac{1}{2\pi \frac{LL}{RL + RS}} = \frac{1}{2\pi \frac{15m}{1.5 + 330m}} = 19.4Hz$$

Note: Ccm & Cdif are op amp internal input common mode & differential input capacitance moved outside op amp to include any effects on 1/β. Note Cdif goes to GND since +In looks like AC short (1nF to GND) since C2 =1nF >> Cdif = 6pF.

OPA548 Noninv V_I Loop.TSC

Use "Noise Gain" or "Non-Inverting Gain" of op amp for 1/β

TEXAS INSTRUMENTS

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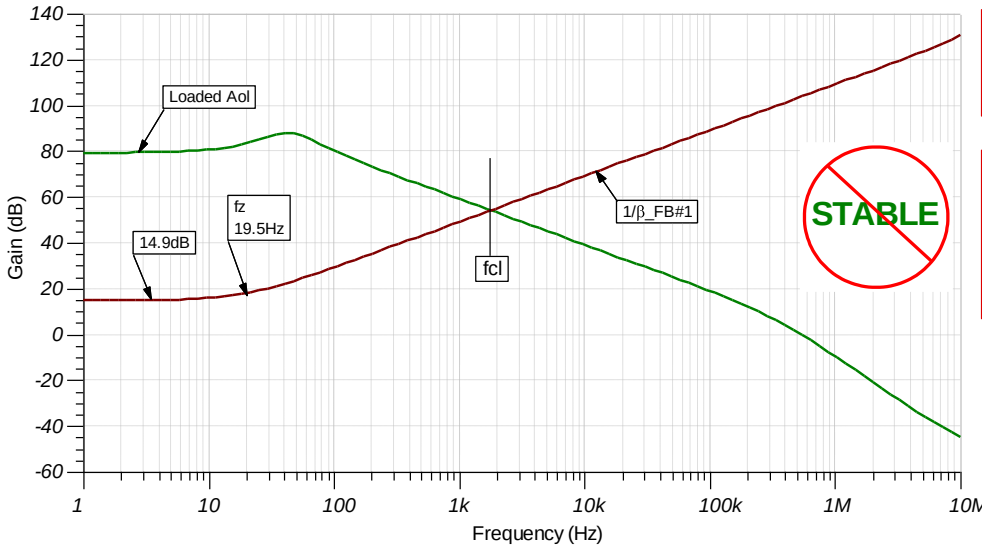
Now that we have the desired scaling for the Floating Load V to I circuit, we need to determine if it is stable. To do that we will need to compute what the 1/Beta should look like before we run a AC SPICE simulation to easily plot 1/Beta on Aol. If we run an AC SPICE simulation without knowing approximately what the answer should be, we cannot be certain if the answer is correct or if there is a connection error in our circuit, or if the op amp macromodel is correct. We will analyze this circuit by breaking the loop on the –input of the op amp as shown here. When we do this L2 will isolate the op amp's input capacitance from the 1/Beta path. So we will add in the op amps input common mode capacitance, Ccm from the –input and the op amp's input differential capacitance, Cdif. The common mode capacitance on the +input is dominated by C2=1nF and therefore is shorted out for any frequency of interest, thereby connect Cdif to AC ground. By injecting our test signal, VG1, into the –input of the op amp, we can measure Loaded Aol, 1/Beta, and Loop Gain (AolBeta) as shown. So we now need to predict 1/Beta before simulation. 1/Beta is always the non-inverting gain of the op amp. At DC, LL=short and we see the 1/Beta is simply 1+RL/RS (14.88dB). As frequency increases the impedance of LL, X(LL), will increase and cause 1/Beta to increase at +20dB decade. This zero, fz, in the 1/Beta plot is predicted by when RS+RL interact with LL and seen to be at 19.4Hz.

FB#1: Aol,1/β

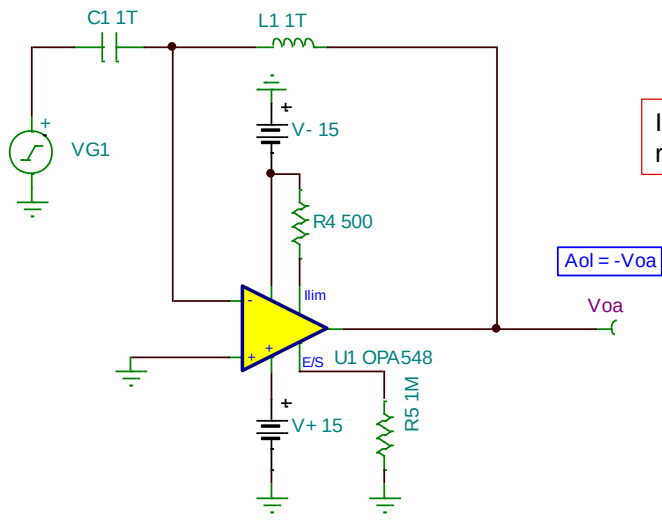


At fcl Rate-of-Closure = 40dB/decade → ***UNSTABLE***

Hump in Loaded Aol is Zo interacting with LL, RL + RS load. We will look at this in detail.

The results of the SPICE simulation here show the expected behavior of 1/Beta with a DC value of 14.9dB and a zero, fz, at 15.9Hz. The intersection of 1/Beta and the Loaded Aol at fcl result in a 40dB/decade rate-of-closure indicating an unstable circuit. There is a “hump” in the Loaded Aol curve which is caused by the OPA548 Zo, open loop small signal AC open loop output impedance, and the load of LL and Rs+RL.

Loaded Aol: *Unloaded Aol*

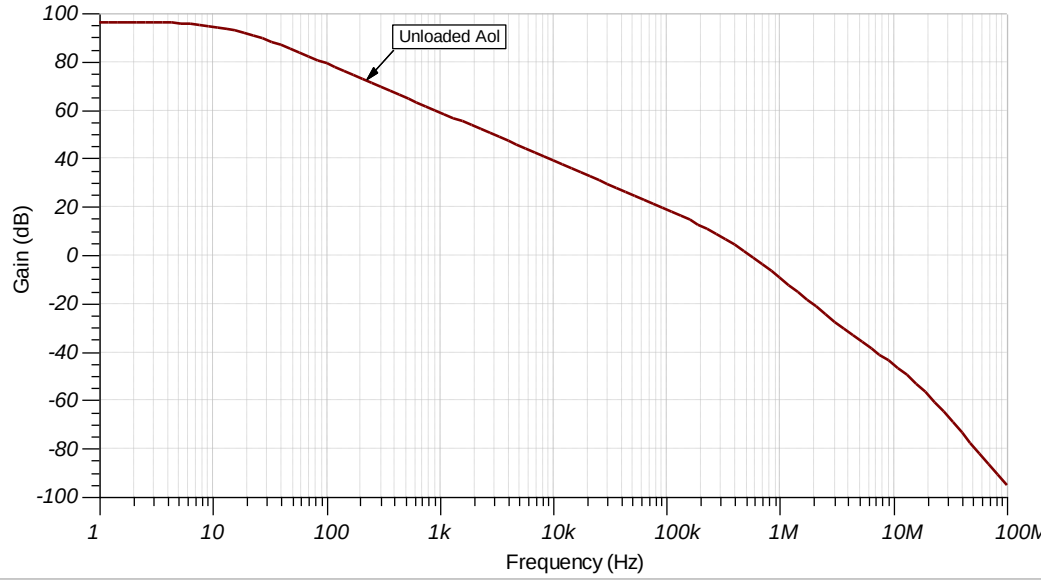


Inverting Gain configuration removes any effects of CMR on Aol.

OPA548 Unloaded Aol.TSC

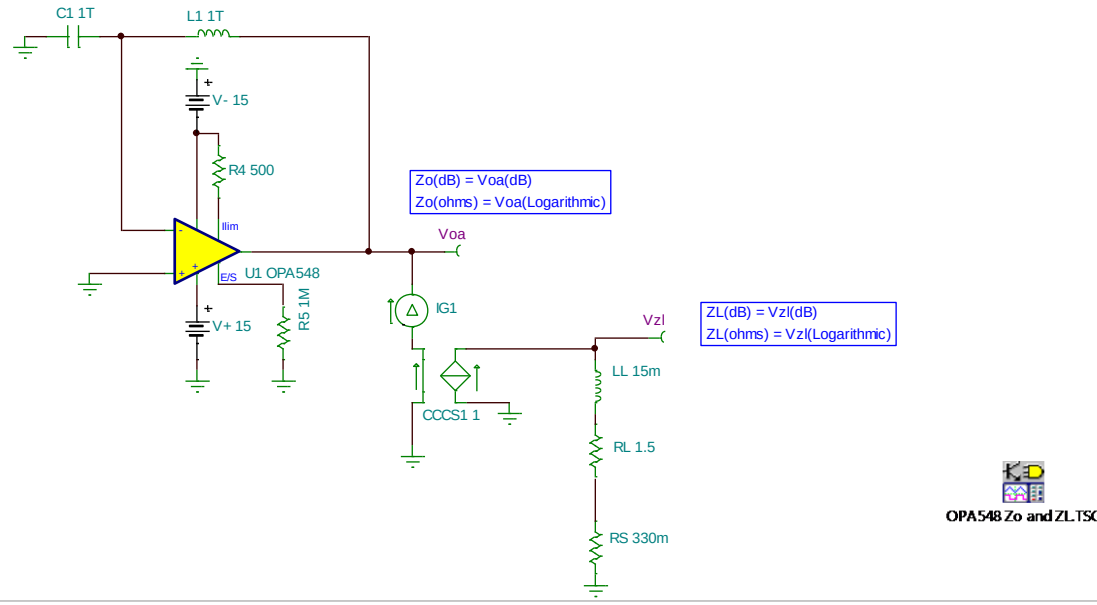
Lets investigate closer the Loaded Aol and its “hump’’ due to Zo interacting with the LL, RL + RS load. We will look in detail for this application and not for follow-on different V-to-I circuits as the procedure will be the same. The datasheet, “Unloaded Aol”, can be tested using the circuit shown here. To get a DC Linear Operating Point we put a large 1TH inductor, L1, in the feedback which will be a short at DC. For any frequency of interest, during our AC Analysis, L1 will look like an open. C1 will look like an open at DC but, for any frequency of interest, during our AC Analysis, will look like a short. We choose an inverting configuration to eliminate any CMR (Common Mode Rejection) effects from showing up in our Unloaded Aol test. If we invert Vos we will get a phase that starts at 0 degrees instead of -180 degrees. For our current purposes we will not be looking at phase, but for completeness of this test technique we mention it. With VG1 injected into the –input, Aol will be equal to –Voa.

Loaded Aol: *Unloaded Aol*



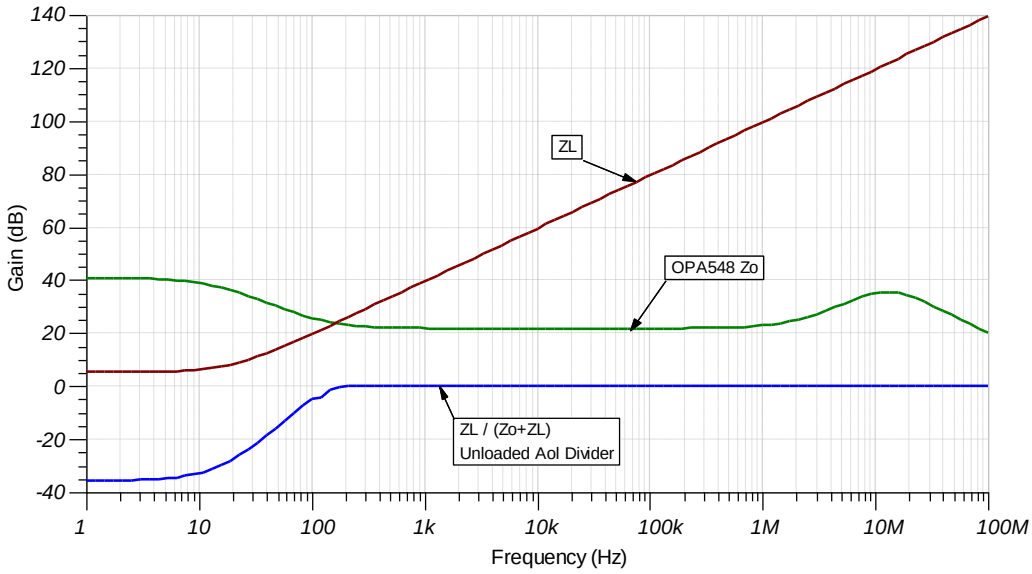
The results of our Unloaded Aol test are shown here.

Loaded Aol: *Zo and ZL*



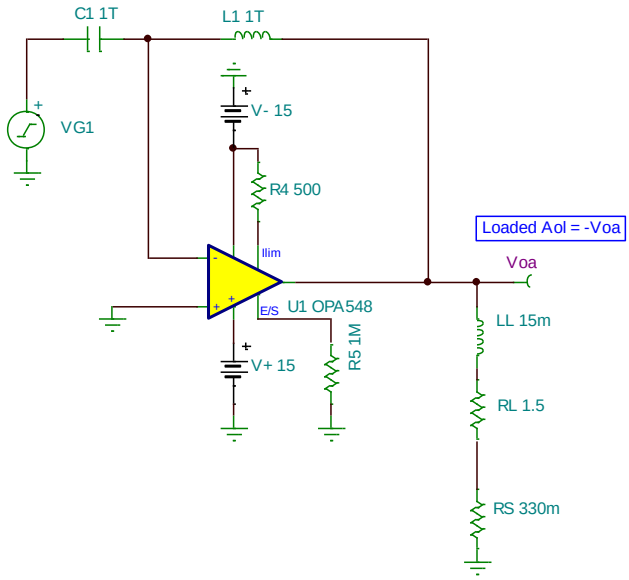
Our next step is to plot the OPA548 Zo, small signal, AC, open loop, output impedance. In addition we will also need to plot ZL, the load impedance connected to the output of the OPA548. We will need to do some post processing math on these two results so they will need to be tested in the same circuit. For an AC Analysis there can only be one excitation source, IG1. By using a Current-Controlled-Current-Source, CCCS1, we will drive the same current into the output of the OPA548 and the load impedances, ZL. Vzl will be the load impedance, ZL. The OPA548 is configured to run open loop for our AC analysis. Therefore, Vos will be Zo for the OPA548. After the AC Analysis run, both Voa and Vzl will be in dB. If we want to easily see Zo and ZL in ohms we can just change the Y-axis in the plot to Logarithmic which will remove the dB scaling resulting in ohms.

Loaded Aol: *Zo and ZL*



The results of our Zo and ZL test are shown here. Note the Unloaded Aol curve inside of the OPA548 will pass through Zo and ZL, forming an impedance divider until the Loaded Aol will appear at Voa. The “Unloaded Aol Divider”, blue curve, above shows the effect of this impedance divider action. We will eave all impedance results in dB for now as it will simplify our next calculation.

Loaded Aol

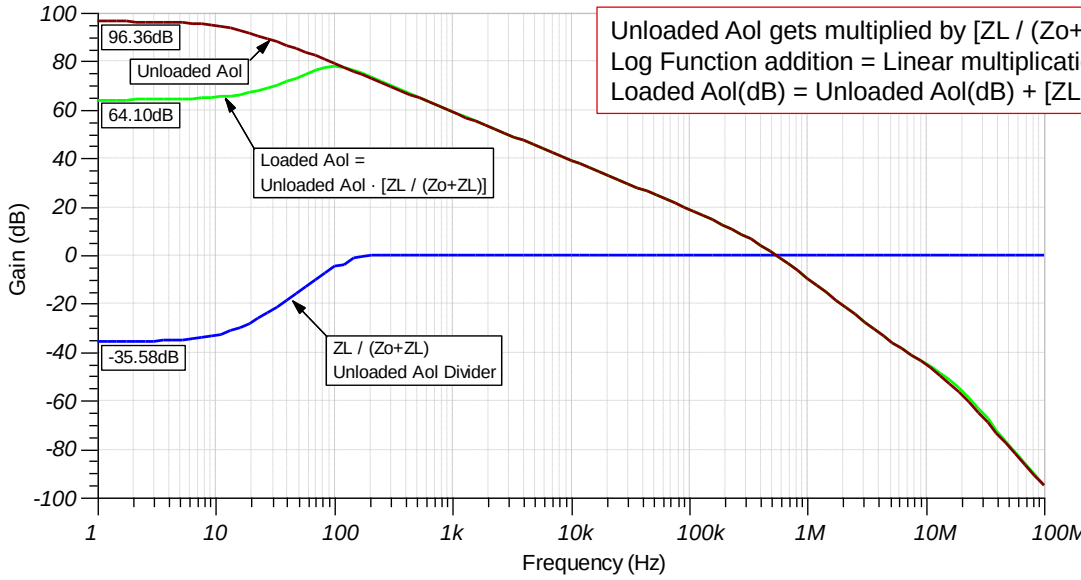


Inverting Gain configuration removes any effects of CMR on Aol.

OPA548 Loaded Aol.TSC

This test circuit will be used to plot the Loaded Aol curve with the final effects of the Unloaded Aol passing through and impedance divider of Zo and ZL.

Loaded Aol: *Final Analysis*



Slight difference due to real transistor stage in model so Unloaded Aol degrades a bit more with I_load

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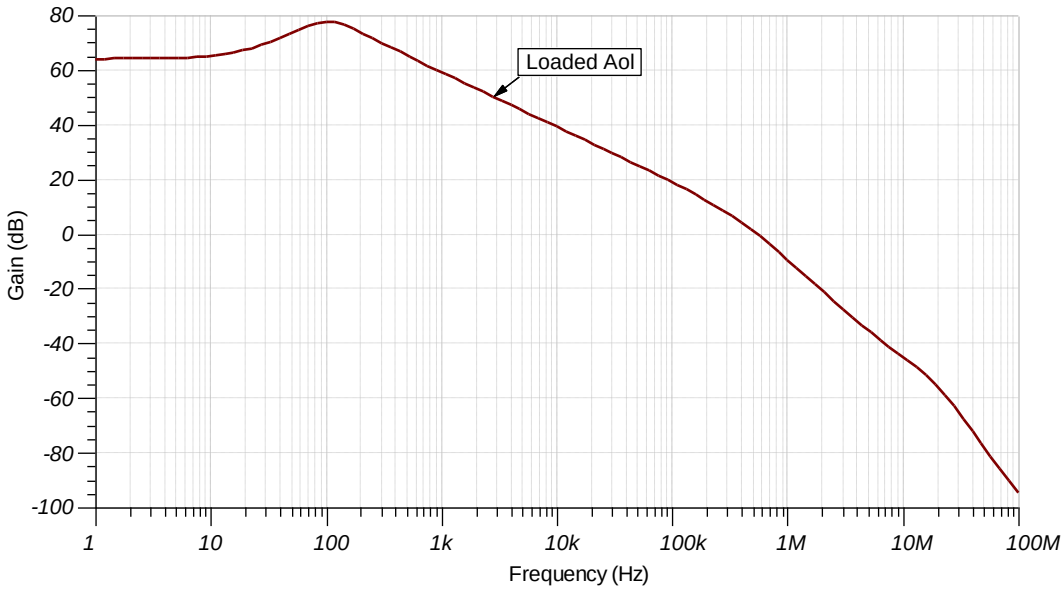
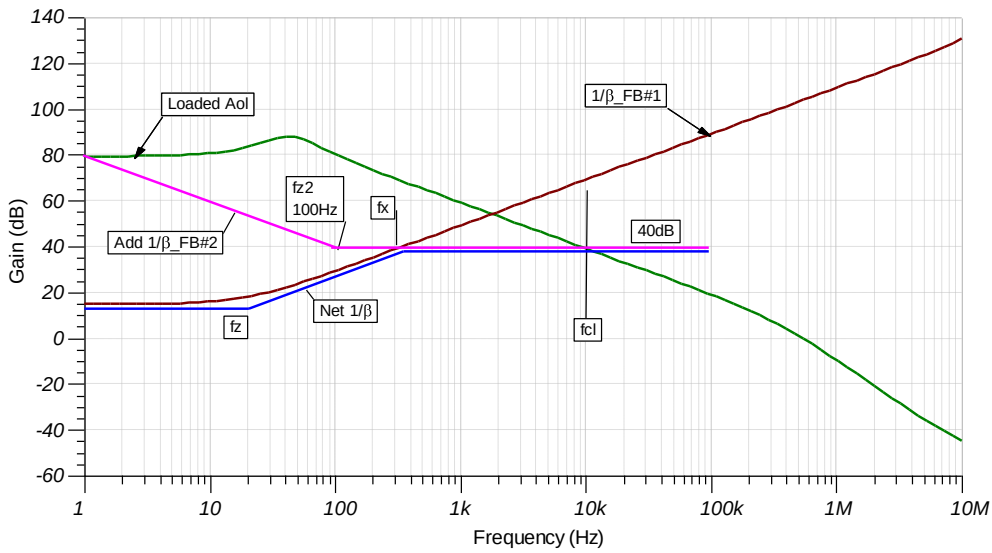
Finally, on one single plot, we see the Unloaded Aol, the Unloaded Aol Divider, and the Loaded Aol Curve. Remember that linear multiplication is addition for a Logarithmic function (like dB). The unloaded Aol curve is multiplied by the Unloaded Aol Divider by simply adding the two together. The results are close and do not account for a slight variation due the op amp macromodel using real transistors in the output and as such Aol is also changing a bit with output current.

Loaded Aol



The Loaded Aol test results are shown here.

FB#1: Aol,1/β → *Add FB#2 for Stability*



At fcl Rate-of-Closure = 20dB/decade → ***STABLE***

Net 1/β will be all the op amp "hears" for feedback.

Put fz2 at least 1/2 * fx. This allows 50% frequency shift in FB#1 or FB#2 due to external component tolerances over process and temperature to avoid the **"BIG NOT"**.

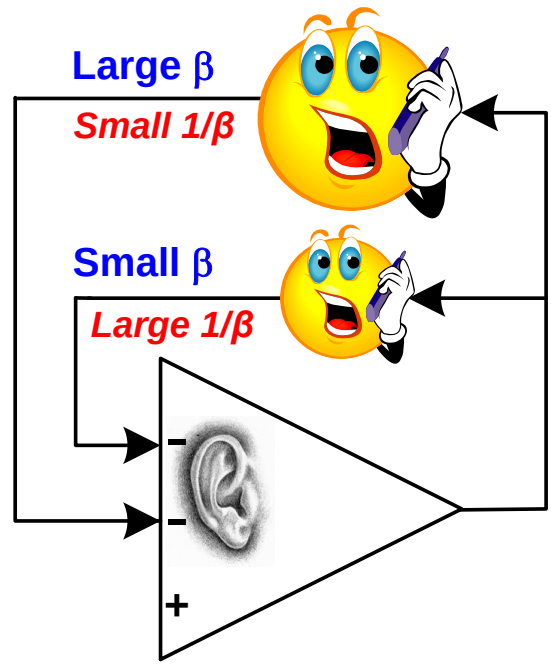
Above fx there is no current control through LL since FB#2 is not through RS (FB#1)

To make this circuit stable, we will add an additional feedback path, FB#2. We can draw in a 1/Beta_FB#2 for our desired result. At fx the 1/Beta_FB#2 will dominate and the Net 1/Beta will follow its path instead of 1/Beta_FB#1. The Net 1/Beta will always be the lowest 1/Beta in op amp circuits that use two feedback paths. This will be explained in the next slide. The location of fz2 is specifically chosen to be at last ½*fx to allow the variance of 1/Beta_FB#1 with load tolerance changes. Most inductive loads can have a tolerance on resistance of +/-20% and inductance tolerance of +/-30%. If 1/Beta_FB#2 ever crosses 1/Beta_FB#1 at a 40dB/decade difference the circuit will become marginally stable or unstable. This "BIG NOT" is described in subsequent slides. In addition we predict that the IOUT/Vin closed loop AC transfer function will begin to roll-off at fx, where 1/Beta_FB#2 begins to dominate and the –input of the op no longer "hears" 1/Beta_FB#1 which is the voltage across RS, directly related to IOUT.

Dual Feedback and 1/β: *How will the two feedbacks combine?*

Answer:

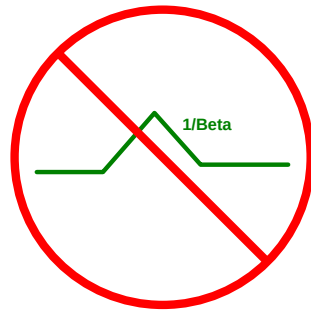
The **Largest β** (***Smallest 1/β***) will dominate!

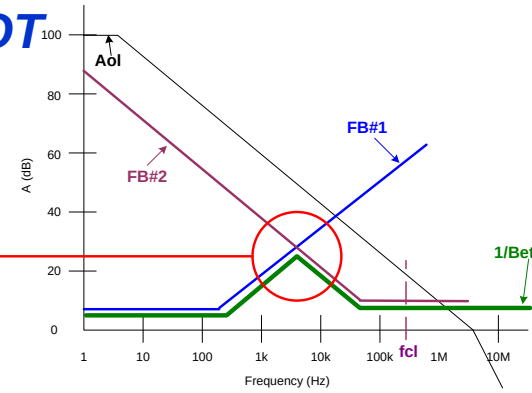


When an op amp has two separate feedback paths into its –input how will they combine? Picture the –input of the op amp as an ear listening to one person whispering (Small Beta) in the ear and another person shouting (Large Beta). Who will the ear hear? Of course it will be the loudest (Large Beta). Largest Beta wins which means smallest 1/Beta wins since they are reciprocals of each other!

Dual Feedback and the *BIG NOT*

WARNING:
This can be hazardous to your circuit!





Dual Feedback and the *BIG NOT*:

1/β Slope changes from +20db/decade to -20dB/decade

- Implies a "complex conjugate pole " in the 1/β Plot with small damping ratio, ζ.
- Implies a "complex conjugate zero" in the Aolβ (Loop Gain Plot) with small damping ratio, ζ.
- +/-90° phase shift at frequency of complex zero/complex pole.
- Phase slope from (+/-90°)/decade slope to +/-180° in narrow band near frequency of complex zero/complex pole depending upon damping ratio, ζ.
- Complex zero/complex pole can cause *severe* gain peaking in closed loop response.

When 1/β FB#1 and 1/β FB#2 cross, difference in slopes = 20dB/decade ONLY!

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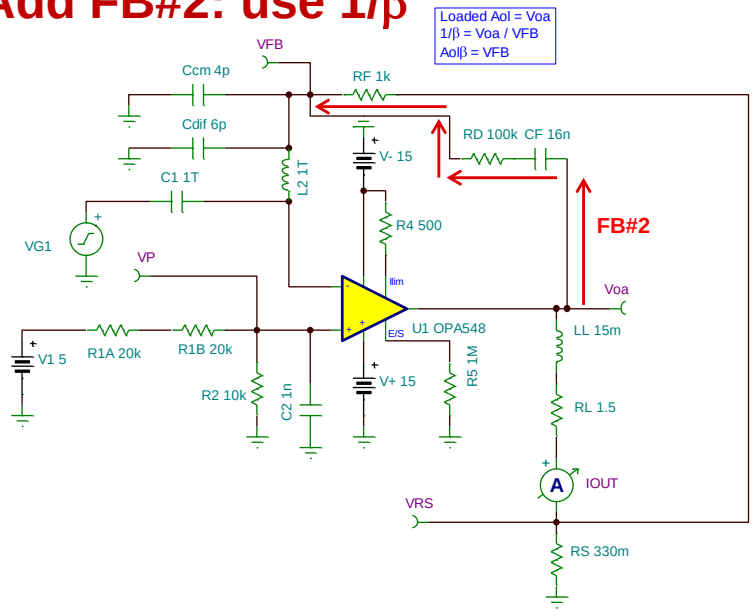
When dual feedback is used it is important not to create a more unstable circuit instead of fixing one. If 1/Beta_FB#1 and 1/Beta_FB#2 cross each other at a 40dB/decade difference in slopes it implies a resonant condition in the Net 1/Beta feedback path. Circuits compensated this way will have severe overshoot and ringing to any disturbance in the system, if not continuous oscillations. A system disturbance can be any transient on either op amp input pin, either power supply pin, or the output pin. When 1/Beta FB#1 and 1/Beta FB#2 cross, difference in slopes = 20db/decade ONLY!

Add FB#2: use 1/β



FB#2 High Frequency:

LL = open, CF = short at high frequency

$$\frac{1}{\beta}(HiF) = 40dB \rightarrow 100$$

$$\frac{1}{\beta}(HiF) = 1 + \frac{RD}{RF + RS} \approx \frac{RD}{RF} = \frac{100k}{1k}$$

FB#2 fz2=100Hz:

$$fz2 = \frac{1}{2\pi RD * CF}$$

$$100Hz = \frac{1}{2\pi 100k * CF} \rightarrow CF = 15.9nF$$

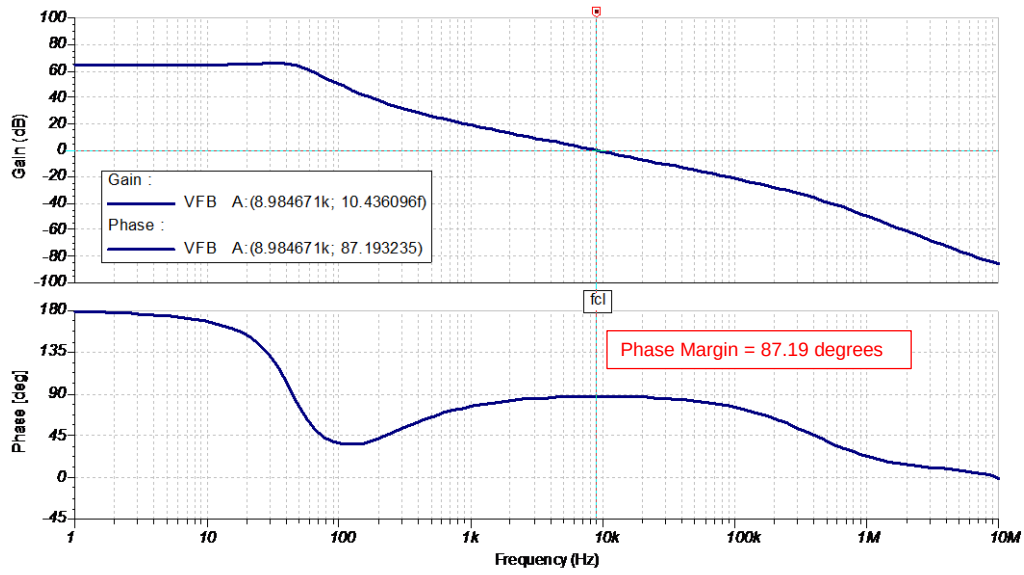
Use 16nF

OPA548 NonInv V_| FB2 Loop.TSC

Use “Noise Gain” or “Non-Inverting Gain” of op amp for FB#2 1/β

From our added 1/Beta_FB#2 plot we need to “map” it back to our circuit to see how to create it to make our circuit stable. With the addition of RD and CF we can implement 1/Beta_FB#2. At high frequency CF=short, LL=open and we can compute the desired high frequency portion of 1/Beta_FB#2 which is needed to be 40dB (100). With RF=1K we choose RD=100k. From our 1/Beta_FB#2 we need fz2 to be 100Hz. fz2 is formed by the interaction of RD and CF which yields CF=15.9nF. We will use a standard value of 16nF.

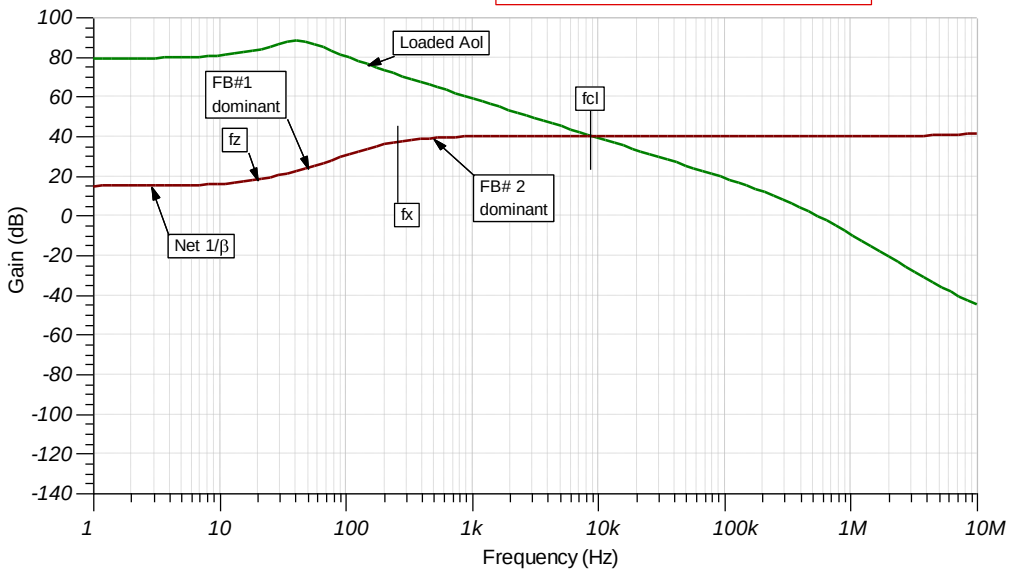
Final Loop Gain Check



With our added compensation by 1/Beta_FB#2 the loop gain simulation of our compensated circuit shows 87.19 degrees of phase margin at fcl where loop gain goes to zero.

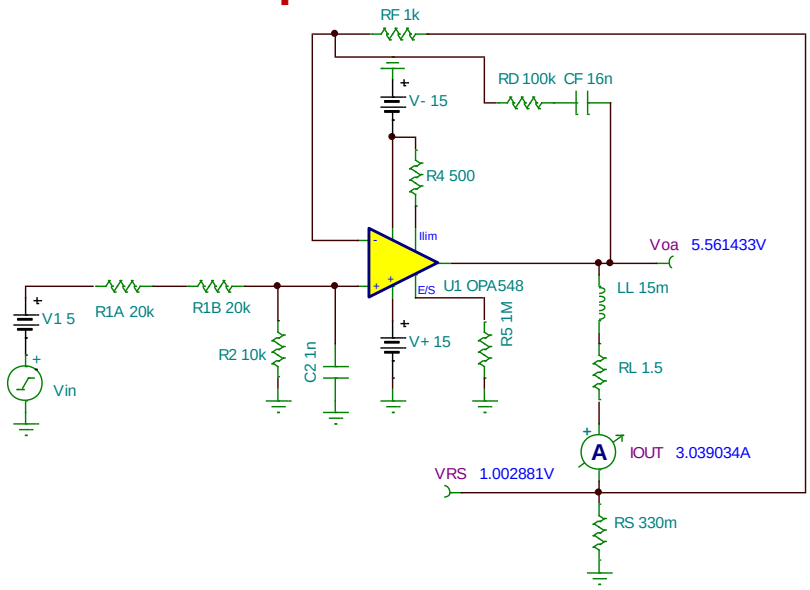
Final Aol,1/β

Net 1/β matches first order lines drawn from FB#1 & FB#2



A simulation of Loaded Aol and Net 1/Beta shows results predicted from our original drawing in of 1/Beta_FB#2 on 1/Beta_FB#1.

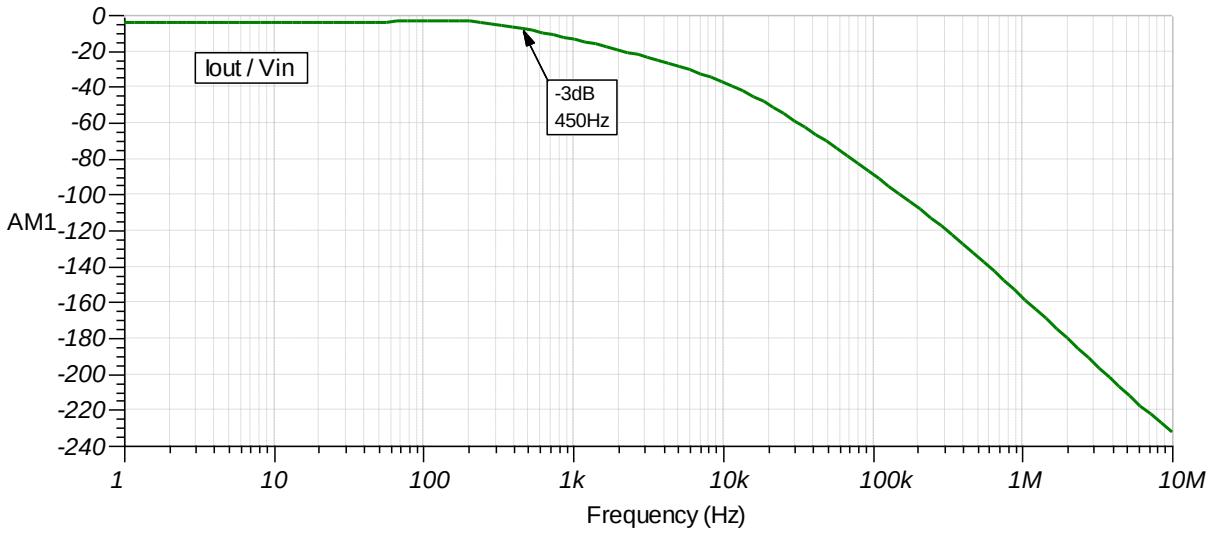
AC Closed Loop Transfer Function



OPA548 Noninv xfer.TSC

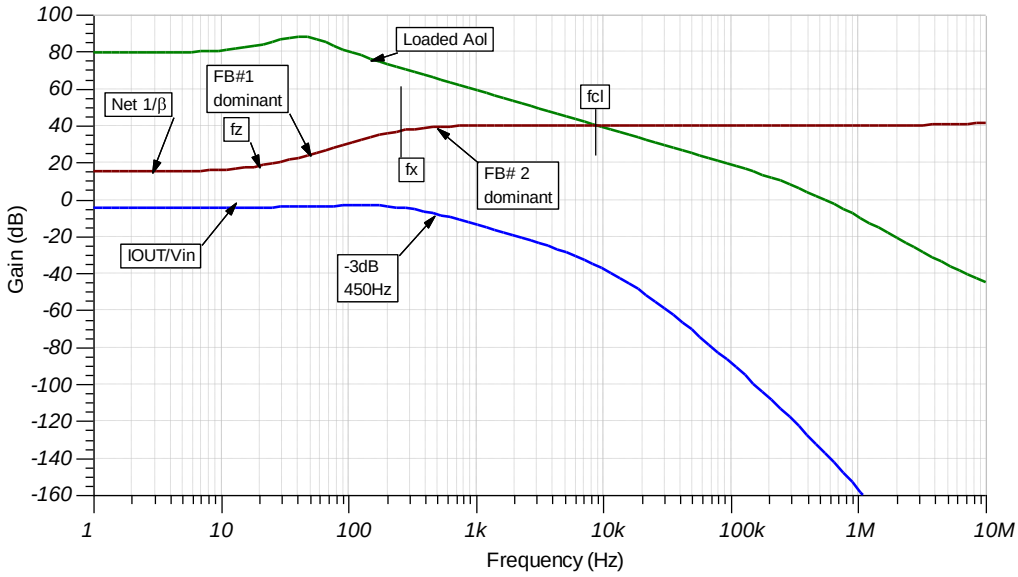
This circuit will be used to analyze IOUT/Vin, the closed loop AC transfer function, after compensating the circuit for stability.

AC Closed Loop Transfer Function



The results of the IOUT/Vin AC SPICE simulation show a -3dB frequency of 450Hz.

Iout/Vin and effects of FB#1 & FB#2



Above fx there is no current control through LL since FB#2 is not through RS (FB#1)

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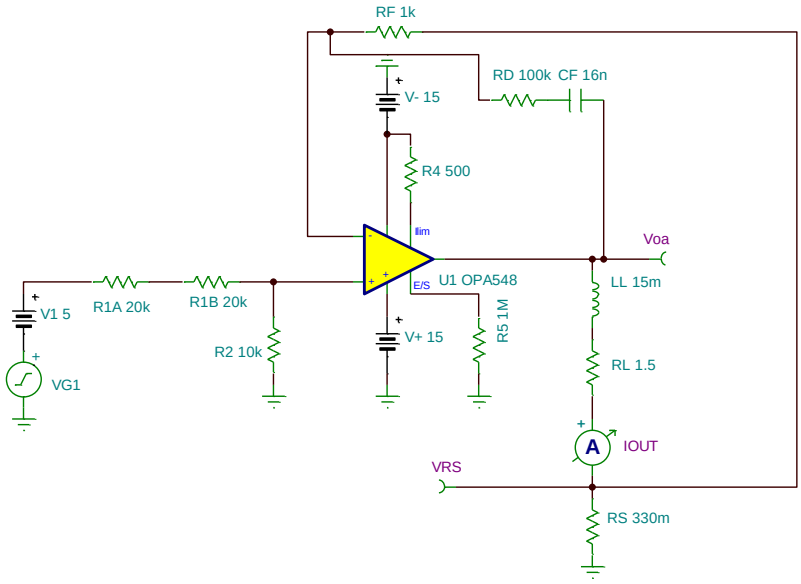
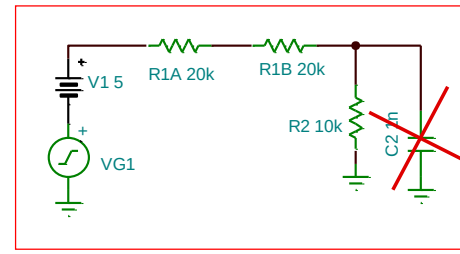
This plot shows the final closed loop AC transfer function of Iout/Vin plotted along with Aol and Net 1/Beta. At fx, 1/Beta_FB#2 begins to dominate and IOUT begins to roll off since 1/Beta_FB#1 no longer dominates.

Small Signal Transient Stability Test



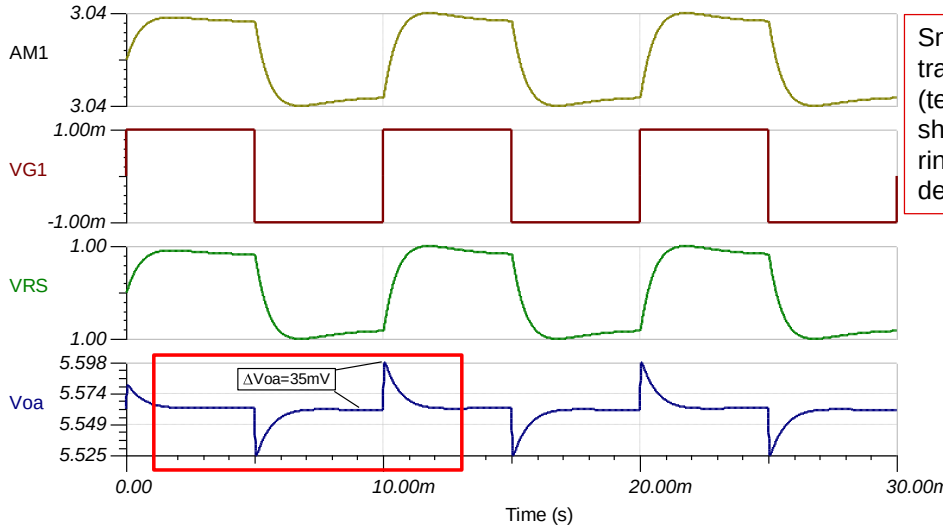
Small signal closed loop transient stability test remove C2. Need fast rising edge into +In to disturb the closed loop system for step response to indicate stability.



OPA548 Noninvtran.TSC

As a final check of our now compensated and stable circuit we will perform a small signal transient stability test on the closed loop version of our circuit. This is equivalent to looking for the damped natural response due to a step input into a closed loop system. To ensure we get a step disturbance we will need to remove C2 so that a small square wave injected into the +input will have a fast rise time. We will adjust the signal generator, V1, to cause about a 50mVp overshoot signal out of the op amp, Voa. It is important to keep this test in the small signal closed loop domain. If the op amp is made to slew by a large signal step on the output and the output hits slew rate limit then the op amp is running open loop and we will get no stability information about our circuit.

Small Signal Transient Stability Test



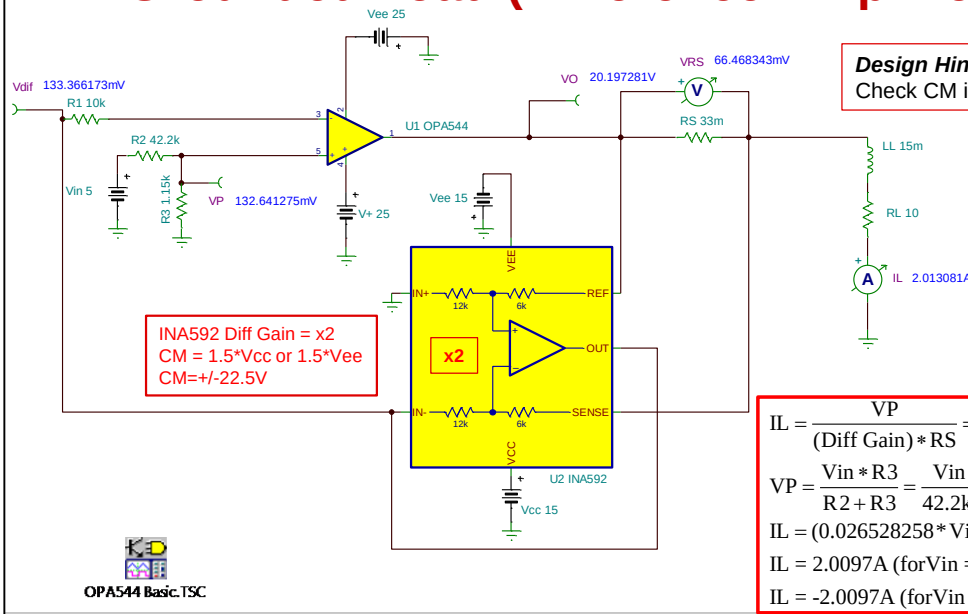
Small signal closed loop transient stability test (test with ΔVoa < 50mV) shows no oscillations or ringing → robust and stable design.

The small signal closed loop transient stability test (test with δελτα_Voa < 50mV) shows no oscillations or ringing → robust and stable design.

Agenda

- Op Amp Stability Critical Tools Review
- V-I Floating Load (Non-Inverting)
- V-I Grounded Load (Difference Amplifier)
- V-I Grounded Load (Improved Howland Current Pump)
- V-I Floating Load (Improved Howland Single Supply Bridge)
- Power Op Amp Protection
- Power Op Amp Power Dissipation
- Precision Amplifiers – Popular Power Op Amps
- Appendix

V-I Grounded Load (Difference Amplifier)



Design Hint:
Check CM input range of difference amplifier.

$$IL = \frac{VP}{(\text{Diff Gain}) * RS} = \frac{VP}{2 * 33m} = VP * 15.15151515$$

$$VP = \frac{Vin * R3}{R2 + R3} = \frac{Vin * 1.15k}{42.2k + 1.15k} = 0.026528258 * Vin$$

$$IL = (0.026528258 * Vin) * 15.15151515 = 0.401943303 * Vin$$

IL = 2.0097A (forVin = +5V)

IL = -2.0097A (forVin = -5V)

OPA544 Basic.TSC

TEXAS INSTRUMENTS

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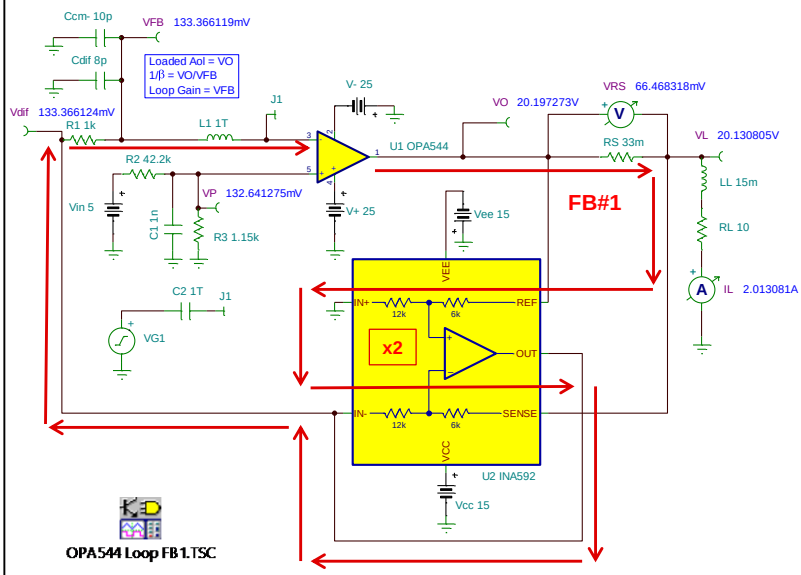
A common way to form a V-to-I circuit is the use a current sense resistor, RS, and monitor he voltage across it, since V=I*R, with a difference amplifier. The difference amplifier amplifies differential input voltage and rejects common mode voltage. The difference amplifier inputs are not high impedance. In this case we see an effective 18kohm (6k+12k) loading. Since this loading on one side will be on the output of the OPA548, which is low impedance for closed loop and, the other side will be the closed loop output impedance of the OPA548 plus 33milli-ohm, the difference amplifier will have little error contribution due to its internal resistors' loading effects. Here we will use the INA592 in a gain of x2. Depending upon how it is connected the INA592 can yield a differential gain of x2 or x1/2.

The scaling for this circuit can be analyzed by observing that the load current, IL, can be analyzed by starting at VP, the +input of the op amp. Working toward RS, VP is divided by 2 (INA592 G=x2) and will be the voltage across RS, VRS. VRS is dived by RS, 33mili-ohms to yield IL. VP is a divided down version of Vin with a scale factor of Vp = 0.026528258 * Vin. Substituting VP in terms of Vin into our IL equation we see the final transfer function of IL=0.4*Vin. So for Vin = +/-2.5V we get IL=+/-2A.

FB#1 Loop Analysis: use β

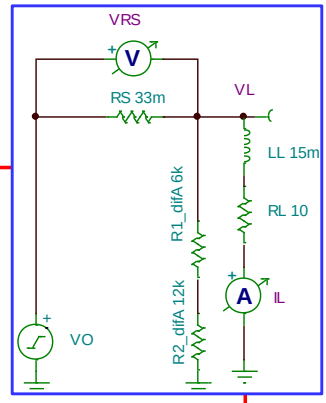


1) FB#1_1/β will be analyzed by first finding FB#1_β since his will be easier to analyze.
2) VRS/VO transfer function will be analyzed first.
3) Then VRS x Gain of INA592 will be analyzed.
4) Final result will be: Vdif = VRS x Gain.
5) Vdif = FB#1_β.

Note: Ccm & Cdif are op amp internal input common mode & differential input capacitance moved outside op amp to include any effects on 1/β. Note Cdif goes to GND since +In looks like AC short (1nF to GND) since C2 =1nF >> Cdif = 8pF.

From our previous analysis of the "V to I Floating Load (Non-Inverting), we suspect that the circuit will not be stable without some sort of compensation. First, we will start by analyzing the feedback for our desired V-to-I scaling, FB#1. It will be easier to analyze FB#1 for Beta and then invert it later for the 1/Beta curve plotted on Loaded Aol to see if it is stable. First the VRS/VO transfer function will be analyzed. Nest VRS will be gained up by the INA592 to yield the final FB#1_Beta = Vdif. Since we are breaking the loop with L1 we need to account for the common mode and differential input capacitance of the OPA544 and add them in externally as shown.

FB#1 β : VRS/VO



$\frac{VRS}{VO}$ Calculation #1

At DC Inductor LL=short:

$IL = \frac{VO}{RS + RL}$

$VRS = IL * RS$

$VRS = \frac{VO}{RS + RL} * RS$

Set VO = 1

$VRS = \frac{RS}{RS + RL} = \frac{33m}{33m + 10} = 3.289m \rightarrow -49.658dB$

Pole when LL interacts with RS+RL:

$fpa = \frac{RS + RL}{2\pi * LL} = \frac{33m + 10}{2\pi * 15m} = 106.45Hz$

A pole (fpa) causes Vrs/Vo to decrease in value.

$\frac{VRS}{VO}$ Calculation #2

At High Frequency LL=open:

$IL = \frac{VO}{RS + R1\_difA + R2\_difA}$

$VRS = IL * RS$

$VRS = \frac{VO * RS}{RS + R1\_difA + R2\_difA}$

Set VO = 1

$VRS = \frac{RS}{RS + R1\_difA + R2\_difA} = \frac{33m}{33m + 6k + 12k} = 1.8333\mu \rightarrow -114.73dB$

Zero when LL interacts with $R1\_difA + R2\_difA$:

$fza = \frac{R1\_difA + R2\_difA}{2\pi * LL} = \frac{6k + 12k}{2\pi * 15m} = 190.98kHz$

A zero (fza) causes Vrs/Vo to increase in value.

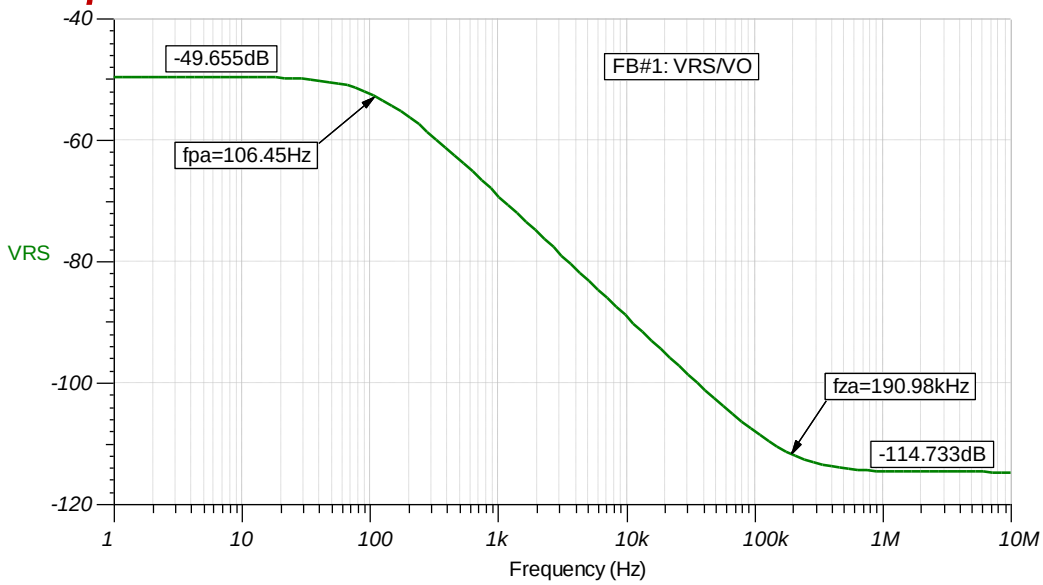
VRS at DC:

Relative to Vo, the output of the OPA544, VRS is computed at DC with LL=short. The load current, IL = Vo/(RS+RL), since RS and RL are << R1_difA and R2_difA. VRS=IL*RS. Substituting we see at DC that VRS = RS/(RS+RL) and is -49.658dB. As frequency increases there will be a pole when LL interacts with RS+RL at 106.45Hz.

VRS at High Frequency:

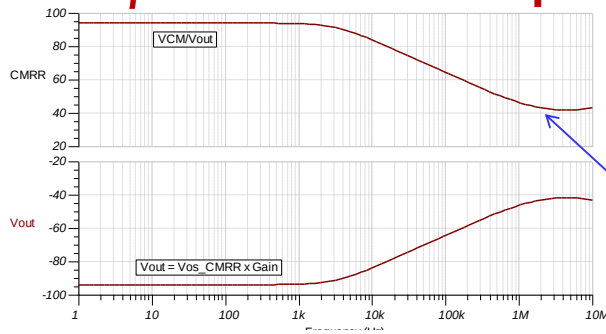
Relative to Vo, the output of the OPA544, VRS is computed at High Frequency with LL=open. The load current, IL = Vo/(RS+R1_difA+R2_difA). VRS=IL*RS. Substituting we see at high frequency that VRS = RS/(RS+R1_difA+R2_difA) and is -114.73dB. Coming fro high frequency to low frequency, there is a zero when LL interacts with R1_difA+R2_difA at 190.98kHz.

FB#1 β : VRS/VO

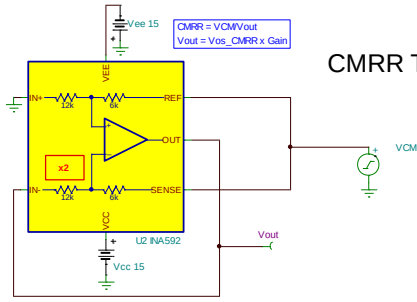


For VRS/VO the simulation results above confirm the low frequency gain = -49.658dB, a pole at fpa=106.45Hz, a zero at fza=190.98kHz, and a high frequency gain = -114.733

FB#1 β : Difference Amplifier CMRR effects

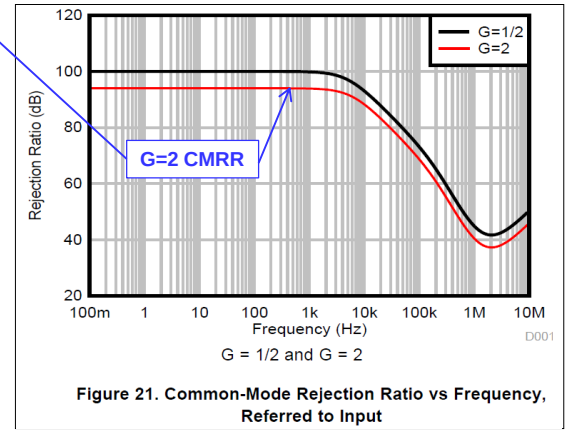


CMRR INA592.TSC



CMRR Test Circuit

Datasheet CMRR Curves

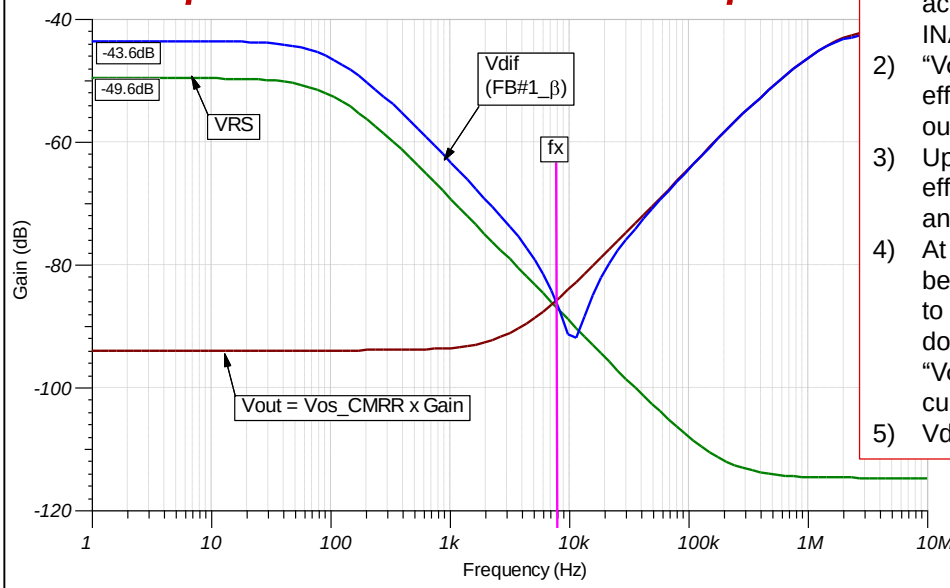


G = 1/2 and G = 2

Figure 21. Common-Mode Rejection Ratio vs Frequency, Referred to Input

The test circuit above checks the op amp macromodel against the datasheet curve of CMRR. The Vout plot shows the effect of Vout as a result of the increase in input offset voltage due to CMRR over frequency times the gain of x2.

FB#1 β : VRS x Gain = Vdif = β



1) "VRS" is voltage feedback across RS over frequency into INA592 Difference Amplifier.
2) "Vout = Vos_CMRR x Gain" is effect of CMRR gained up to the output of INA592.
3) Up to fx CMRR is high so its Vos effects are small, VRS is high and Vdif = 2 x VRS.
4) At frequencies above fx, VRS becomes smaller and Vout, due to reducing CMRR, becomes dominant. Now Vdif follows the "Vout = Vos_CMRR x Gain" curve.
5) Vdif = FB#1_β.

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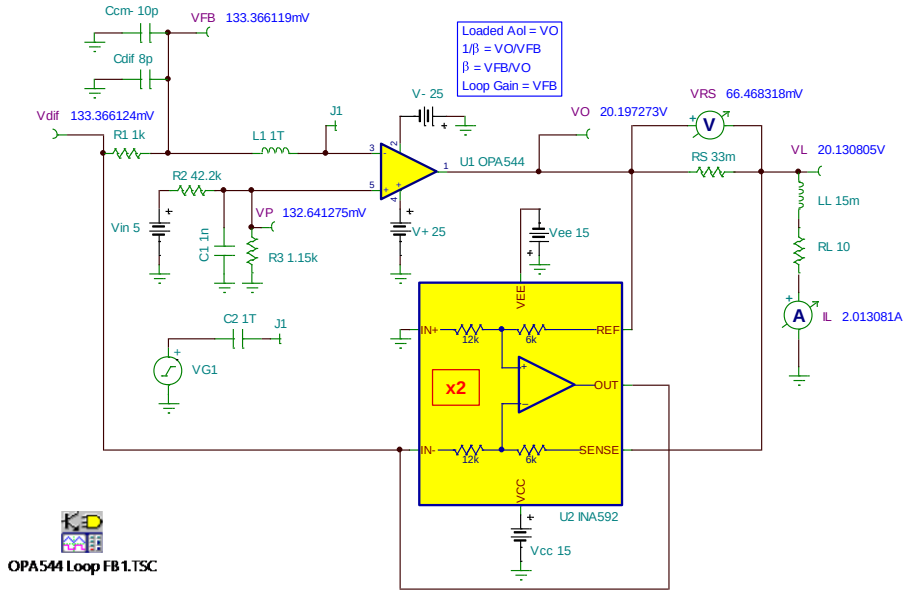
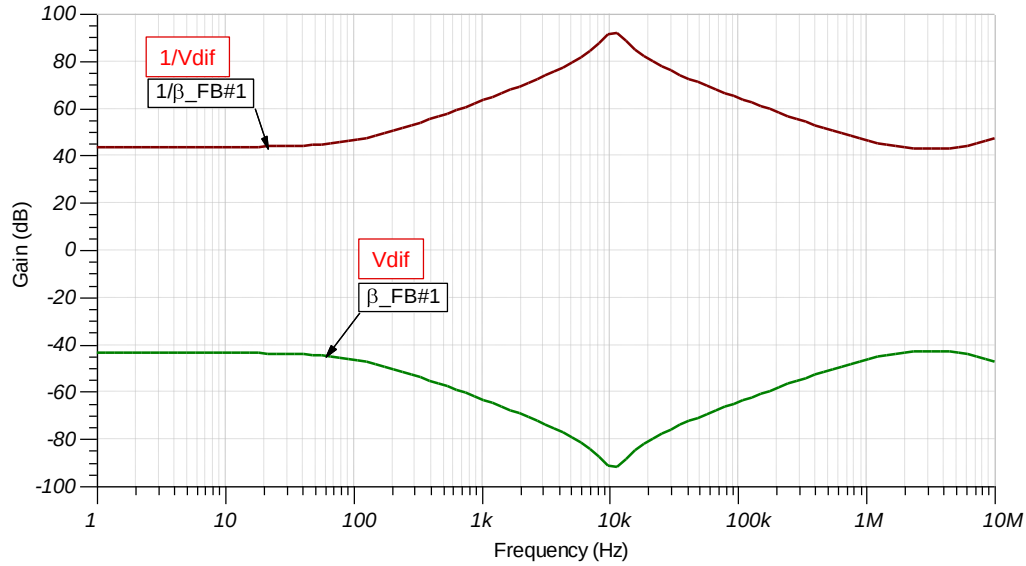
Here we plot the VRS curve along with the "Vout = Vos_CMRR x Gain" curve. Also plotted is the net output of the INA592 difference amplifier, Vdif.
From DC to about fx, Vdif = Vrs x 2, since the CMRR is very large and the Vos_CMRR x Gain values are very small in comparison to VRS x 2. Above fx, the VRS is small compare to the Vos_CMRR x Gain values and the CMRR dominates as shown in the Vdif curve.

FB#1: β & 1/β



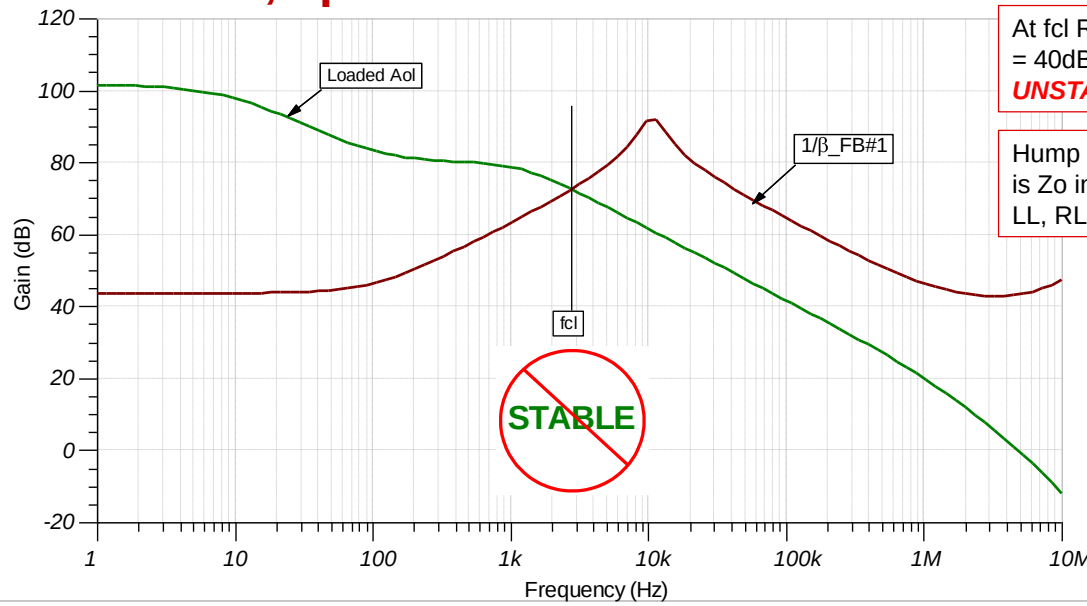
From our loop gain circuit, repeated here, we see than FB#1_Beta = Vdif and FB#1_1/Beta = 1/Vdif.

FB#1: β & 1/β



The loop gain simulation results yield FB#1_Beta = Vdif and FB#1_1/Beta = 1/Vdif.

FB#1: Aol,1/β

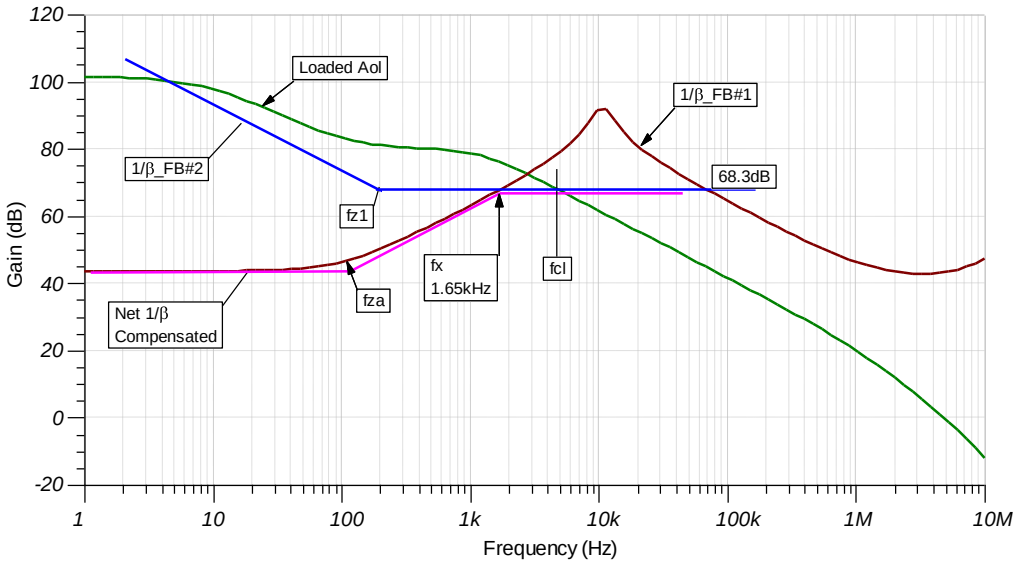


At fcl Rate-of-Closure = 40dB/decade → ***UNSTABLE***

Hump in Loaded Aol is Zo interacting with LL, RL+RS load.

Our loop gain plot also yields the Loaded Aol curve. 1/Beta_FB#1 plotted on Loaded Aol curve yields a 40dB/decade rate-of-closure at fcl where loop gain goes to 0db indicating an UNSTABLE circuit! Note the hump in the Aol curve is due to Zo interacting with LL and RL. The details will be skipped here but the technique of proving and analyzing this are the same as those used for the "V to I Floating Load (Non-Inverting)".

FB#1: A_{OL},1/β → *Add FB#2 for Stability*



At fcl Rate-of-Closure = 20dB/decade → ***STABLE***

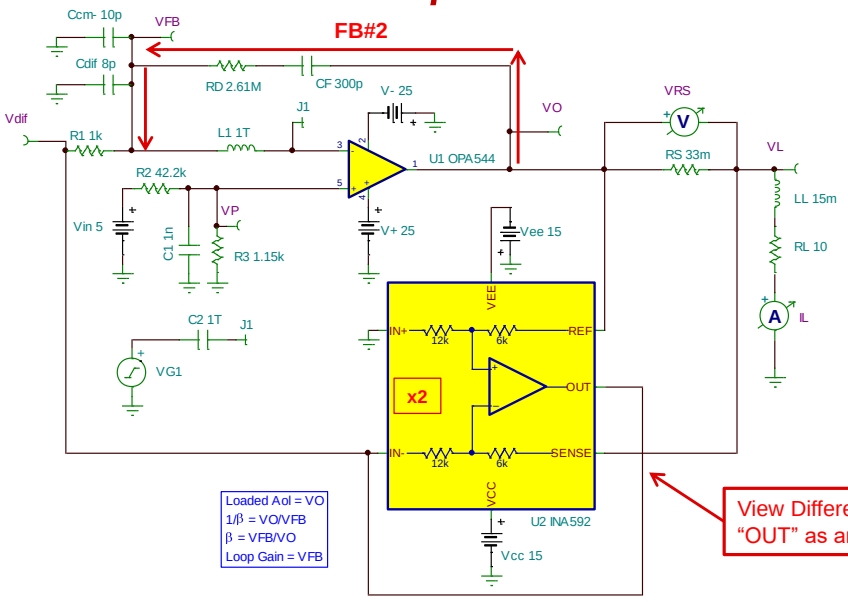
Net 1/β will be all the op amp "hears" for feedback.

Put fz1 at least 1/2 * fx. This allows 50% frequency shift in FB#1 or FB#2 due to external component tolerances over process and temperature to avoid the **"BIG NOT"**.

Above fx there is no current control through LL since FB#2 is not through RS (FB#1)

Our next step is to add 1/Beta_FB#2 to create a NET 1/Beta Compensated that will intersect the Loaded Aol at a rate-of-closure = 20dB/decade.
We want to put fz1, in the 1/Beta_FB#2 curve, at least ½ * fx to allow for tolerance variances in LL (+/-30%) and RS(0.1%)+RL(+/-20%) which form fza. From this plot we see the high frequency gain of 1/Beta_FB#2 is 68.3dB and we graphically choose fz1 = 200Hz.

Add FB#2: use 1/β



FB#2 High Frequency:

LL = open, CF = short at high frequency

$$\frac{1}{\beta}(\text{HiF}) = 68.3\text{dB} \rightarrow 2600$$

$$\frac{1}{\beta}(\text{HiF}) = \frac{RD}{R1} = \frac{RD}{1k} = 2600 \rightarrow RD = 2.6M$$

FB#2 fz1=200Hz:

$$fz1 = \frac{1}{2\pi RD * CF}$$

$$200\text{Hz} = \frac{1}{2\pi * 2.6M * CF} \rightarrow CF = 306\text{pF}$$

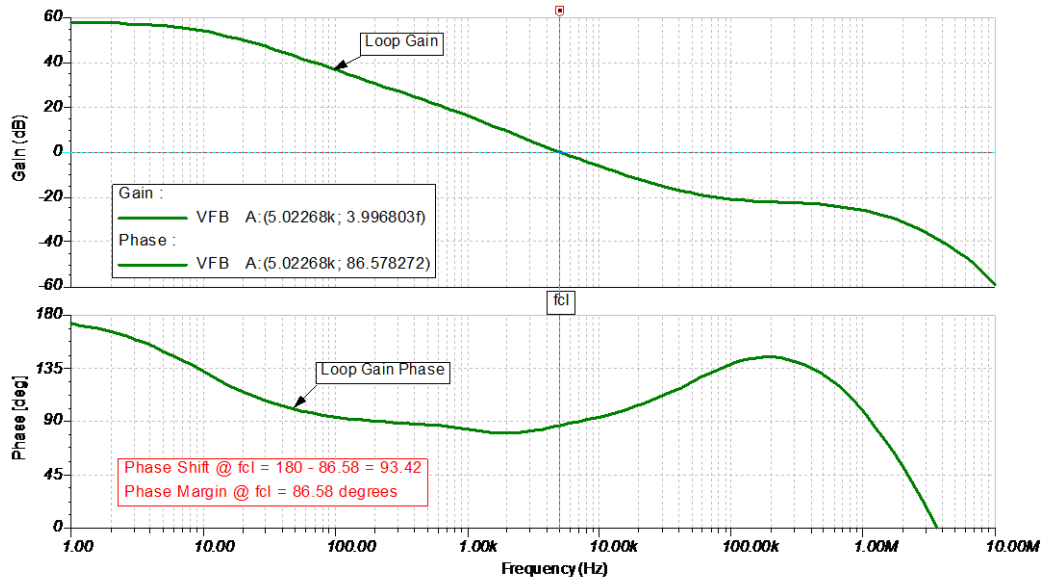
Use 300pF

OPA544 Loop FB2.TSC

Use "Noise Gain" or "Non-Inverting Gain" of op amp for FB#2 1/β

Now we need to add FB#2 components into our basic circuit. If we add RD and CF, we can analyze from the desired high frequency gain of 1/Beta_FB#2 the value for RD and the desired value for CF based on the fz1 needed to prevent the "BIG NOT". For the desired high frequency 1/Beta we will use Rd/R1 with the desired value of RD=2.6Meg-ohm. Note that this will be close enough as we know the actual 1/Beta = 1 + Rd/R1. fz1 is determined by the interaction of RD and CF and determines CF=300pF.

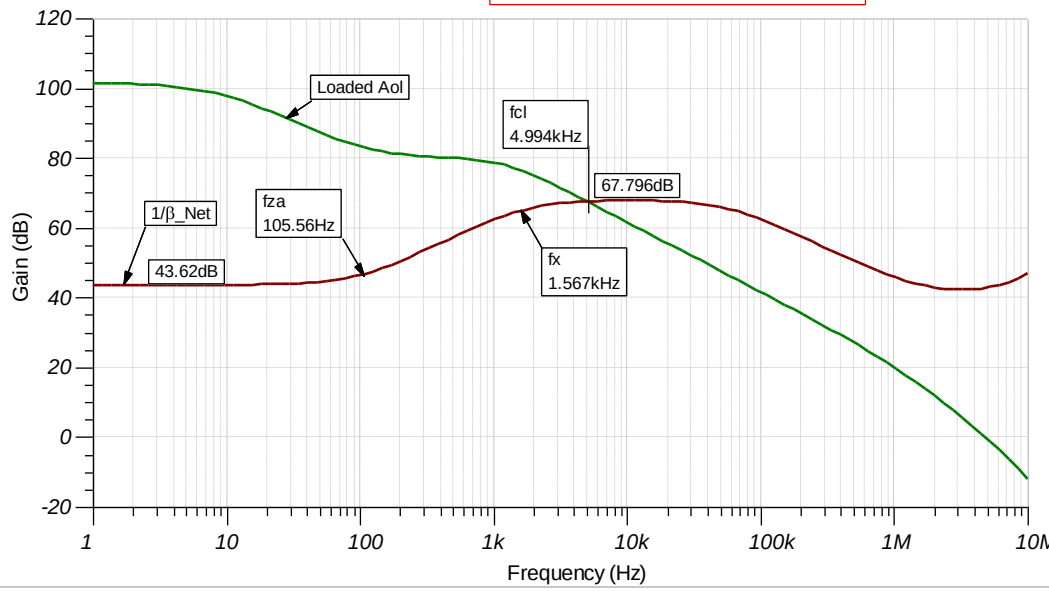
Final Loop Gain Check



With our compensation of RD and Cf we see the final loop gain phase margin plot here with loop gain phase margin at fcl, where loop gain goes to 0dB, to be 86.58 degrees.

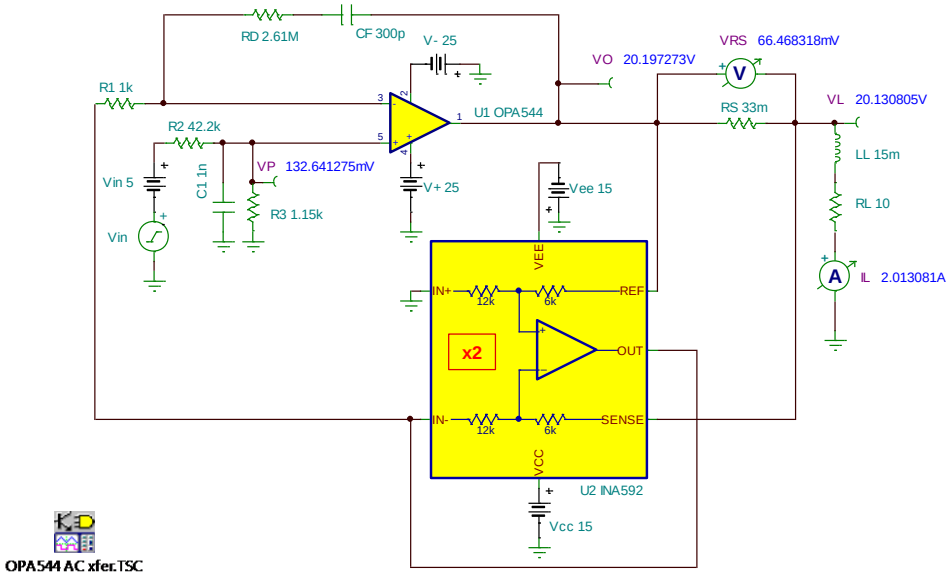
Final A_{OL},1/β

Net 1/β matches first order lines drawn from FB#1 & FB#2



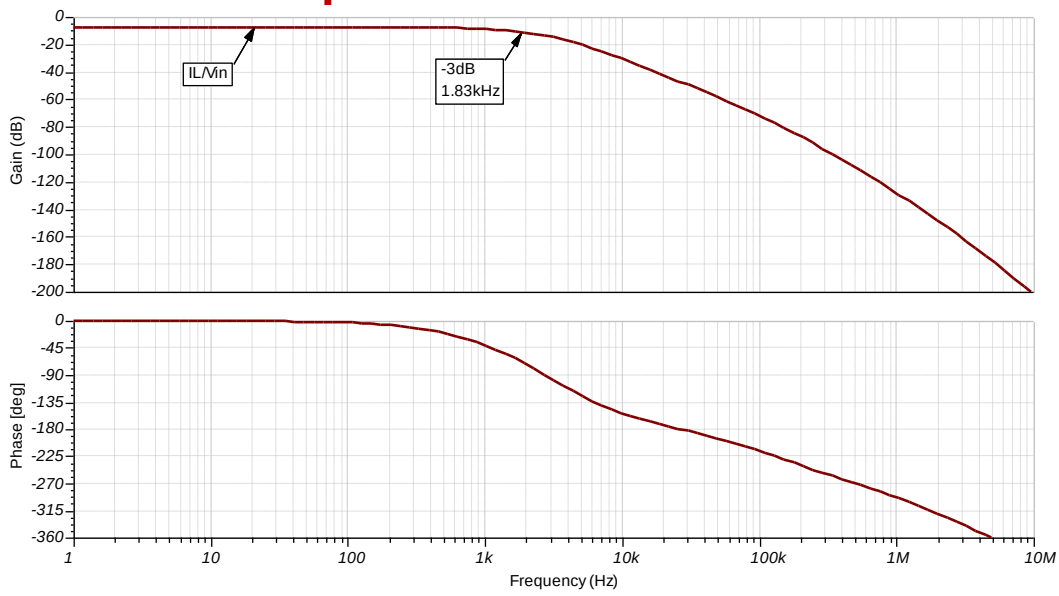
When we plot 1/Beta_Net n the loaded Aol curve we see the predicted results from our analysis of 1/Beta_FB# 1 and 1/Beta_FB#2.

AC Closed Loop Transfer Function: IL/Vin



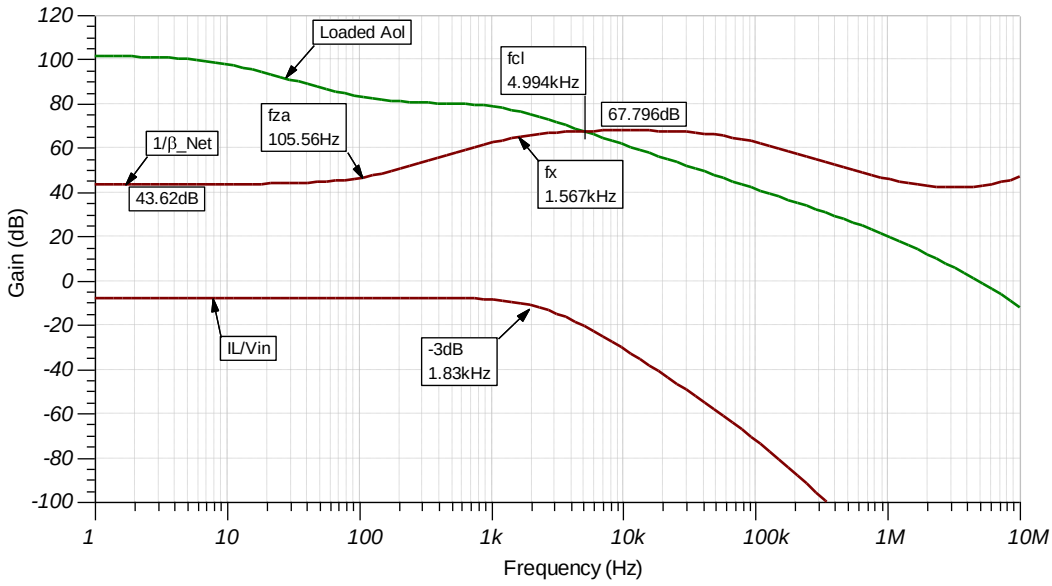
The compensated closed loop AC transfer function of IL/Vin will be simulated using this test circuit.

AC Closed Loop Transfer Function: IL/Vin



The closed loop AC transfer function , IL/Vin is shown here to have a -3dB point at 183kHz. Our original first order sketch of 1/Beta_FB#2 on 1/Betas_FB#1 had predicted their intersection at 1.65kHz. Where 1/Beta_FB#2 intersects 1/Beta_FB#1 is the point at which the accuracy of current across VRS will begin to be reduced as the op amp will begin to listen only to FB#2.

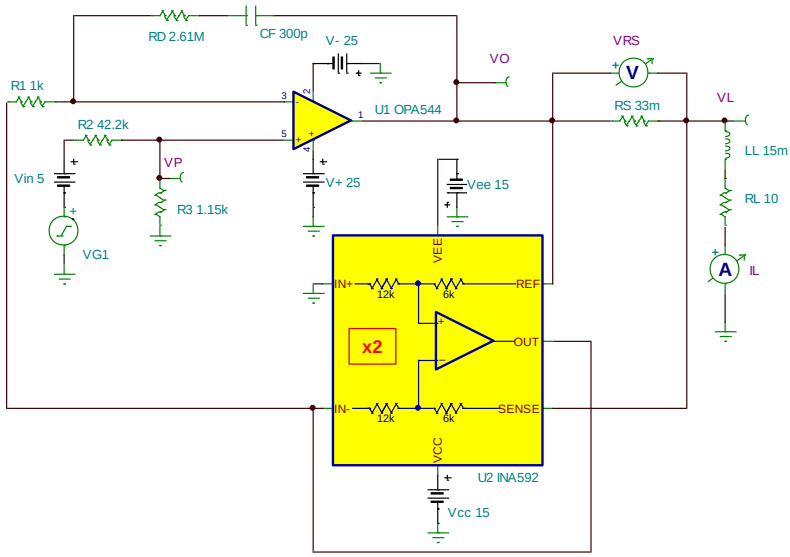
Iout/Vin and effects of FB#1 & FB#2



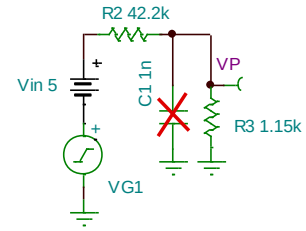
Above fx there is no current control through LL since FB#2 is not through RS (FB#1).

Here we see in the 1/Beta_Net plot the effect of FB#2 at fx=1.567kHz. This causes the IL/Vin closed loop AC transfer function to start to roll-off with a -3dB drop at 1.83kHz.

Small Signal Transient Stability Test



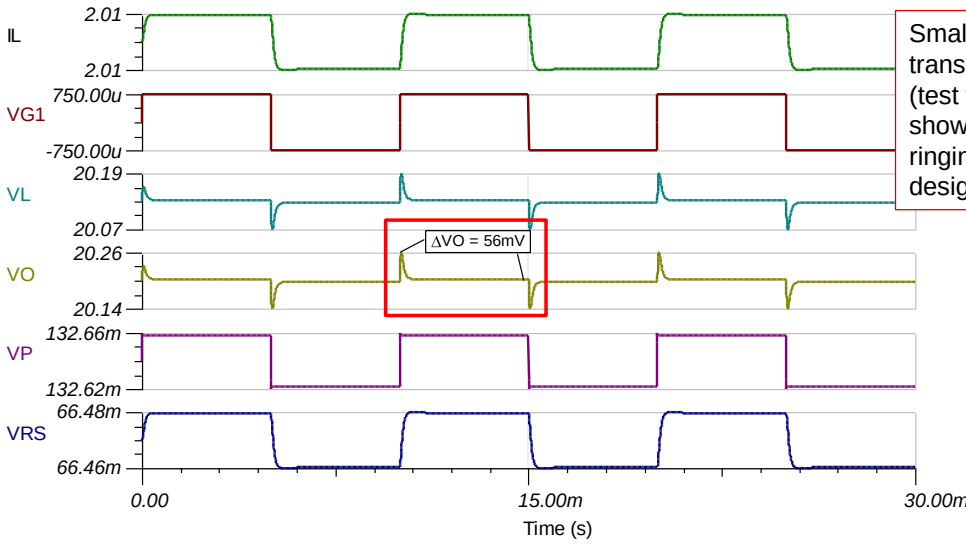
Small signal closed loop transient stability test remove C1. Need fast rising edge into +In to disturb the closed loop system for step response to indicate stability.



OPA544 tran.TSC

Our final test for stability will be a closed loop, small signal, transient test. To observe the effects of a step disturbance and the circuit's damped natural response we will remove C1 and apply a small signal step input, adjusted such that VO<100mpp, to keep the disturbance inside of the small signal domain and the loop closed.

Small Signal Transient Stability Test



Small signal closed loop transient stability test (test with ΔVO ≈< 50mV) shows no oscillations or ringing → robust and stable design.

The result of our small signal, transient stability test shows VO with no severe ringing and its voltage <100mVpp.

Agenda

- Op Amp Critical Stability Tools Review
- V-I Floating Load (Non-Inverting)
- V-I Grounded Load (Difference Amplifier)
- V-I Grounded Load (Improved Howland Current Pump)
- V-I Floating Load (Improved Howland Single Supply Bridge)
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- Power Op Amp Power Dissipation
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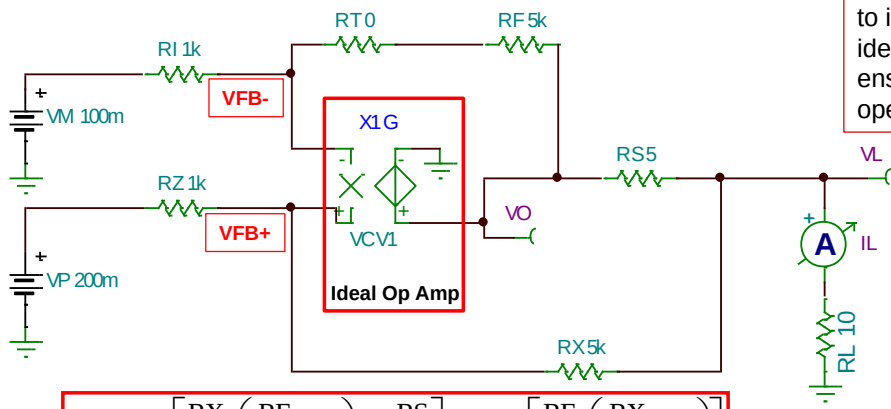
V-I Grounded Load (Improved Howland Current Pump) IL Accuracy Circuit

RT allows for trim to optimize Z_{OUT} to its highest value to approach an ideal current source. Need to ensure VBF- > VFB+ for stable operation.



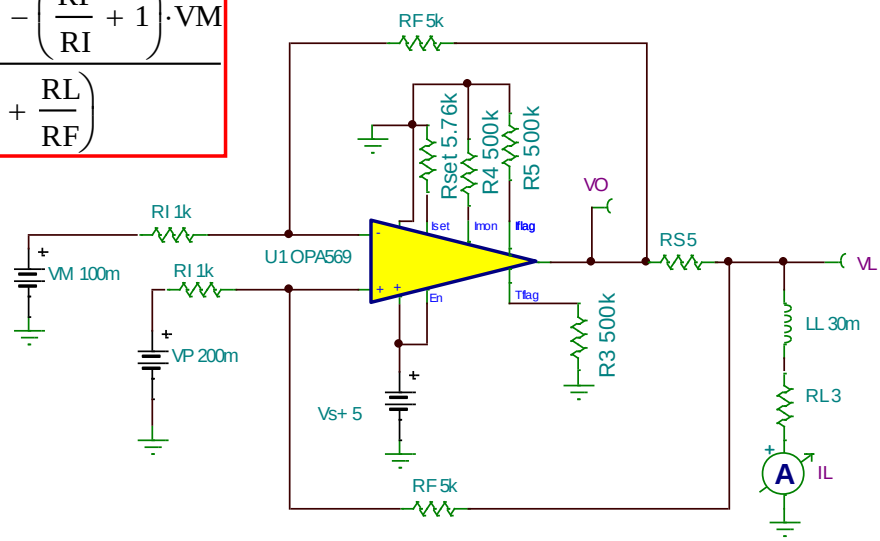
$$IL := \frac{VP \cdot \left[\frac{RX}{RZ} \cdot \left(\frac{RF}{RI} + 1\right) + \frac{RS}{RZ}\right] - VM \cdot \left[\frac{RF}{RI} \cdot \left(\frac{RX}{RZ} + 1\right)\right]}{\left[\frac{RS}{RL} \cdot \left(1 + \frac{RX}{RZ}\right) + \left(\frac{RS + RX}{RZ}\right) - \frac{RF}{RI}\right] \cdot RL}$$

Our next V-to-I circuit topology will be for a grounded load using the Improved Howland Current Pump. RL as shown can be a grounded load. RS senses the current through RL. There is a differential feedback across RS to the –input and +input of the op amp. Note that RT in some applications can be adjusted to increase the output impedance of the entire circuit to make it resemble closer to an ideal current source, with high output impedance. However, to keep the circuit stable it must be ensured that there is always more feedback to the –input of the op amp than to the +input of the op amp. The basic circuit function is to take the difference in the input voltages, VP and VM, gain it up and differentially impress it across RS which forces the scaled current through RL. At first look the exact equation for IL loks complex. There are several practical assumtpions we will make to simplify this equation.

Improved Howland Current Pump: *General Equation*

$$IL := \frac{VP \cdot \left[\left(1 + \frac{RF}{RI}\right) + \frac{RS}{RF}\right] - \left(\frac{RF}{RI} + 1\right) \cdot VM}{RS \cdot \left(1 + \frac{RI}{RF} + \frac{RL}{RF}\right)}$$

General Equation:
Set RX=RF, RZ=RI
Set RT=0

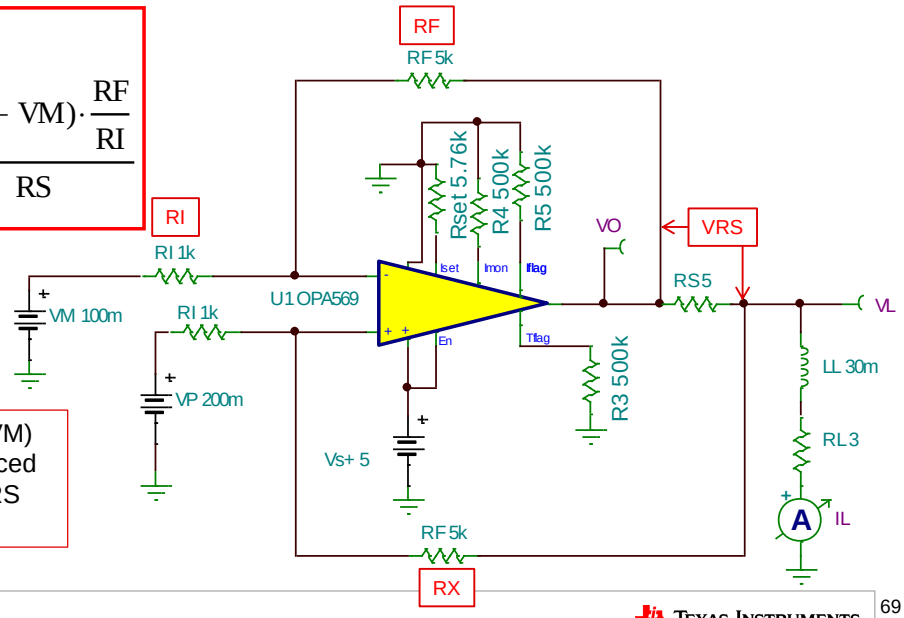


To simplify the Improve Howland Current Pump general equation to a practical form we will set RX=RF, RZ=RI, and RT=0.

Improved Howland Current Pump: *Simplified Equation*

Assume:
RF = RX
RI = RZ
RF>>RS
RF>>RL

$$IL := \frac{(VP - VM)\cdot\frac{RF}{RI}}{RS}$$



Input command voltage (VP-VM) is gained up by RF/RI and forced across RS. VRS divided by RS becomes IL.

The result of our simplification shows that (Vp-VM) will be gained up by RF/RI and differentially impressed across RS generating a voltage VRS which then forces IL=VRS/RS. For practical implementations of this circuit RF=RX, RI=RZ, RF>>RS, and RF>>RL.

Improved Howland Current Pump: V-I DC Accuracy Calculations

RT	RF	RX	RI	RZ	RS	RL	*IL*	*VL*	*VO*	AM1 Sensitivity (%)	Comments
2.858407	**5000**	**5000**	**1000**	**1000**	**5**	**10**	**0.100000052**	**1.000000100**	**1.500667000**	**0.000000000**	Rt adjusted for Ideal IL
0	5000	5000	1000	1000	5	10	0.099866893	0.998668931	1.498669000	0.133158931	Rt=0, Nominal Values
2.858407	***5050***	5000	1000	1000	5	10	0.102371216	1.023712000	1.536255000	-2.371162767	1% Resistor Changes
2.858407	5000	***5050***	1000	1000	5	10	0.098700599	0.987005991	1.481159000	1.299452324	1% Resistor Changes
2.858407	5000	5000	***1010***	1000	5	10	0.097727653	0.977276527	1.466563000	2.272397818	1% Resistor Changes
2.858407	5000	5000	1000	***1010***	5	10	0.101353602	1.013536000	1.520981000	-1.353549296	1% Resistor Changes
2.858407	5000	5000	1000	1000	***5.05***	10	0.099009365	0.990094651	1.490756000	0.990686485	1% Resistor Changes
2.858407	5000	5000	1000	1000	5	***10.1***	0.099999329	1.009993000	1.510665000	0.000723	1% Resistor Changes
0	***5050***	***4950***	***990***	***1010***	***4.95***	***10***	***0.108995522***	***1.089955000***	***1.630222000***	*-8.995465322*	***1% Worst Case w/RT=0)***
2.858407	***5050***	***4950***	***990***	***1010***	***4.95***	***10***	***0.109152449***	***1.091524000***	***1.632570000***	*-9.152392241*	***1% Worst Case w/RT=Nom)***

1% Resistors (w/RT=0) could yield only 9% Accuracy at T=25°C
0.1% Resistors (w/RT=0) could yield only 0.9% Accuracy at T=25°C

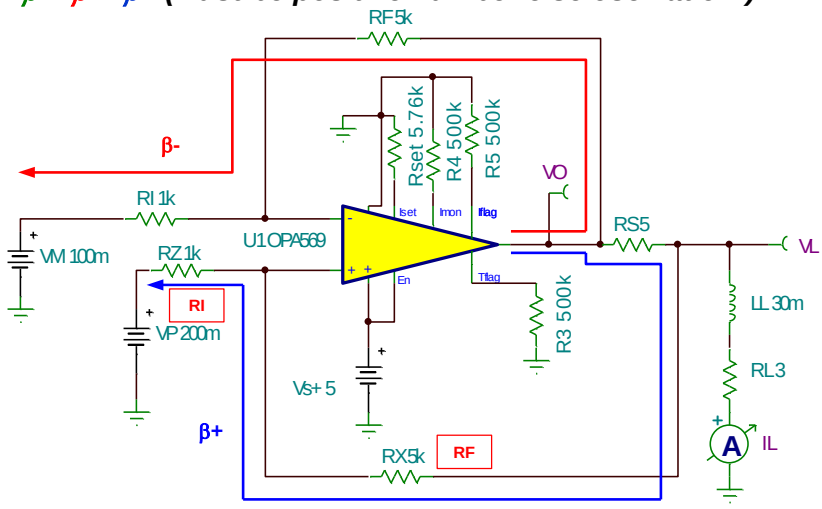
Still useful for V-I control in Motors/Valves → Vin to Iout → Torque Out Control. Outer position feedback adjusts Vin to reach final position.

The improved Howland Current Pump is not inherently the most accurate V-to-I circuit. As shown above you can achieve worst case accuracy of 9% using 1% tolerance resistors and 0.9% using 0.1% tolerance resistors. For many applications this is still a preferred circuit because of its simplicity and component count. Remember that torque in a motor or valve is proportional to current . Some systems have an outside positioning feedback lop and want to command changes in torque to move to a new position. Here the Improved Howland Current Pump can drive a grounded load and provide the V-to-I conversion.

Improved Howland AC Analysis

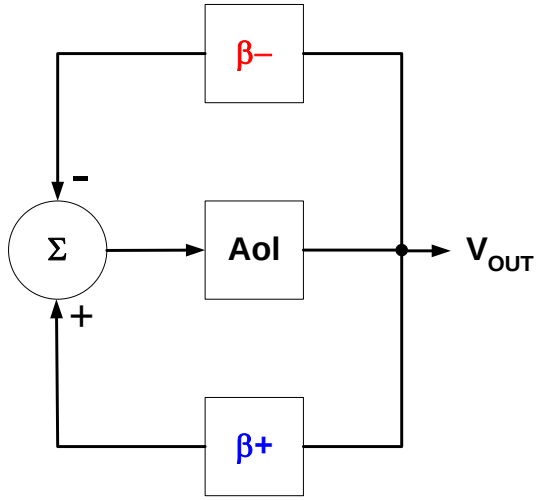
Op Amp sees differential [(-IN) – (+IN)] feedback

β = β- - β+ (Must be positive number else oscillation!)



There are two different feedback paths in the Improved Howland Current Pump, Beta- and Beta+. The difference between Beta- and Beta+ is the differential voltage fed back to the op amp input terminals. Beta- must always be greater than Beta+ for stable operation. In the circuit above Beta- will always be more positive than Beta+, since Beta- feeds back directly from the op amp output and Beta+ as an additional voltage drop, now matter how small from current passing through RS.

Improved Howland AC Analysis

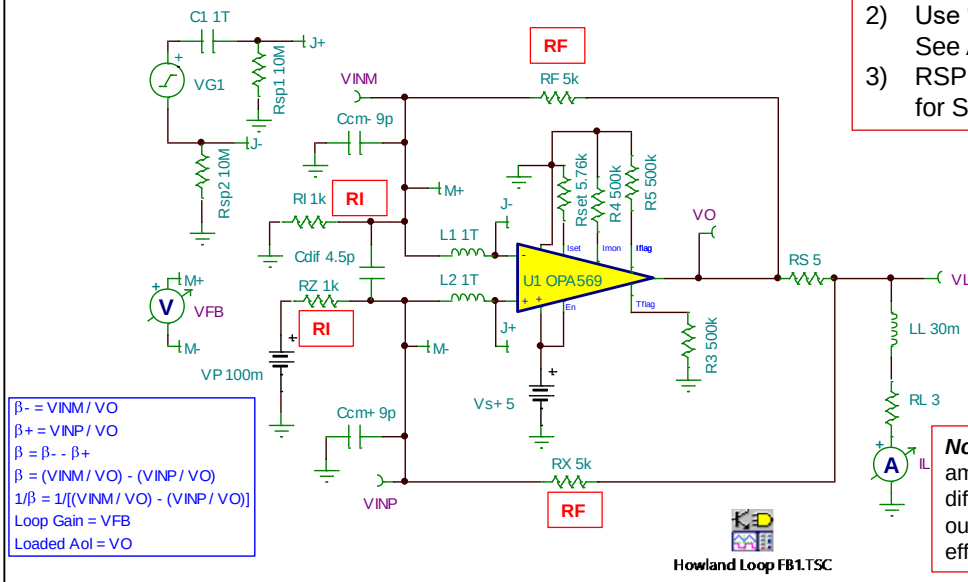


$$1/\beta = \frac{1}{(\beta-) - (\beta+)}$$

For our circuit stability the analysis of Beta- and Beta+ and their differential feedback to the op amp inputs will be key. The proof and derivation of the 1/Beta = 1/[(Beta-) – (Beta+)] equation shown is detailed in the Appendix: "Double L Break for Op Amp Stability Analysis". For now we will accept this theorem for our stability analysis use.

Improved Howland AC Analysis

1) Need to break both feedback paths.
2) Use “Double L Break” – See Appendix.
3) RSP1 & RSP2 may be needed for SPICE convergence.



$$IL = \frac{V\_RS}{RS}$$

$$IL = \frac{VP * \frac{RF}{RI}}{RS} = \frac{VP * \frac{5k}{1k}}{5}$$

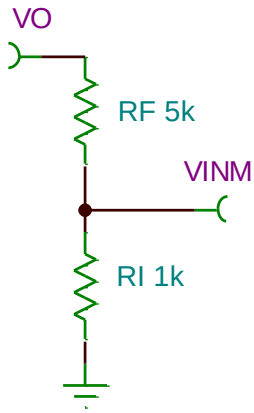
$$IL = VP$$

Note: Ccm+, CCM-, & Cdif are op amp internal input common mode & differential input capacitance moved outside op amp to include any effects on 1/β.

Howland Loop FB1.TSC

From our circuit we see that the derivation of the transfer function of IL/VP will start with IL=V_RS/RS. We know the gain of the Improved Howland Current Pump is the difference in applied voltages at the input (VP-VM) times RF/RI. Here VM=0V and RX=RF and RZ=RI. So from this we see IL=[VP*(RF/RI)]/RS. Substituting in values we get IL=[VP*(5k/1k)]/5 → IL = VP. In order for us to use loop gain analysis for stability analysis we will need to open both feedback paths, Beta+ and Beta-, for AC analysis but keep them closed for the DC operating point. This will be accomplished by using the “Double L Break”, with details and derivation in the Appendix: “Double L Break for Op Amp Stability Analysis”. Since we are isolating each Beta path from the input capacitances of the OPA569 we will add these back in externally as Ccm-, Ccm+, and Cdif. With the Double L Break we can write the equations for Beta-, Beta+, 1/Beta, Loop Gain and Loaded Aol as detailed here.

β- Analysis



β- is constant over frequency since there are no reactive elements in the feedback path.

$$\beta- = \frac{VINM}{VO}$$

$$\text{Set } VO=1 \rightarrow \beta- = VINM$$

$$VINM = \frac{VO * RI}{RF + RI}$$

$$VINM = \frac{1*1k}{5k+1k} = 0.166666666$$

$$\beta- = 0.166666666$$

For this analysis it will be easier for us to analyze each Beta path, Beta- and Beta+, and then combine them together and take the reciprocal to find the 1/Beta. We will start by analyzing Beta-, which will be constant over frequency since there are no reactive elements, only resistors. As shown Beta- = VINM/VO = 0.166666666 for the given resistor values. It will be important in these calculations to carry as many decimal places as possible since Beta- and Beta+ can be close together in some frequency ranges.

β+ Analysis

β+ DC Calculation:

LL = short

$$\beta+ = \frac{VINP}{VO}$$

Set VO=1 → β+ = VINP

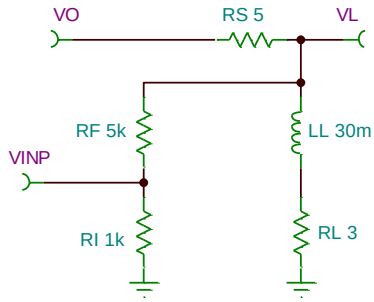
Since RF & RI >> RS & RL:

$$VL = \frac{VO * RL}{RS + RL} = \frac{1*3}{5+3} = 0.375$$

$$VINP = \frac{VL * RI}{RF + RI} = \frac{0.375*1k}{5k+1k} = 0.0625$$

$$\beta+\_DC = 0.0625$$

LL Inductor:
Short for β+ DC
Open for β+ High Frequency



β+ AC Calculation:

β+ Zero at fz due to series interaction of Rs+RL with LL

$$fz = \frac{RS + RL}{2\pi * LL} = \frac{5+3}{2\pi * 30m} = 42.44Hz$$

β+ Pole at fp due to parallel interaction of RF+RI with LL

$$fp = \frac{RF + RI}{2\pi * LL} = \frac{5k+1k}{2\pi * 30m} = 31.83kHz$$

β+ High Frequency Calculation:

LL = open

$$\beta+ = \frac{VINP}{VO}$$

Set VO=1 → β+ = VINP

$$VINP = \frac{RI}{RF + RI + RS} = \frac{1k}{5k+1k+5} = 0.166527893$$

$$\beta+\_HiF = 0.166527893$$

The Beta+ analysis will consist of two parts: DC Calculation and AC Calculation.
DC Calculation:
LL = short
RF & RI >> RS & RL
Beta+ = VINP/VO
The initial voltage divider of VO to VL will be dominated by RS and RL and as shown above will be 0.375
A second divider action by RF and RI will yield B+_DC = 0.0625
AC Calculation:
The Beta+ will have a zero or increase in Beta+ when RS+RL interact with LL as computed above to be fz=42.44Hz
The Beta+ will have a pole or decrease in Beta+ when RF+RI interact with LL as computed above to be fp=31.83kHz
Beta+_HiF will be determined by LL=open and the resistor divider action of RF, RI, and RS aas shown above to be Beta+_HiF=0.166527893

β = (β–) – (β+) Analysis

β- and β+ information will be combined to compute β

$\beta- = 0.166666666$

$\beta+\_DC = 0.0625$

$\beta+\_fz = \frac{RS+RL}{2\pi*LL} = \frac{5+3}{2\pi*30m} = 42.44Hz$

$\beta+\_fp = \frac{RF+RI}{2\pi*LL} = \frac{5k+1k}{2\pi*30m} = 31.83kHz$

$\beta+\_HiF = 0.166527893$

$\beta = (\beta-)-(\beta+)$

$\beta\_DC = (\beta-)-(\beta+\_DC) = 0.166666666 - 0.0625 = 0.104166666$

$\beta\_HiF = (\beta-)-(\beta+\_HiF) = 0.166666666 - 0.166527893 = 0.000138773$

$\beta+\_fz = \frac{RS+RL}{2\pi*LL} = \frac{5+3}{2\pi*30m} = 42.44Hz$

At β+_fz, β+ will increase in value → $\beta = (\beta\text{-})-(\beta+ \text{ increase}) = \beta$ decrease

$\beta\_fp = \beta+\_fz = 42.44Hz$

$\beta+\_fp = \frac{RF+RI}{2\pi*LL} = \frac{5k+1k}{2\pi*30m} = 31.83kHz$

At β+_fp, β+ will decrease in value → $\beta = (\beta\text{-})-(\beta+ \text{ decrease}) = \beta$ increase

$\beta\_fz = \beta+\_fp = 31.83kHz$

In order to compute 1/Beta (which we need for stability check) we will need to compute the net Beta. Beta will be calculated using previous results for Beta- and Beta+. The Beta_DC and Beta_HiF are easily computed as shown above. The poles and zeros for Beta are not as obvious on first inspection. At Beta+_fz, Beta+ will increase. However Beta = (Beta-)-(Beta+ increase) = Beta decrease and so it will appear for Beta as a pole. Beta_fp = Beta+_fz = 42.44Hz. At Beta+_fp, Beta+ will decrease. However Beta = (Beta-)-(Beta+ decrease) = Beta increase and so it will appear for Beta as a zero. Beta_fz = Beta+_fp = 31.83kHz.

1/β Analysis

$\frac{1}{\beta}$ Calculation:

$\beta\_DC = (\beta-) - (\beta+\_DC)$

$\beta\_DC = 0.166666666 - 0.0625 = 0.104166666$

$\frac{1}{\beta}\_DC = 9.6 \rightarrow 19.465dB$

$\beta\_HiF = (\beta-) - (\beta+\_HiF)$

$\beta\_HiF = 0.166666666 - 0.166527893 = 0.000138773$

$\frac{1}{\beta}\_HiF = 7206 \rightarrow 77.15dB$

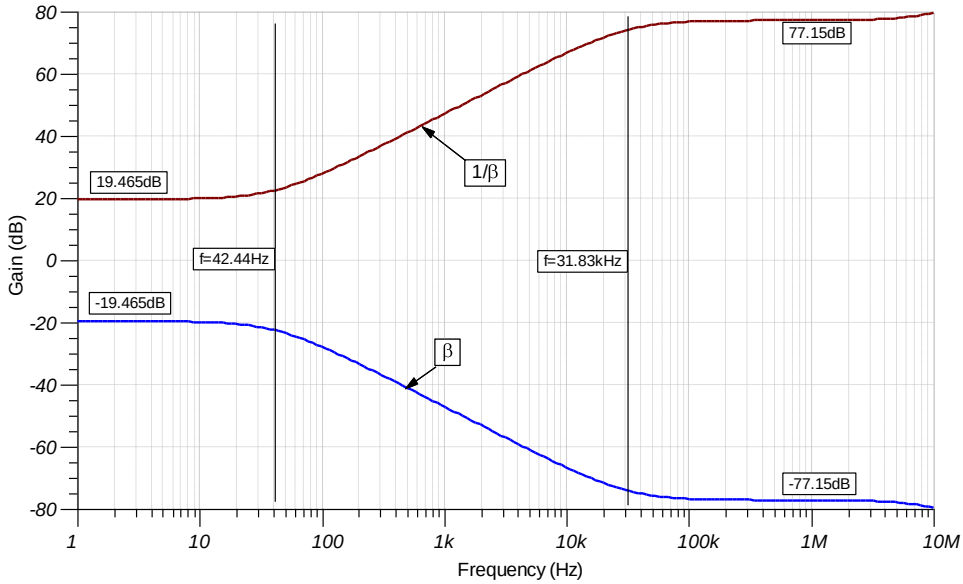
$\frac{1}{\beta}$ Poles and Zeros are reciprocals from β Calculation:

$\beta\_fp = 42.44Hz \rightarrow \frac{1}{\beta}\_fz = 42.44Hz$

$\beta\_fz = 31.83kHz \rightarrow \frac{1}{\beta}\_fp = 31.83kHz$

The 1/Beta analysis will utilize the previous computation for Beta since they are the reciprocal of each other. As shown, 1/Beta_DC=19.465dB, 1/Beta_HiF=77.15dB. 1/Beta_fz = 42.44Hz and 1/Beta_fp = 31.83kHz. Note poles and zeros in Beta and 1/Beta change places since they are reciprocals of each other.

β and 1/β Analysis

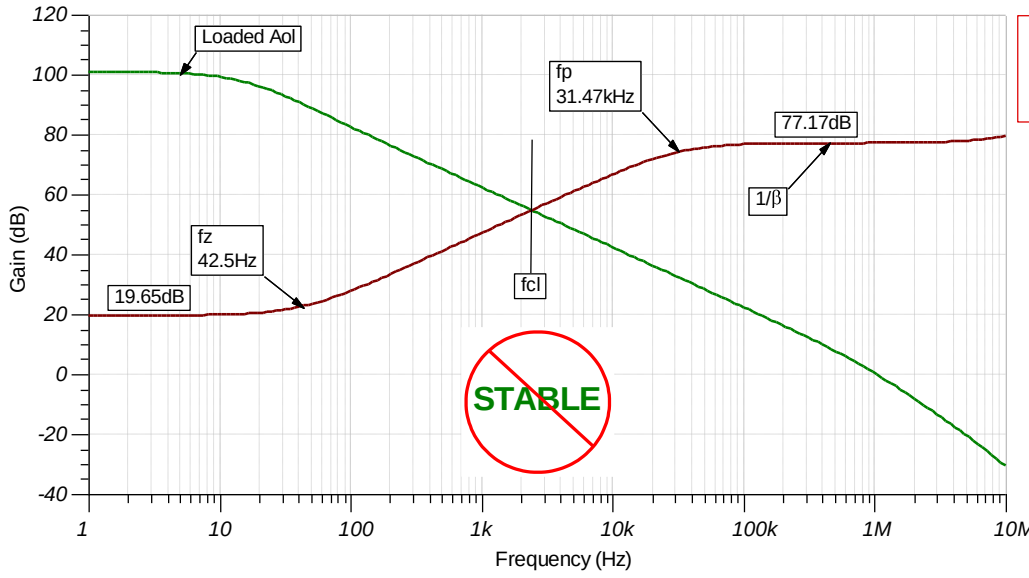


β:
β_fp = 42.44Hz
β_fz = 31.83kHz
β_DC = -19.465dB
β_HiF = -77.15dB

1/β:
1/β_fz = 42.44Hz
1/β_fp = 31.83kHz
1/β_DC = 19.465dB
1/β_HiF = 77.15dB

The simulation results for Beta and 1/Beta confirm our hand calculations for Beta_DC, Beta HiF, Beta_fp, and Beta_fz correlate.
As we would then expect the simulation results correlate as well for 1/Beta_DC, 1/Beta HiF, 1/Beta_fz, and Beta_fp.

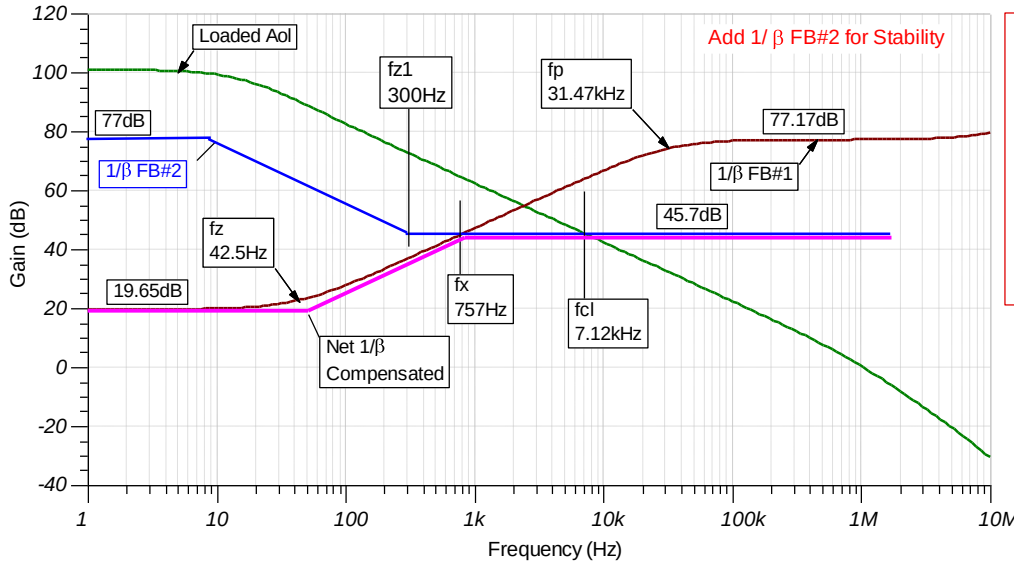
Loop Gain Analysis



At fcl Rate-of-Closure = 40dB/decade → ***UNSTABLE***

Loop gain analysis for 1/Beta plotted on Loaded Aol shows 40dB/decade rate-of-closure at fcl implying an unstable circuit.

FB#1: A_{OL},1/β → *Add 1/β FB#2 for Stability*

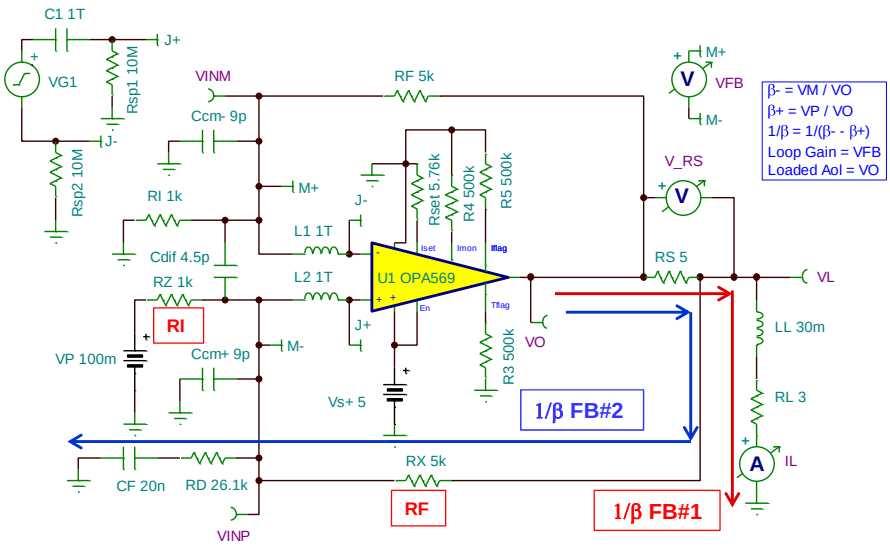


Put fz1at least 1/2 * fx. This allows 50% frequency shift in FB#1 or FB#2 due to external component tolerances over process and temperature to avoid the **"BIG NOT"**.

Above fx there is no current control through LL since 1/β FB#2 dominates.

So now we will use our stabilizing technique as seen on previous V-to-I circuit topologies and add a 1/Beta FB#2.. If we can create a Net 1/Beta compensated curve as shown in Fuchsia we will intersect at fcl with a rate-of-closure that is 20dB/decade and implied stability. Our rules of thumb for avoiding the "BIG NOT" apply here for 1/Beta FB#2 and we will set fz1 at least 50% less in frequency than fx.

Add 1/β FB#2 for Stability

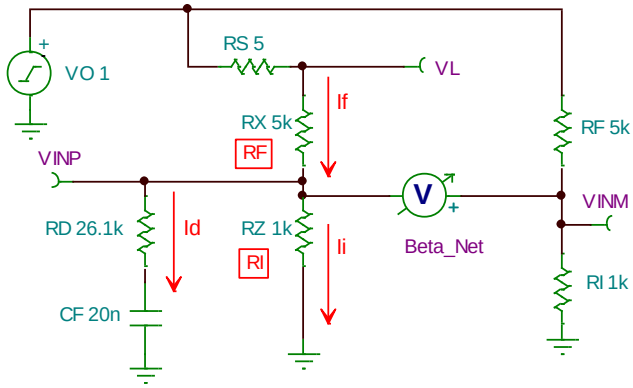


1) As frequency increases X(LL) becomes large and less voltage is fed back through FB#1 and more through FB#2.
2) As frequency increases X(CF) becomes smaller. Which reduces the voltage fed back to VINP as β+.
3) Reducing β+ increases β since β = (β-) – (β+).
3) Increasing β decreases 1/β which is what we want at high frequency for stability.

Howland BetaPlus FB2.TSC

We will analyze 1/Beta FB#2 using superposition. For that we will assume LL = open. Once we have synthesized and analyzed 1/Beta FB#2 we can plot it on the original 1/Beta without FB#2 and see that the lowest 1/Beta path will dominate to yield Net 1/Beta.

Add 1/β FB#2 for Stability: use β calculations



FB#2 DC β & DC $\frac{1}{\beta}$ Calculation:

$$\beta- = \frac{VINM}{VO}$$

Set VO=1 → β− = VINM

$$VINM = \frac{VO * RI}{RF + RI}$$

$$VINM = \frac{1*1k}{5k + 1k} = 0.166666666$$

$$\beta- = 0.166666666$$

β+ DC Calculation:

$$\beta+ = \frac{VINP}{VO}$$

Set VO=1 → β+ = VINP:

$$VINP = \frac{VO * RI}{RS + RF + RI} = \frac{1*1k}{5 + 5k + 1k} = 0.166527893$$

$$\beta+ = 0.166527893$$

$$\beta = (\beta-) - (\beta+) = 0.166666666 - 0.166527893 = 0.000138772$$

$$\frac{1}{\beta} = 7206 \rightarrow 77.15dB$$

Use superposition to analyze 1/β FB#2 with LL=open

Here we analyze DC Beta and 1/Beta for FB#2. Beta- is computed to be 0.166666666 and Beta+ is 0.166527893. This results in Beta = 0.000138772 which translates to 77.15dB.

Add 1/β FB#2 for Stability: use β calculations

β+ FB#2 HiF Calculation:

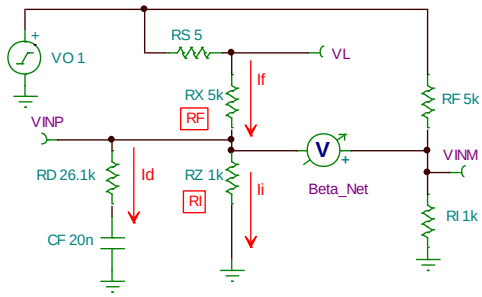
LL=Open, CF=short

Desired $\frac{1}{\beta}$_HiF = 45.7dB → 192.75

Desired β=0.005188067

β+ = (β–) – β

β+ = 0.166666666 – 0.005188067 = 0.161478599



β+ FB#2 HiF Calculation (cont):

$\beta+ = \frac{VINP}{VO}$

Set VO=1 → β+ = VINP

$If = \frac{VO - VINP}{RF}$; since RF >> RS

$If = \frac{1 - 0.161478599}{5k} = 167.7\mu A$

$Ii = \frac{VINP}{RI} = \frac{0.161478599}{1k} = 161.479\mu A$

Id = If – Ii

Id = 167.7μA – 161.479μA = 6.221μA

$RD = \frac{VINP}{Id} = \frac{0.161478599}{6.221\mu A} = 25.957k$

RD = 26.1k; standard value

Use superposition to analyze 1/β FB#2 with LL=open

For Beta+ at high frequency CF=short. Since we know what high frequency Beta we want we can solve for the required Beta+ = 0.161478599. Through standard nodal analysis using currents we can solve for the required RD value to yield the desired high frequency Beta+. A standard value of 26.1k ohms will be used.

Add 1/β FB#2 for Stability

As frequency increases from DC then $\frac{1}{\beta}$ decreases

CF approaches a short when X(CF) = RD $\rightarrow$

$\frac{1}{\beta}$ must have a zero to keep flat as frequency increases

Zero in $\frac{1}{\beta} \rightarrow \frac{1}{\beta}$ increase $\rightarrow$

β decrease = (β-)-(β+ increase) $\rightarrow$

β+ increase $\rightarrow$ Zero in β+

$\frac{1}{\beta}$ fz1 = β+_fz1 zero

1/β FB#2: fz1=300Hz Calculation:

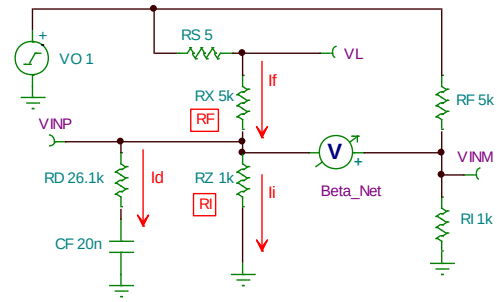
(Zero in 1/β; Zero in β+)

$$\frac{1}{\beta}\_fz1 = \beta+\_fz1 = \frac{1}{2\pi * RD * CF}$$

$$CF = \frac{1}{2\pi * RD * fp1}$$

$$CF = \frac{1}{2\pi * 26.1k * 300Hz} = 20.326nF$$

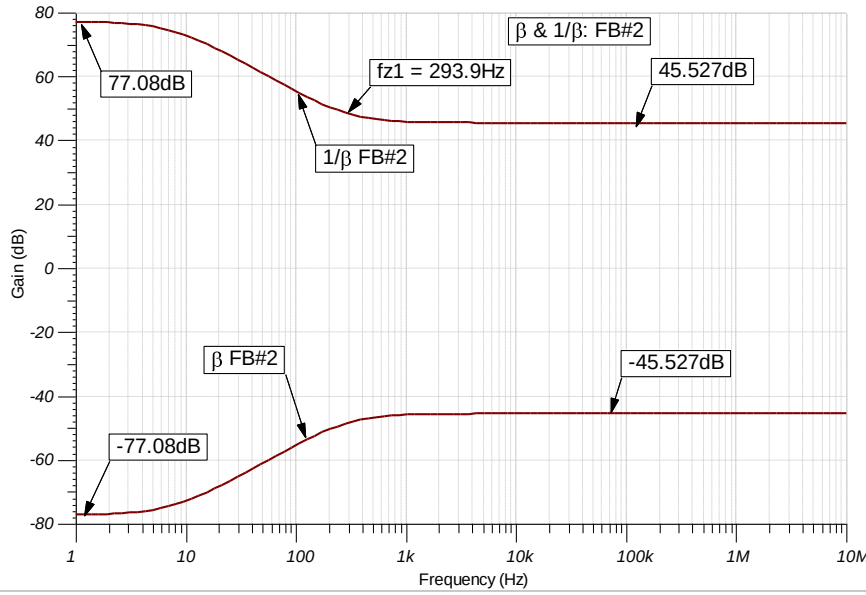
CF = 20nF; standard value



Use superposition to analyze 1/β FB#2 with LL=open

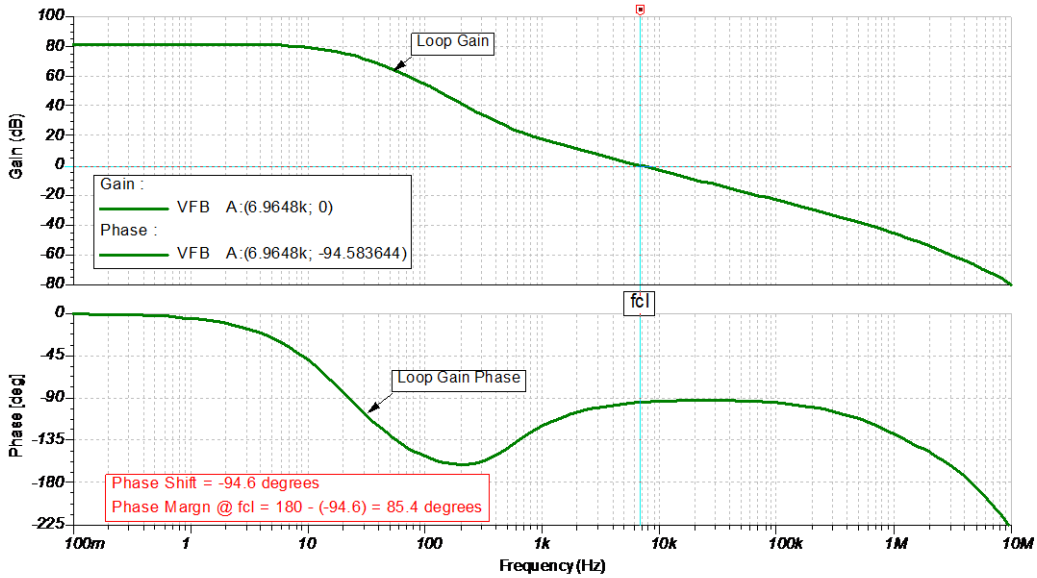
To complete our 1/Beta FB#2 design we need to get a value for CF. We want fz1=300Hz and this zero in 1/Beta FB#2 is set by the interaction of RD and CF. A standard value of CF=20nF is chosen.

Add 1/β FB#2 for Stability



Based on our superposition synthesis and analysis of 1/Beta FB#2 we simulates and see predicted results above. Note the key location of fz1 = 293.9Hz.

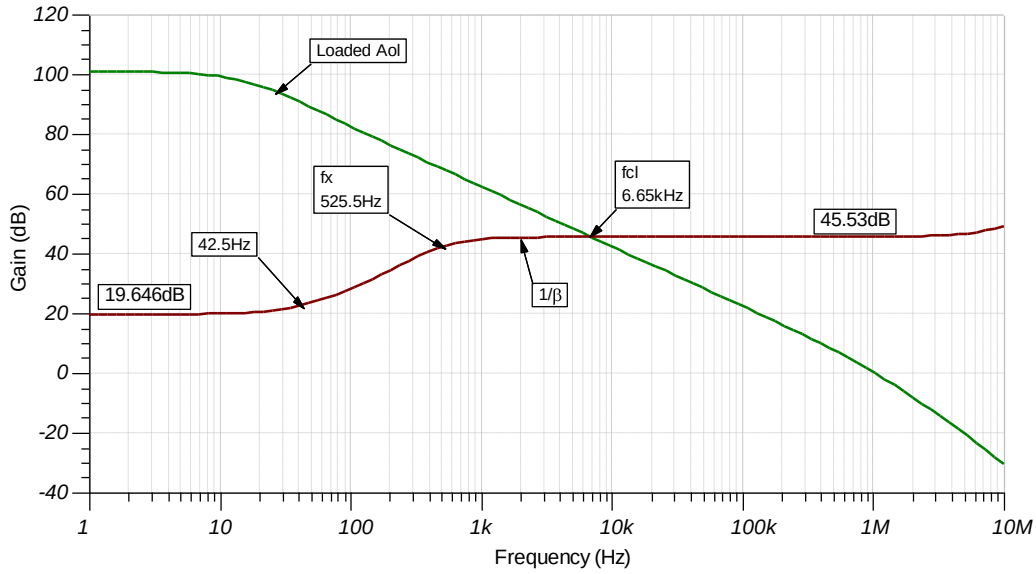
Final Loop Gain Check



A final loop gain check of our compensated circuit confirms we have achieved a stable design with 85.4 degrees of phase margin at fcl where loop gain goes to zero dB.

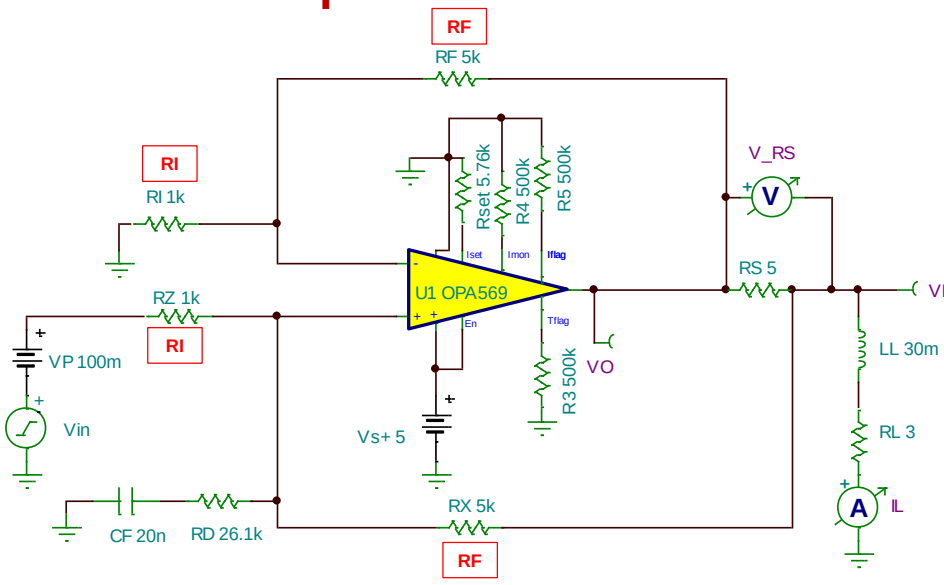
Final Aol,1/β

Net 1/β correlates with the first order lines drawn from FB#1 & FB#2



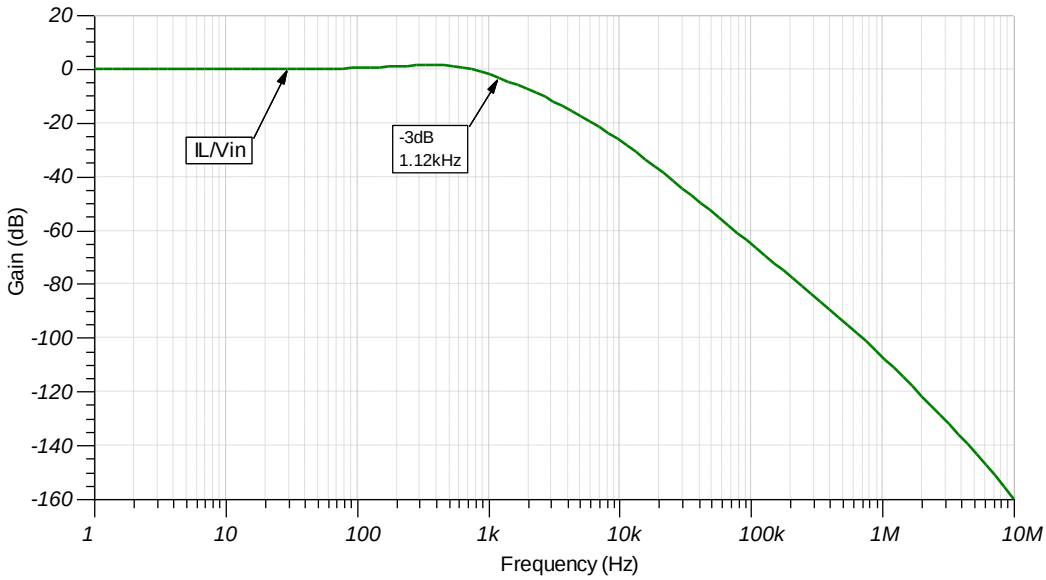
As a double check on our methodology we can plot the final 1/Beta curve on the Loaded Aol curve. The Net 1/Beta correlates closely to our first order lines drawn from FB#1 And FB#2.

AC Closed Loop Transfer Function



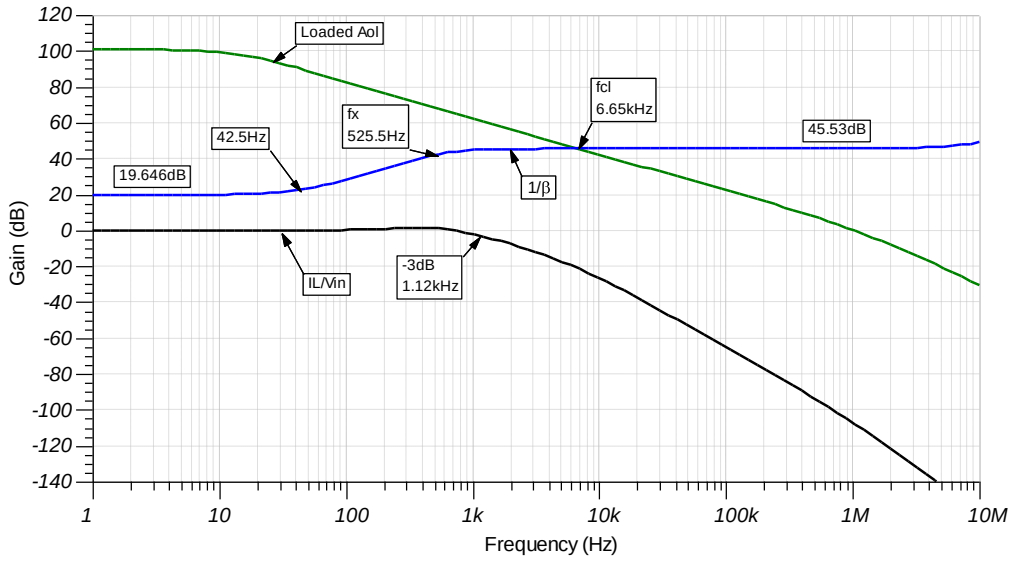
This test circuit will allow us to check the closed loop AC bandwidth of current control in our load. We will look at the closed loop AC transfer function of IL/Vin to determine this.

AC Closed Loop Transfer Function



Our closed loop AC transfer function shows the IL/Vin curve to have a -3dB point at 1.12kHz which means we have frequency control over our load up to 1.12kHz.

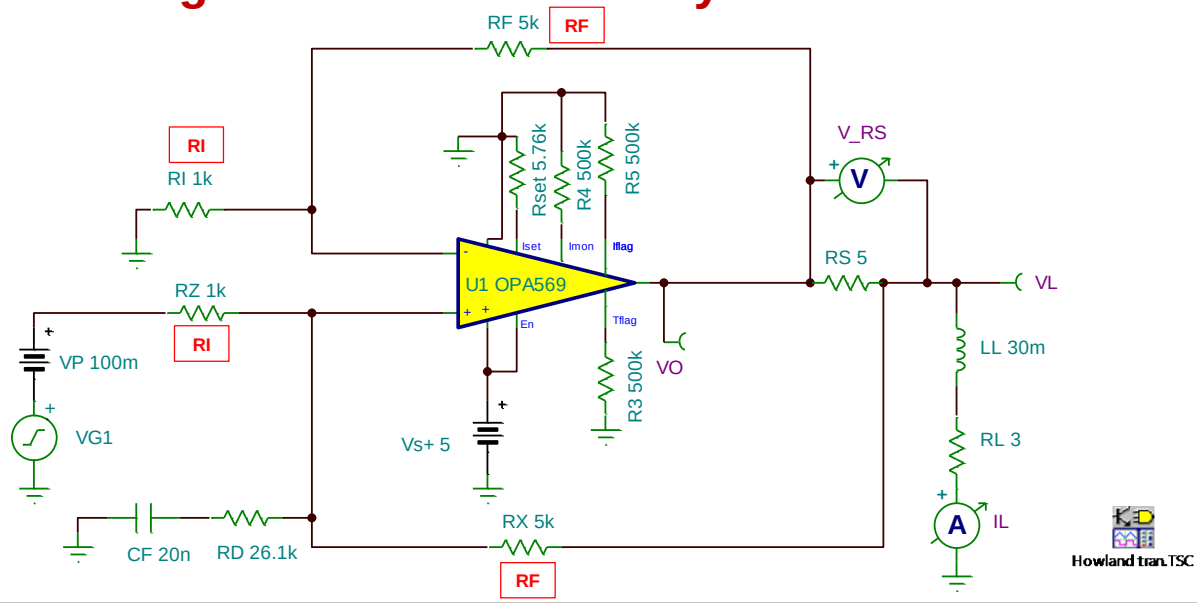
Iout/Vin and effects of FB#1 & FB#2



Above fx there is no current control through LL since β+ FB#2 is not through LL (FB#1)

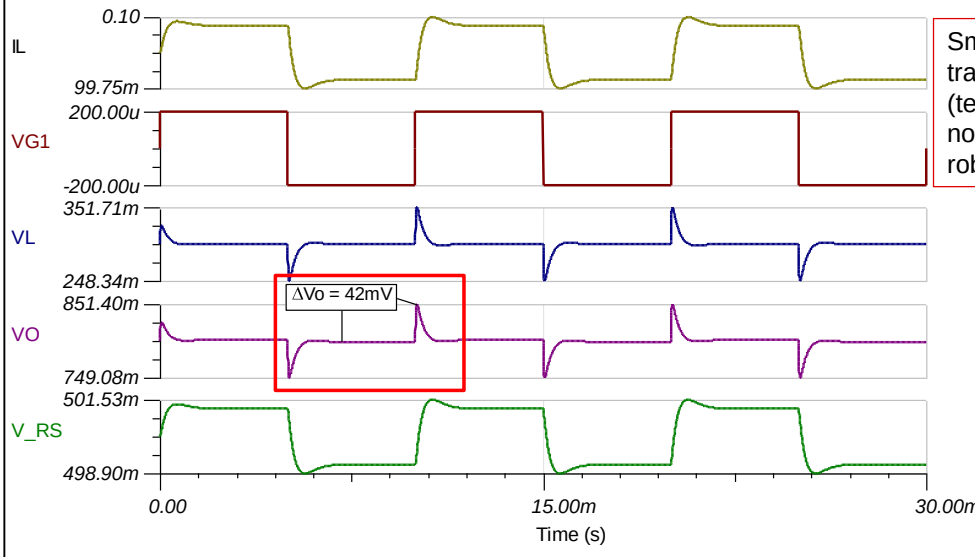
As a final look at our AC responses we plot Loaded Aol, 1/Bea, and IL/Vin all on the same plot. We had predicted, at fx, on our 1/Beta curve, the point at which current control would no longer be flat since we modified the Beta+ feedback path. The actual -3dB point shown on Il/Vin is 1.132kHz. This is good correlation from our stability analysis predictions.

Small Signal Transient Stability Test



As a final stability check on our circuit we will perform a closed loop, small signal, transient stability test using the circuit shown here. In order for this to be a small signal transient test with the loop remaining closed we will adjust VG1 to keep VO<50mVp.

Small Signal Transient Stability Test



Small signal closed loop transient stability test (test with ΔVO < 50mV) shows no oscillations or ringing → robust and stable design.

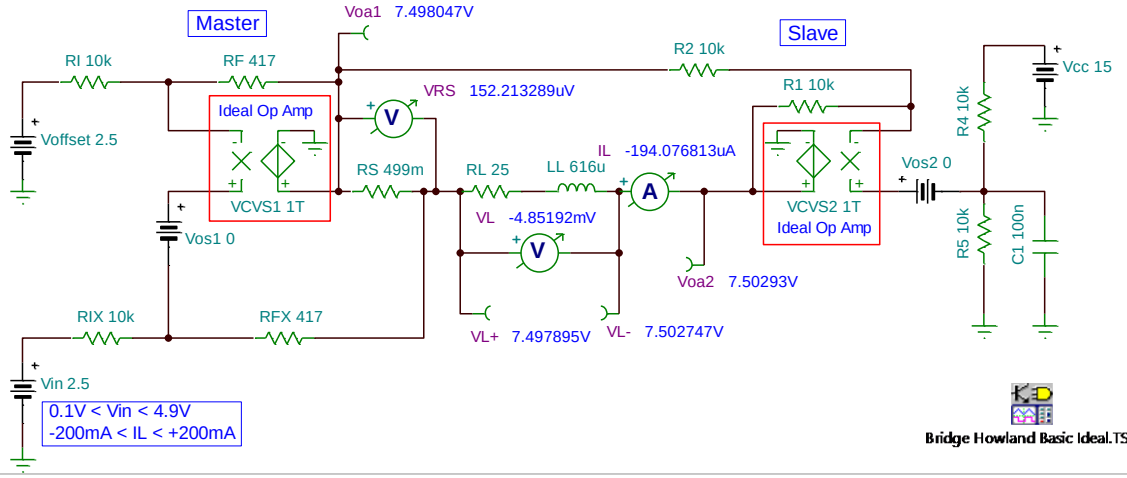
The results of our closed loop, small signal, transient stability test show VO, the output of the OPA569 to be less than 50mVp and no excessive ringing or oscillations are present indicating a stable circuit.

Agenda

- Op Amp Critical Stability Tools Review
- V-I Floating Load (Non-Inverting)
- V-I Grounded Load (Difference Amplifier)
- V-I Grounded Load (Improved Howland Current Pump)
- V-I Floating Load (Improved Howland Single Supply Bridge)
- Power Op Amp Protection
- Power Op Amp Power Dissipation
- Precision Amplifiers – Popular Power Op Amps
- Appendix

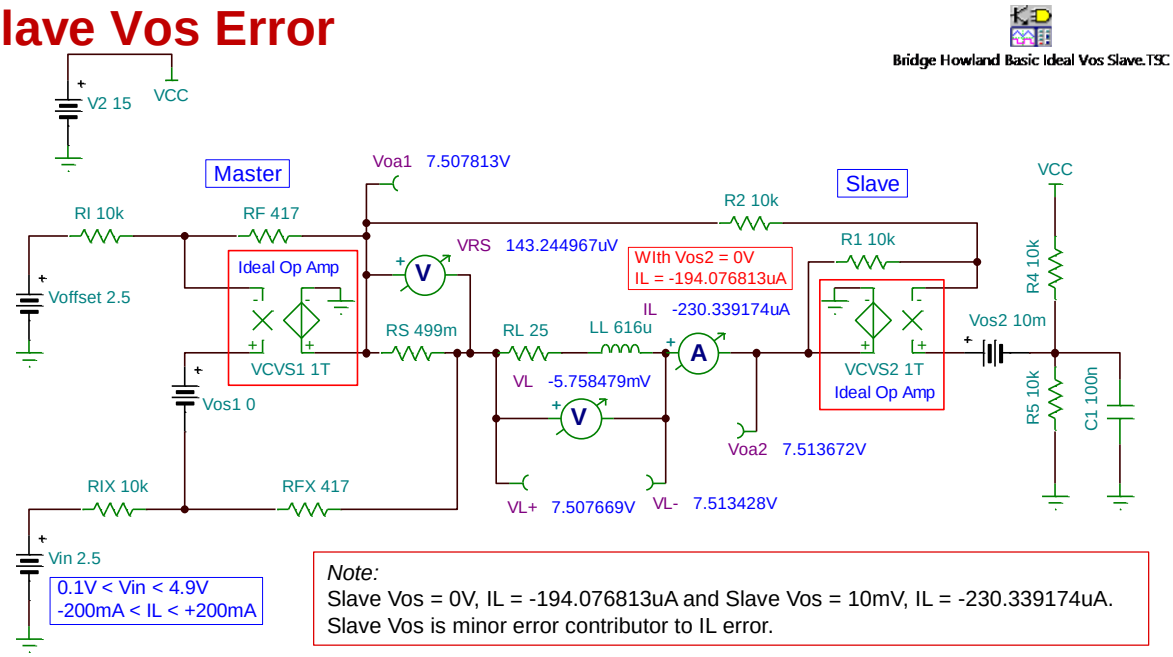
V-I Floating Load (Improved Howland Single Supply Bridge)

1) Positive and negative current can flow through the floating load.
2) Positive and negative voltages across the load are created on a single supply voltage.
3) Double the slew rate across load. Voa1 goes up at 1V/us and Voa2 goes down at 1V/us → 2V/us across load.
4) Balanced power dissipation by using Master/Slave Configuration.
4) Small error in "Zero Output Current" setting, even with Vos1=Vos2=0V, and an "Ideal Op Amp".



This Bridge V-to-I topology utilizes the Improved Howland Current Pump in a bridge configuration to yield bidirectional current drive from a single supply. Notice that the load must "float" with neither end tied to ground. In addition positive and negative voltages can be created across the floating load from a single supply. The load will see double the voltage slew rate across it when compared to a either op amp output since as Voa1 goes up at 1V/us, then simultaneously Voa2 goes down at 1V/us yielding a net 2V/us slew rate across the floating load. The Master/Slave configuration shown will ensure equal power dissipation in each op amp for any output current. There is a slight imbalance in the output current for a zero input total command, using ideal op amps with no input offset voltages.

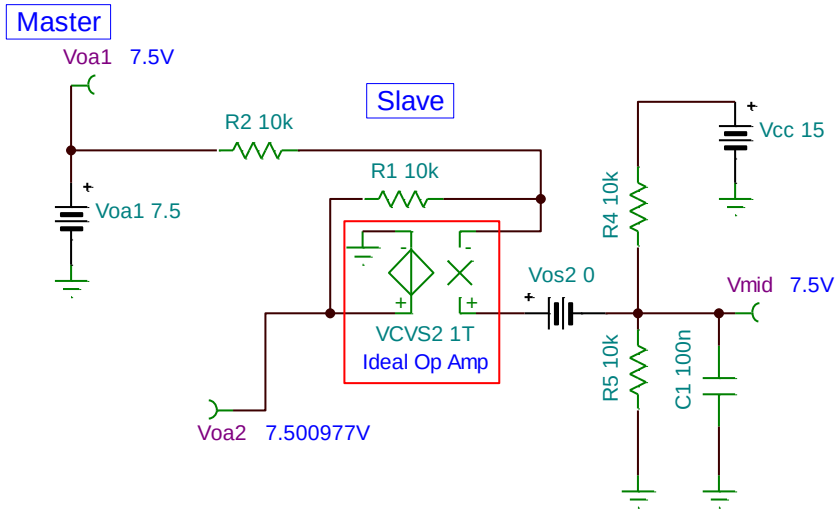
Slave Vos Error



To check the slave amplifier for the zero command error current in IL we change the slave input Vos, Vos2, to 10mV and see only a slight increase in error current in IL from when Vos1=Vos2=0V. The slave op amp is not a major IL error contributor to zero command input.

Slave Scaling

Slave Scaling.TSC



Slave Scaling:

$$Voa2 = \left(\frac{Vcc}{2} * 2\right) - (1 * Voa1)$$

$$Voa2 = Vcc - Voa1$$

Master Voa1	Slave Voa2	Load VL = Voa1-Voa2
0V	15V	-15V
7.5V	7.5V	0V
15V	0V	+15V

The slave scaling is set to swing about the mid-supply voltage on a single supply application. Here, Vcc=15V and a Vmid=7.5V is created by a 10kohm voltage divider consisting of R4 and R5. he slave op amp scaling yields its output, Voa2 = Vcc-Voa1. What this accomplishes is that, given ideal op amp outputs, the master amplifier output, Voa1, swinging from 0V to 15V will cause the slave output , Voa2, to swing from 15V to 0V out of phase yielding +/-15V across the floating load.

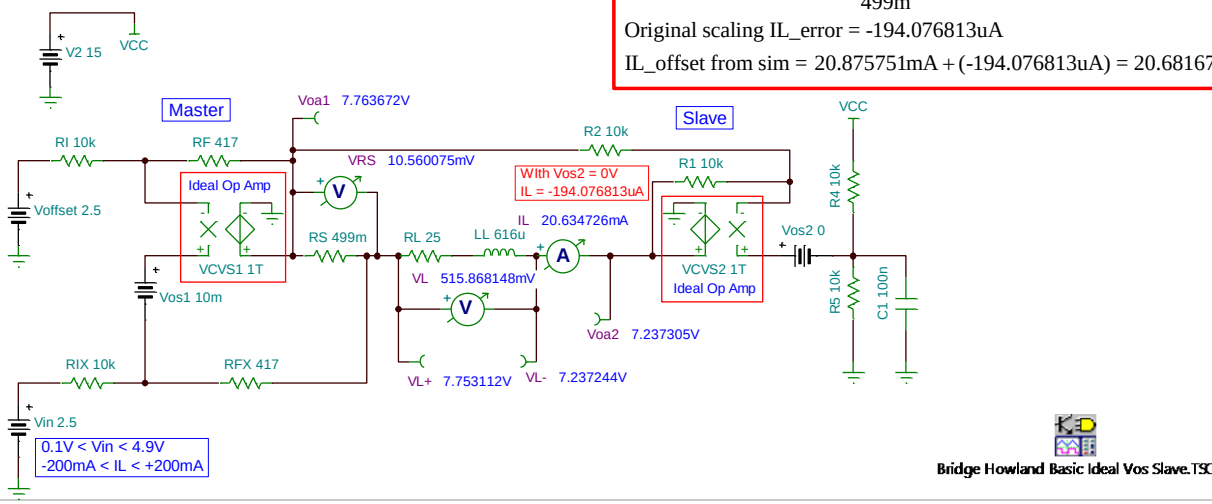
Master Vos Error

$$IL\_offset = \frac{(Vin + Vos1 - Voffset) * \left(1 + \frac{RF}{RI}\right)}{RS}$$

$$IL\_offset = \frac{(2.5V + 10mV - 2.5V) * \left(1 + \frac{417}{10k}\right)}{499m} = 20.875751mA$$

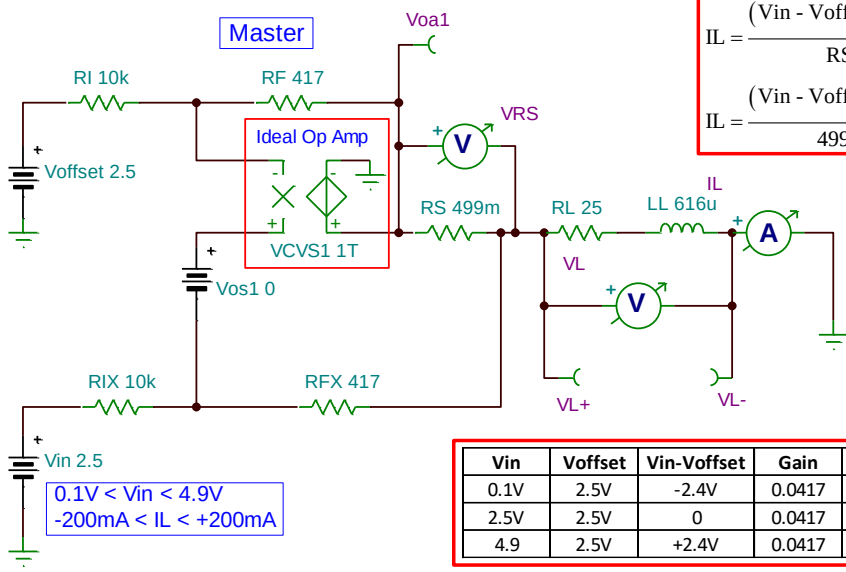
Original scaling IL_error = -194.076813uA

IL_offset from sim = 20.875751mA + (-194.076813uA) = 20.681674mA



Here we will check the master op amp contribution to zero command error current in IL. We will set the master input offset voltage, Vos1, equal to 10mV. We find that this input offset voltage is gained up across RS by 1+RF/RI and can cause a proportional error current to flow. Despite this error current the bidirectional current control on a single supply offers many applications a way to control current and thus torque in linear actuators or motors where the IL zero command error is overridden by an outer positioning control loop.

Master Scaling



Master Scaling:

$$IL = \frac{(Vin - Voffset) * \frac{RF}{RI}}{RS}$$

$$IL = \frac{(Vin - Voffset) * \frac{417}{10k}}{499m} = (Vin - Voffset) * (0.83567134)$$

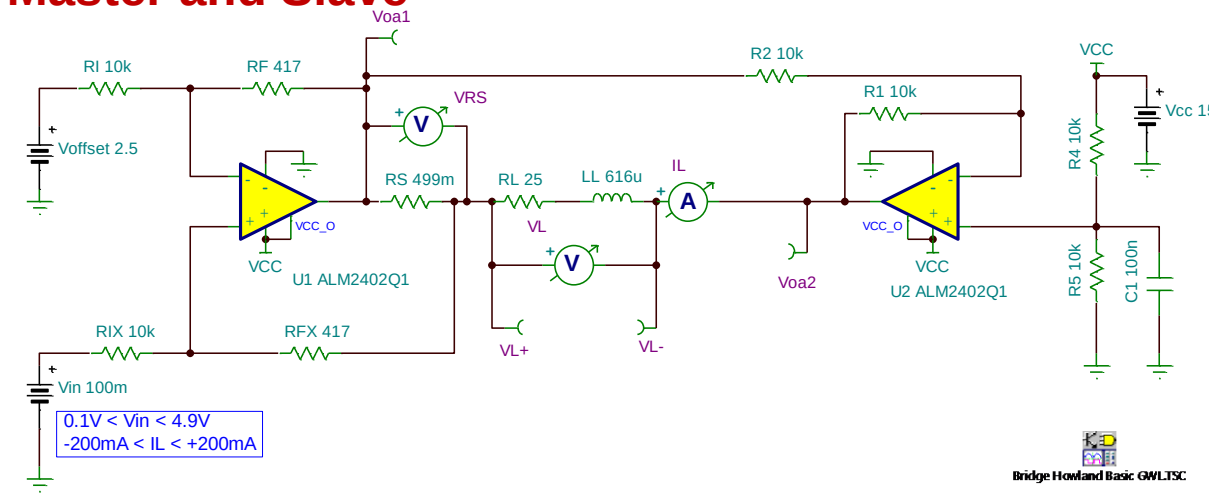
Design Hint:
Set VRS=100mV for full scale IL to achieve reasonable accuracy and resolution.

Master Scaling.TSC

Vin	Voffset	Vin-Voffset	Gain	VRS	RS	IL
0.1V	2.5V	-2.4V	0.0417	-100.08mV	499mΩ	-200.561122mA
2.5V	2.5V	0	0.0417	0V	499mΩ	0
4.9	2.5V	+2.4V	0.0417	+100.08mV	499mΩ	+200.561122mA

Our master op amp scaling for this example is simply IL = [(Vin – Voffset) * RF/RI]/RS. For 0.1V to 4.9V input of Vin we will scale to yield IL = +/-200mA. For Vin = 2.5V we will get IL=0V. One rule-of-thumb for magnitude of RS is to scale it such that for full scale positive or negative peak current there is 100mV of across RS. This is to get a reasonable signal resolution from IL= 0 Amps to IL= Full Scale Amps.

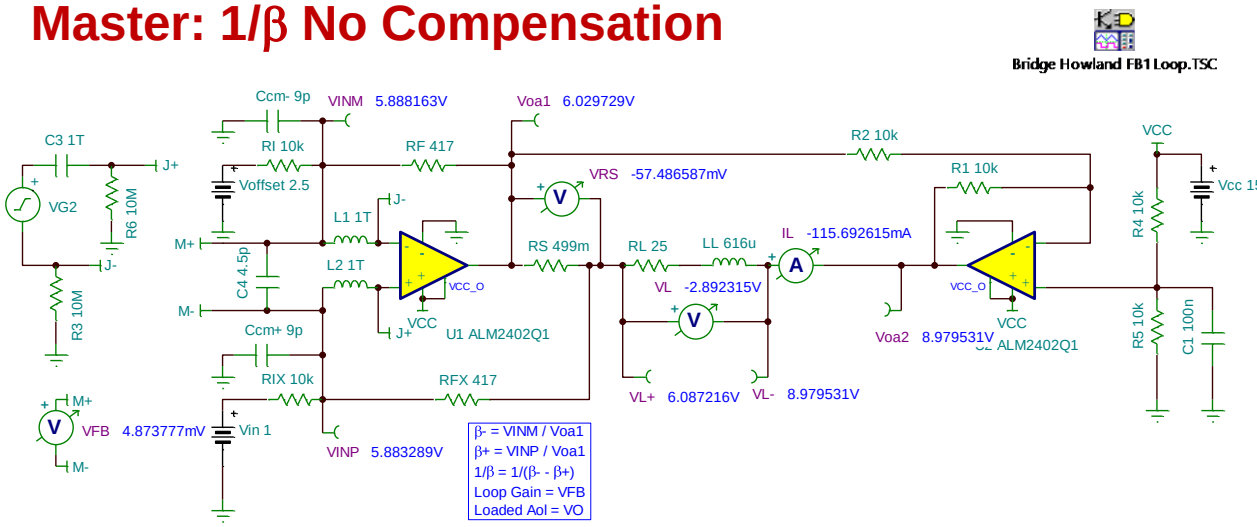
Master and Slave



Vin	Voffset	Vin-Voffset	Gain	VRS	RS	IL	VL	Voa1	Voa2
0.1V	2.5V	-2.4V	0.0417	-100.08mV	499mΩ	-200.561122mA	-5.01402805V	4.942945975V	10.05705402V
2.5V	2.5V	0	0.0417	0V	499mΩ	0	0V	7.5V	7.5V
4.9	2.5V	+2.4V	0.0417	+100.08mV	499mΩ	+200.561122mA	+5.01402805V	10.05705402V	4.942945975V

Here we will design a single supply, Vcc=15V, bridge circuit using the Improved Howland Current Pump to yield positive and negative current control through a floating load. We will use the dual power op amp, ALM2402Q1. Our master and slave op amp scaling was discussed in detail previously. Here we can clearly see all of the node voltages, load voltage, and load currents for the desired Vin range of 0.1V to 4.9V. Note the polarity change of VL = +/-5V VL, IL = +/-200mA though RL+LL, and also the symmetrical swings of Voa1 and Voa2 about the mid-supply voltage of 7.5V.

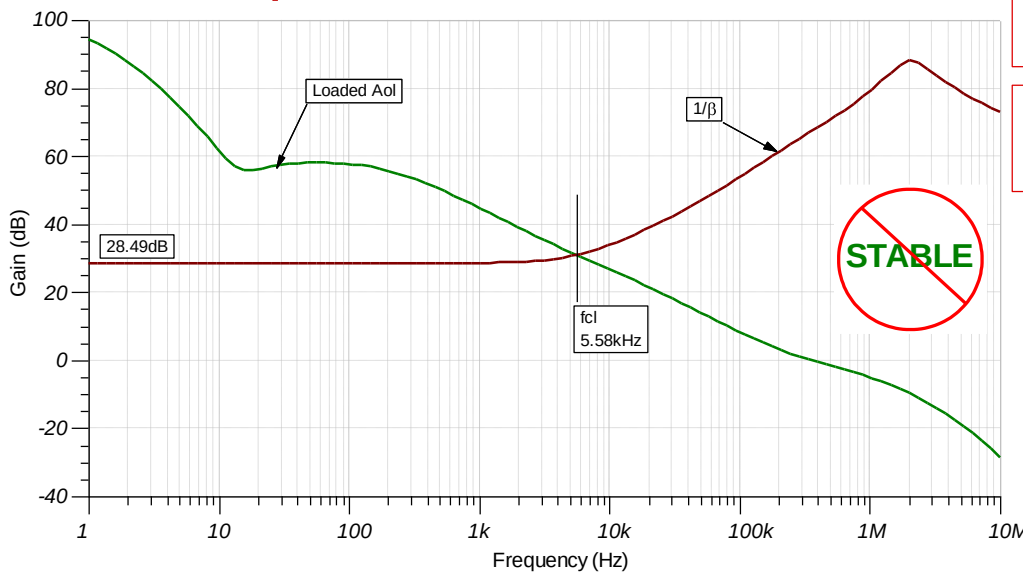
Master: 1/β No Compensation



Note: Ccm-, Cm+, & Cdif are op amp internal input common mode & differential input capacitance moved outside op amp to include any effects on 1/β.

Similar to the Improved Howland Current Pump stability analysis performed before, we will use the "Double L Break" on the master op amp to check for stability. Note that for accurate stability analysis we will leave the slave op amp fully connected to account for all of its closed loop output impedance effects on our stability analysis.

Master: 1/β & Aol, No Compensation

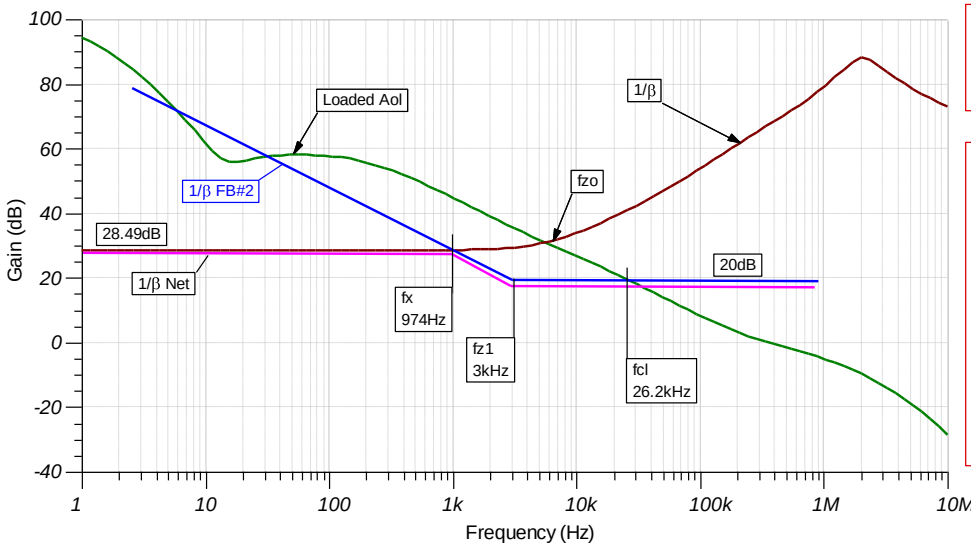


At fcl Rate-of-Closure = 40dB/decade → ***UNSTABLE***

Hump in Loaded Aol is Zo interacting with LL, RL load.

Here we plot 1/Beta on Loaded Aol and notice that at fcl, where loop gain goes to 0dB, the rate-of-closure is 40dB/decade indicating an unstable circuit. Notice the hump in the loaded Aol curve is due to Zo interacting with LL and RL. This effect was analyzed in the "V-I Floating Load (Non-Inverting)" section and will not be repeated here.

Master: FB#1: A_{OL},1/β → *Add 1/β FB#2 for Stability*

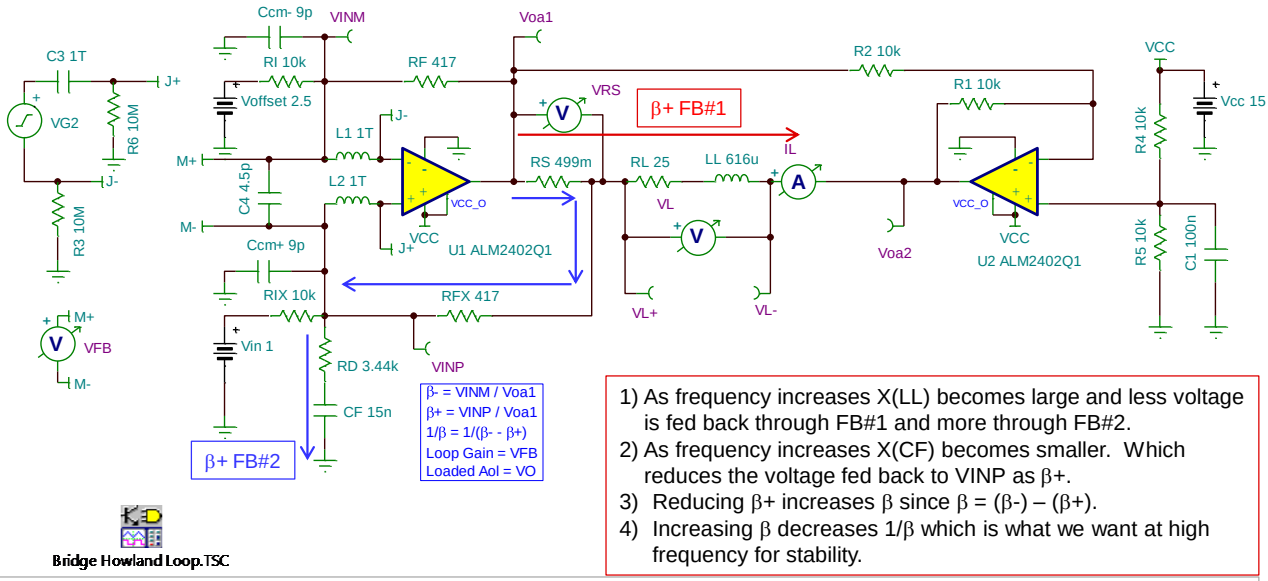


Expect IL/Vin to roll-of at fx, where 1/β FB#2 begins to dominate.

Ensure fx at least 1/2 * fzo, where fzo is zero in 1/β due to inductive load. This allows 50% frequency shift in original 1/β or FB#2 due to external component tolerances over process and temperature to avoid the **"BIG NOT"**.

So now we will use our stabilizing technique as seen on previous V-to-I circuit topologies and add a 1/Beta FB#2. This feedback path will be shown If we can create a Net 1/Beta compensated curve as shown in Fuchsia we will intersect at fcl with a rate-of-closure that is 20dB/decade and implied stability. Our rules of thumb for avoiding the "BIG NOT" apply here for 1/Beta FB#2 and we will set fx at least 50% less in frequency than fzo.

Master: Add 1/β FB#2 for Stability



1) As frequency increases X(LL) becomes large and less voltage is fed back through FB#1 and more through FB#2.
2) As frequency increases X(CF) becomes smaller. Which reduces the voltage fed back to VINP as β+.
3) Reducing β+ increases β since β = (β-) – (β+).
4) Increasing β decreases 1/β which is what we want at high frequency for stability.

We will analyze 1/Beta FB#2 using superposition. For that we will assume LL = open. Once we have synthesized and analyzed 1/Bets FB#2 we can plot it on the original 1/Beta without FB#2 and see that the lowest 1/Beta path will dominate to yield Net 1/Beta.

Master: Add 1/β FB#2 for Stability

β+ FB#2 HiF Calculation:

LL=open, CF=short

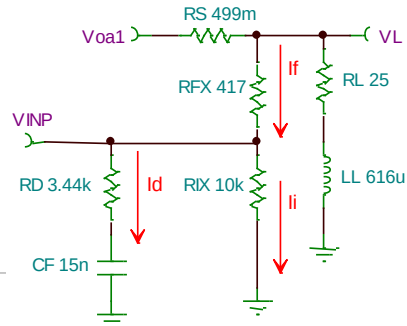
Desired $\frac{1}{\beta}\_HiF = 20dB \rightarrow 10$

Desired β=0.1

$\beta+ = (\beta-) - \beta$

$\beta- = \frac{RI}{RI+RF} = \frac{10k}{10k+417} = 0.959969281$

$\beta+ = 0.959969281 - 0.1 = 0.859969281$



β+ FB#2 HiF Calculation (cont):

$\beta+ = \frac{VINP}{Voa1}$

Set Voa1=1 → β+ = VINP

$If = \frac{Voa1 - VINP}{RFX}$; since RFX>>RS

$If = \frac{1 - 0.859969281}{417} = 335.81\mu A$

$Ii = \frac{VINP}{RIX} = \frac{0.859969281}{10k} = 85.996928\mu A$

$Id = If - Ii$

$Id = 335.81\mu A - 85.996928\mu A = 249.813\mu A$

$RD = \frac{VINP}{Id} = \frac{0.859969281}{249.813\mu A} = 3.442k$

RD = 3.44k; standard value

1/β FB#2: fz1=3kHz Calculation:

(Zero in 1/β; Zero in β+)

$\frac{1}{\beta} fz1 = \beta\ fz1 = \frac{1}{2\pi * RD * CF}$

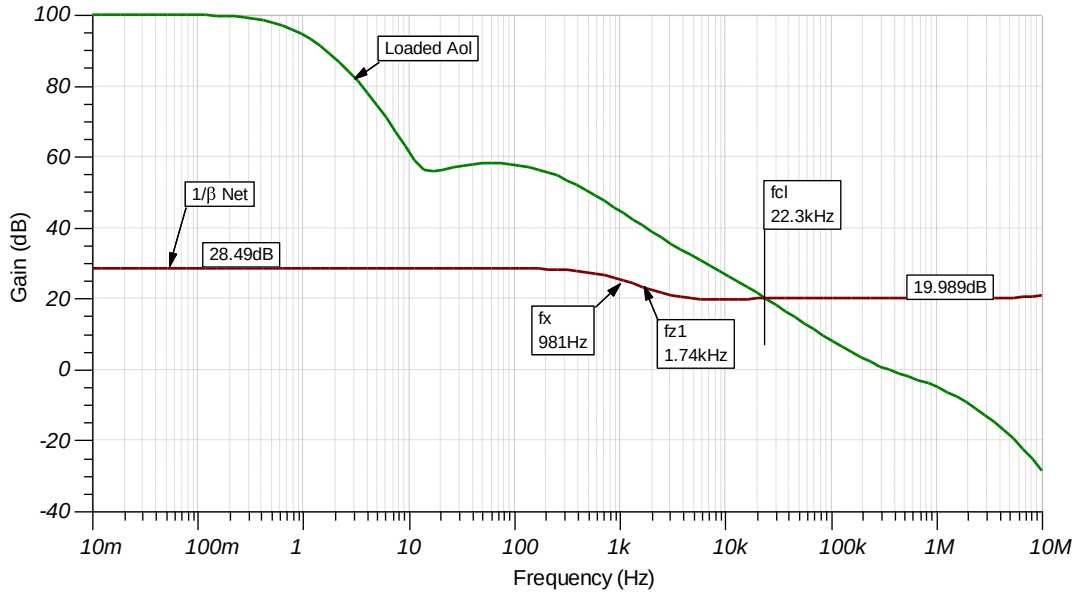
$CF = \frac{1}{2\pi * RD * fz1}$

$CF = \frac{1}{2\pi * 3.44k * 3kHz} = 15.42nF$

CF = 15nF; standard value

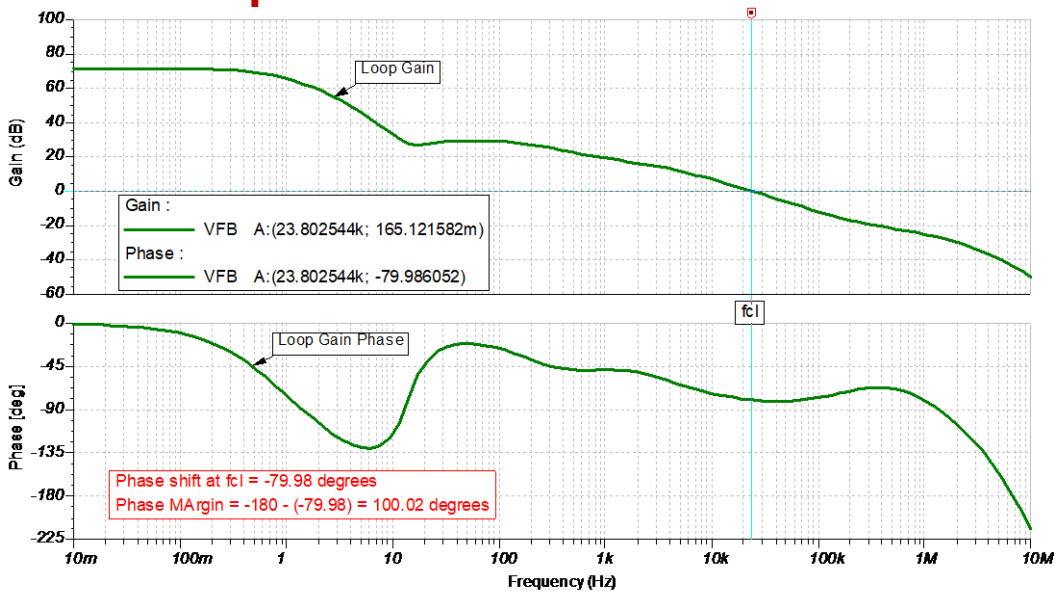
In this slide we will do the detailed calculations to yield the desired 1/Beta at high frequency and also compute capacitor value need to set the 1/Beta FB#2 fz1. We will start by calculating what we need for Beta+ to be at high frequency to yield our desired 1/Beta at high frequency. We set LL=open and CF=short. From our previous knowledge of 1/Beta and the relationship of Beta, Beta+ and Beta- we see we need Beta+ = 0.859969281. Through standard nodal analysis using currents, we can determine the required value for RD and choose the closest standard value of 3.44k ohms. To complete our 1/Beta FB#2 design we need to get a value for CF. We want fz1=3kHz and this zero in 1/Beta FB#2 is set by the interaction of RD and CF. A standard value of CF=15nF is chosen.

Master 1/β & Aol



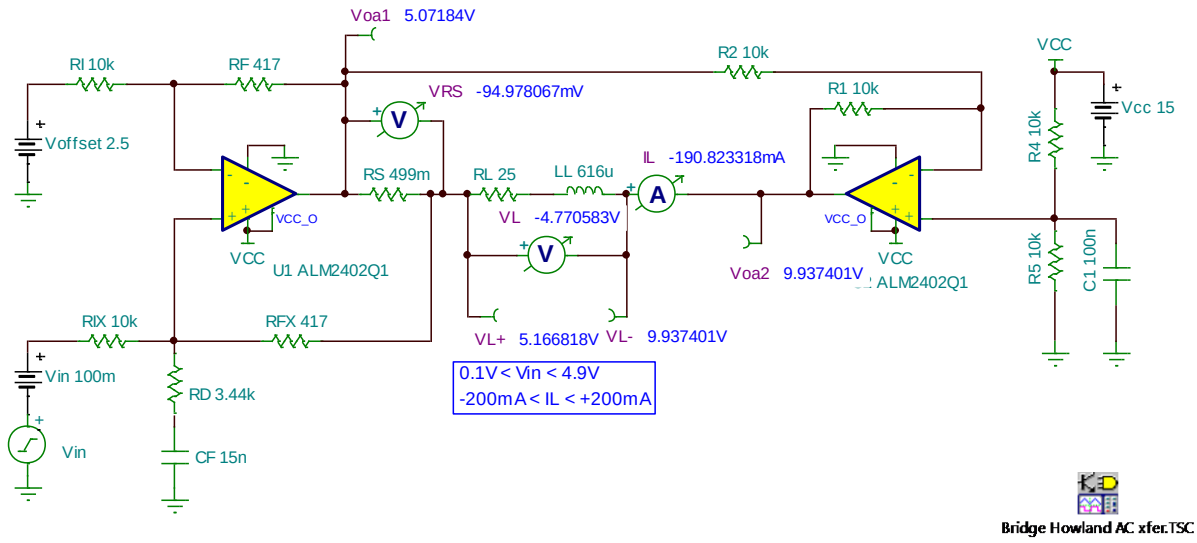
Our simulations of the final 1/Beta curve on the Loaded Aol curve show close correlation to our predicted net 1/Beta.

Master: Loop Gain



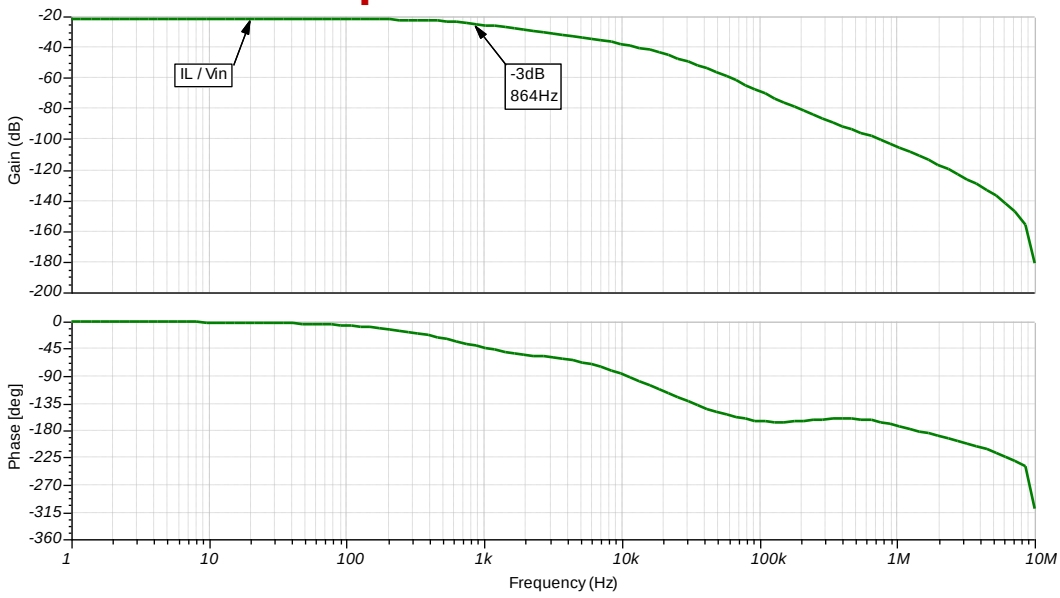
A final loop gain check of our compensated circuit confirms we have achieved a stable design with 100 degrees of phase margin at fcl where loop gain goes to zero dB.

AC Closed Loop Transfer Function



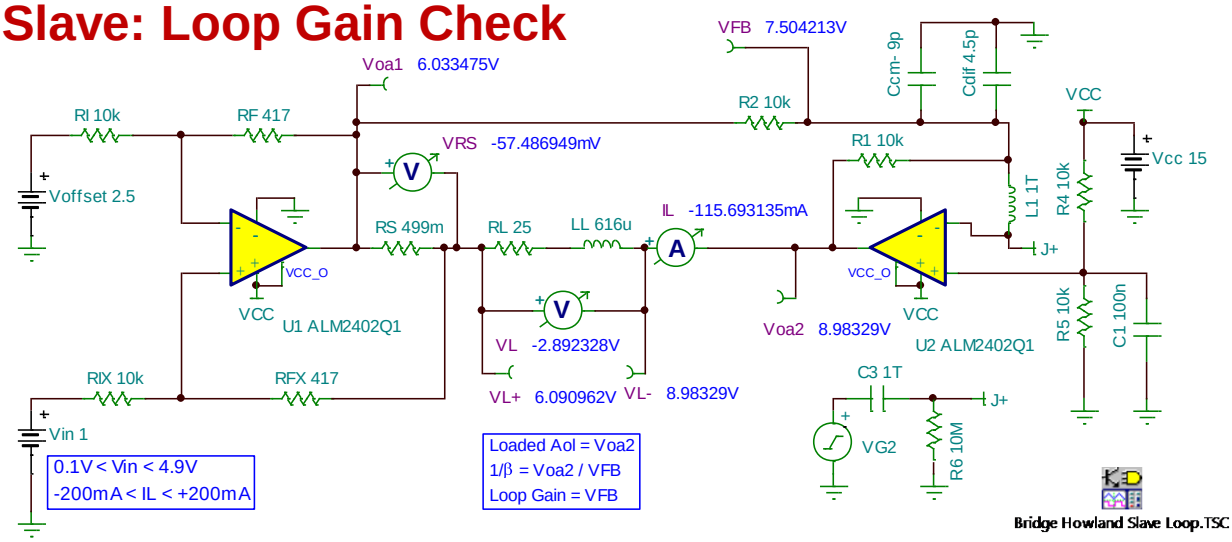
This test circuit will allow us to check the closed loop AC bandwidth of current control in our load. We will look at the closed loop AC transfer function of IL/Vin to determine this.

AC Closed Loop Transfer Function



Our closed loop AC transfer function shows the IL/Vin curve to have a -3dB point at 864Hz which means we have frequency control over our load up to 864Hz. Our predicted closed loop bandwidth based on lines adding in Beta+ FB#2 was 974Hz so we see close correlation between first order predictions and final results.

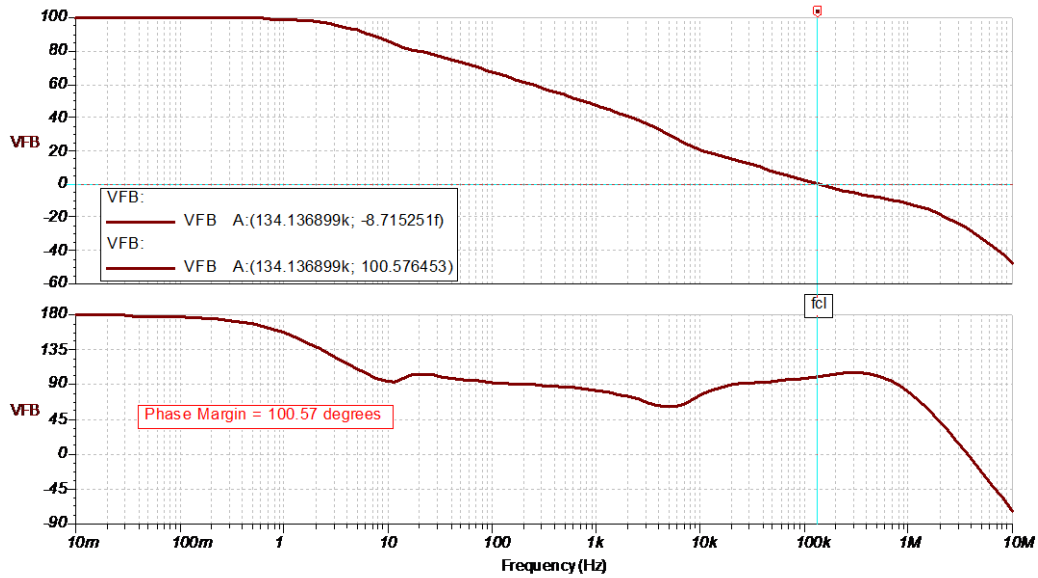
Slave: Loop Gain Check



Note: Ccm- & Cdif are op amp internal input common mode & differential input capacitance moved outside op amp to include any effects on 1/β. Note Cdif goes to GND since +In looks like AC short (1nF to GND) since C2 =1nF >> Cdif = 4.5pF.

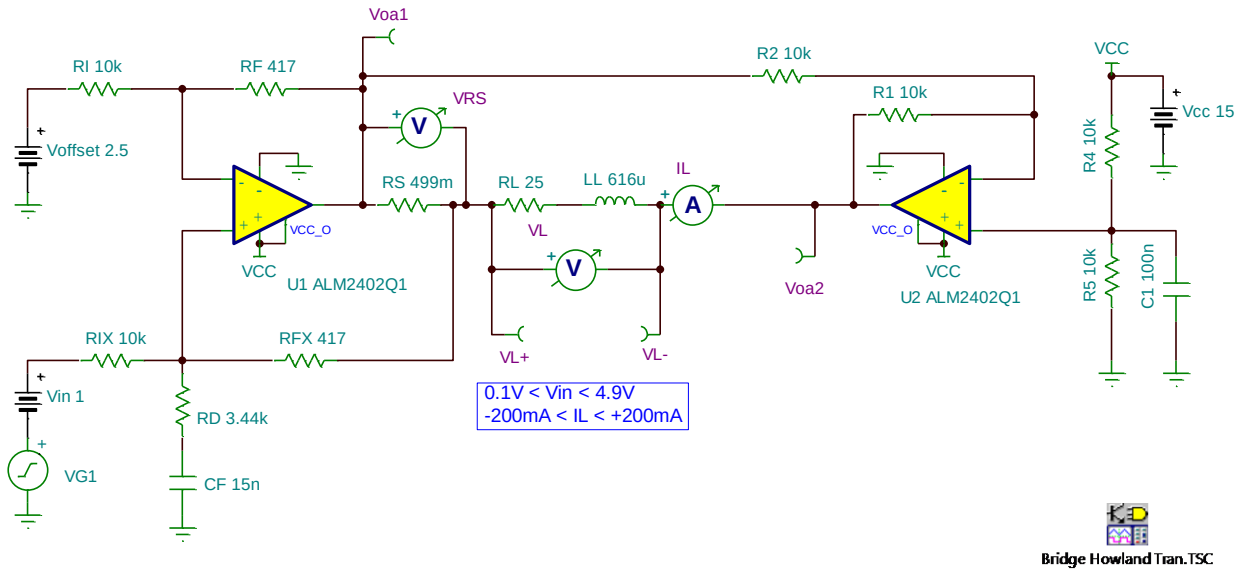
For completeness we must ensure that both the master op amp and slave op amp are stable for a robust design. For the slave op amp stability we can break the loop on the –input of U2.We will need to move the internal common mode and differential input capacitance of the ALM2402Q1 op amp external to include any effects on 1/Beta.

Slave: Loop Gain Check



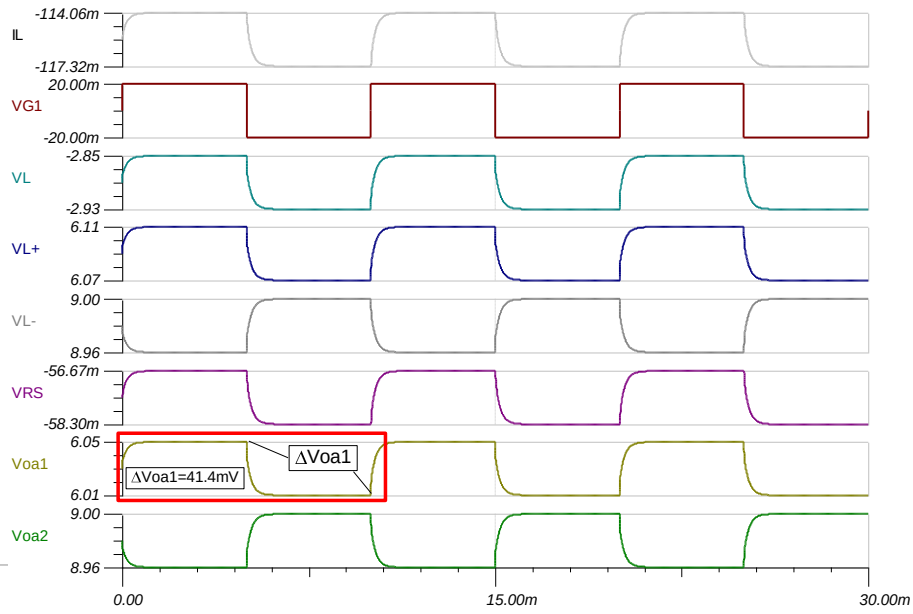
The slave op amp loop gain plot shows 100 degrees of phase margin at fcl where loop gain goes to 0dB.

Small Signal Transient Stability Test



Included in our standard suite of stability tests is the closed loop, small signal, transient stability test. The circuit here will provide us the topology to run this test. In order for this to be a small signal transient test with the loop remaining closed we will adjust VG1 to keep Voa1<50mVp and Voa2<50mVp.

Small Signal Transient Stability Test



Small signal closed loop transient stability test (test with ΔVoa1 < 50mV) shows no oscillations or ringing → robust and stable design.

The results of our closed loop, small signal, transient stability test show both Voa1 and Voa2, the outputs of the ALM2402Q1, dual op amp, to be less than 50mVp and no excessive ringing or oscillations are present indicating a stable circuit.

Agenda

- Op Amp Critical Stability Tools Review
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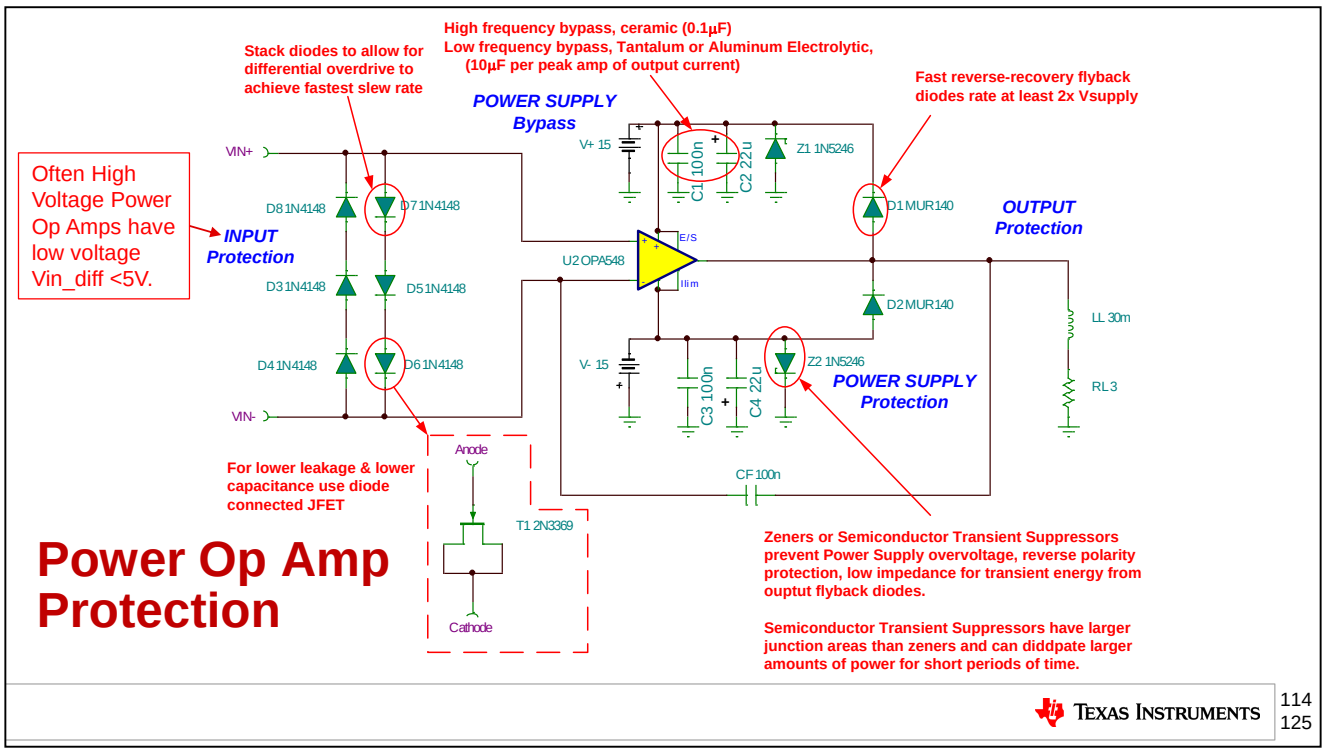


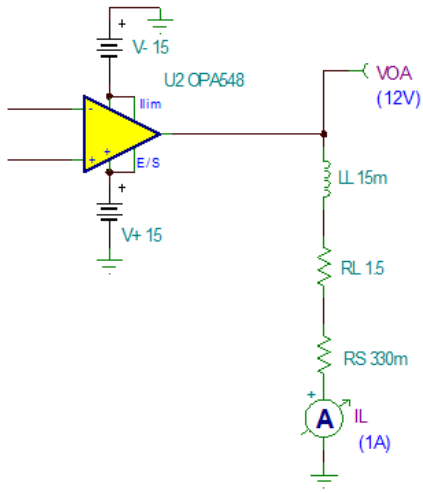
When connecting power op amps to reactive loads, additional protection concerns must be considered in contrast to many small signal op amp applications.

Outputs: External Schottky diodes may be needed to protect from inductive or piezo kick-back voltage transient. The internal ESD diodes to each rail on the output may not be adequate to handle these transients without destruction.

Power Supplies: Recommend a high frequency bypass capacitor directly at the op amp power supply pins to a single point ground. In addition bulk capacitors of about 10uF per peak amp of output current are recommended. In addition each supply should have a unidirectional TVS diode from its power supply pin to a single pint ground. These will absorb any energy driven back through the external Schottky didoes on the output to each supply rail.

Inputs: Many power op amps do not have inputs capable of handling the full supply voltage, (V+) – (V-), differentially across the + and – inputs. Therefore additional protection must be added. This can be accomplished using low leakage signal diodes. If low capacitance and low leakage equivalent diodes are desired, JFETs can be connected as diodes as shown.

V-to-I Large Signal Limits: V=Ldi/dt



"IL dt" = Fastest dt for inductor current
"VOA dt" = Fastest dt for op amp output voltage

Laws of Physics dictate:
V=Ldi/dt
dt = Ldi/V

Rule of Thumb:
V_{LL} = VOA - V_{RL} - V_{RS}
V_{LL} = VOA - IL*RL - IL*RS

V_{LL} = 12 - 1*1.5 - 1*0.330 = 10.17V

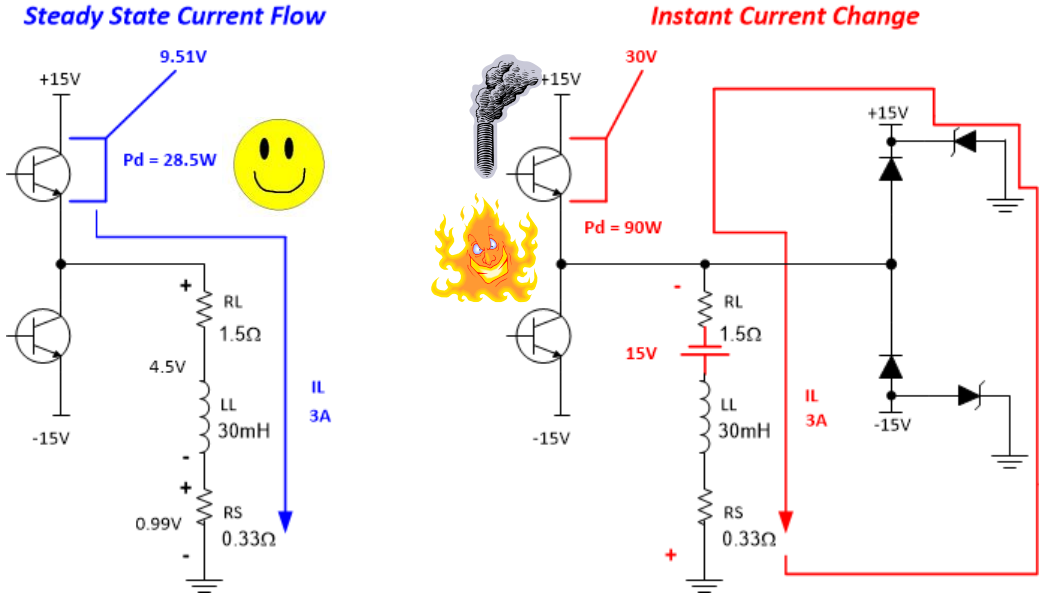
IL dt = LL*dIL/VLL
IL dt = 15m*1/10.17 = 1.47ms
Fastest IL/VIN Slew Rate = 1A/1.47ms
Limit VIN Slew Rate x V-I Gain to match IL/VIN Slew Rate

OPA548 Slew Rate = 10V/us
VOA dt = VOA/(Slew Rate)
VOA dt = 12V/(10V/us) = 1.2us

Rule of Thumb:
VOA dt < (IL dt)/10
1.2us < 1470us/10
1.2us < 147us
Op Amp VOA dt < (IL/VIN Slew Rate)/10

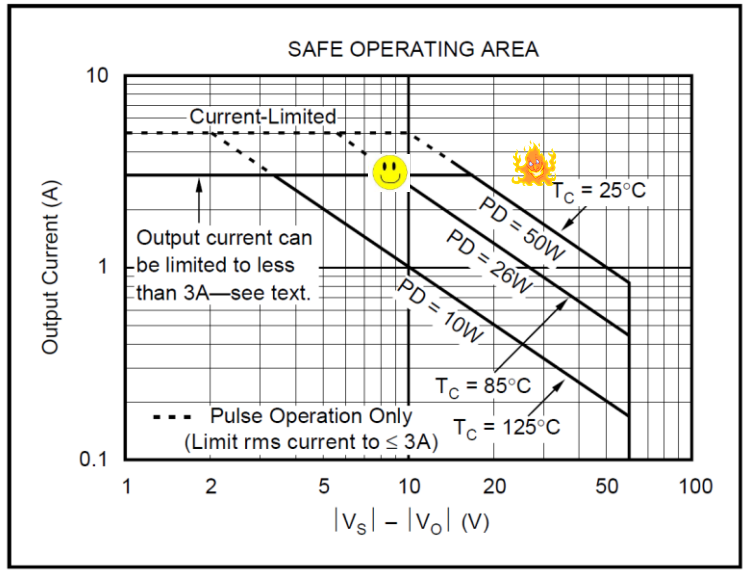
When designing V-to-I circuits driving inductive loads, it is important to understand the limitations set by V=L*di/dt. Current through the inductor can only change as fast as the voltage available to be impressed across the inductor after the required voltage headroom has been allowed for the drop across the op amp output plus the IL*RS drop across the load plus the IL*RS drop across the sense resistor. IL dt is the fastest dt allowed across the inductor, LL, based on VLL, the voltage left to drive current change across the inductor. VOA dt is the fastest the output voltage of the op amp can change based on its voltage slew rate. For the op amp slew rate limitation check keep the op amp VOA dt at least 10 times faster than the IL dt time computed.

Violate the Laws of Physics and Pay the Price!



In general square wave current commands into a V-to-I circuit to instantly reverse current can cause power op amp destruction. A steady state condition on the right shows 3A driven into an inductive load with a bipolar output power stage. Note the steady state power dissipation is Pd=28.5W. If an instantaneous command is made to reverse the current in the inductor, the inductor's local magnetic field will try to keep the current flow in the original direction and can produce large voltages only limited by any diodes to the rail on the output used for protection. Now we see the power dissipation, Pd has risen to 90W, which is way outside of the SOA curve as we will see in the next slide. Result is power op amp destruction.

Instant V-to-I Reversal → SOA Violations



Steady State

Instant Reversal

As shown here instant V-to-I current reversal on inductive loads can force power op amp destruction and operation way outside of the SOA allowed operation.

Agenda

- Op Amp Critical Tools Review
- V-I Floating Load (Non-Inverting)
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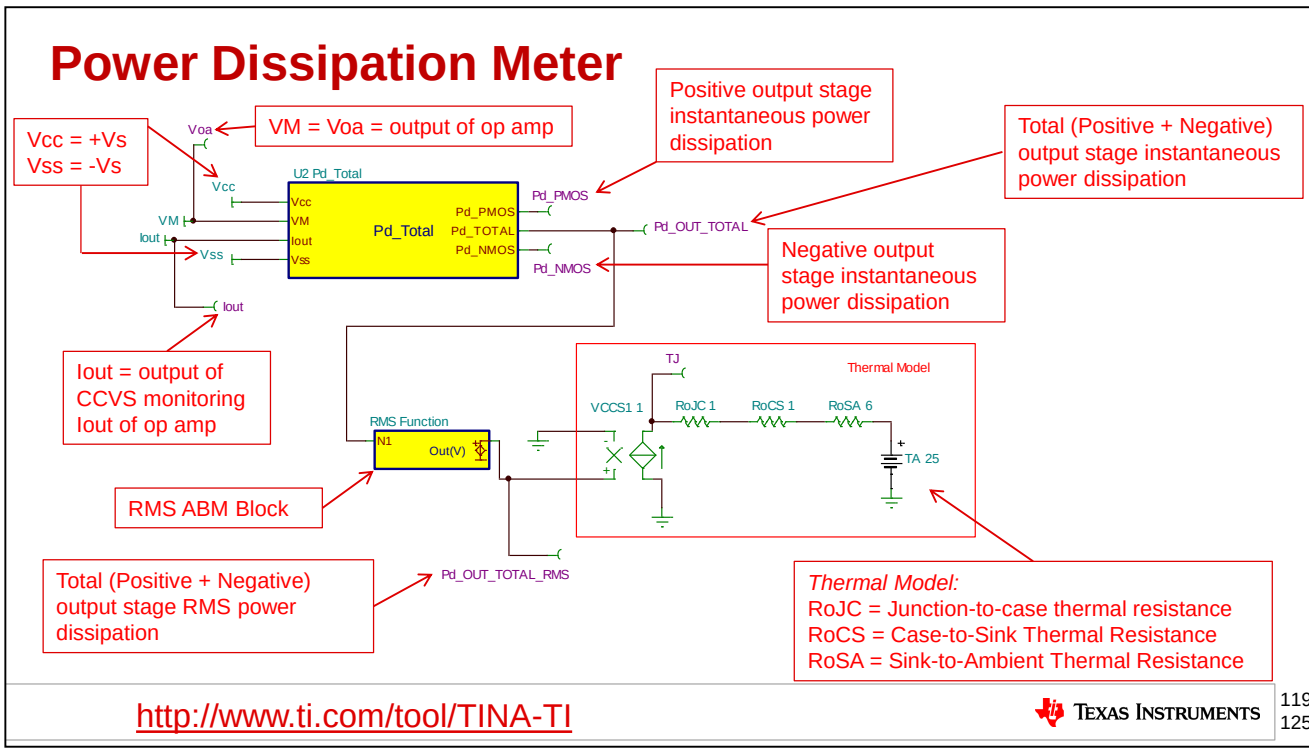
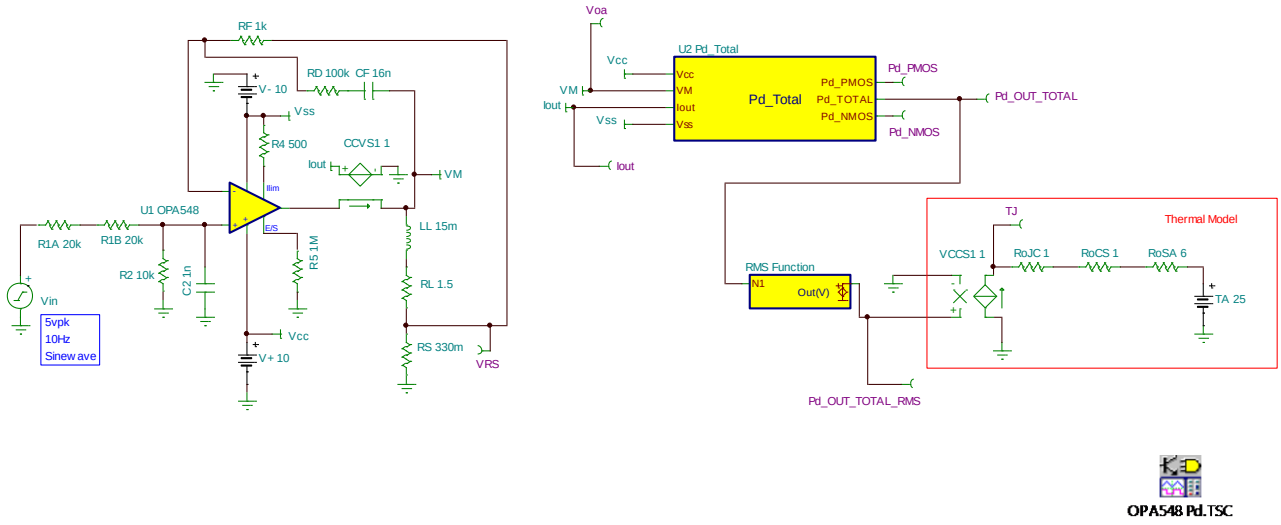
- V-I Floating Load (Improved Howland Single Supply Bridge)
- Power Op Amp Protection
- Power Op Amp Power Dissipation
- Precision Amplifiers – Popular Power Op Amps
- Appendix



Often times when driving inductors and other reactive loads it is not easy to know what the instantaneous power dissipation and Total RMS Power Dissipation is for selecting the right heatsinking to keep the power op amp junction temperature below a desired goal. The Pd_Total meter shown above for TINA-TI SPICE simulator offers a way to easily simulate instantaneous power dissipation. Each input and output is labeled on where to connect it to a typical power op amp circuit. An additional Analog Behavioral Model (ABM) block is added called RMS Function. The total instantaneous power dissipated in the output stages, Pd_OUT_TOTAL, is processed through the RMS Function block to generate RMS power dissipation, Pd_OUT_TOTAL_RMS. This can then be converted to a current through VCSS1 (Voltage Controlled Current Source) and into a common thermal model. The thermal model allows one to run a transient SPICE simulation and see the junction temperature of the power op amp based on the thermal design and ambient temperature.

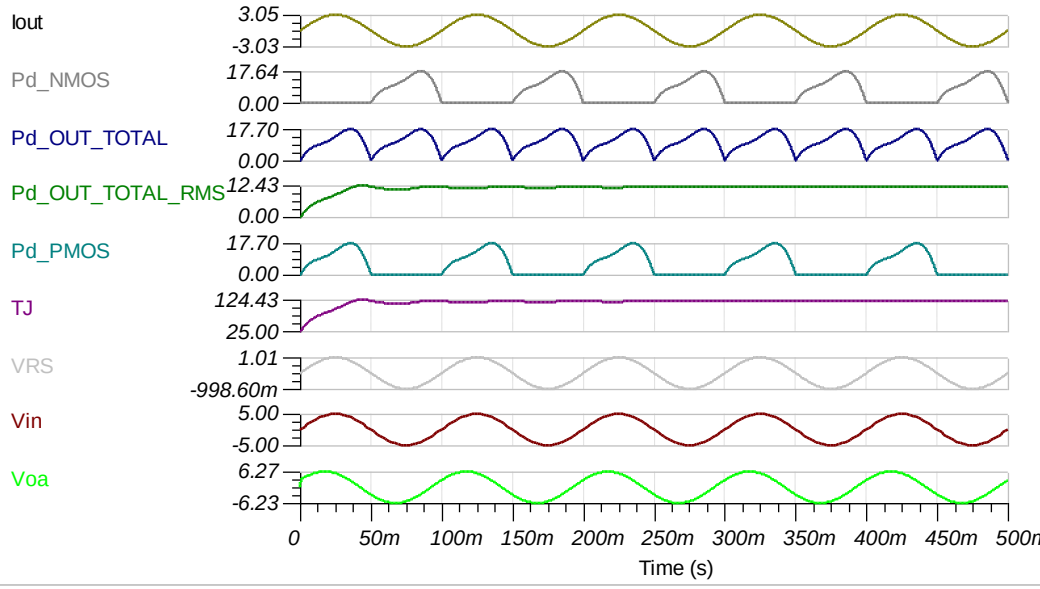
Power Op Amp Power Dissipation



OPA548 Pd.TSC

Here we see a definition-by-example of how to use the Pd_Total meter to compute instantaneous power dissipations as well as RMS power dissipation. The OPA548 is configured as a V-to-I circuit driving bidirectional current through an inductive load, using a dual supply of +/-10V. The input command voltage will be a 10Hz, 5Vpk, sinewave resulting in +/-3.03A of Iout current. The next slide will show the results of our transient analysis simulation.

Power Op Amp Power Dissipation



The results of our simulation using the Pd_Total power meter, RMS Function block, and Thermal Model are shown here. For the Iout=3.03Apk current output , we can see the Pd_NMOS and Pd_PMOS instantaneous power dissipation for each output stage (source and sink output stages). The total instantaneous power dissipation is shown at Pd_OUT_TOTAL. After running through the RMS Function we get Pd_OUT_TOTAL_RMS. This RMS power dissipation is converted into current and injected into our Thermal Model resulting in the TJ (junction temperature) of the power op amp reaching 124.43 degrees Celsius.

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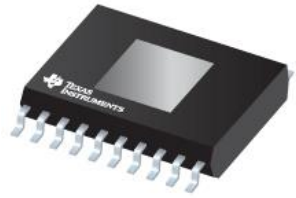
Who put the “Power” in Power Op Amps?

TEXAS INSTRUMENTS

Who can get the “Power” out of Power Op Amps?
Precision Amplifiers’ Applications Team!



High Current Power Op Amps (≥200mA)

Part	Features	Supply Max	Supply Min	Iout	UGBW	Slew Rate	Vos Max	Vos Drift	Iq	Vout (V)	Pkg	$USD
		(V)	(V)	(mA)	(MHz)	(V/us)	(mV)	uV/C)	(mA/Ch)	(V-) + ? (V+) - ?		(1k Qty)
OPA541	Adj Curent Lim	80	20	10000	1.6	10	1	15	20	4 3.2	TO-220-11	12.60
OPA549	Shutdown, Adj Current Lim	60	8	8000	0.9	9	5	20	26	2.7 1.4	TO-220-11	13.50
OPA548	Shutdown, Adj Current Lim	60	8	3000	1	10	10	30	17	2.1 1.0	TO220-7 TO263-7	7.94
LM675	Decomp, G=10	60	16	3000	5.5	8	10	25	18	4 4	TO-220-5	2.44
OPA521	Shutdown, Adj Current Lim PLC Drive, G=7	24	7	2500	3.82	75	-----	-----	51	2.25 1.5	VQFN-20	1.25
OPA569	Shutdown, Adj Current Lim	5.5	2.7	2400	1.2	1.2	2	1.3	9	RRO RRO	SOIC-20	3.90
OPA567	Shutdown, Adj Current Lim	5.5	2.7	2400	1.2	1.2	2	1.3	9	RRO RRO	VQFN-12	2.30
OPA544	Shutdown	70	20	2000	1.4	8	5	10	12	3.8 3.1	TO220-5 TO263-5	9.09
OPA564	Shutdown, Adj Current Lim	24	7	1500	17	40	20	10	39	2 1	HSOP-20	2.75
OPA547	Shutdown, Adj Current Lim	60	8	500	1	6	5	25	10	1.5 0.8	TO220-7 TO263-7	5.75
ALM2402-Q1	Shutdown, Dual, High Cload	16	5	400	0.6	0.17	15	9	5	0.13 0.2	HSSOP-14 SON-12	1.29
OPA552	Shutdown, Decomp, G=5	60	8	380	12	24	3	7	7	2 2	PDIP-8 SOIC-8 TO-263-8	1.75
OPA551	Shutdown	60	8	200	3	15	3	7	7	2 2	PDIP-8 SOIC-8	1.90

High Voltage Power Op Amps (≥45V)

Part	Features	Supply Max (V)	Supply Min (V)	Iout (mA)	UGBW (MHz)	Slew Rate (V/us)	Vos Max (mV)	Vos Drift uV/C)	Iq (mA/Ch)	Vout (V) (V-) + ? (V+) - ?	Pkg	$USD (1k Qty)
OPA454	Shutdown	100	10	50	2.5	13	4	1.6	3.2	1	SOIC-8	2.75
OPA445	-----	90	20	20	2	15	3	10	4.2	5 5	PDIP-8 SOIC-8 TO-99-8	4.75
OPA452	-----	80	20	50	1.8	7.2	3	5	5.5	2 2	TO220-7 TO263-7	2.90
OPA453	Decomp, G=5	80	20	50	7.5	23	3	5	5.5	2 2	TO220-7 TO263-7	3.30
OPA541	Adj Curent Lim	80	20	10000	1.6	10	1	15	20	4 3.2	TO-220-11	12.60
OPA544	Shutdown	70	20	2000	1.4	8	5	10	12	3.8 3.1	TO220-5 TO263-5	9.09
OPA549	Shutdown, Adj Current Lim	60	8	8000	0.9	9	5	20	26	2.7 1.4	TO-220-11	13.50
OPA548	Shutdown, Adj Current Lim	60	8	3000	1	10	10	30	17	2.1 1.0	TO220-7 TO263-7	7.94
OPA547	Shutdown, Adj Current Lim	60	8	500	1	6	5	25	10	1.5 0.8	TO220-7 TO263-7	5.75
OPA551	Shutdown	60	8	200	3	15	3	7	7	2 2	PDIP-8 SOIC-8 TO-263-8	1.90
OPA552	Shutdown, Decomp, G=5	60	8	380	12	24	3	7	7	2 2	PDIP-8 SOIC-8 TO-263-8	1.75
LM675	Decomp, G=10	60	16	3000	5.5	8	10	25	18	4	TO-220-5	2.44

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Appendix

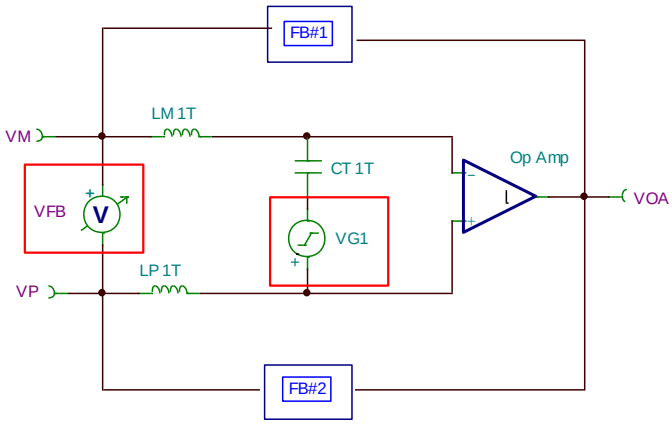
- Double L Break for Op Amp Stability Analysis
- Trust But Verify SPICE Op Amp Macromodels for Stability Analysis
- SPICE Convergence Tricks

“Double L Break”
For Op Amp Stability Analysis

Texas Instruments

This appendix will cover dual feedback paths and the Double L Break.

SPICE “Double L” Loop Gain Break Derivation



$\text{AolB} = \text{Loop Gain}$

$\beta = (\beta\text{-}) - (\beta+)$

$\beta- = \dfrac{VM}{VOA}$

$\beta+ = \dfrac{VP}{VOA}$

$\text{Aol} = VOA$

$\text{AolB} = VOA * \left(\dfrac{VM}{VOA} - \dfrac{VP}{VOA}\right)$

$\text{AolB} = VM - VP$

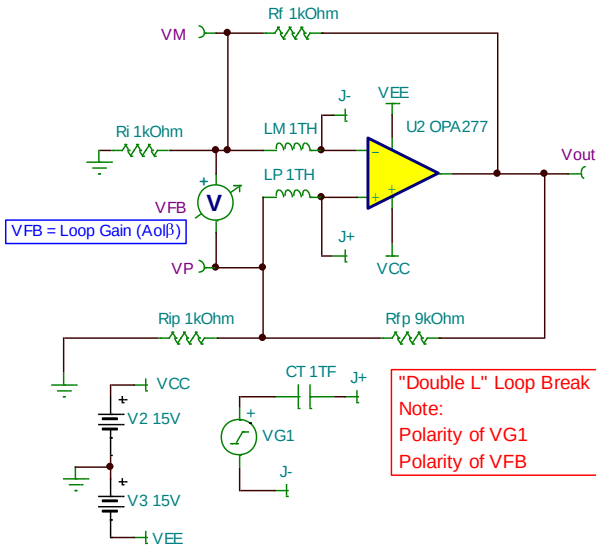
$VFB = VM - VP$

$\text{AolB} = VFB$

(Note polarity of meter VFB and VG1)

For SPICE analysis we will use the technique above to simulate for AolBeta, Loop Gain. By post processing math other plots can also be obtained for Beta+, Beta-, and 1//Beta as needed.

SPICE “Double L” Loop Gain Break Test



"Double L" Loop Break for Loop Gain Analyis
Note:
Polarity of VG1
Polarity of VFB

Loaded Aol = Vout

Loop Gain (Aolβ) = VFB

$$\beta- = \frac{VM}{Vout}$$

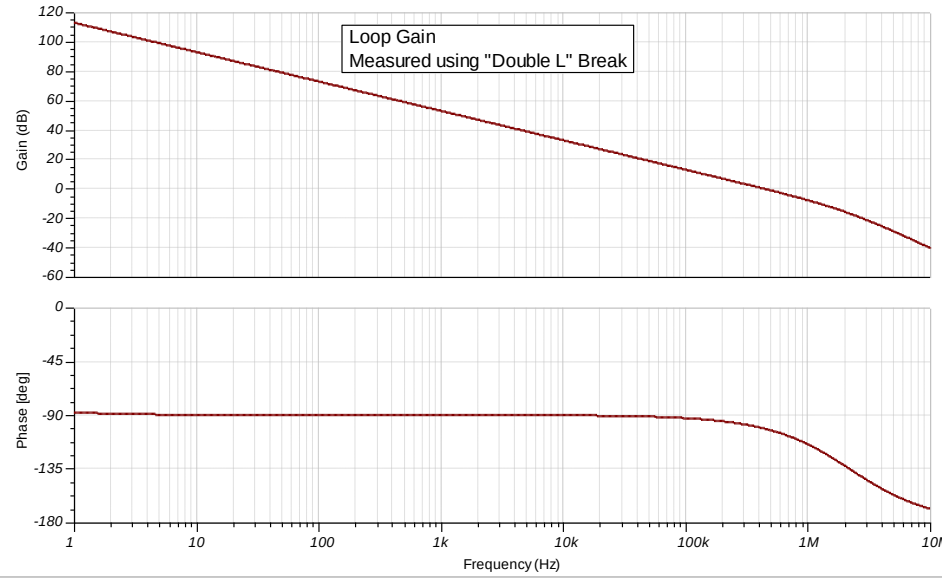
$$\beta+ = \frac{VP}{Vout}$$

$$\frac{1}{\beta} = \frac{1}{(\beta-)-(\beta+)} = \frac{1}{\left(\frac{VM}{Vout}\right)-\left(\frac{VP}{Vout}\right)}$$

Texas Instruments

This circuit will be used to test the double L break analysis for loop gain, AolBeta.

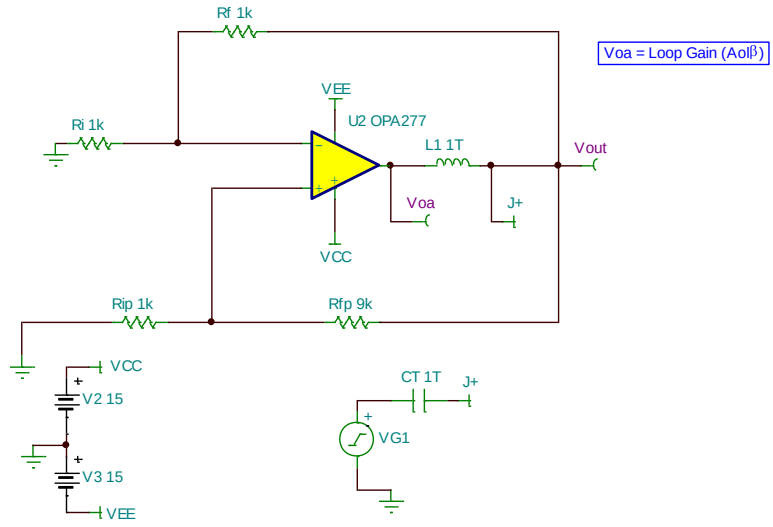
SPICE “Double L” Loop Gain Break Test



TEXAS INSTRUMENTS

Simulation results are shown here for the double L break technique to obtain loop gain, AolBeta.

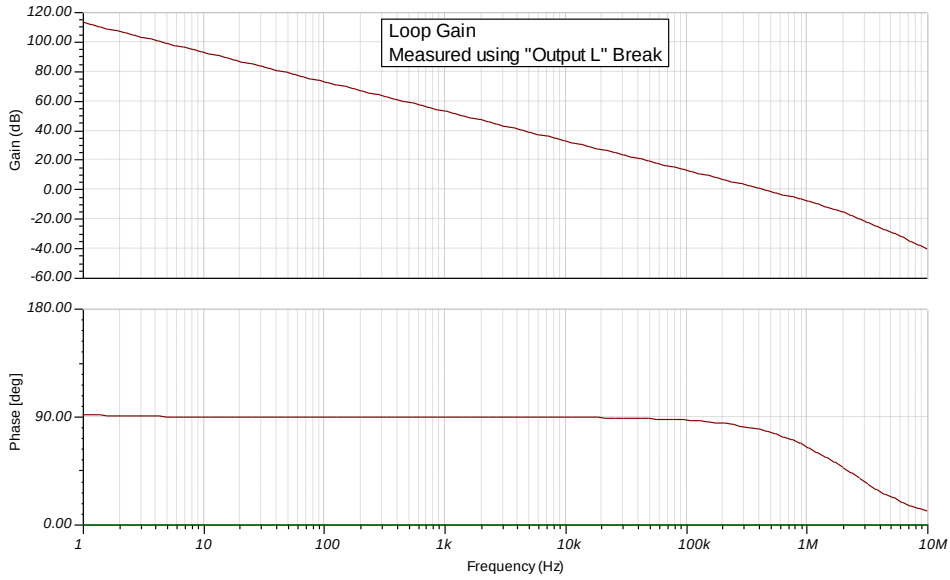
SPICE “Output L” Break Test



TEXAS INSTRUMENTS

To check that our double L break technique is accurate we will open the loop a different way with only one inductor in the output of the op amp using the output L break technique.

SPICE “Output L” Break Test matches “Double L” Break Test !



Texas Instruments

The output L Break technique matches our double L break technique.

Why “Double L” Break is Best

VFB = Loop Gain (Aolβ)

1) For capacitive loads, CL, “Double L” Break includes effects of Zo in Loop Gain Analysis.

2) If input op amp capacitance is of concern add Ccm+, Ccm-, Cdiff externally as shown.

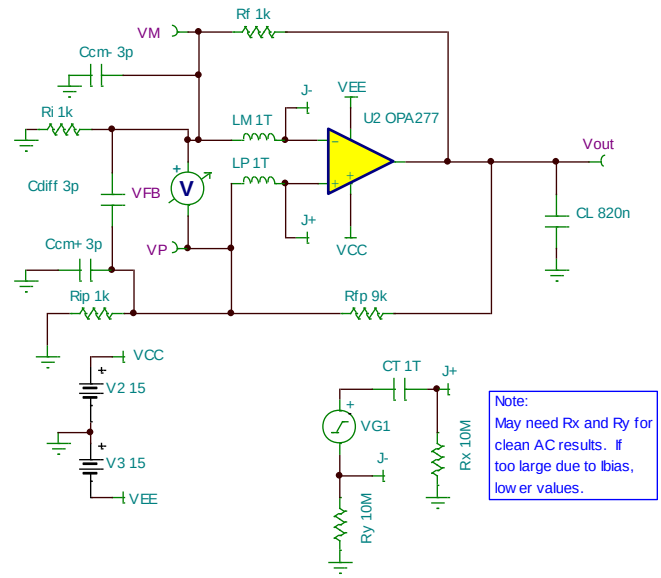
Loaded Aol = Vout

Loop Gain (Aolβ) = VFB

$$\beta- = \frac{VM}{Vout}$$

$$\beta+ = \frac{VP}{Vout}$$

$$\frac{1}{\beta} = \frac{1}{(\beta-)-(\beta+)} = \frac{1}{\left(\frac{VM}{Vout}\right)-\left(\frac{VP}{Vout}\right)}$$



TEXAS INSTRUMENTS

As shown above there are several advantages to the double L break technique when simulating in SPICE.

Appendix

- Double L Break for Op Amp Stability Analysis
- Trust But Verify SPICE Op Amp Macromodels for Stability Analysis
- SPICE Convergence Tricks

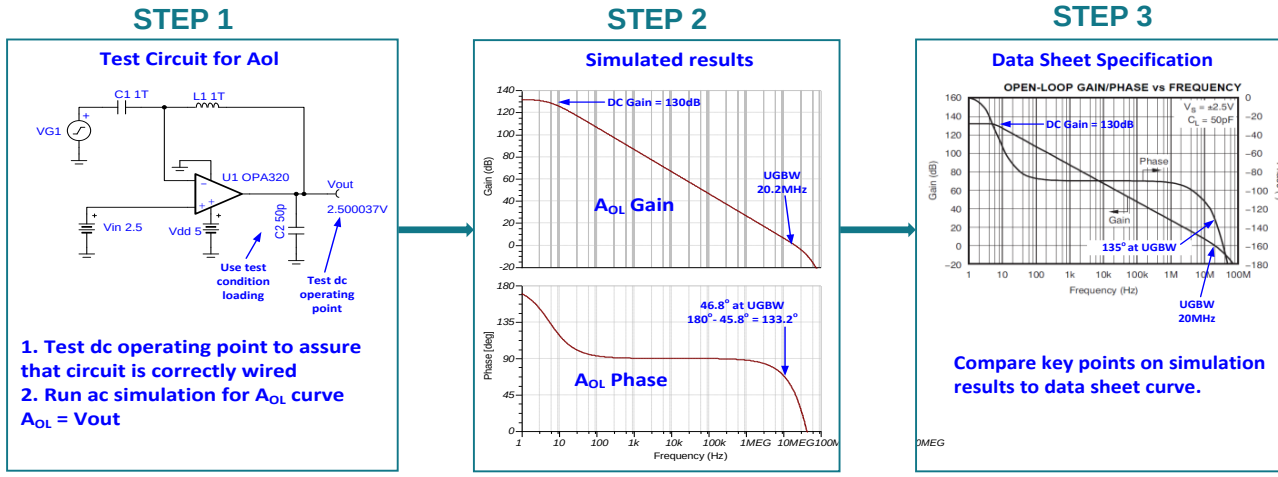
Trust But Verify
SPICE Op Amp Macromodels for Stability Analysis

Texas Instruments

For any Op Amp stability analysis to be accurate, the op amp macromodel must match the datasheet which matches real silicon. For op amp stability analysis the key parameters to “Trust, But Verify” are Aol (open loop gain) and Zo (op amp small signal AC open loop output impedance) or Zout (op amp small signal AC closed loop output impedance). How to test a SPICE op amp macromodel for these key parameters are presented in this appendix.

Op amp model: Open loop gain

Aol opa320_TG.TSC



Aol = -1*V_{OUT} for same phase in datasheet

http://www.ti.com/tool/TINA-TI

Texas Instruments

Simulation can be an incredibly powerful tool, but if you are going to rely on models to design your system then it is always a good idea to double check that the model behaves according to the datasheet specifications. Most modern models are sophisticated and cover many of the parameters that concern designers. However, it's easy to check the models and it's better to be confidant in its operation. This slide shows how you would test the model for open loop gain. First we see the Aol test circuit we discussed previously. In the center you can see the TINA spice simulation results, and at the right the data sheet specification for open loop gain of this particular device. To compare two plots look at a few points on the magnitude and phase plot. Some key points to consider are the dc gain, and the unity gain bandwidth on the magnitude plot. In the phase plot check the phase at the unity gain bandwidth frequency. Note that sometimes the phase plot will be off by a 180° as the phase depends on how the circuit is measured, to have the simulation phase match the datasheet you can use the post-processor tool to generate the negative of the Aol curve. In this example you can see good agreement between the simulated results and the data sheet curve.

Some data sheets specify Z_{OUT} *NOT* Z_O

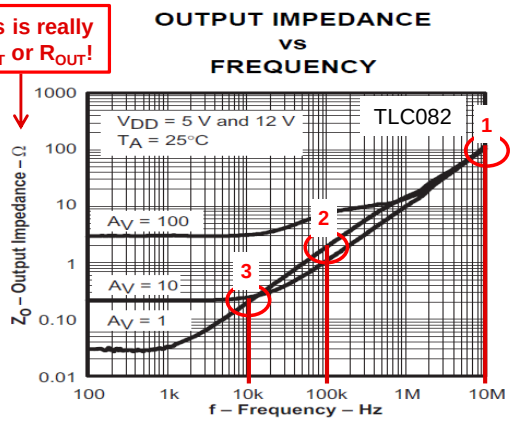
Recognize R_{OUT} instead of R_O:

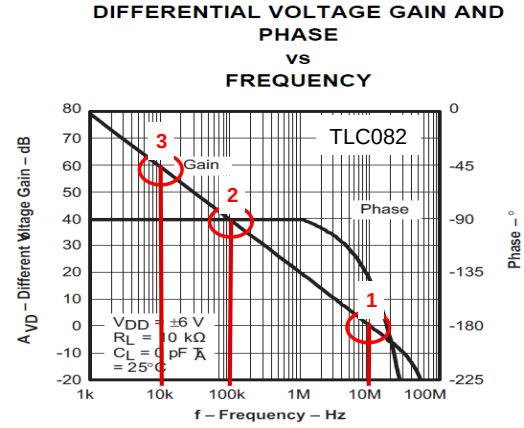
R_{OUT} inversely proportional to AoI:

$$R_{OUT} = \frac{R_O}{1 + Aol\beta}, \text{where } R_{OUT} \propto \frac{1}{Aol}$$

R_{OUT} typically <100Ω at high frequency

This is really Z_{OUT} or R_{OUT}!

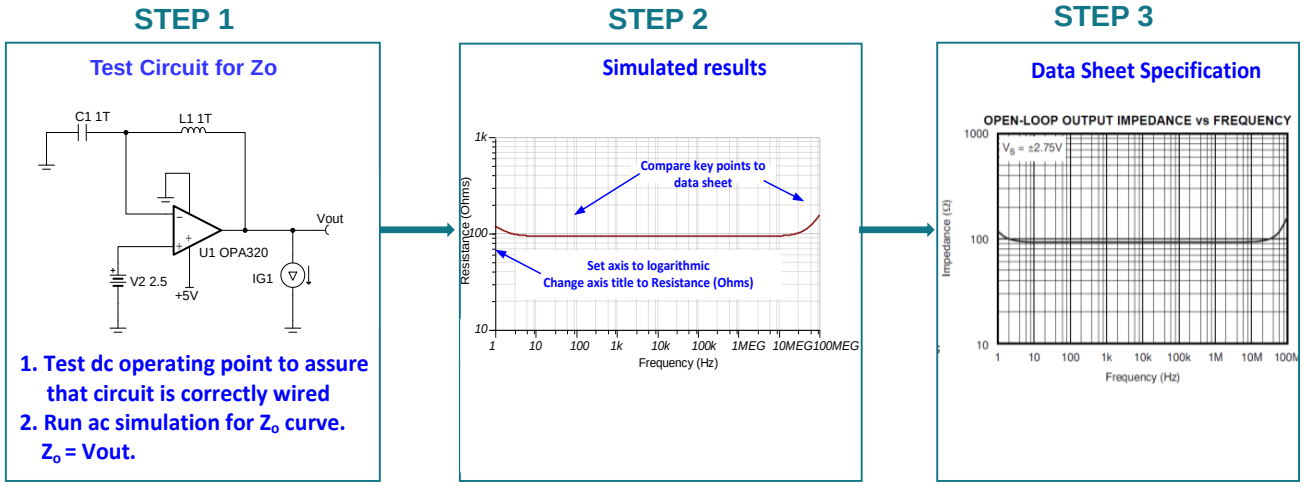




Texas Instruments

Not all manufacturers will specify parameters in the same way or provide the same curves, so it is important to understand which curve you are looking at. Within Texas Instruments, we try to use the term Zo to refer to the open loop output impedance and Zout to refer to the closed loop output impedance, but not all datasheets conform to this standard. The easiest way to identify which curve you are looking at is to check for a gain specification associated with the curve. In the above example we can see curves for a gain of 1, 10, and 100. This immediately tells us the amplifier must have been in a closed loop configuration for the measurement and thus we know we are looking at the closed loop output impedance. Additionally, the closed loop output impedance is going to be inversely proportional to Aol, whereas the open loop output impedance is completely independent of Aol. The last hint is that the closed loop output impedance will tend to be much smaller and is typically less than 100 Ohms even out at high frequency.

Op amp model: Open loop output impedance

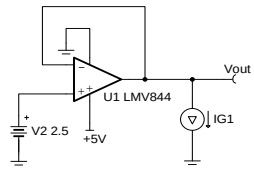


As discussed, another important curve is the open loop output impedance. The circuit used for this test is similar to the open loop gain test, as the feedback loop is broken for AC but is shorted for DC operation. The output here is connected to an AC current generator, and a voltage measurement probe is included. Also notice that the input is biased so that the output will be in a linear voltage range. This is necessary if you choose to simulate the device with a single supply. Again, for any simulation it is important to verify the DC operation before the AC simulation. This helps avoid problems caused by incorrect wiring. Once the circuit is connected and it's DC operation is confirmed you can run the "AC Analysis>AC Transfer Characteristic". For this simulation the output voltage is equal to the open loop output impedance, that is Zo (dB) = Vout (dB). Make sure that you change the vertical axis to logarithmic and scale to match the data sheet curve. In this case, you can see that the simulation result closely matches the data sheet specification so this model has properly modeled open loop output impedance.

Op amp model: Closed loop output impedance

STEP 1

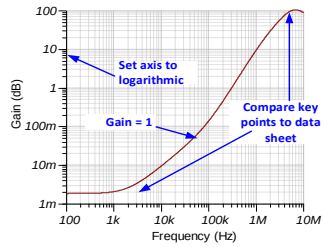
Test Circuit for Zout



1. Test dc operating point to assure that circuit is correctly wired
2. Run ac simulation for Z_{out} curve. Z_{out}= Vout.
3. Change the vertical axis to logarithmic scale

STEP 2

Simulated results



Y-axis = Logarithmic → Ohms

STEP 3

Data Sheet Specification

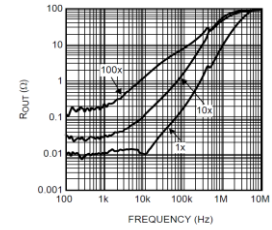


Figure 33. Closed-Loop Output Impedance vs Frequency

http://www.ti.com/tool/TINA-TI

LMV844 Zout_TG.TSC

TEXAS INSTRUMENTS

If the manufacturer only provides a closed loop output impedance curve, the open loop output impedance is directly related so it is sufficient to verify either curve. So in cases where the data sheet provides a closed loop output impedance curve, you can simulate this test circuit. Since this is closed loop impedance the feedback network is set according to the required gain. This example shows a gain of 1, but other gains may be needed depending on the data sheet graph. The output is connected to a current generator and a voltage measurement probe. Closed loop output impedance is equal to the output voltage in this simulation, that is Zout (dB) = Vout(dB). By changing the Y-axis to Logarithmic we get Zout in ohms (Zout(ohms) = Vout(Logarithmic)). Notice that the simulation results closely match the data sheet curve for unity gain. As long as the Aol and Zout curves of the model match the datasheet, then you can be confident that the open loop output impedance is also modeled accurately.

Appendix

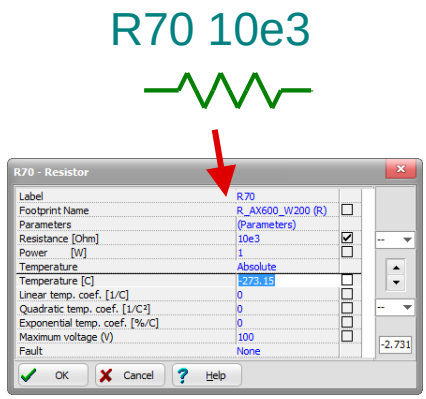
- Double L Break for Op Amp Stability Analysis
- Trust But Verify SPICE Op Amp Macromodels for Stability Analysis
- SPICE Convergence Tricks

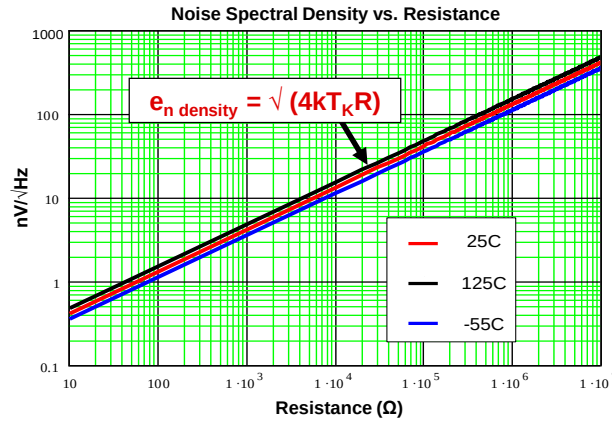
SPICE Convergence Tricks

This appendix offers some handy SPICE simulation tricks for circuits that are having trouble with convergence.

SPICE Performance Tip – Noiseless Resistors

- Use noiseless resistors to ensure noise is only set by designated noise sources
  - Set resistor temperature to -273.15°C to remove thermal noise
    - Thanks Samir Cherian for the tip!





Texas Instruments

Resistors generate noise based on their resistance value and temperature, so higher-value resistors in the signal path contribute to noise

This may be a problem for low-noise amplifiers that need certain resistor scaling to optimize convergence.

Setting the component-level absolute temperature to absolute zero (-273.15C, or 0K) will eliminate this noise.

The component-level temperature setting will override any global simulation temperature settings.

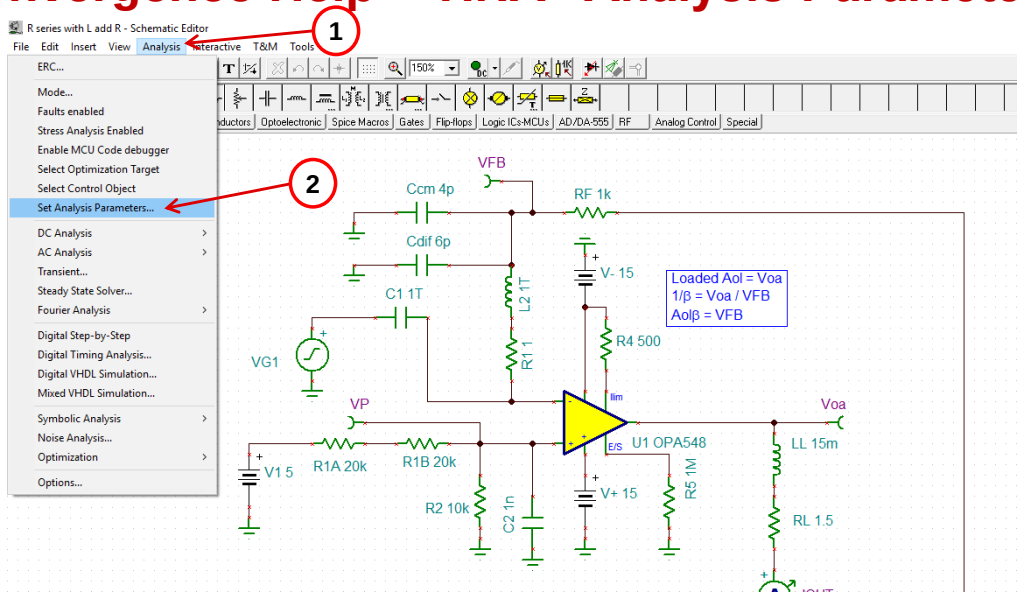
Convergence Help - Analysis Parameters

Option	Default	Relaxed	Effect
ABSTOL	1e-12	1e-10	Sets the absolute tolerance of nodal currents between DC iterations
RELTOL	1e-3	3e-3	Sets the relative tolerance of the nodal voltages at each DC iteration compared to the first
GMIN	1e-12	1e-10	Adds conductance parallel to every p-n junction
CSHUNT	0	1e-15	Adds capacitance from every node to ground

The names of these parameters may vary with the simulator software!

This table shows some common Analysis Parameters that can be adjusted to help with SPICE simulations that are having convergence problems.

Convergence Help – TINA "Analysis Parameters"

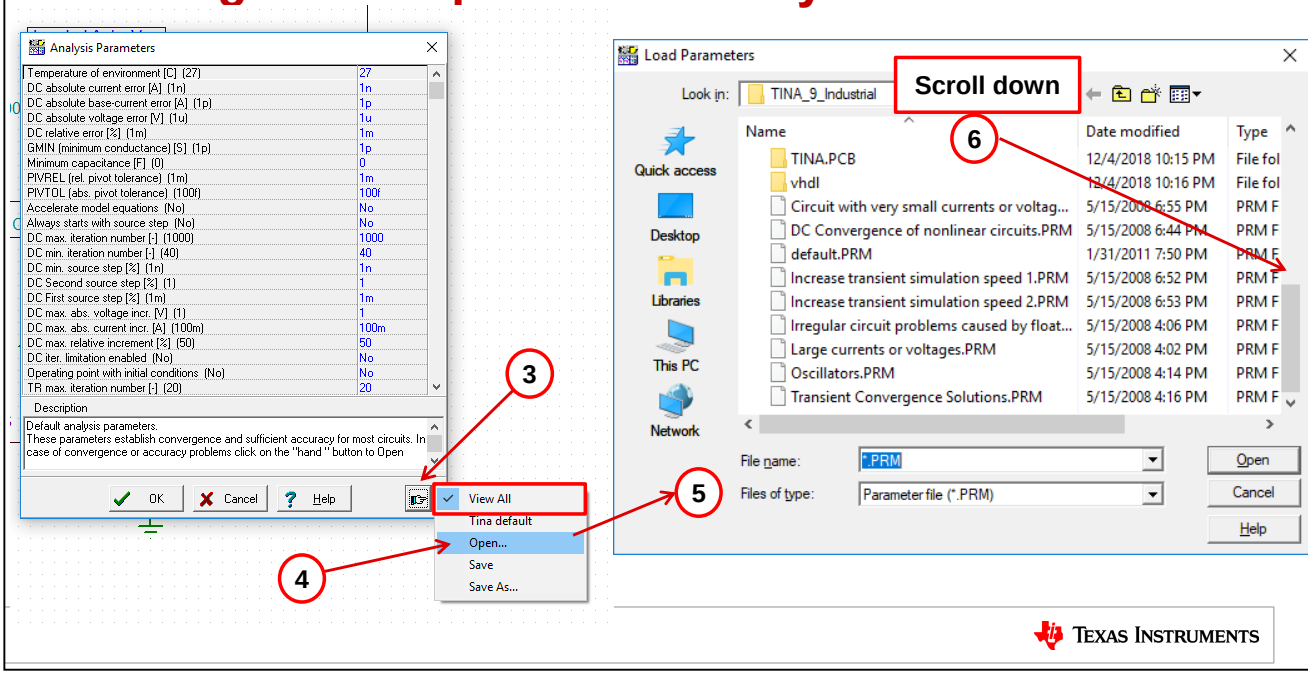


http://www.ti.com/tool/TINA-TI

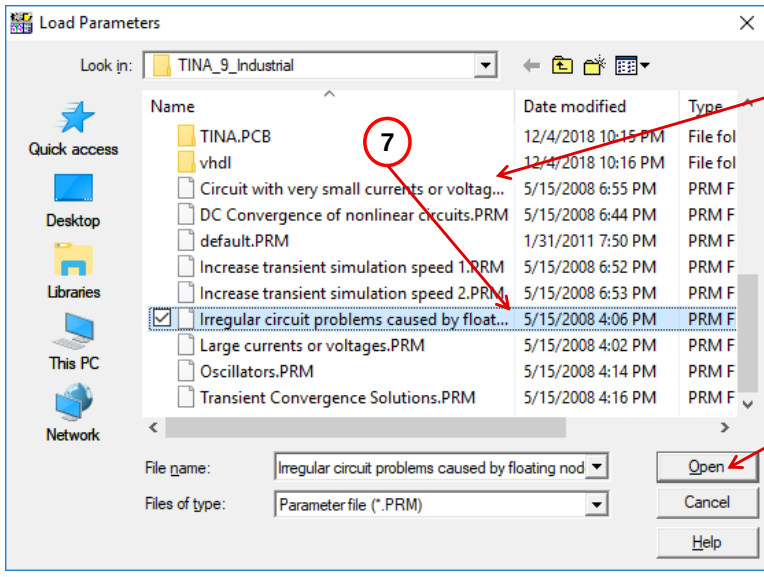
Texas Instruments

The next few slides will cover a way to get to special settings for Analysis Parameters when a circuit is not converging on a simulation using TINA-TI SPICE, a free SPICE simulator from Texas Instruments.

Convergence Help – TINA "Analysis Parameters"

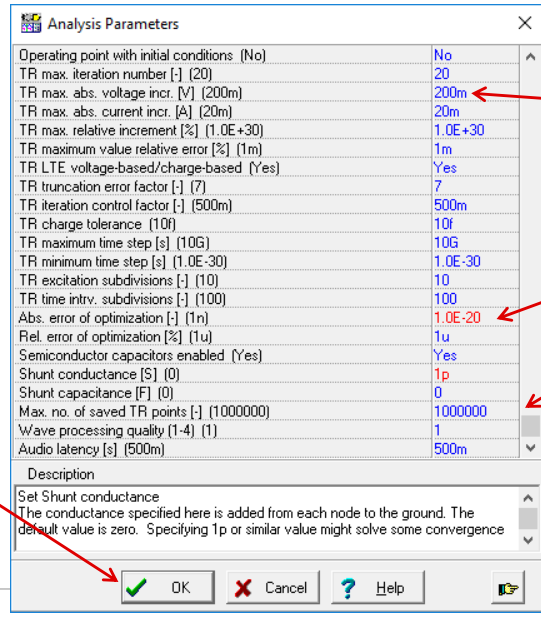


Convergence Help – TINA "Analysis Parameters"



Note the recommended files for the convergence problem.

Convergence Help – TINA "Analysis Parameters"



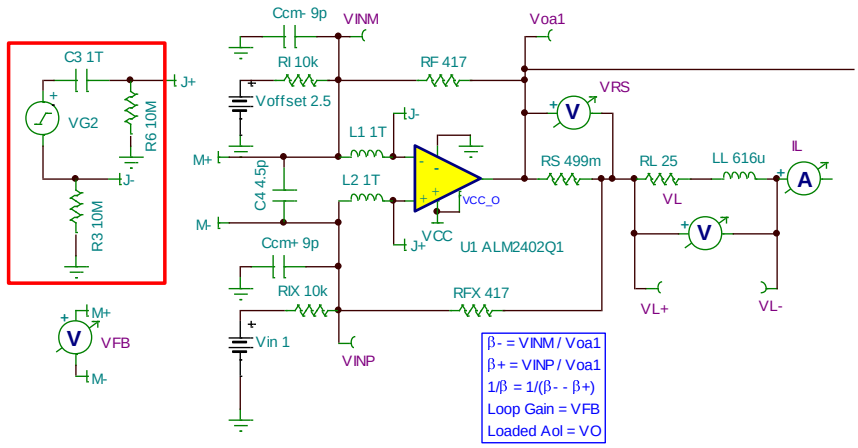
TINA Default Parameters stay blue. Changed Parameters turn red.

May need to scroll down to see Changed Parameters.

9

Convergence Help – DC Path to GND

- Look for a clear DC path to GND for all nodes in the schematic
- Add large value resistors as needed for a DC Path to GND
- Resistors can easily be made “noiseless”

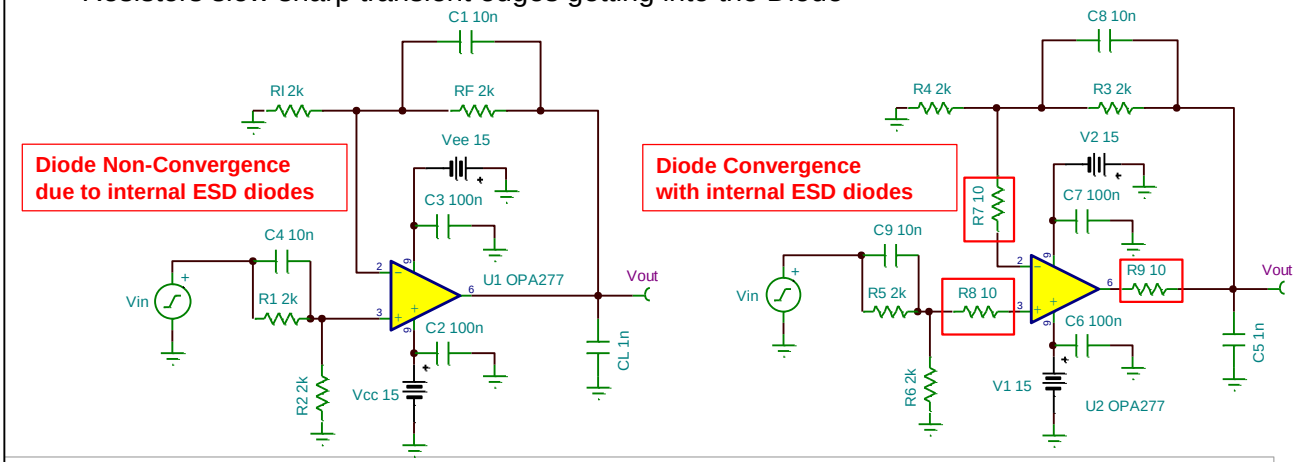


TEXAS INSTRUMENTS

When analyzing a circuit for simulation that is having convergence problems, check that all nodes have a clear and “easy” path to Ground as shown by this example.

Convergence Help – Diode Errors

- Diodes can be a difficult device for SPICE to converge on
- If Convergence Error shows any Diode add series resistors (noiseless if needed) as shown
- Resistors slow sharp transient edges getting into the Diode



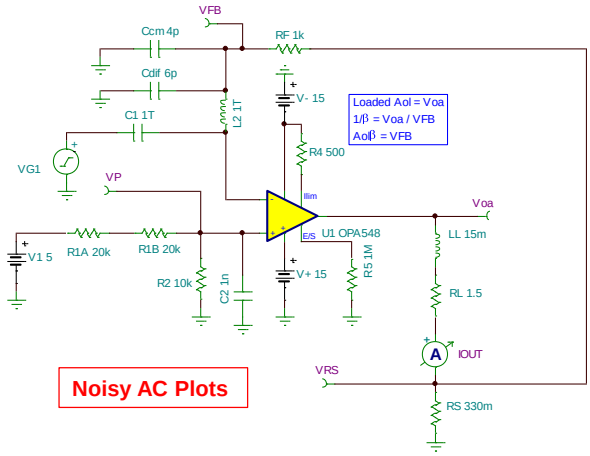
Texas Instruments

If you get an error in a circuit simulation that reference a diode, sometimes internal to an op amp macromodel on their inputs or outputs, add a series resistor to help SPICE converge on sharp transients by slowing down voltages and currents into and around the diode.

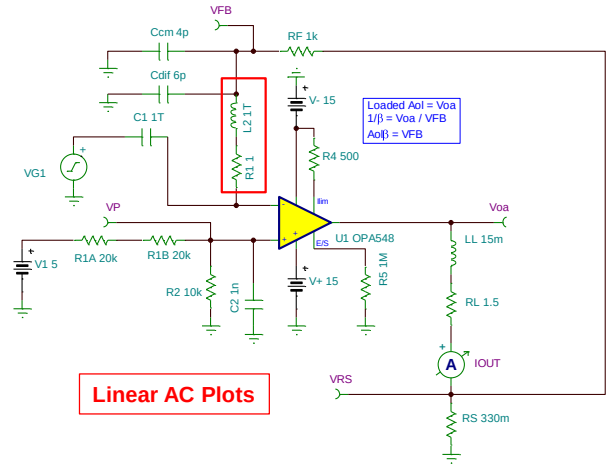
Convergence Help – Large Inductors/Capacitors

If AC Bode plots, when doing loop analysis, contain large noisy plots (random and large spiking of the plot – not a smooth continuous line):

1) **Add small series resistor with L2 and/or C1**
2) **Lower values of L2 and C1 (1T→1M)**



Noisy AC Plots



Linear AC Plots

TEXAS INSTRUMENTS

When using large inductors, L2 here, such as when running loop gain simulations for stability analysis, add a small series resistor, R1, to help if convergence issue occur or if the AC analysis shows “noisy” Bode plots with large and frequent transitions in the plot. Sometimes this is referred to as “math noise”. You may also need to add a small series resistor with the large value capacitor, C1. Depending upon the op amp macromodel used you may need to lower the values of L2 and C1 from 1Tera to 1Meg.

Thanks for your time!