AFE031 Transmit Path

use either AFE031 or MCU DAC
DAC output range is limited by TX_PGA input range to 1.65V ±1.55V

TX_PGA input voltage range 1.65±1.55V
TX_PGA gain 0.25, 0.5, 0.707 or 1.0
TX_PGA output voltage range 1.65±1.55V

TX_F input voltage range 1.65±1.55V
TX_F 4rth order unity gain LPF, fc 95KHz
TX_F output voltage range 1.65±1.55V

TX_PA input voltage range -0.1 to V(pa_vs)+0.1V
HPF formed by C51 and PA_IN R(in) 20kΩ, fc=1/2(PI)(C51)(20kΩ)
TX_PA gain -6.5 (fixed)
TX_PA output voltage offset V(pa_vs)/2

AFE031 Receive Path

BPF, 25kHz to 65kHz

HPF formed by C55 and RX_PGA1 Rin, fc=1/2(PI)(.01uf)(Rin), fc 663Hz to 1.6kHz*
RX_PGA1 Rin 10k to 24kΩ*
RX_PGA1 input voltage range 10Vpp
RX_PGA1 gain 0.25, 0.5, 1 or 2
RX_PGA1 output voltage range 1.65±1.55V

RX_F input voltage range 1.65±1.55V
RX_F 4rth order unity gain LPF 90kHz
RX_F output voltage range 1.65±1.55V

RX_PGA2 1st order HPF, fc 300Hz to 9.36kHz*
RX_PGA2 Rin 1.7k to 53kΩ*
RX_PGA2 input voltage range 1.65±1.55V
RX_PGA2 gain 1, 4, 16 or 64
RX_PGA2 output voltage range 1.65±1.55V
RX_PGA2 max. output impendance 1Ω

* gain dependent

CLT+ Analog Front End (AFE)

Sheet 4 Layout Notes
1. PCB should be designed such that AFE031 thermal pad provides the least thermal resistance as is realistically practical, see TI's AFE031 application report SBOA130A
2. Traces originating at AFE031 pins 42 & 43 and ending at J8 should be rated for 1.5A
3. R36, R40, C67, C68, C69 should be close to their AFE031 pads