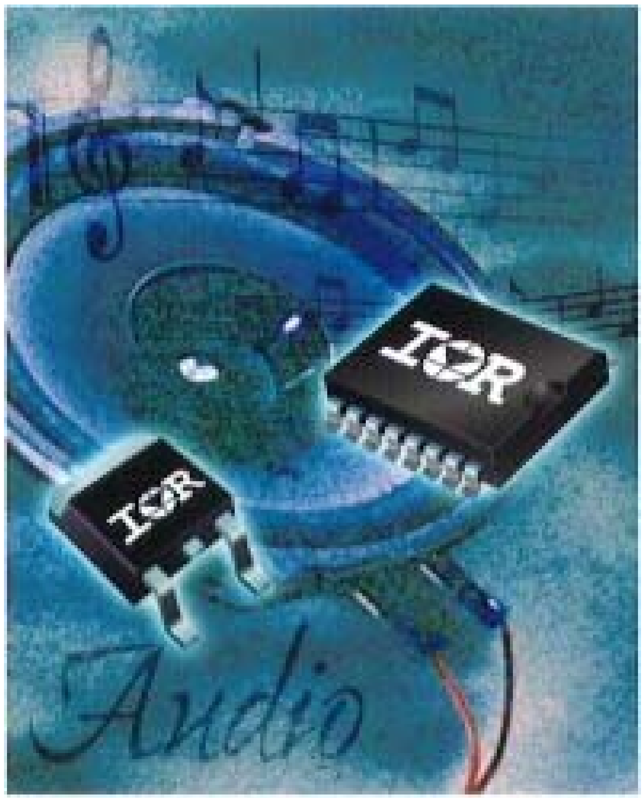
Class D Audio Amplifier Design



- **Class D Amplifier Introduction**

  Theory of Class D operation, topology comparison

- **Gate Driver**

  How to drive the gate, key parameters in gate drive stage

- **MOSFET**

  How to choose, tradeoff relationships, loss calculation

- **Package**

  Importance of layout and package, new packaging technology

- **Design Example**

  200W+200W stereo Class D amplifier

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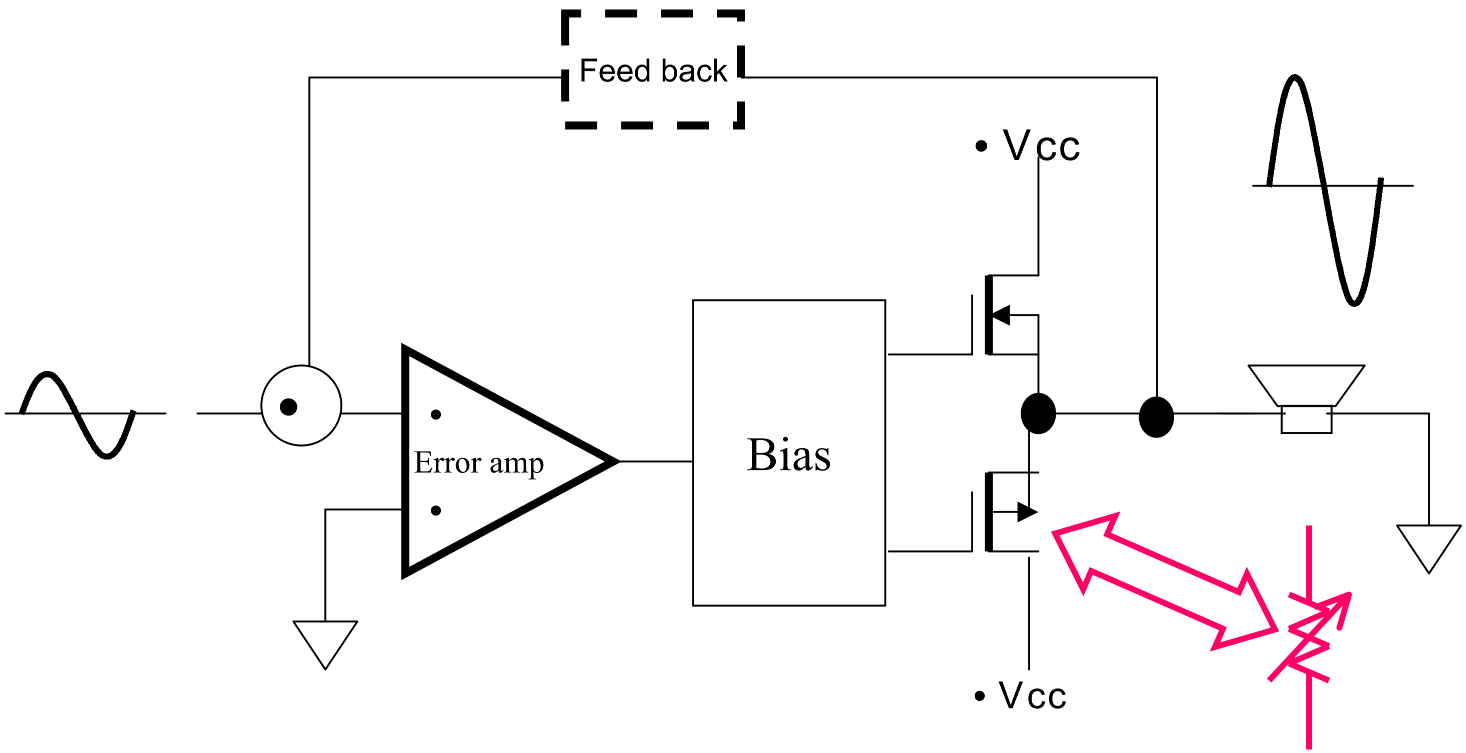
Prepared Oct.8 2003 by Jun Honda and Jorge Cerezo

Trend in Class D Amplifiers

- **Make it smaller!**
  - **- higher efficiency**
  - **- smaller package**
  - **- Half Bridge**

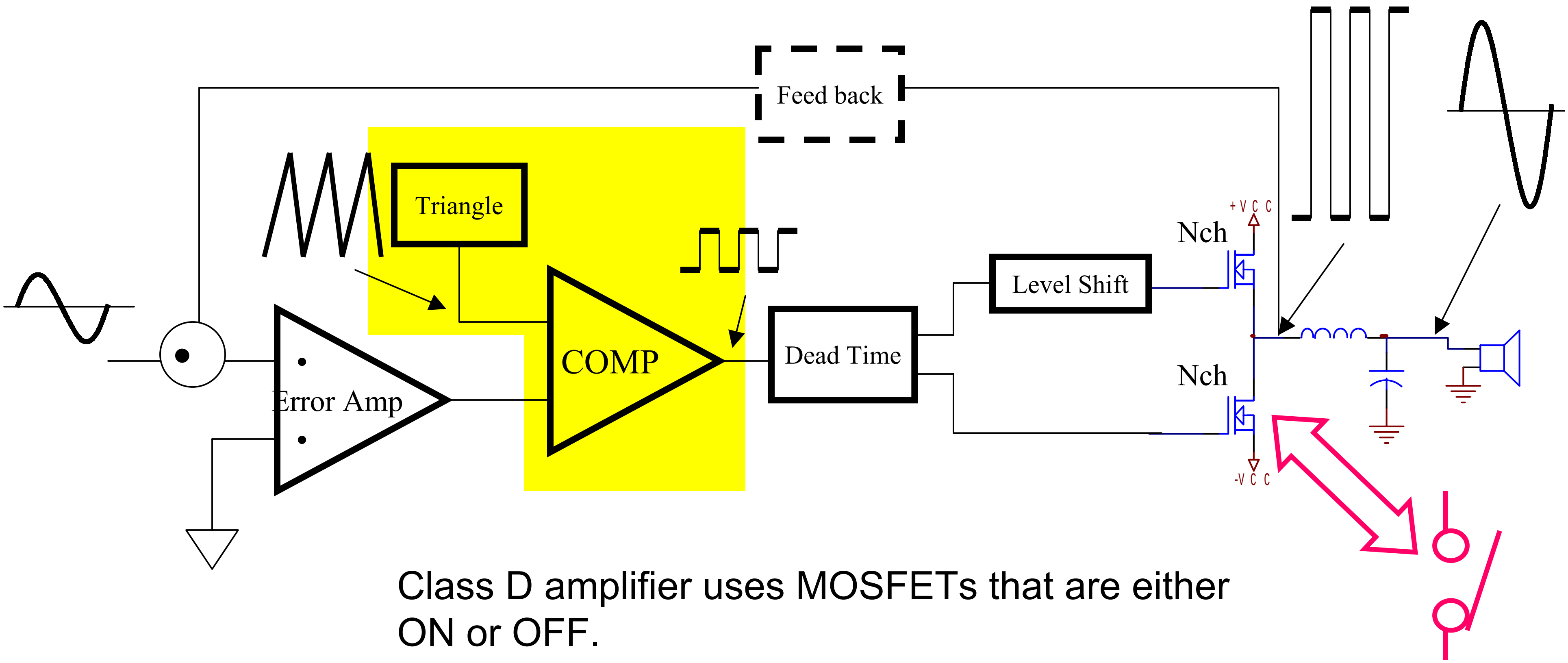
- **Make it sound better!**
  - **- THD improvement**
  - **- fully digitally processed modulator**

Traditional Linear Amplifier



Class AB amplifier uses linear regulating transistors to modulate output voltage. η = 30% at temp rise test condition.

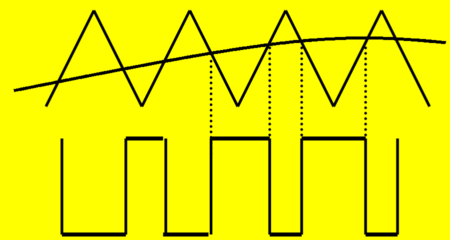
How a Class D Amplifier Works



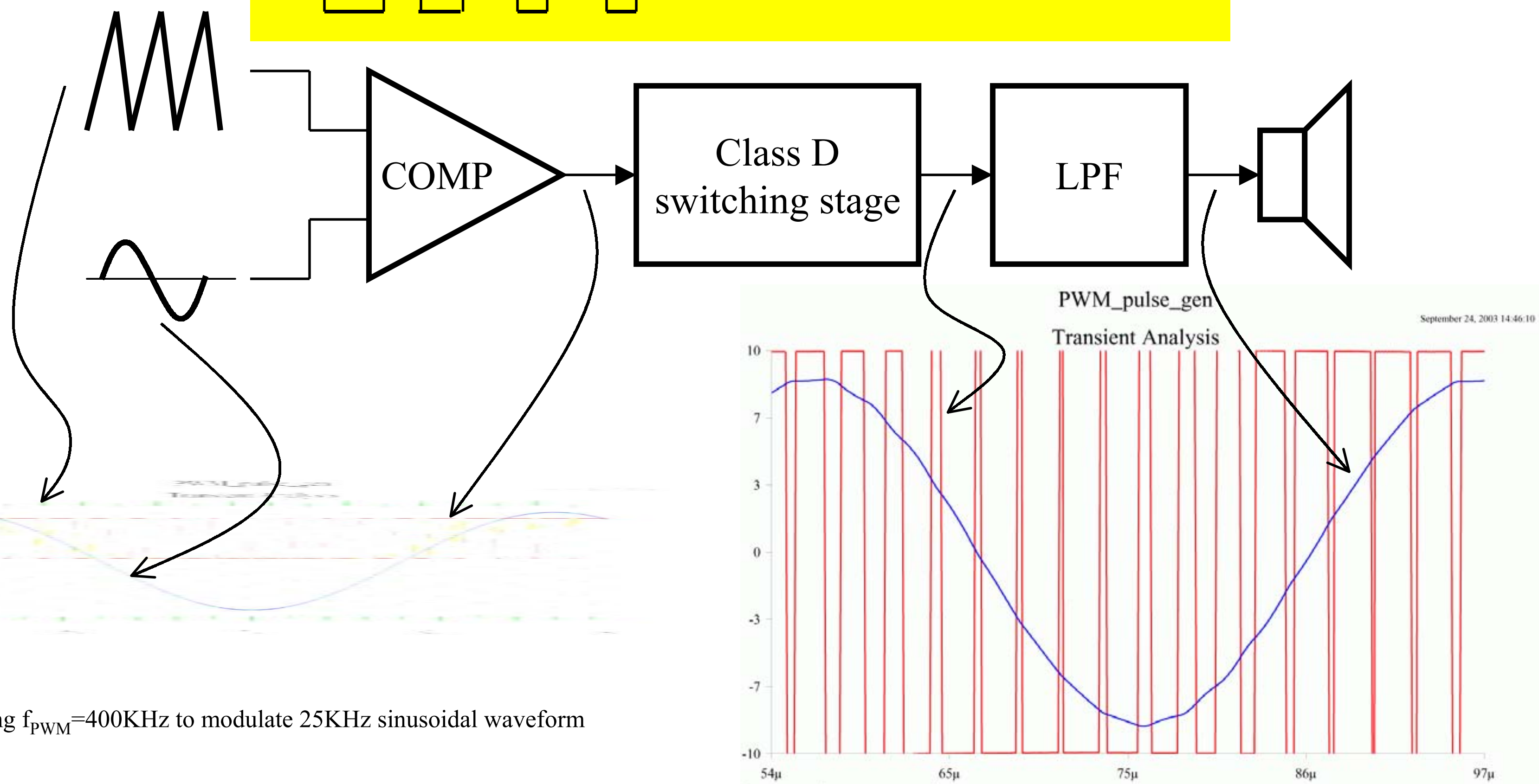
Class D amplifier uses MOSFETs that are either ON or OFF.

PWM technique is used to express analog audio signals with ON or OFF states in output devices.

Basic PWM Operation

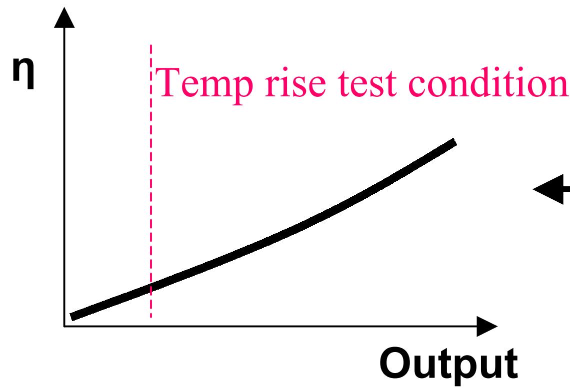


The output signal of comparator goes high when the sine wave is higher than the sawtooth.

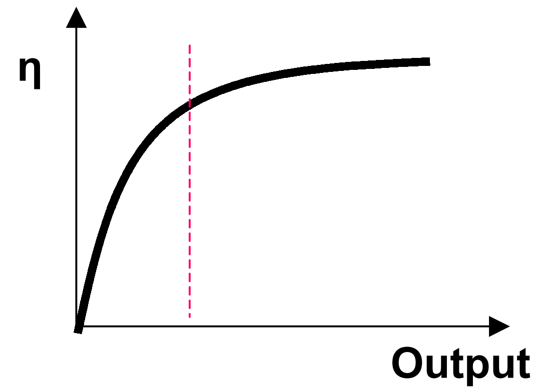


Using f_{PWM}=400KHz to modulate 25KHz sinusoidal waveform

Topology Comparison: Class AB vs Class D



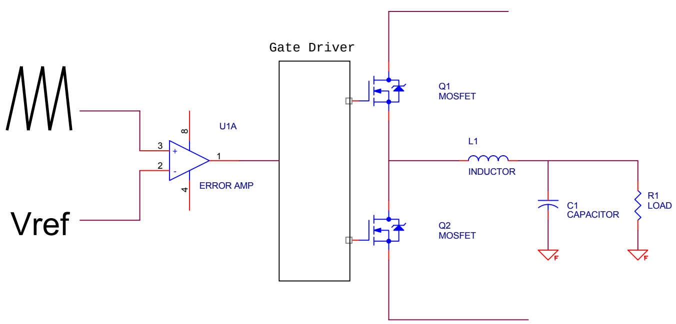
← Efficiency →



Class AB		Class D
Constant over Vbus ←	Gain	→ Proportional to Vbus
Good ←	PSRR	→ 0 dB
Always from supply to load ←	Direction of energy flow	→ Both way Creates Vbus pumping phenomena

Analogy to Buck DC-DC Converter

Buck Converter



Load Current Direction

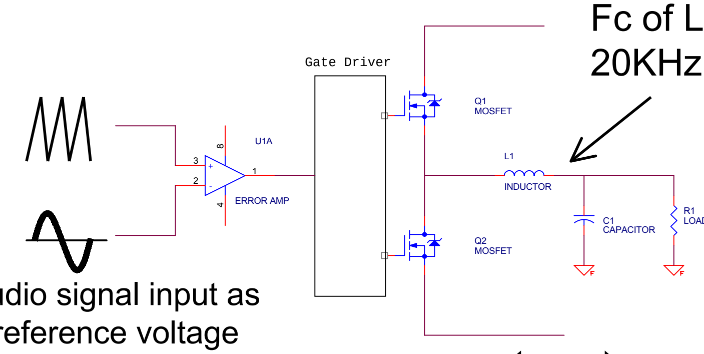
Duty ratio is fixed

→Independent optimization for HS/LS

→Low $R_{DS(ON)}$ for longer duty, low Qg for shorter duty

Class D Amplifier

Fc of LPF is above 20KHz



Audio signal input as a reference voltage

Both current directions

→ Influence of dead time is different

→ Dead time needs to be very tight

Duty varies but average is 50%

→Same optimization for both MOSFETs

→Same $R_{DS(ON)}$ required for both sides

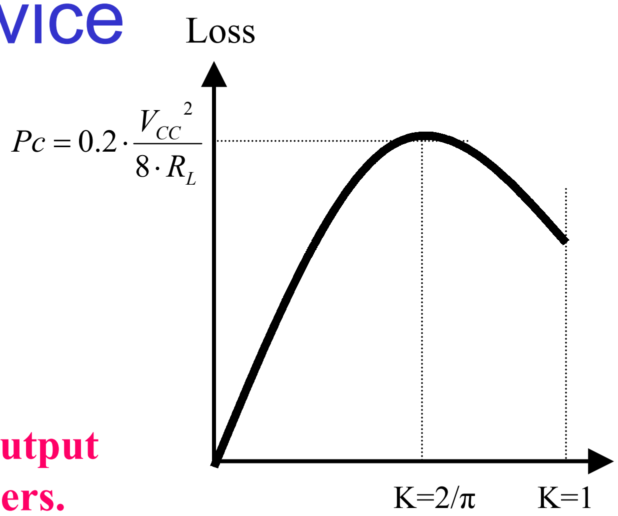
Loss in Power Device

Loss in class AB

$$P_C = \frac{1}{2\cdot\pi}\cdot\int_0^{\pi}\frac{Vcc}{2}(1-K\sin\omega\cdot t)\frac{Vcc}{2\cdot R_L}K\sin\omega\cdot t\bullet d\omega\cdot t$$

$$= \frac{Vcc^2}{8\pi\cdot R_L}\cdot\left(\frac{2K}{\pi}-\frac{K^2}{2}\right)$$

Regardless of output device parameters.

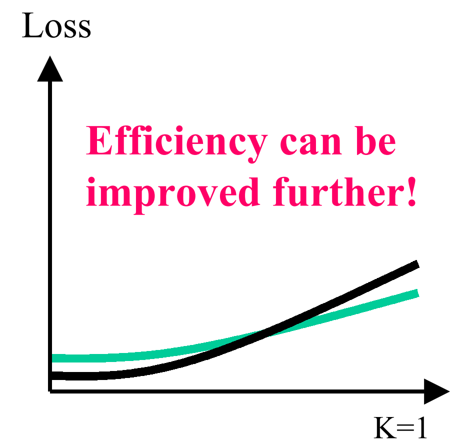


Loss in Class D

$$P_{TOTAL} = Psw + Pcond + Pgd$$

$$Pcond = \frac{R_{DS(ON)}}{R_L}\cdot Po \qquad Pgd = 2\cdot Qg\cdot Vgs\cdot f_{PWM}$$

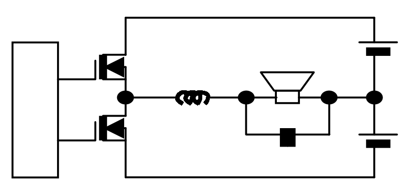
$$Psw = C_{OSS}\cdot V_{BUS}^2\cdot f_{PWM} + I_D\cdot V_{DS}\cdot t_f\cdot f_{PWM}$$

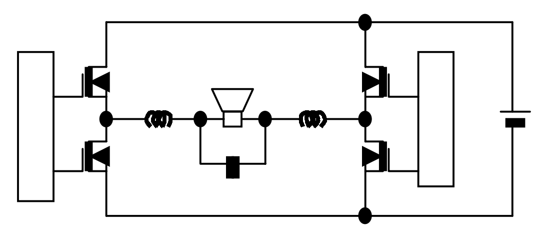


K is a ratio of Vbus and output voltage.

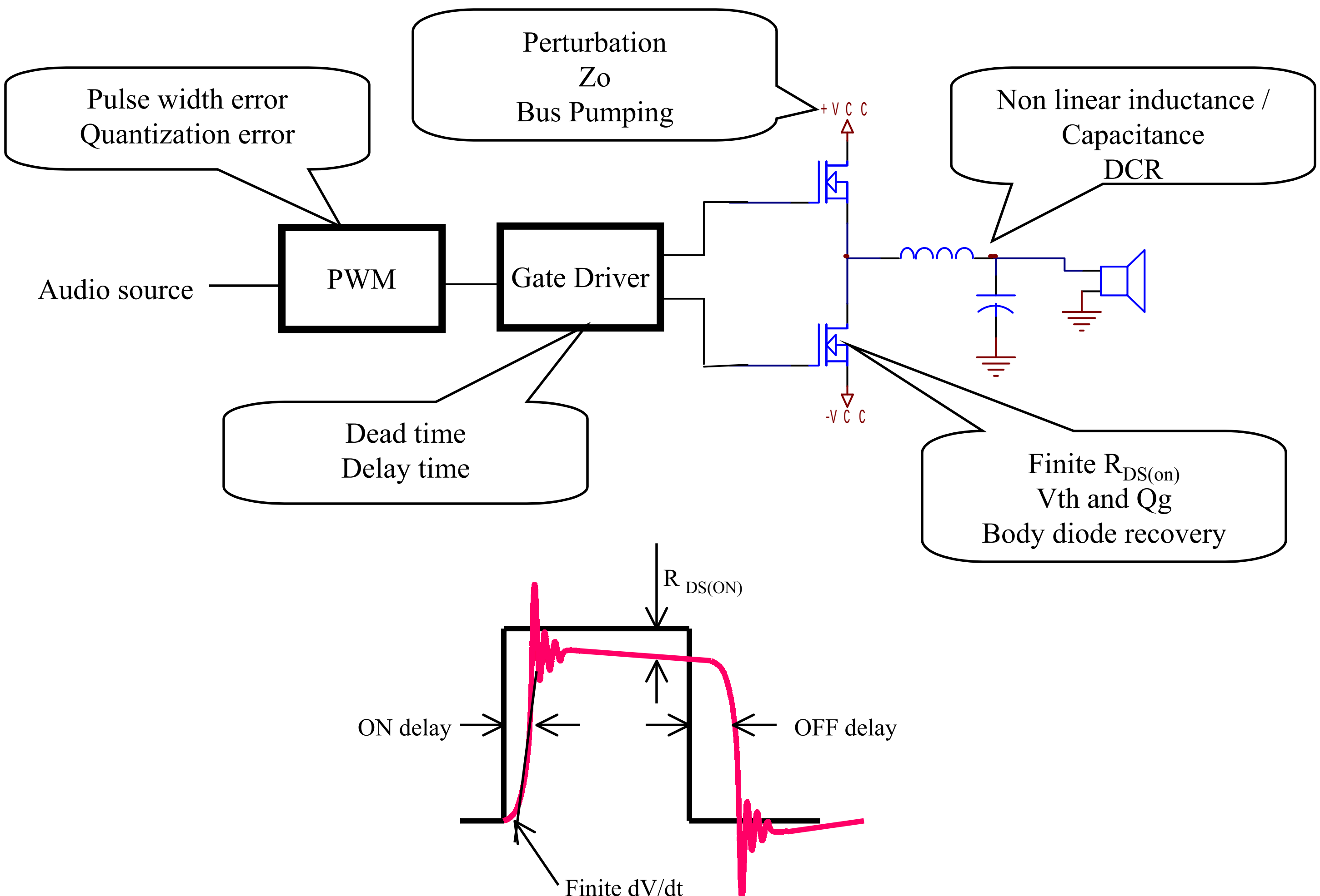
Half Bridge vs Full Bridge

Supply voltage	0.5 x 2ch	1
Current ratings	1	2
MOSFET	2 MOSFETs/CH	4 MOSFETs/CH
Gate Driver	1 Gate Driver/CH	2 Gate Drivers/CH
Linearity		Superior (No even order HD)
DC Offset	Adjustment is needed	Can be cancelled out
PWM pattern	2 level	3 level PWM can be implemented
Notes	Pumping effect Need a help of feed back	Suitable for open loop design

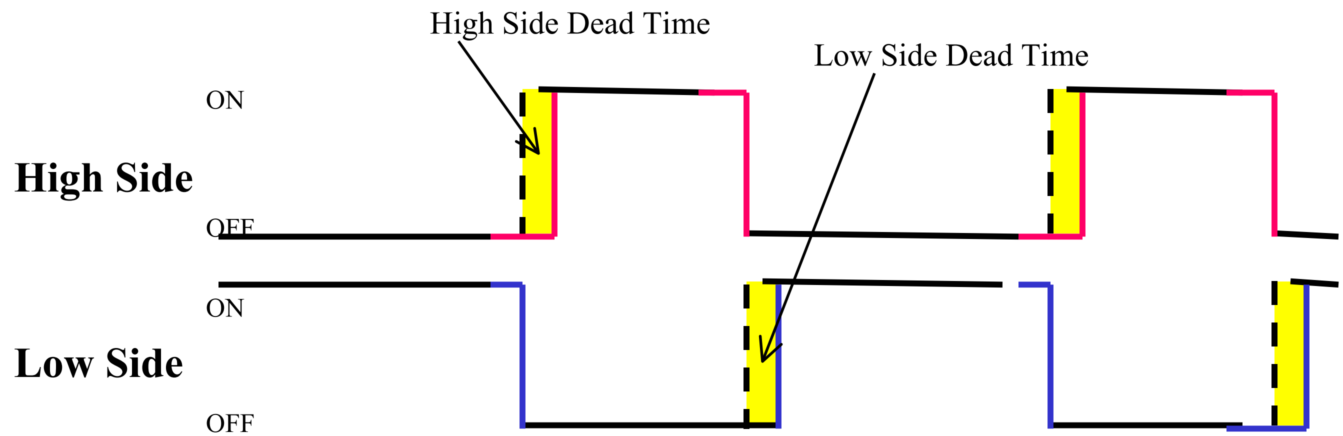


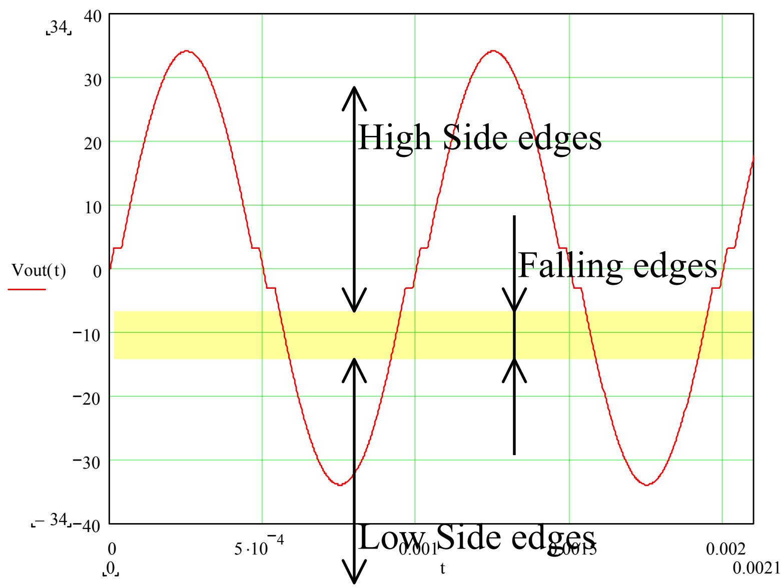


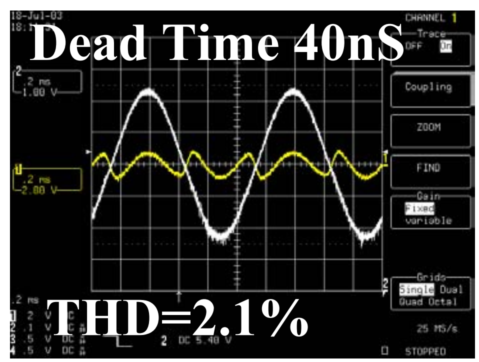
Major Cause of Imperfection

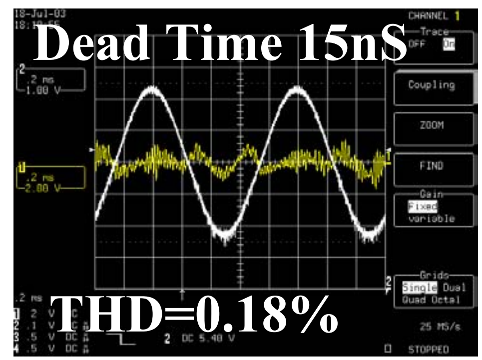


THD and Dead Time





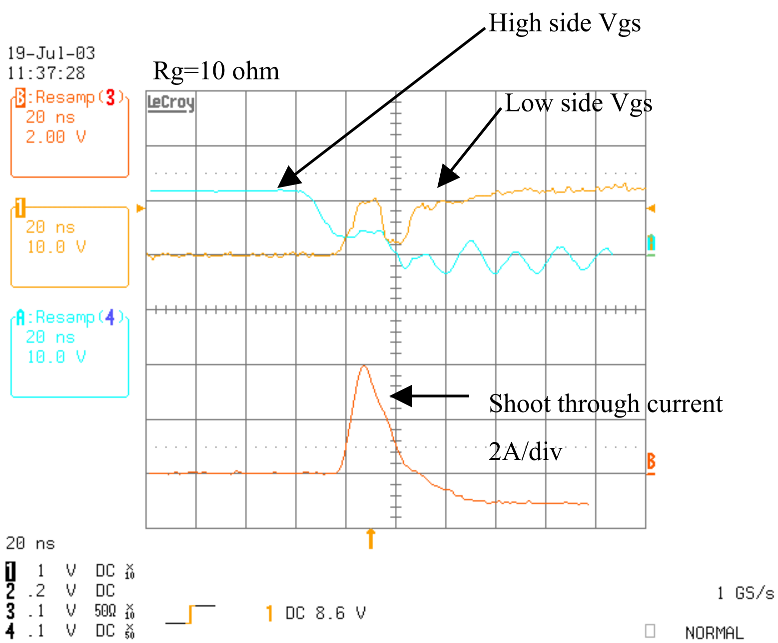


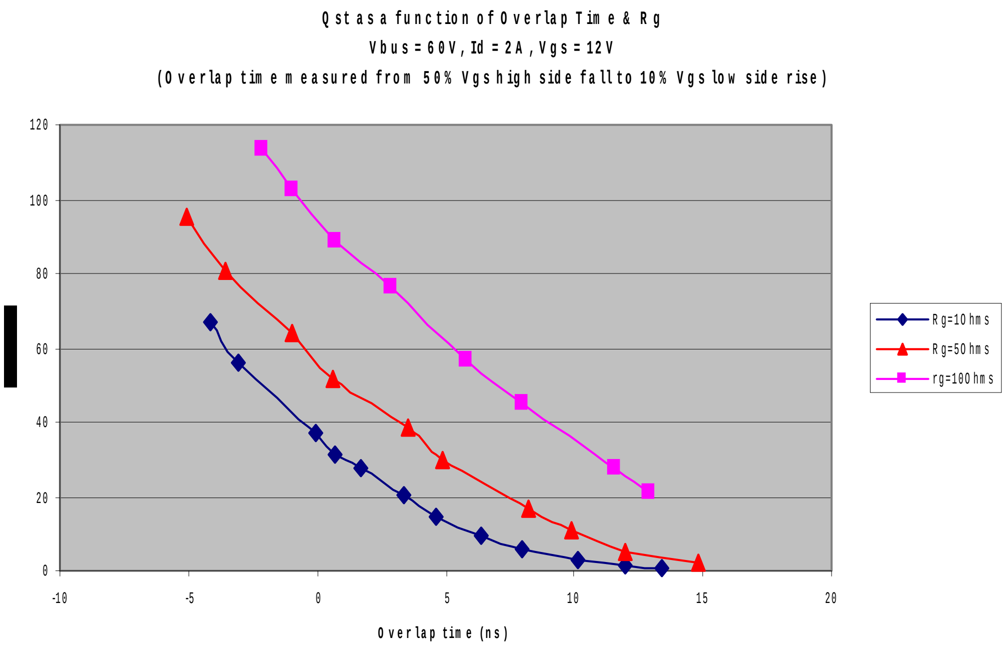


Note: THD (Total Harmonic Distortion) is a means to measure linearity with sinusoidal signal.

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + \cdots}}{V_{fundamental}}$$

Shoot Through and Dead Time

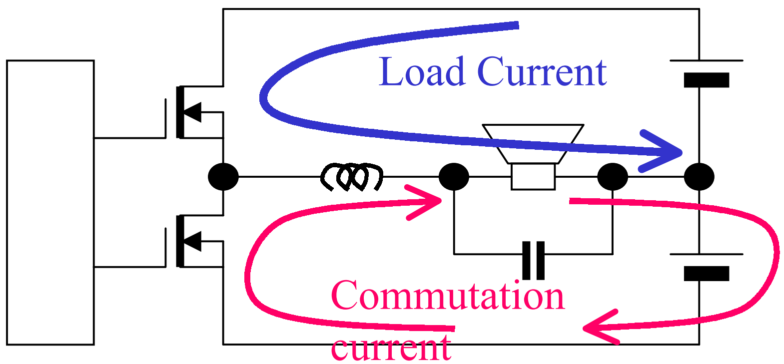




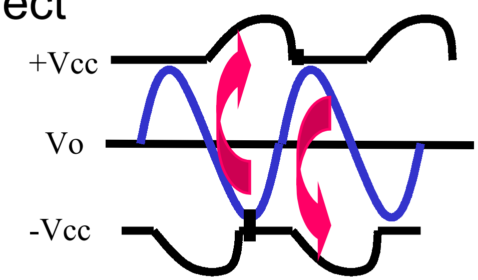
-Shoot through charge increases rapidly as dead time gets shorter.

-Need to consider manufacturing tolerances and temperature characteristics.

Power Supply Pumping



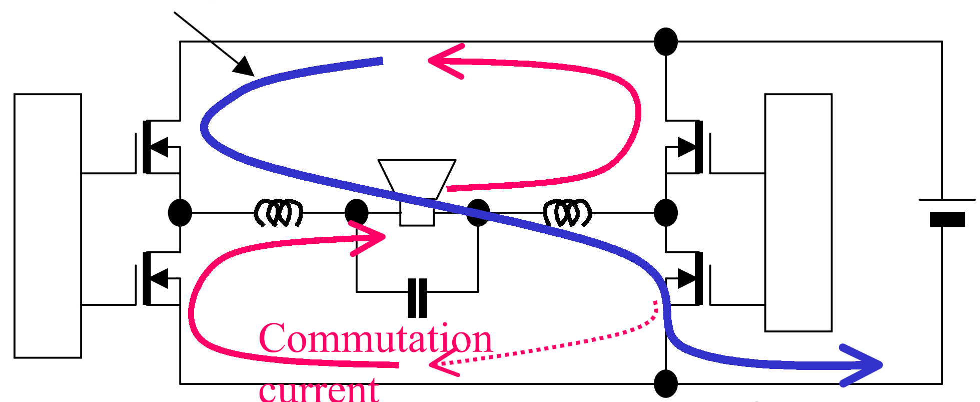
Half Bridge



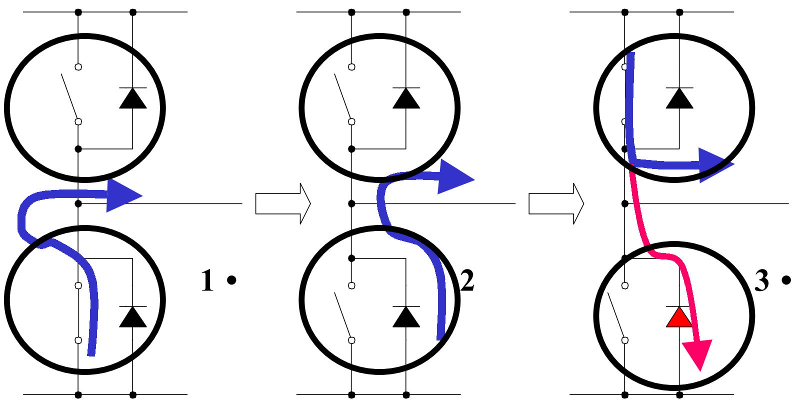
$$\Delta V_{BUS}\max = \frac{V_{BUS}}{8\cdot\pi\cdot f_{PWM}\cdot R_{LOAD}\cdot C_{BUS}}$$

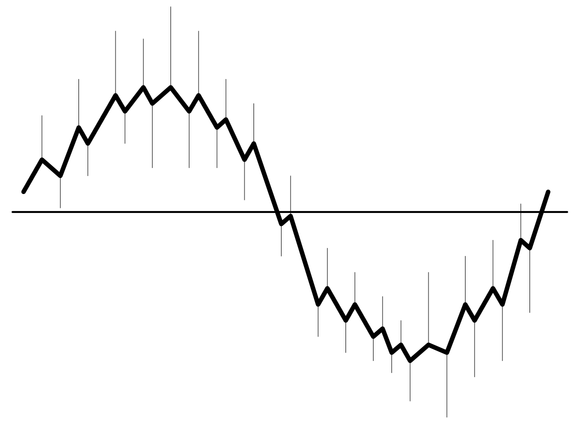
- -Significant at low frequency output
- -Significant at low load impedance
- -Significant at small bus capacitors
- -Largest at duty = 25%, and 75%

Full Bridge



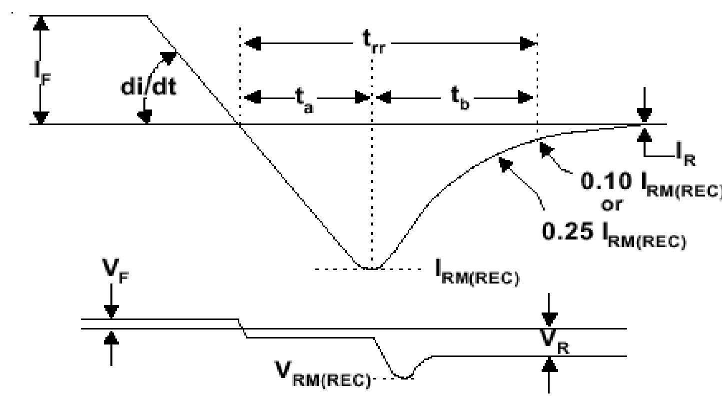
EMI consideration: Qrr in Body Diode





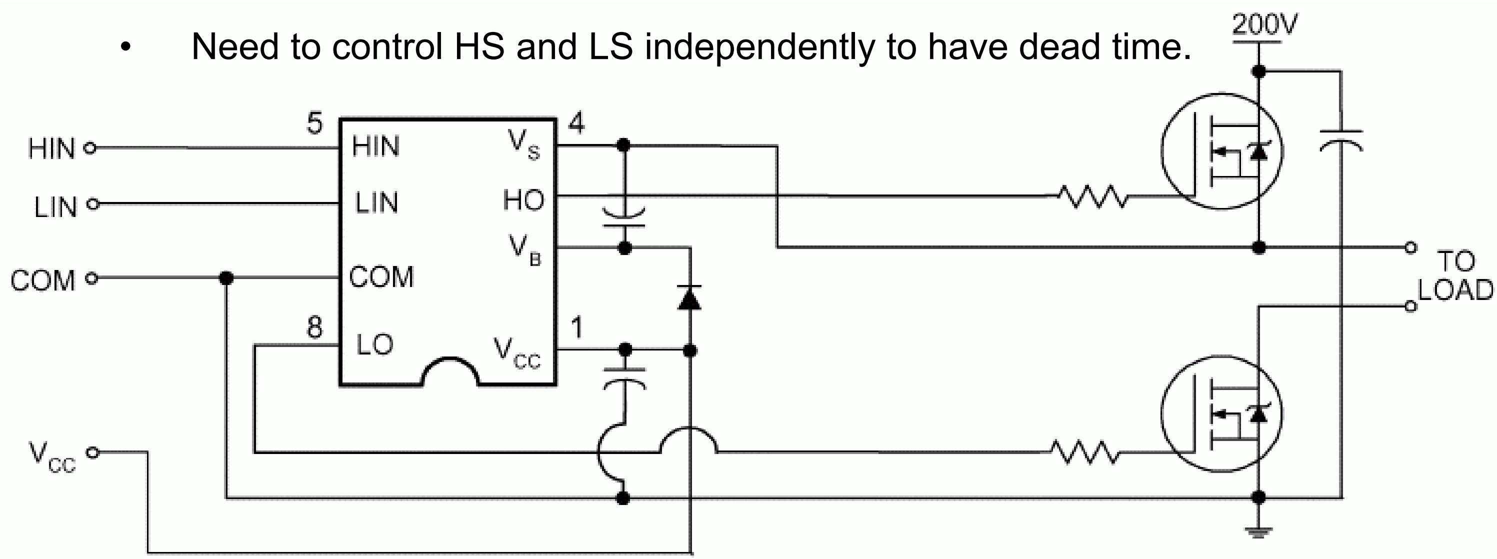
1. Low side drains inductor current
2. During dead time body diode of low side conducts and keep inductor current flow
3. At the moment high side is turned ON after dead time, the body diode is still conducting to wipe away minority carrier charge stored in the duration of forward conduction.

➔This current generates large high frequency current waveform and causes EMI noises.

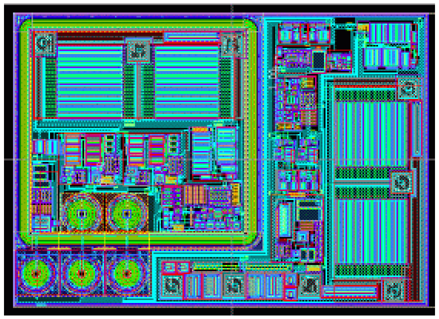


Gate Driver: Why is it Needed?

- Gate of MOSFET is a capacitor to be charged and discharged. Typical effective capacitance is 2nF.
- High side needs to have a gate voltage referenced to it's Source.
- Gate voltage must be 10-15V higher than the drain voltage.
- Need to control HS and LS independently to have dead time.

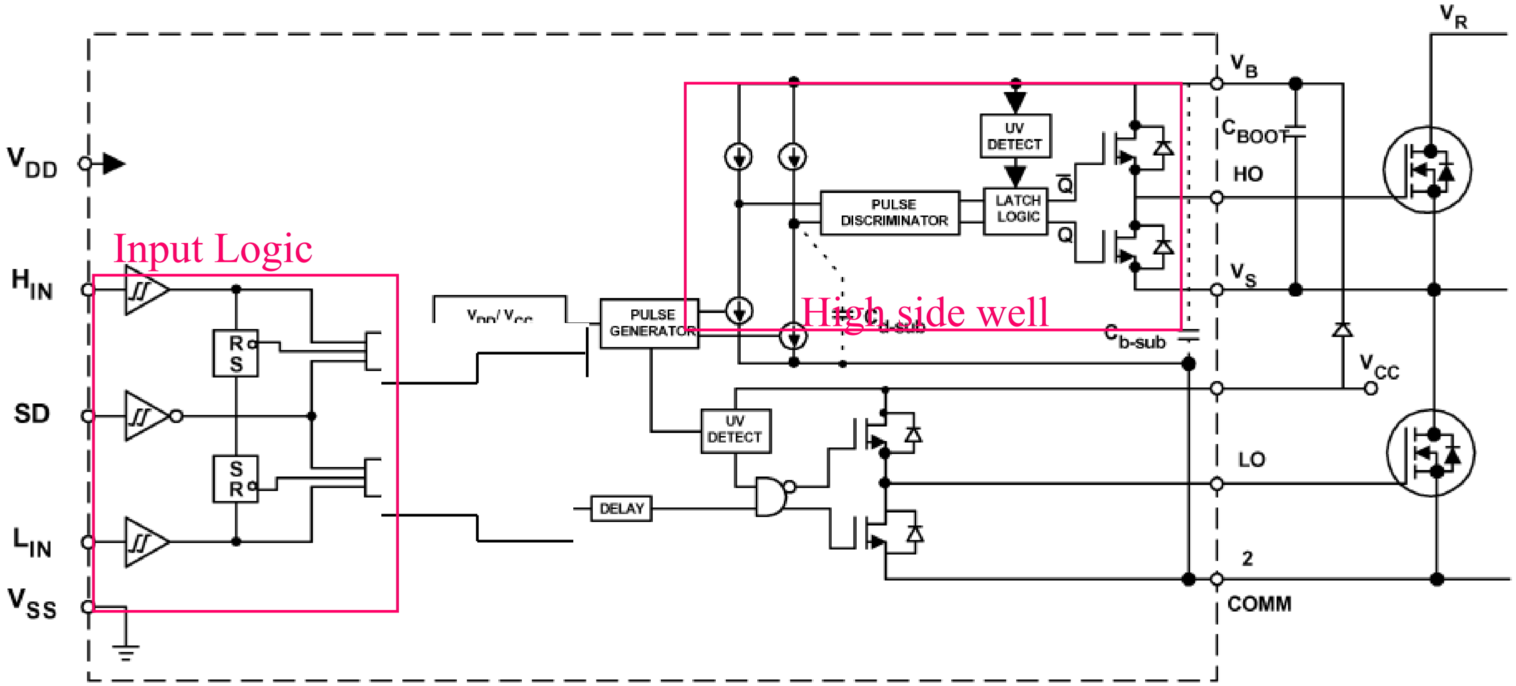


Functional Block Diagram Inside Gate Driver

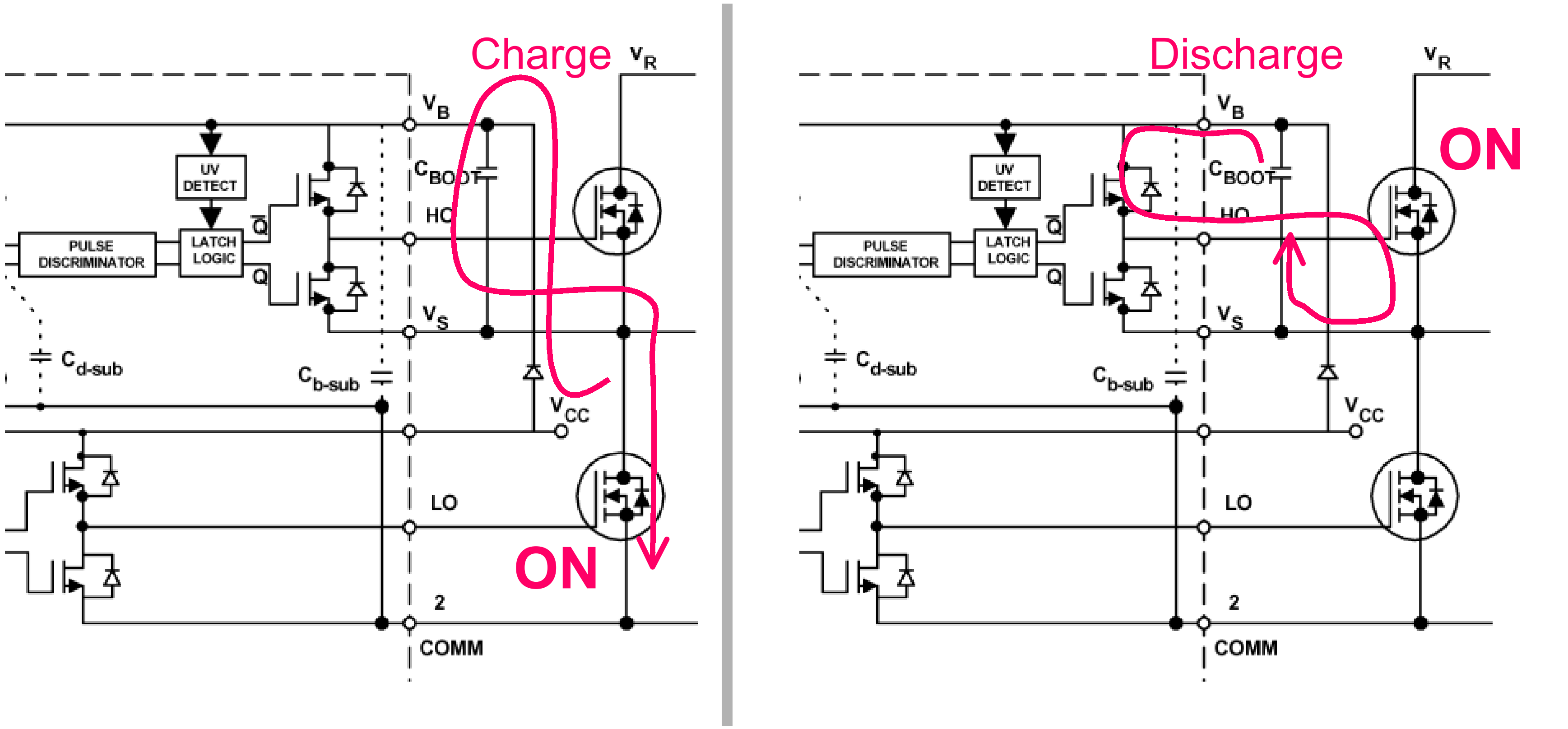


International Rectifier's family of MOS gate drivers integrate most of the functions required to drive one high side and one low side power MOSFET in a compact package.

With the addition of few components, they provide very fast switching speeds and low power dissipation.



Boot Strap High Side Power Supply



When Vs is pulled down to ground through the low side FET, the bootstrap capacitor (C_{BOOT}) charges through the bootstrap diode (Dbs) from the Vcc supply, thus providing a supply to Vbs.

Boot Strap High Side Power Supply (Cont'd)

- ## Boot Strap Capacitor Selection

$$C \geq \frac{2\left[2Q_g + \frac{I_{qbs(\max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f}\right]}{V_{cc} - V_f - V_{LS} - V_{Min}} \qquad \text{EQ(2)}$$

Where:

V_f = Forward voltage drop across the bootstrap diode

V_{LS} = Voltage drop acros FET (or load for a high side driver)

V_{Min} = Minimum voltage between V_B and V_S

To minimize the risk of overcharging and further reduce ripple on the Vbs voltage the Cbs value obtained from the above equation should be should be multiplied by a factor of 15 (rule of thumb).

- ## Boot Strap Diode Selection

The bootstrap diode (Dbs) needs to be able to block the full power rail voltage, which is seen when the high side device is switched on. It must be a fast recovery device to minimize the amount of charge fed back from the bootstrap capacitor into the Vcc supply.

VRRM = Power rail voltage, max trr = 100ns, IF > Qbs x f

For more details on boot strap refer to DT98-2

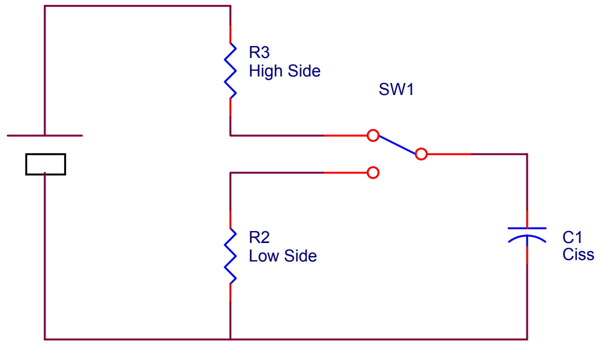
Power Dissipation in Gate Driver

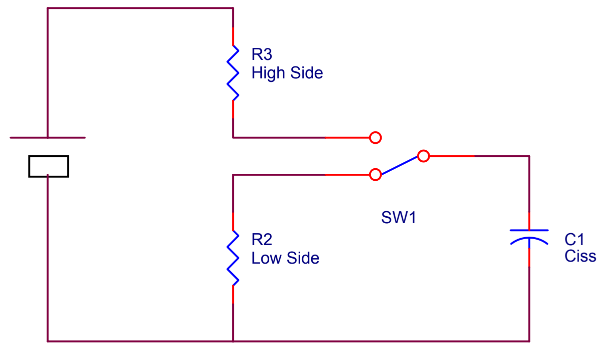
- Whenever a capacitor is charged or discharged through a resistor, half of energy that goes into the capacitance is dissipated in the resistor. Thus, the losses in the gate drive resistance, internal and external to the MGD, for one complete cycle is the following:

$$P_G = V \cdot f_{SW} \cdot Q_G$$

For two IRF540 HEXFET® MOSFETs operated at 400kHz with Vgs = 12V, we have:

PG = 2 • 12 • 37 • 10^{-9} • 400 • 10^{3} = 0.36W





For more details on gate driver ICs, refer to AN978

Power Dissipation in Gate Driver (Cont'd)

- The use of gate resistors reduces the amount of gate drive power that is dissipated inside the MGD by the ratio of the respective resistances.

- These losses are not temperature dependent.

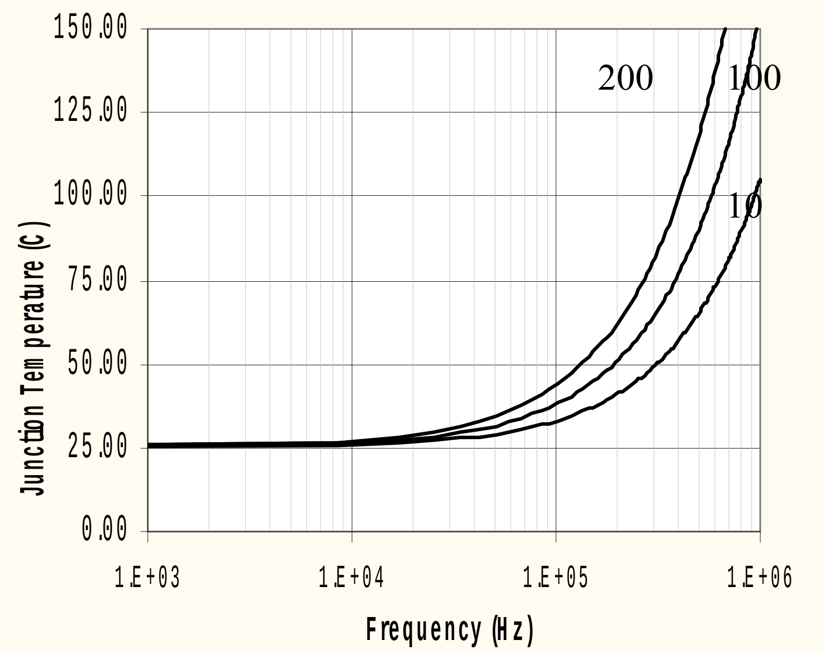
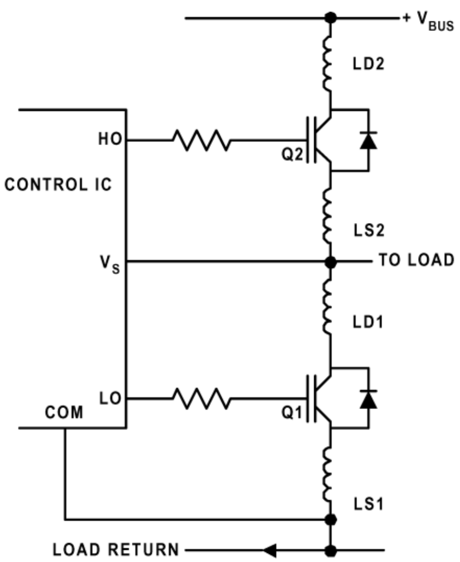


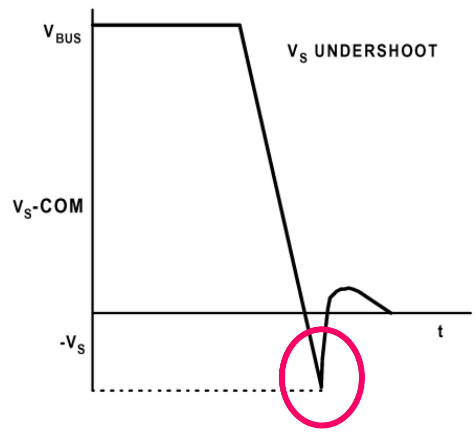
Figure 32: IR2010S Tj vs Frequency

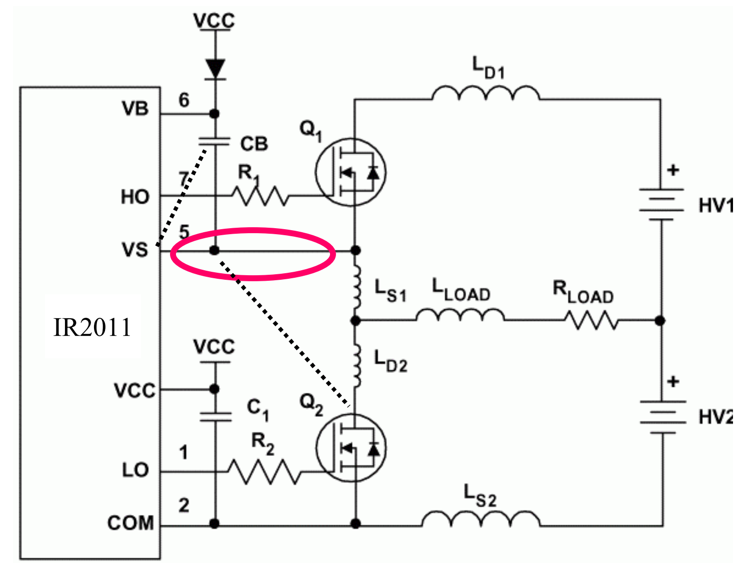
R_{GATE} = 10 Ohm, Vcc = 15V with IRFPE50

Layout Considerations

- Stray inductance LD1+LS1 contribute to undershoot of the Vs node beyond the ground







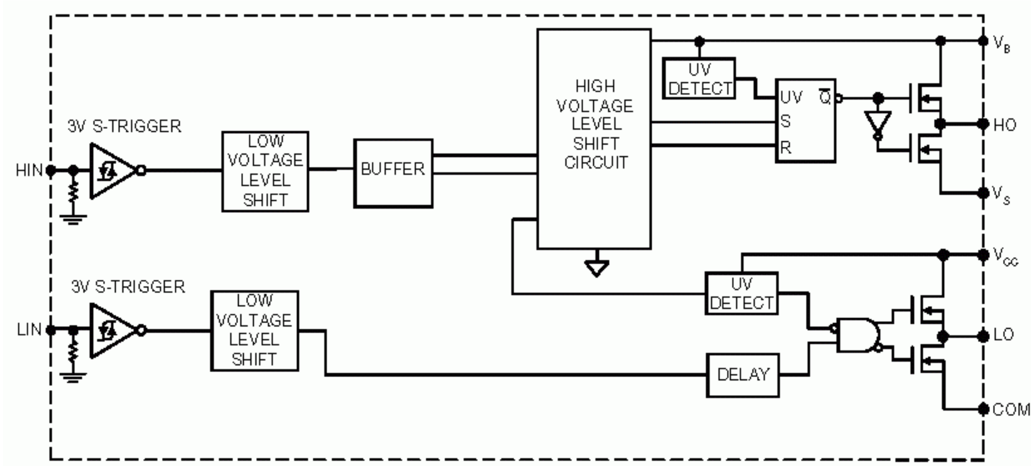
As with any CMOS device, driving any of parasitic diodes into forward conduction or reverse breakdown may cause parasitic SCR latch up.

Gate Driver for Class D Applications

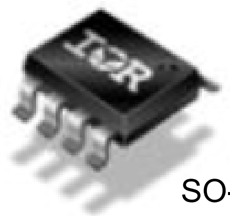
IR2011(S)

Key Specs

V_{OFFSET}	200V max.
I_O+/-	1.0A /1.0A typ.
V_{OUT}	10 - 20V
$t_{on/off}$	80 & 60 ns typ.
Delay Matching	20 ns max.



- Fully operational up to +200V
- Low power dissipation at high switching frequency
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Tolerant to negative transient voltage, dV/dt immune
- SO-8/DIP-8 Package

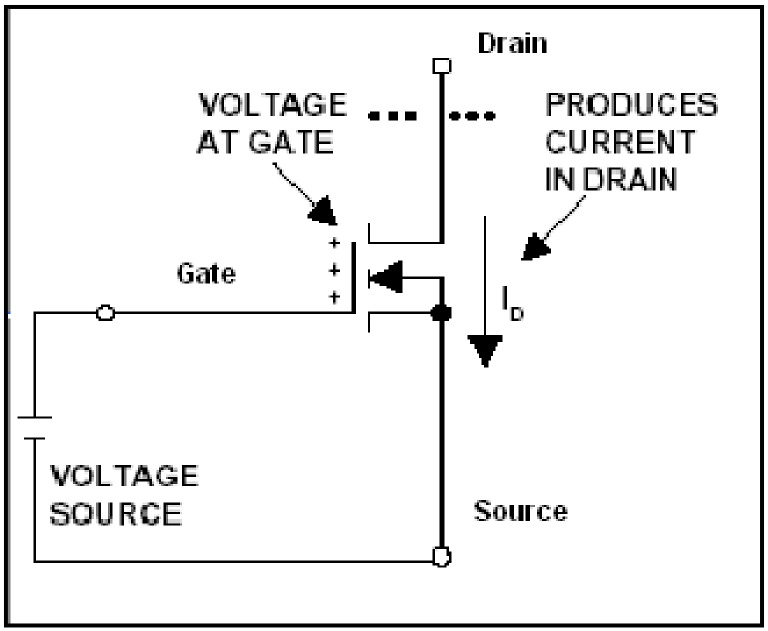


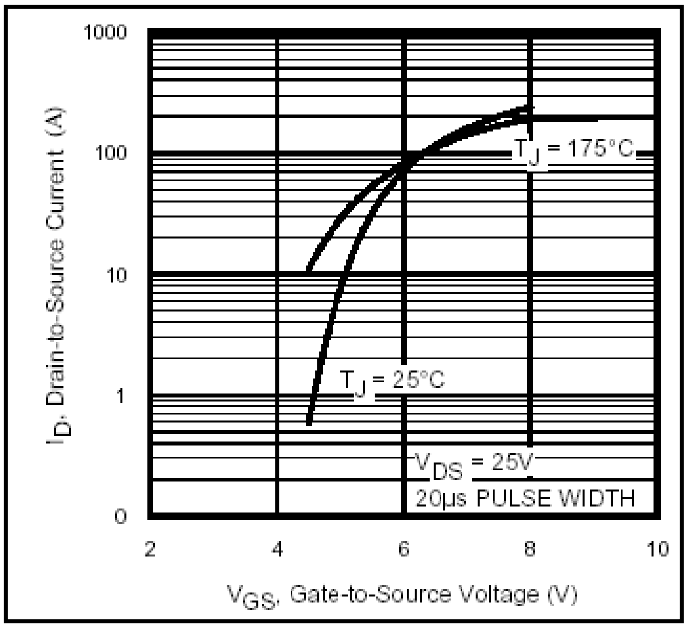
SO-8

How MOSFETs Work

- **A MOSFET is a voltage-controlled power switch.**

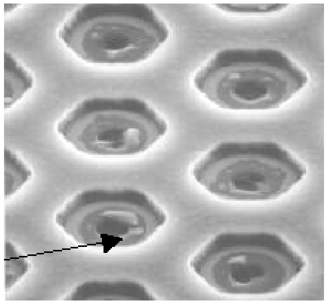
  A voltage must be applied between Gate and Source terminals to produce a flow of current in the Drain.



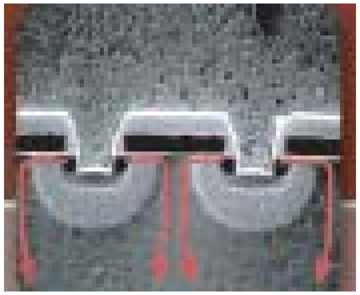


MOSFET Technologies (1)

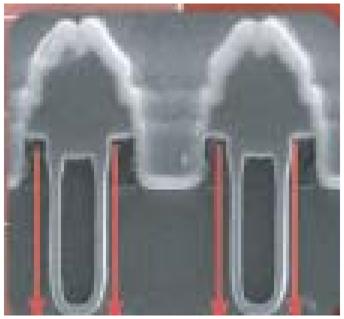
- **IR is striving to continuously improve the power MOSFET to enhance the performance, quality and reliability.**
- **Hexagonal Cell Technology**



- **Planar Stripe Technology**

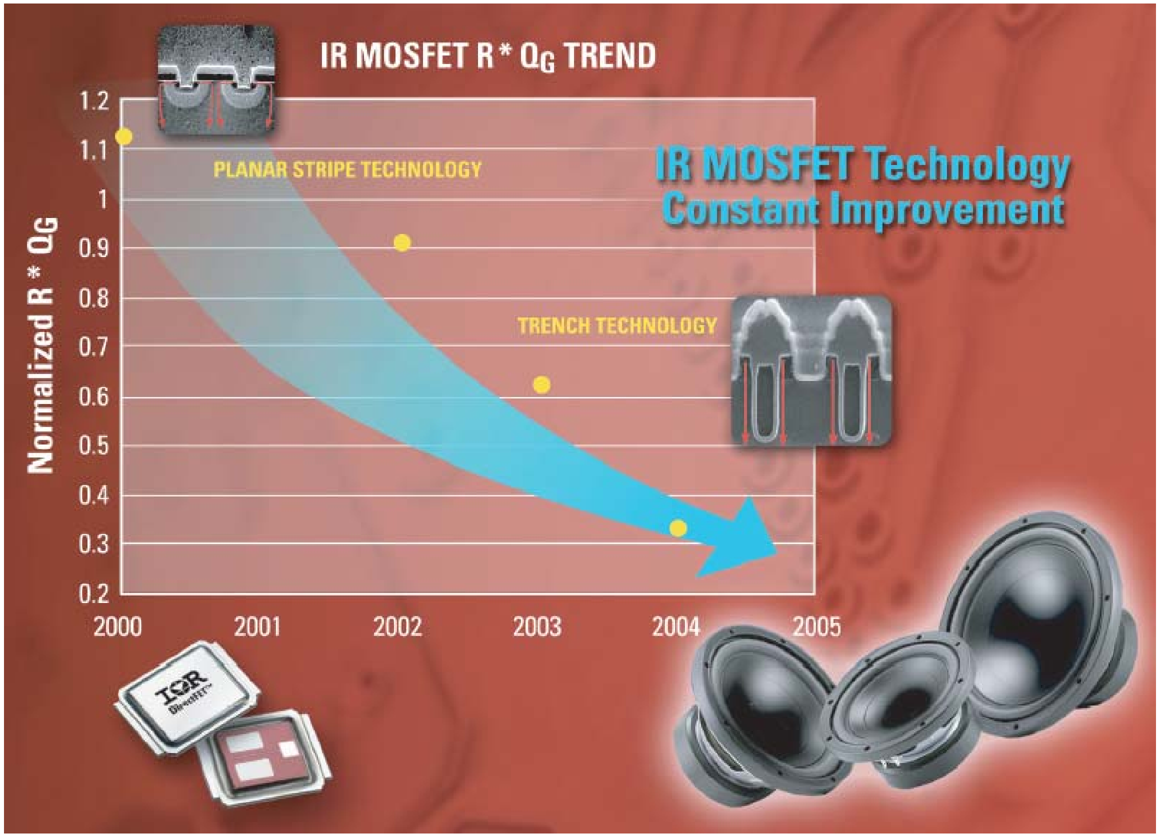


- **Trench Technology**



MOSFET Technologies (2)

- **Power MOSFET FOMs (R*Qg) have significantly improved between the released IR MOSFET technologies**



Key Parameters of MOSFETs (1)

- **Voltage Rating, BV_{DSS}**

This is the drain-source breakdown voltage (with VGS = 0). BV_{DSS} should be greater than or equal to the rated voltage of the device, at the specified leakage current, normally measured at Id=250uA.

This parameter is temperature-dependent and frequently $\Delta BV_{DSS}/\Delta Tj$ (V/°C) is specified on datasheets.

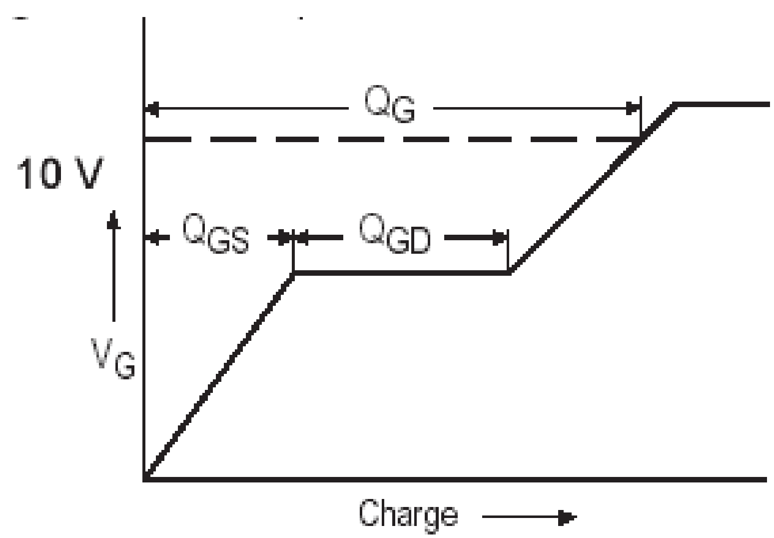
BV_{DSS} MOSFET voltages are available from tens to thousand volts.

Key Parameters of MOSFETs (2)

- **Gate Charge, Qg**

This parameter is directly related to the MOSFET speed and is temperature-independent. Lower Qg results in faster switching speeds and consequently lower switching losses.

The total gate charge has two main components: the gate-source charge, Qgs and, the gate-drain charge, Qgd (often called the Miller charge).



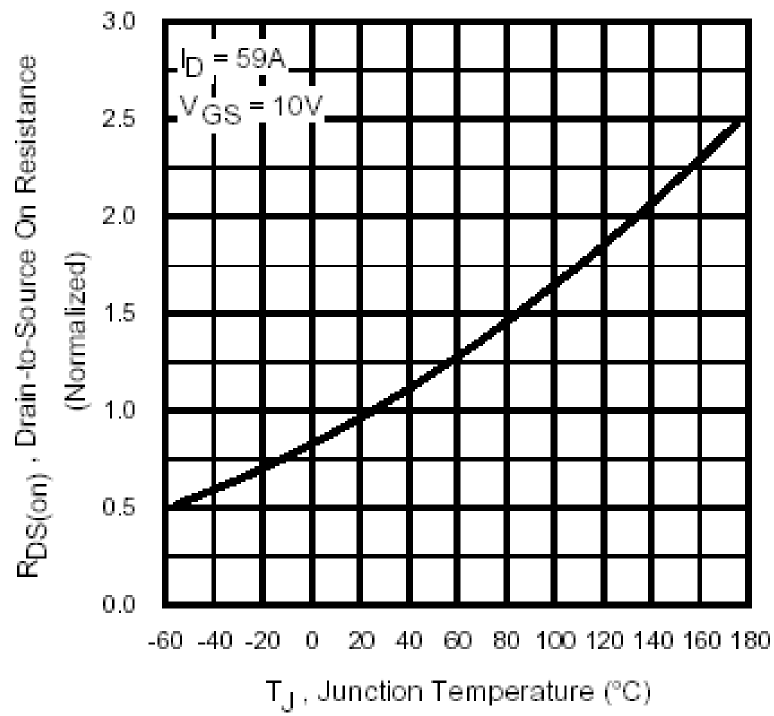
Basic Gate Charge Waveform

Key Parameters of MOSFETs (3)

- **Static Drain-to-Source On-Resistance, $R_{DS(ON)}$**

This is the drain-source resistance, typically specified on data sheet at 25°C with VGS = 10V.

$R_{DS(ON)}$ parameter is temperature-dependent, and is directly related to the MOSFET conduction losses. lower $R_{DS(ON)}$ results in lower conduction losses.



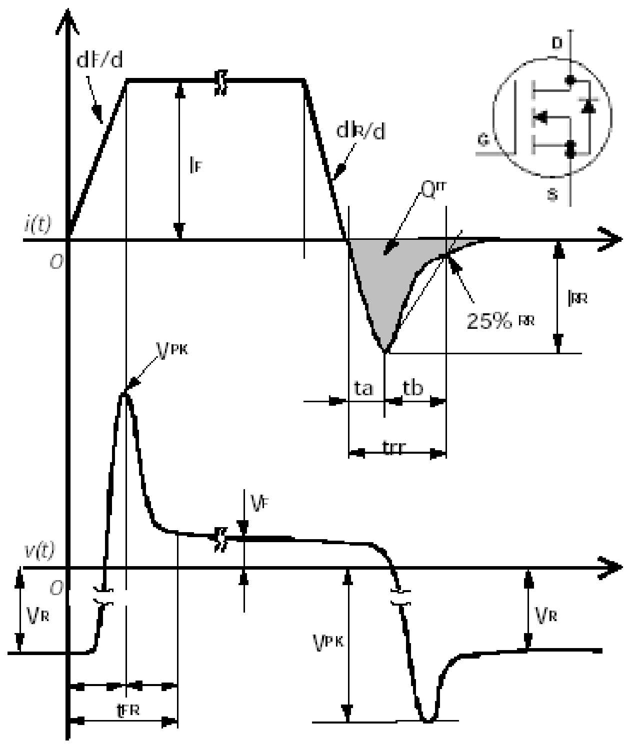
Normalized On-Resistance vs. Temperature

Key Parameters of MOSFETs (4)

- **Body Diode Reverse Recovery Characteristics, Q_{rr}, t_{rr}, I_{rr} and S factor.**

Power MOSFETs inherently have an integral reverse body-drain diode. This body diode exhibits reverse recovery characteristics. Reverse Recovery Charge Qrr, Reverse Recovery Time trr, Reverse Recovery Current Irr and Softness factor (S = tb/ta), are typically specified on data sheets at 25°C and di/dt = 100A/us.

Reverse recovery characteristics are temperature-dependent and lower trr, Irr and Qrr improves THD, EMI and Efficiency η.



Typical Voltage –Current Waveforms for a MOSFET Body Diode

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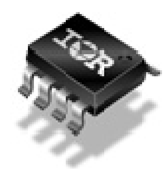
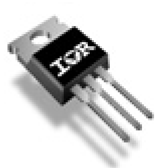
Key Parameters of MOSFETs (5)

- **Package**

  MOSFET devices are available in several packages as SO-8,TO-220, D-Pak, I-Pak, TO-262, DirectFET™, etc.

  The selection of a MOSFET package for a specific application depends on the package characteristics such as dimensions, power dissipation capability, current capability, internal inductance, internal resistance, electrical isolation and mounting process.

Choosing the MOSFET Voltage Rating for Class D applications (1)

- **MOSFET voltage rating for a Class D amplifier is determined by:**
  - **Desired P_{OUT} and load impedance (i.e. 250W on 4Ω)**
  - **Topology (Full Bridge or Half Bridge)**
  - **Modulation Factor M (80-90%)**

$$VB_{DSS\,min} = \sqrt{\frac{2 * P_{OUT} * R_{LOAD}}{M}} * 1.5$$

Typical additional factor due to stray resistance, power supply fluctuations and MOSFET Turn-Off peak voltage

Choosing the MOSFET Voltage Rating for Class D Applications (2)

- **Full-Bridge Topology Class D amplifier**

	BVDSS Minimum					Corresponding IR MosFET BVDSS				
	Load (Ohms)					Load (Ohms)				
Output Power (W)	1	2	4	6	8	1	2	4	6	8
100	25.0	35.3	49.9	61.1	70.6	30	40	55	75	75
150	30.6	43.2	61.1	74.9	86.5	40	55	75	75	100
200	35.3	49.9	70.6	86.5	99.8	40	55	75	100	100
500	55.8	78.9	111.6	136.7	157.8	75	100	150	150	200
1000	78.9	111.6	157.8	193.3	223.2	100	150	200	200	250

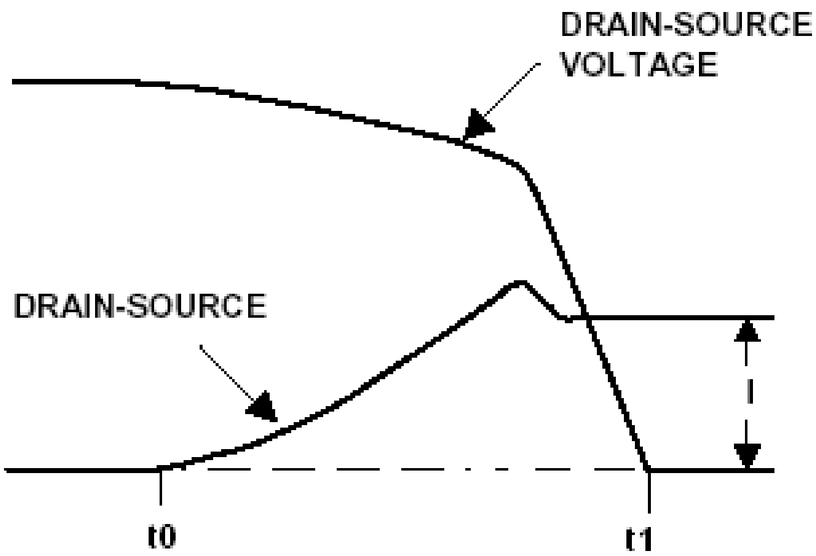
- **Half-Bridge Configuration Class D amplifier**

	VBDSS Minimum					Corresponding IR MosFET BVDSS				
	Load (Ohms)					Load (Ohms)				
Output Power (W)	1	2	4	6	8	1	2	4	6	8
100	49.9	70.6	99.8	122.3	141.2	55	75	100	150	150
150	61.1	86.5	122.3	149.7	172.9	75	100	150	150	200
200	70.6	99.8	141.2	172.9	199.7	75	100	150	200	200
500	111.6	157.8	223.2	273.4	315.7	150	200	250	300	400
1000	157.8	223.2	315.7	386.6	446.4	200	250	400	400	450

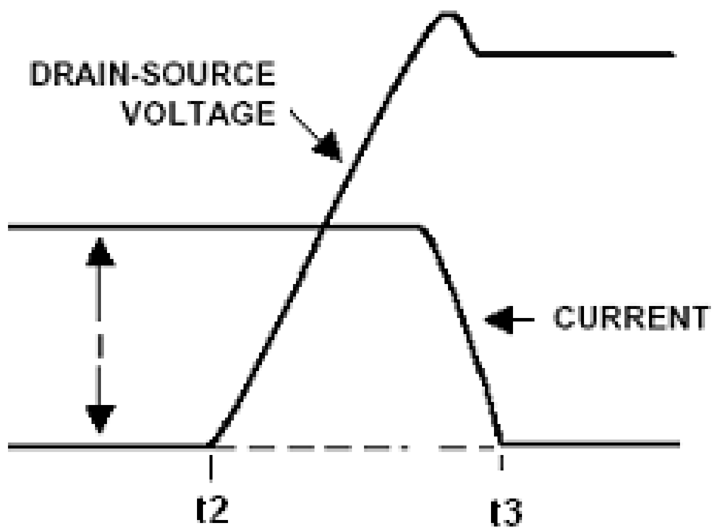
Note 1. Modulation Factor M = 85%

Calculation of Switching Loss (1)

- **Switching Losses are the result of turn-on and turn-off switching times**



MOSFET Turn-On



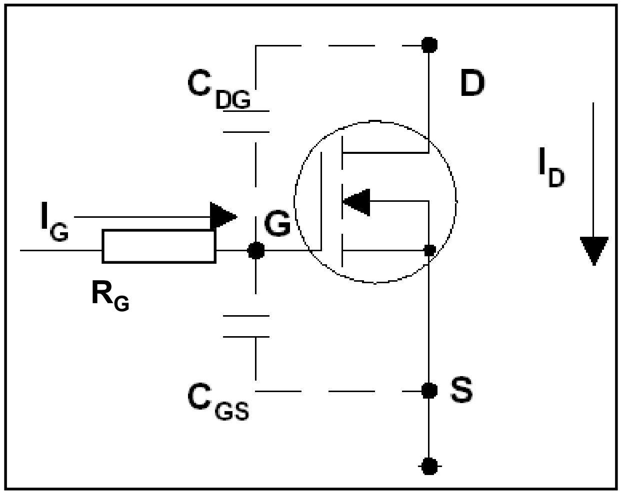
MOSFET Turn-Off

Calculation of Switching Loss (2)

- **Gate resistance Rg, and gate charge Qg, have a significant influence on turn-on and turn-off switching times**

$$\uparrow Rg \Rightarrow \downarrow Ig \Rightarrow \uparrow t_{SWITCHING} \Rightarrow \uparrow P_{SWITCHING}$$

$$\uparrow Qg \Rightarrow \uparrow t_{SWITCHING} \Rightarrow \uparrow P_{SWITCHING}$$



Estimation of Switching Losses (1)

- **Switching losses can be obtained by calculating the switching energy dissipated in the MOSFET**

$$E_{sw} = \int_0^t V_{DS}(t) * I_D(t)\, dt$$

Where t is the length of the switching pulse.

- **Switching losses can be obtained by multiplying switching energy with switching frequency.**

$$P_{SWITCHING} = E_{SW} * F_{SW}$$

Estimation of Conduction Loss (2)

- **Conduction losses can be calculated using $R_{DS(ON)}$ @ Tj max and $I_{D\ RMS}$ current of MOSFET**

$$P_{CONDUCTION} = (I_{D\ RMS})^2 * R_{DS(ON)}$$

$I_{D\ RMS}$ is determined using amplifier specifications:

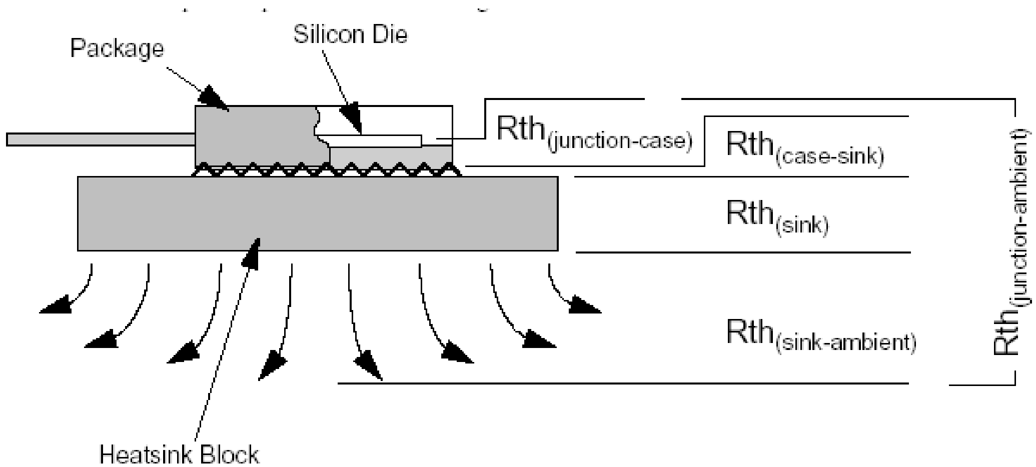
$$I_{D\ RMS} = \sqrt{\frac{P_{OUT}}{R_{LOAD}}}$$

$R_{DS(ON)}$ data can be obtained from the MOSFET data sheet.

Thermal Design

- **Maximum allowed power dissipation for a MOSFET mounted on a heat sink:**

$$P_{max} = \Delta Tj / R_{thja\ max}$$



$$P_{max} = (T_{amb} - Tj_{max}) / (R_{thjc\ max} + R_{thcs\ max} + R_{ths\ max} + R_{thsa\ max})$$

Where: T_{amb} = Ambient Temperature

Tj_{max} = Max. Junction Temperature

$R_{thjc\ max}$ = Max. Thermal Resistance Junction to Case

$R_{thcs\ max}$ = Max. Thermal Resistance Case to Heatsink

$R_{ths\ max}$ = Max. Thermal Resistance of Heatsink

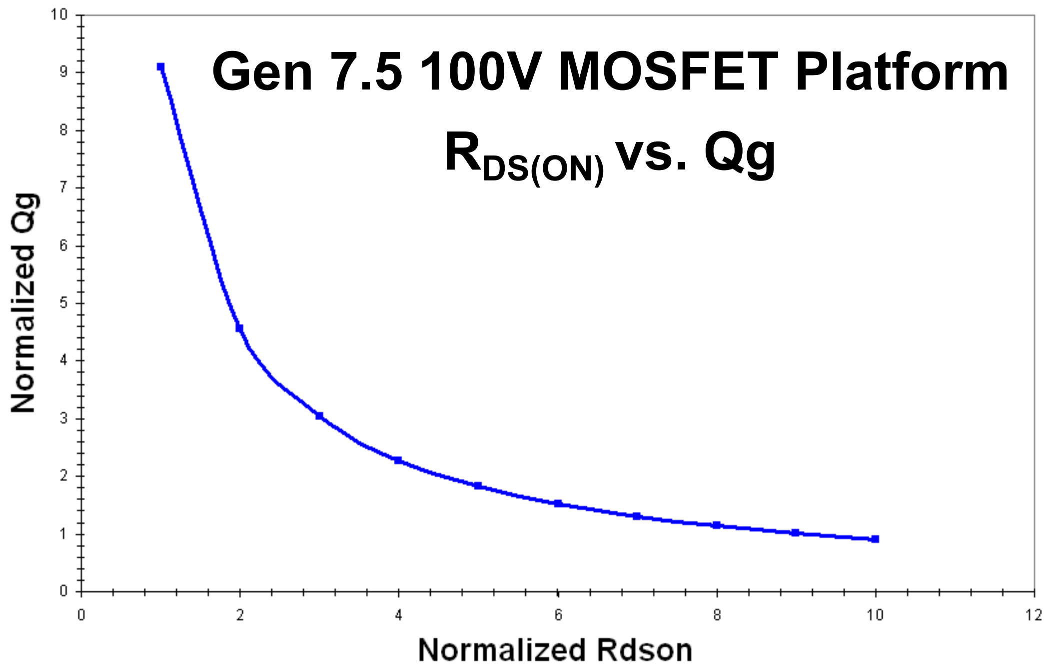
$R_{thsa\ max}$ = Max. Thermal Resistance Heatsink to Ambient

$R_{DS(ON)}$ vs Qg

- **There is tradeoff between Static Drain-to-Source On-Resistance, $R_{DS(ON)}$ and Gate charge, Qg**

Higher $R_{DS(ON)}$ ⇒ Lower Qg ⇒ Higher $P_{CONDUCTION}$ & Lower $P_{SWITCHING}$

Lower $R_{DS(ON)}$ ⇒ Higher Qg ⇒ Higher $P_{SWITCHING}$ & Lower $P_{CONDUCTION}$

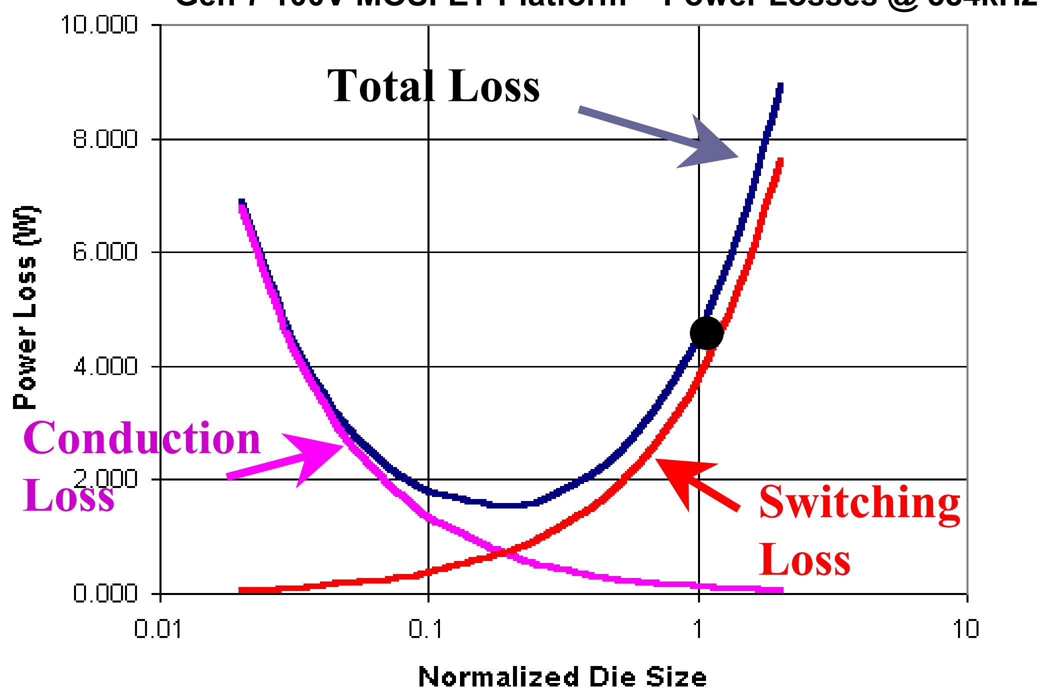


Die Size vs Power Loss (1)

- **Die size has a significant influence on MOSFET power losses**

Smaller Die ⇒ Higher $P_{CONDUCTION}$ & Lower $P_{SWITCHING}$

Bigger Die ⇒ Higher $P_{SWITCHING}$ & Lower $P_{CONDUCTION}$

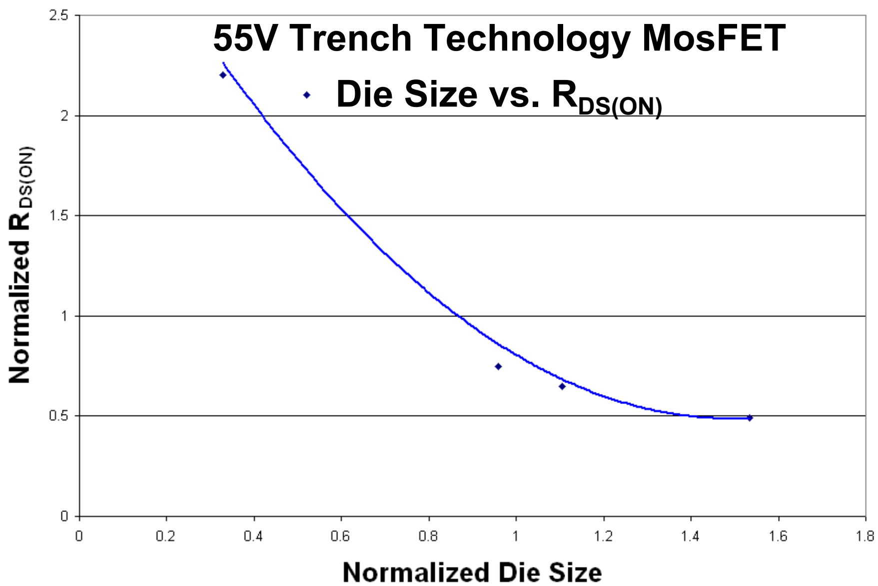


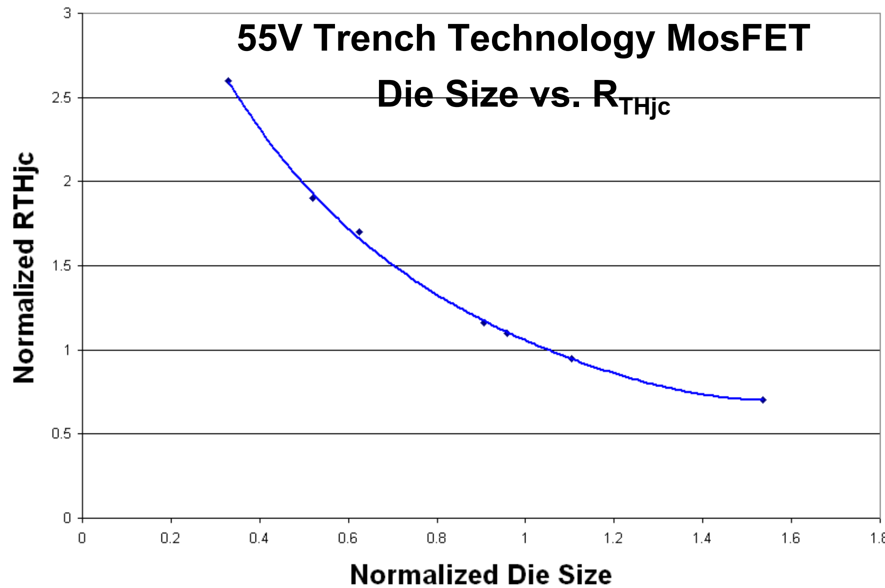
Die Size vs Power Loss (2)

- **Die size is directly related with $R_{DS(ON)}$ and R_{THjc} of the MOSFET**

  Smaller Die ⇒ Higher $R_{DS(ON)}$ and Higher R_{THjc}

  Bigger Die ⇒ Lower $R_{DS(ON)}$ and Lower R_{THjc}





Choosing the Right MOSFET for Class D Applications (1)

- **The criteria to select the right MOSFET for a Class D amplifier application are:**
  - VB_{DSS} should be selected according to amplifier operating voltage, and it should be large enough to avoid avalanche condition during operation
  - Efficiency η is related to static drain-to-source on-resistance, $R_{DS(ON)}$. smaller $R_{DS(ON)}$ improves efficiency η. $R_{DS(ON)}$ is recommended to be smaller than 200mΩ for mid and high-end power, full-bandwidth amplifiers
  - Low gate charge, Qg, improves THD and efficiency η. Qg is recommended to be smaller than 20nC for mid and high-end power, full-bandwidth amplifiers

Choosing the Right MOSFET for Class D Application (2)

- Amplifier performance such as THD, EMI and efficiency η are also related to MOSFET reverse recovery characteristics. Lower trr, Irr and Qrr improves THD, EMI and efficiency η
- Rthjc should be small enough to dissipate MOSFET power losses and keep $T_j <$ limit
- Better reliability and lower cost are achieved with higher MOSFET Tj max
- Finally, selection of device package determines the dimensions, electrical isolation and mounting process. These factors should be considered in package selection. Because cost, size and amplifier performance depend on it.

Development of Class D Dedicated Devices

- **Performance of the Class D amplifying stage strongly depends on the characteristics of MOSFETs and ICs.**

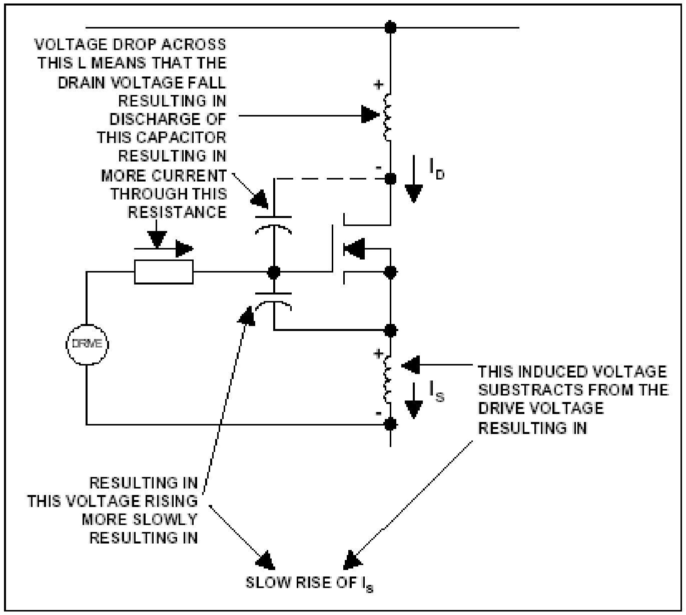
- **Designers of driver IC and MOSFET silicon need to keep the special requirements of the Class D application in mind.**

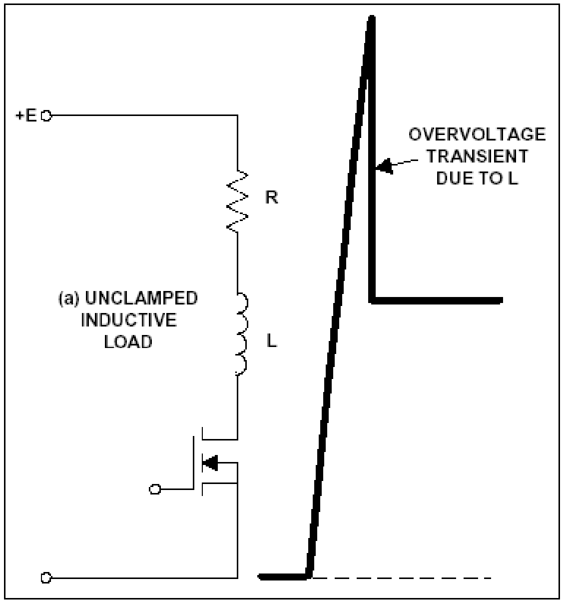
Influences of Stray Inductance

- **PCB layout and the MOSFET internal package inductances contribute to the stray inductance (L_S) in the circuit.**

- **Stray inductances affect the MOSFET performance and EMI of the system.**

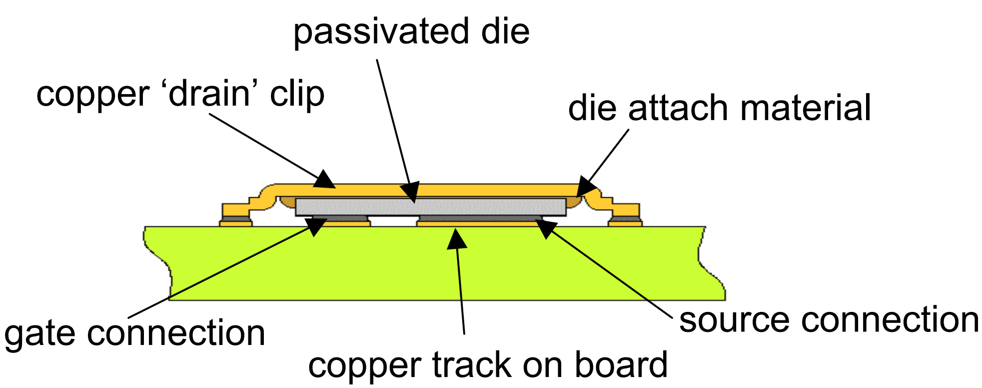
Influences of Stray Inductance

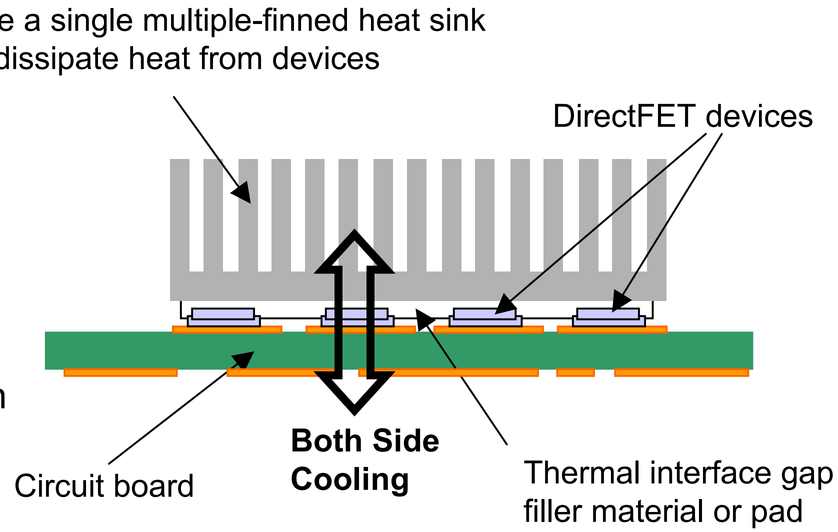


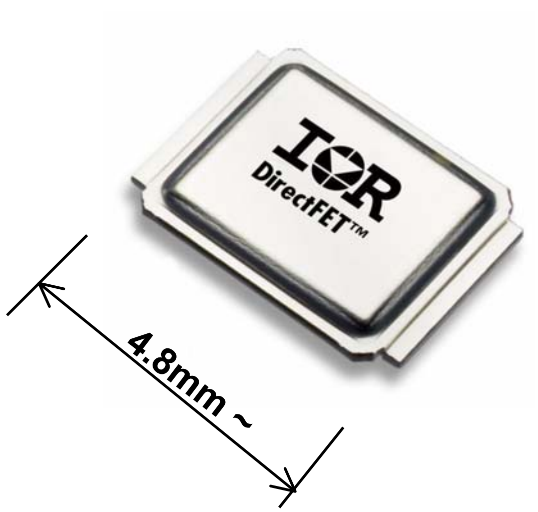


- Drain and source stray inductances reduces the gate voltage during turn-on resulting in longer switching time.
- Also during turn-off, drain and source stray inductances generate a large voltage drop due to dI_D/dt, producing drain to source over-voltage transients.

DirectFET™ Packaging



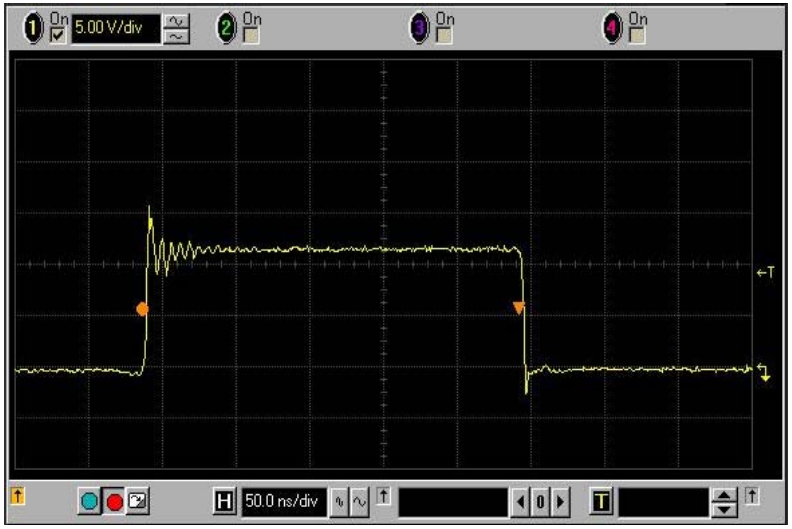




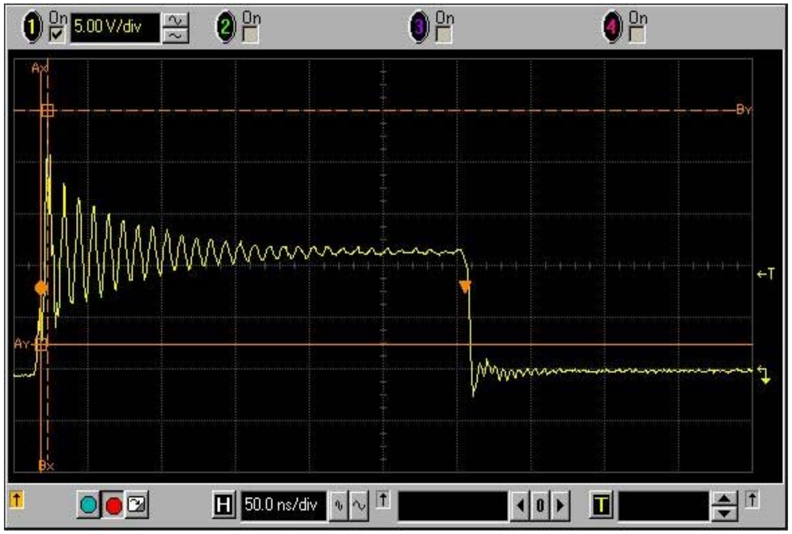
- Remove wirebonds from package and replace with large area solder contacts
- Reduced package inductance and resistance
- Copper can enables dual sided cooling

DirectFET™ Packaging

DirectFET waveform



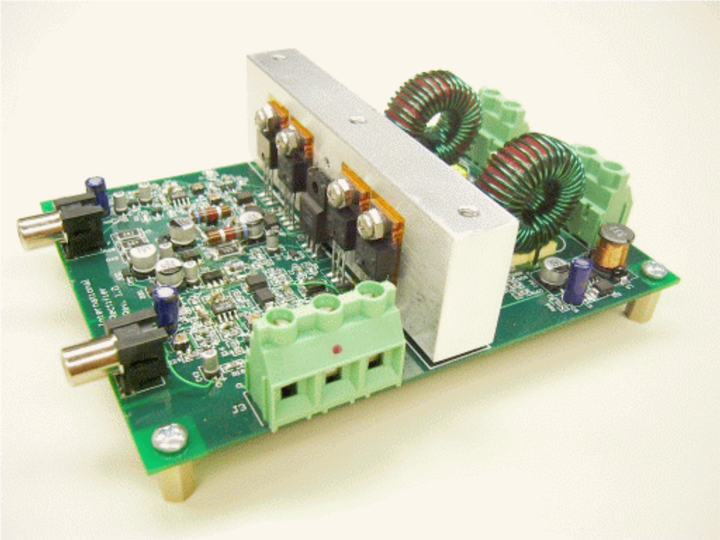
SO-8 waveform



- 30A VRM output current
- 500 kHz per phase
- Silicon of the near identical active area, voltage and generation used in both packages
- Inductance related ringing greater in case of SO-8

Class D Amp Reference Design

- **Specs**



Topology: Half Bridge

IR Devices: IR2011S, IRFB23N15D

Switching frequency: 400kHz (Adjustable)

Rated Output Power: 200W+200W / 4 ohm

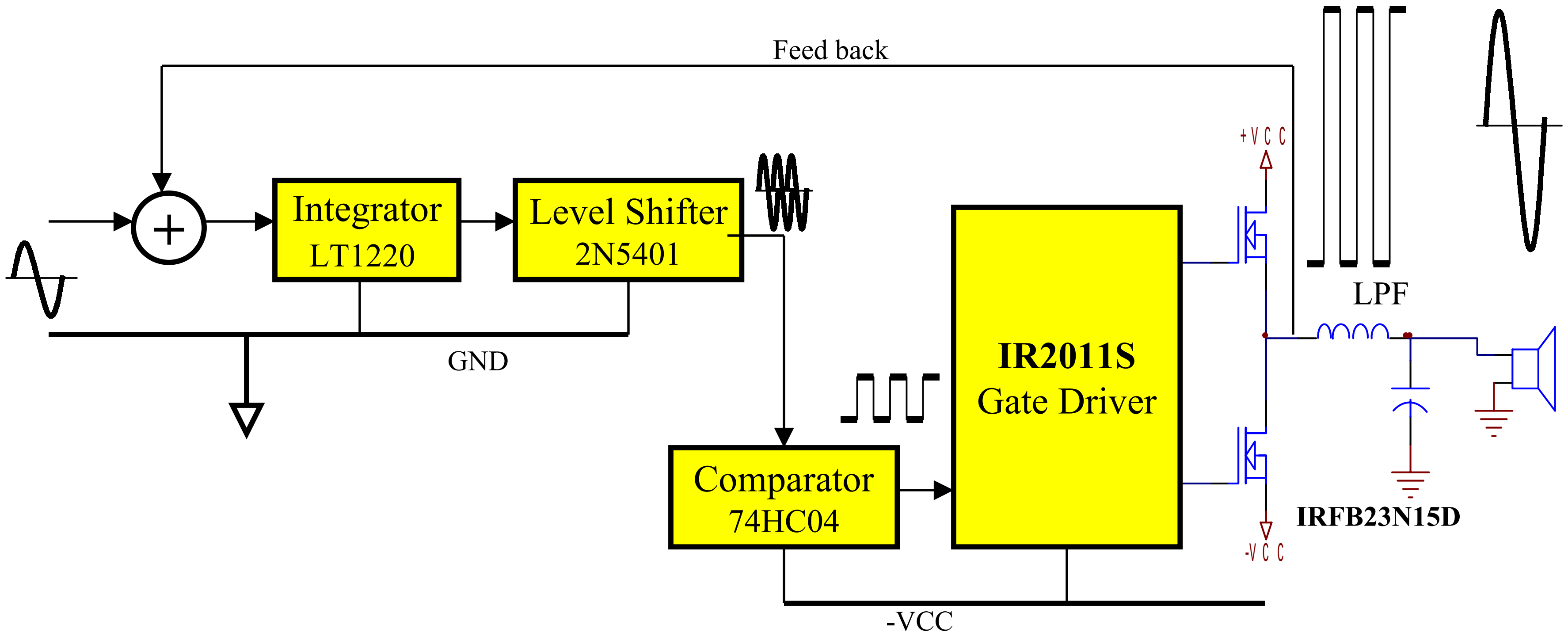
THD: 0.03% @1kHz, Half Power

Frequency Response: 5Hz to 40kHz (-3dB)

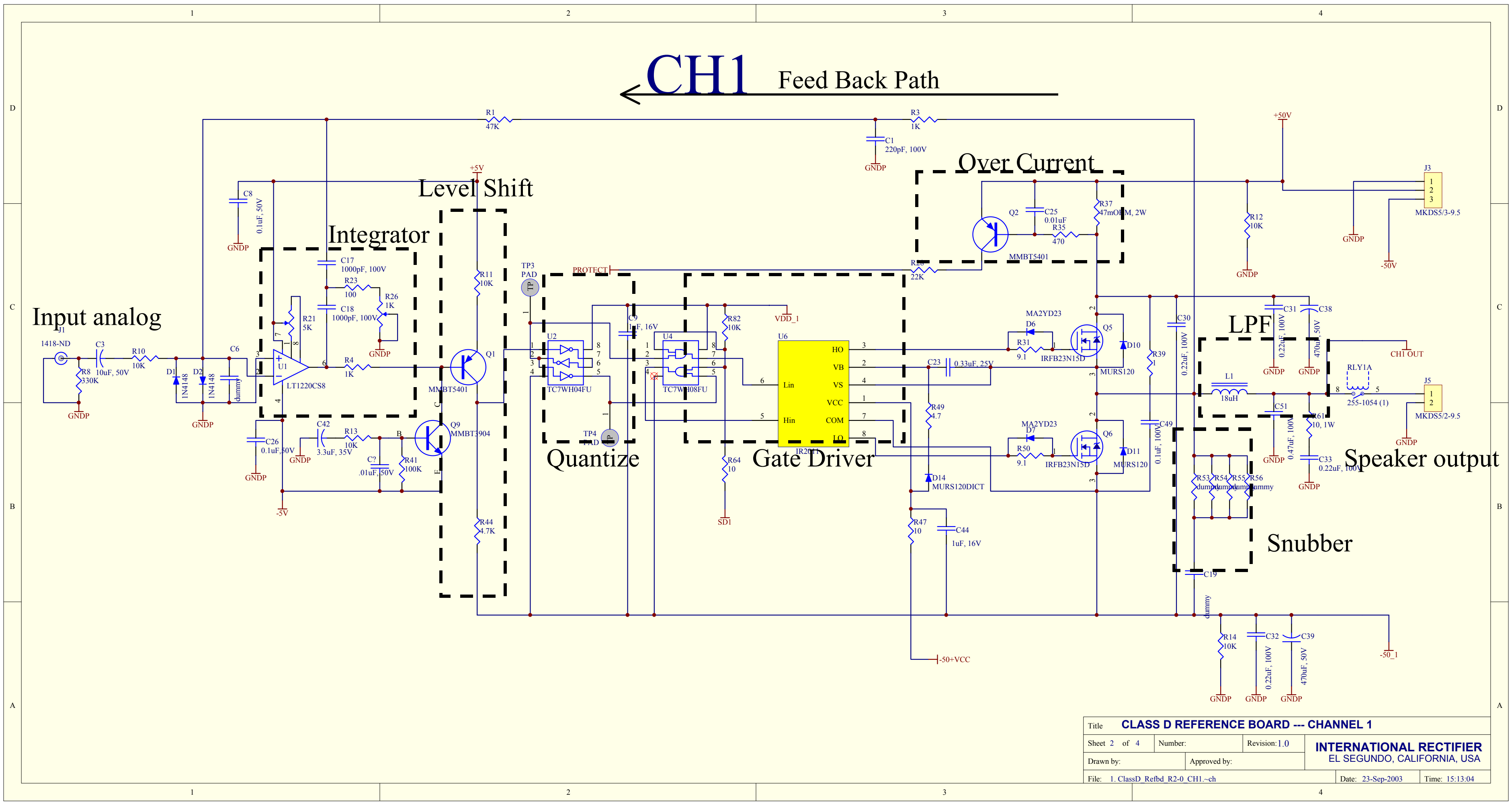
Power Supply: ~ ±50V

Size: 4.0” x 5.5”

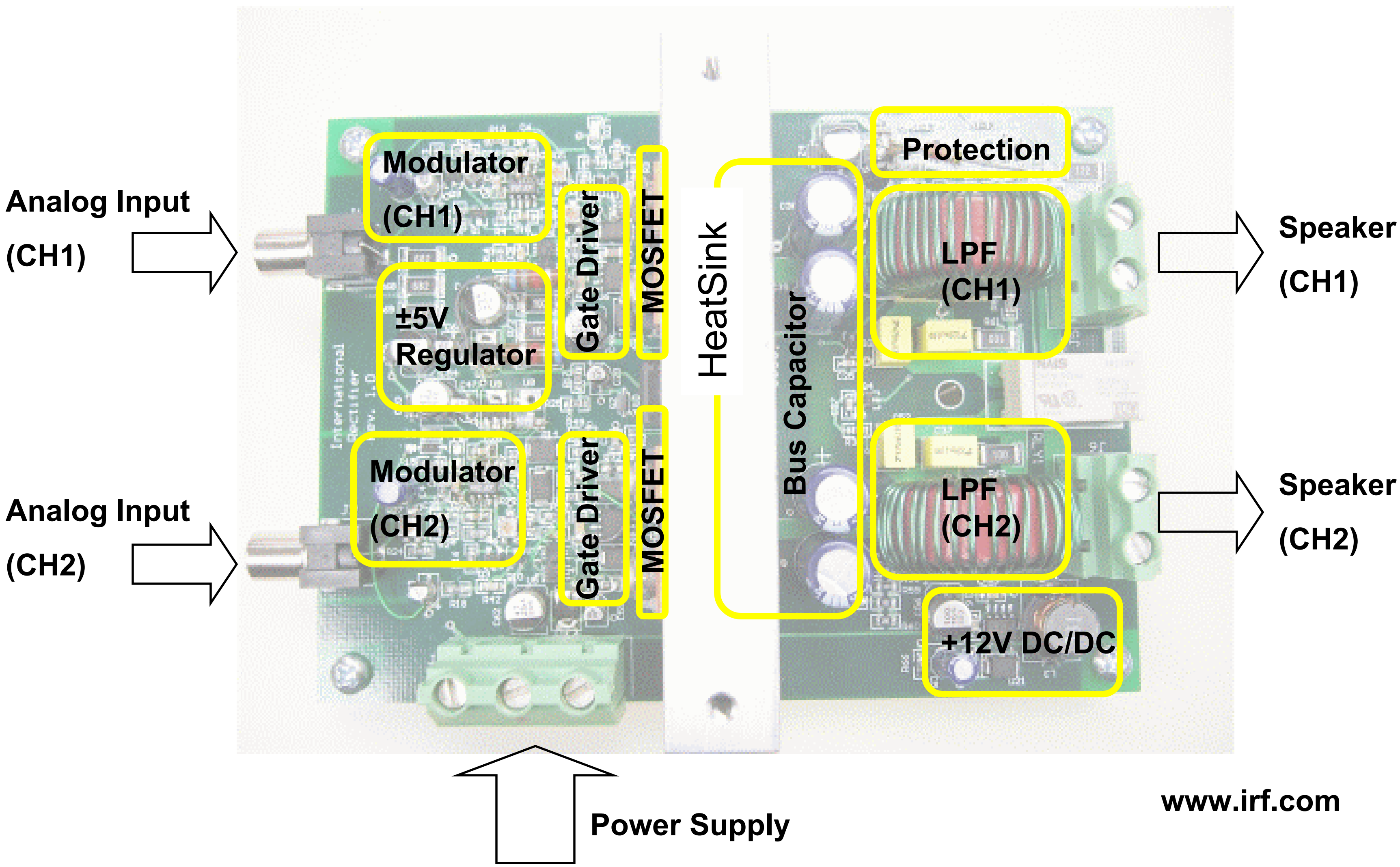
Class D Amp Reference Board: Block Diagram



Circuit Diagram

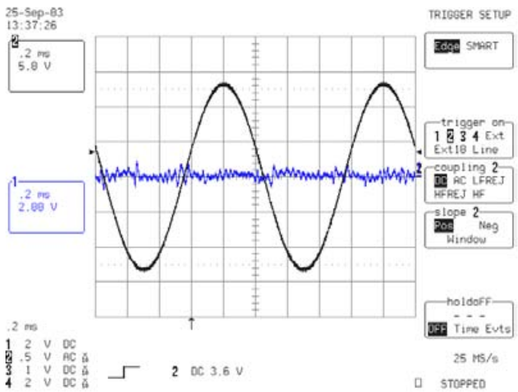


Class D Amp Reference Board: Layout

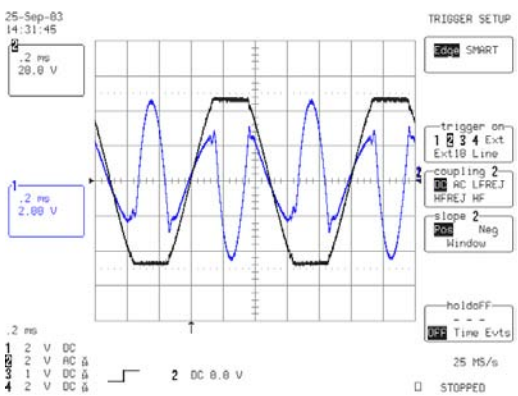


Performance

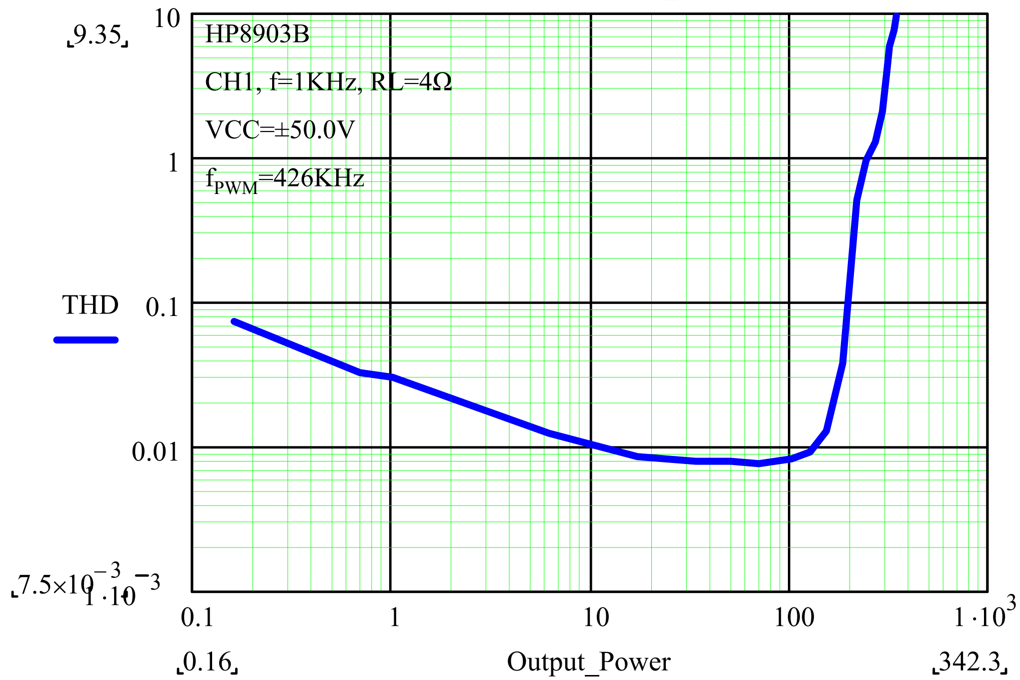
50W / 4Ω, 1KHz, THD+N=0.0078%



342W / 4Ω, 1KHz, THD+N=10%



THD+N v.s. Output Power



- **Peak Output Power (f=1KHz)**
  - **120W / 8Ω / ch, THD=1%**
  - **180W / 8Ω / ch, THD=10%**
  - **245W / 4Ω / ch, THD=1%**
  - **344W / 4Ω / ch, THD=10%**

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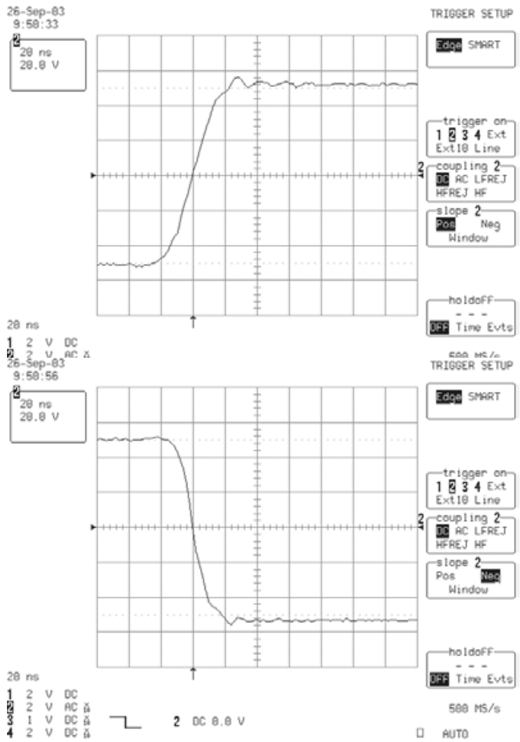
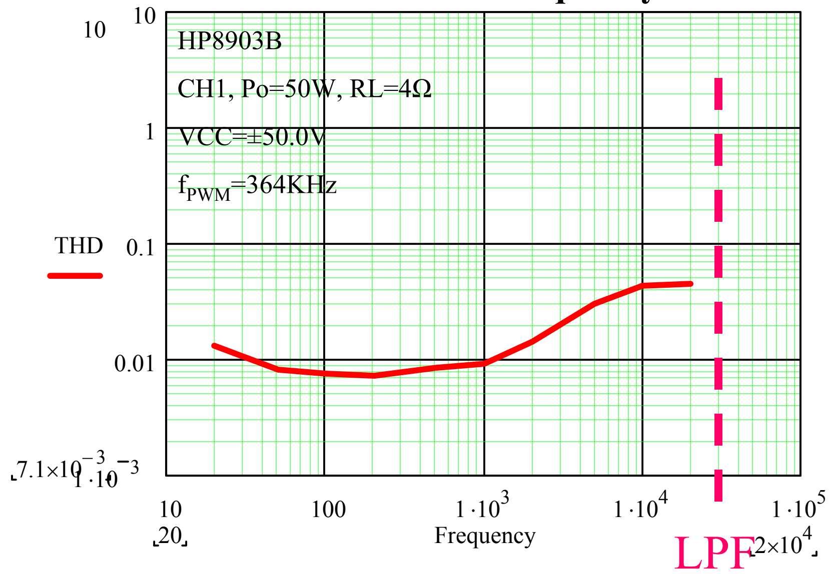
Performance (Cont'd)

Switching waveform



THD+N v.s. Frequency



Residual Noise: 62.5µVrms, A-Weighted, 30KHz-LPF

Conclusion

- Highly efficient Class D amplifiers now provide similar performance to conventional Class AB amplifiers -

  If key components are carefully selected and the layout takes into account the subtle, yet significant impact due to parasitic components.

Constant innovation in semiconductor technologies helps the growing Class D amplifiers usage due to improvements in higher efficiency, increased power density and better audio performance.