# Gate Driver with 10 / 15ns In-Transition Variable Drive Current and 60% Reduced Current Dip

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***Abstract*—In various fields, there is a growing need for electric motor drives and inductive power converters. To achieve better switching behavior and lower EME in inductive switching applications, very precise gate control of the power MOSFETs by the gate driver is required. The driver presented in this paper can operate at voltages up to 60V, and it is able to change the gate current in 10 / 15ns (rise / fall delay) within a range of 20mA to 500mA. Achieved by a class B buffer in the output stage, this enables multiple current changes in a 100ns switching transition. A dip in the output current, caused by parasitic capacitances, is reduced from 80% of the full scale current to 20% by a cascode configuration in the driver output stage. The gate voltage is clamped to 11.5V, with a precise clamping circuit to reduce $R_{DS,on}$ with the full gate current, but without stressing the gate oxide with any over voltage. By fully integrating this concept in 130nm HV-BiCMOS, a reduction in external components for limiting overshoot, stress and EME can be achieved.**

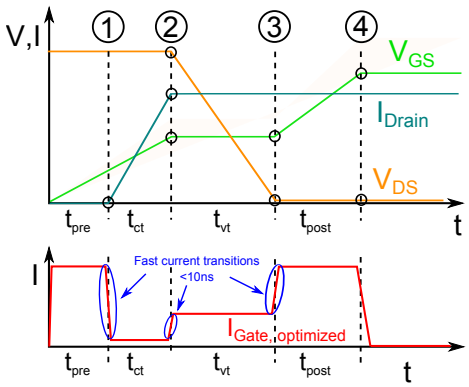


Figure 1: Idealized turn-on switching transition for a bridge setup with inductive load

## I. Introduction

Today, only few solutions with fast and precise gate current control for MOSFETs exist. Solutions for IGBTs are more common because the transitions usually take longer (between 1µs and 5µs). In high speed MOSFET applications, the driver has to also be immune to influences of the fast switching transition. A gate driver that enhances the electromagnetic compatibility (EMC), and reduces stress caused by ringing / overshoot can not just slow down the whole switching transition as this would cause a huge increase of the switching losses. By changing the drive current while in the switching transition, a trade-off between overshoot / ringing and switching losses can be achieved.

In order to influence the switching transition of a MOSFET, the voltage at the gate has to be controlled precisely. This can be achieved by a gate driver with very fast changing variable current output. Such a driver enables an independent control of the voltage and / or current transition, Fig. 1. The transition of current / voltage in inductive switching applications consists of five phases indicated by $t_{pre}$, $t_{ct}$, $t_{vt}$, $t_{post}$ in Fig. 1 [1]. In the first phase, the gate is charged until the threshold voltage $V_{th}$ is reached at (1). Now, the transition of the current from the body-diode of one MOSFET to the active MOSFET switch begins. Once the final drain current is reached at (2), the voltage begins to drop until it reaches almost zero at (3). At this point, the active switching transition is finished and the gate of the transistor is charged to its final voltage at (4) to reduce $R_{DS,on}$. The EMC relevant parts of the switching transition are the current transition ($t_{ct}$) and the voltage transition ($t_{vt}$). In these parts of the transition, a lower current would be preferable; while in $t_{pre}$ and $t_{post}$ a high gate current is preferable to reduce the phase delay and reach a low $R_{DS,on}$ as soon as possible. With a fast enough gate driver, these two phases of the transition can be addressed with different current settings and it is possible to reach an optimal trade-off point [2].

State of the art in gate driver designs are hard switching drivers that charge the gate of a MOSFET by connecting it to a voltage rail $V_{drv}$ (Fig. 2a). The charging / discharging currents are limited by a resistor $R_{Gate}$ in the current path [3]. In such a configuration, the gate currents are heavily influenced by the capacitors of the power MOSFET. This results in a current profile with an high current peak in the beginning, and then a constantly decreasing current [4]. The high initial current reduces phase delay, but can cause large overshoot and stress

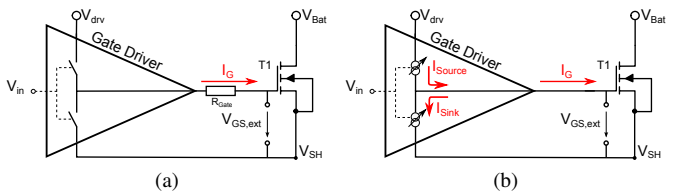


Figure 2: (a) Hard switching gate driver; (b) Current source gate driver

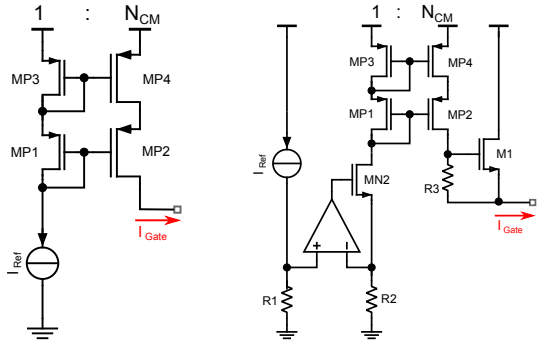


Figure 3: Current source output stage concepts for a gate driver, (a) Gate driver with current mirror output stage; (b) Low side reference stage with an opamp current regulator

on the power device because of the fast current transition. On the other hand, if the gate resistor is too large, the switching losses increase.

Another way to influence the gate current is to use a gate driver with more than one output transistor [5]. This way, the gate current can be controlled digitally by enabling more or less output transistors. However, this concept is very complex as every transistor requires an enable signal that has to be level-shifted to the high side of the circuit.

A third approach is to configure the driver output stage as a current source, Fig. 2b. This topology provides a set current to the power MOSFET's gate until it is fully charged. No gate resistor is required, as the current can be controlled by an internal reference current.

A basic concept to build such a driver is to use a current mirror, Fig. 3a. By changing the reference current, a variable gate current can be achieved. A cascode current mirror is usually not acceptable, due to area consumption and very slow reaction times to current changes. Alternatively, a circuit, such as shown in Fig. 3b, can be used. The operational amplifier provides a feedback loop that regulates the voltage across the resistors $R_1$ and $R_2$ to be equal. Thereby, the current is increased by the ratio $R_1/R_2$, and then mirrored with a mirror ratio of $N_{CM}$. For area reasons an *nmos* transistor M1 acts as an output current source. The output current $I_{Gate}$ is controlled by the $V_{GS}$ of M1, which is set by the current through $R_3$, Eqn. (1).

$$I_{Gate} = \frac{\beta_{M1}}{2} \cdot \left( \frac{R_1 \cdot R_3}{R_2} N_{CM} I_{Ref} - V_{th} \right)^2 \qquad (1)$$

The drawback of this circuit is the reference current, which is not matched to variations in the $V_{GS}$ of the output transistor M1. To compensate these variations, the opamp is replaced by MN1 in Fig. 4. The reference current $I_{Ref}$ increases the voltage at the gate of MN2 until enough current flows through $R_2$ to provide a sufficient gate voltage at MN1 for it to conduct $I_{Ref}$. The transistor MN1 is a minimal sized replica of the output transistor M1, hence Eqn. (1) modifies to Eqn. (2).

$$I_{Gate} = \frac{\beta_{M1}}{2} \left[ N_{CM} \cdot \frac{R_3}{R_2} \left( V_{th} + \sqrt{\frac{2 I_{ref}}{\beta_{MN1}}} \right) - V_{th} \right]^2 \qquad (2)$$

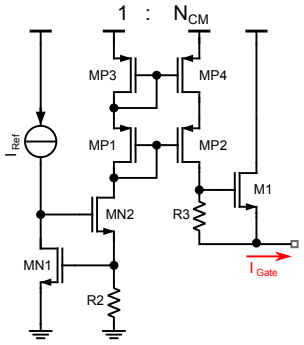


Figure 4: Gate driver with current source output and reference generation

To eliminate the nonlinearity in Eqn. (2), the current mirror ratio $N_{CM}$ and the resistor ratio $R_3/R_2$ have to cancel each other out. The output current $I_{Gate}$ is then only dependent on the ratio between the reference transistor MN1 and the output transistor M1, Eqn. (3).

$$\frac{I_{Gate}}{I_{ref}} = \frac{\left(\frac{W}{L}\right)_{M1}}{\left(\frac{W}{L}\right)_{MN1}} \qquad (3)$$

Using the same transistor types for MN1 and M1 also enables good matching options, and process variations are canceled out. A large ratio of the transistor size can be achieved, while still keeping the cascode current mirror small and the circuit responsive. Multiple reference circuits, consisting of MN1, MN2 and R2, can be built on the low side to switch between different current settings at high speed, and still use the same current mirror. Fig. 5 shows an implementation of the concept of Fig. 4. To be able to switch on the current $I_{CTRL1}$ instantaneously, an on / off switch was implemented in the reference generation circuit. While MN2 forces correct biasing of MN1, a second path transfers the actual current to the high-side via MN3, activated by MN5. The diode D2 ensures a low settling time at the switching event by matching the potential at the two resistors $R_{LS}$.

## II. Proposed Driver Circuit

The circuit of Fig. 5 is the basis for the innovations that are presented in this section with the goal to change the gate current faster, to make the current source more robust against large common mode changes, and to clamp the gate voltage

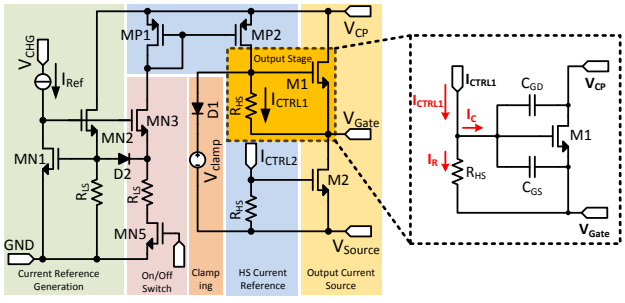


Figure 5: Current source gate driver with low side current reference

more precisely. The proposed gate drive circuit is shown in Figures 6 and 7.

### A. Fast Changeable Gate Currents

To be able to switch between different current levels in a very short time, the capacitors $C_{GS}$ and $C_{GD}$ (Fig. 5) have to be charged / discharged rapidly to match the new $V_{GS,M1}$. In Fig. 5, for a given size of M1, the speed is limited by the resistor $R_{HS}$, and the reference current $I_{CTRL1}$. This results in a gate current transition speed of 100ns from 0mA to 300mA. A class B buffer stage was inserted at the gate of the current source transistor M1 to increase the transition speed by 10x to 10ns without increasing the control current $I_{CTRL1}$ (Fig. 6).

The class B buffer stage has a dead band of $V_{thn}$ to $V_{thp}$ between input and output. The dead band was minimized by offsetting the reference current for the class B buffer $I_{CTRL,CB}$ to compensate for $V_{thn}$ / $V_{thp}$. This compensation of the dead band is achieved by inserting a source follower in the low side reference stage. The gate of the transistor MN4 in Fig. 7 is connected to $R_{LS,CB}$, and the source is connected to the gate of MN1 and to the resistor $R_{LS}$. This way the transistor MN5 of the buffer stage works as a source follower with resistor $R_{HS}$ in Fig. 6. The dc-level at the gate of M1 is set by the current $I_{CTRL1}$ through $R_{HS}$. $V_{thp}$ of MP5 is eliminated by a similar circuit (not shown). When the signal to transition to low output current is activated, MP5 discharges the gate of the output transistor M1 until the voltage level set by $I_{CTRL1}$ is reached. This ensures fast charging of the MOSFET capacitances in the driver output stage, and thus, a fast change of the output current. A similar circuit is implemented in the discharging path formed by M2 in Fig. 5.

### B. Reduced Current Dip

The switching transition causes a potential change at every ground referenced capacitance in the signal path. The gate-drain capacitance of M1 (Fig. 5) is of dominant influence and requires a surge in current to keep the voltage across $R_{HS}$ constant. The current $I_R$ through $R_{HS}$ in Fig. 5 is reduced by the current $I_C$ which flows into the drain-gate capacitance of M1. This lowers the $V_{GS}$ of M1 and thereby reduces the current provided by M1 significantly. This can be observed as a dip in the driver output current. To reduce this phenomenon, a cascode transistor M3 has been implemented as shown in Fig. 6. This transistor will keep the drain voltage of M1 nearly constant. The charging current of the drain-gate capacitance of M3 is delivered from its gate bias, shown in Fig. 7 (MN6, R7 and Z5). MN6 keeps the gate voltage of the cascode at a constant level that is set by $I_{bias,casc}$, R8 and Z3, referred to $V_{Gate}$. The class B buffer stage (boxes in Fig. 7) will also reduce the current dip because the buffer will provide a low impedance path to push / pull the gate voltage of M1 to the desired level. The cascode transistor is omitted as the discharge path needs no clamping and the area needed by the cascode transistor can be saved.

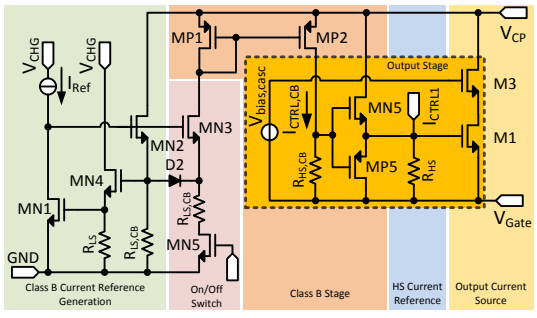


Figure 6: High-Side driver circuit with added class B buffer and cascode M3

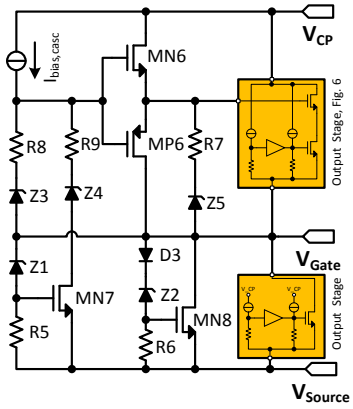


Figure 7: Biasing and clamping of the output stage

### C. Two-Stage Clamping Circuit

The cascode transistor M3 is also used by a two stage clamping circuit. This circuit limits the voltage between $V_{Gate}$ and $V_{Source}$ to a typical value of 12V, in order to prevent overvoltage stress on the external power MOSFET. A two stage design is required for this circuit in order to prevent the control currents from overcharging the gate of an external power MOSFET after the first clamping stage has activated. The first stage of the clamping circuit consists of Z1, R5 and MN7, Fig. 7. Z1 and R5 set the clamping voltage of the first stage to 10.5V. Once this level is reached, MN7 activates and turns MP6 on, which then switches the cascode M3 off and cuts the main current supply to $V_{Gate}$. The residue currents from the current references are clamped by the second stage of the clamping circuit, which consists of D3, Z2, R6 and MN8. Because of D3, this clamping stage kicks in 0.6V after the first stage and clamps $V_{Gate}$ via MN8 to approximately 11V, which fits various types of discrete power MOSFETs.

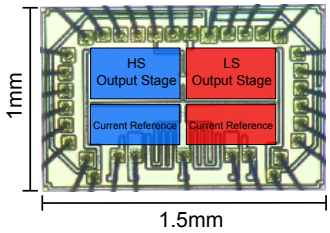


Figure 8: Chip photograph of the proposed driver in a 130nm HV-BiCMOS technology

## III. Measurement Results

The proposed driver circuit was implemented in a 130nm HV-BiCMOS technology and can operate at supply voltages up to 60V, Fig. 8. All measurements were performed with a test PCB containing a half bridge setup consisting of 40V IPD90N04S3_04 MOSFETs. The MOSFETs have an $R_{DS,on}$ of 3.6mΩ and a gate charge of 60nC. A 300µH air-coil was used as load element. The current dip and clamping circuit were measured in Fig. 9. With the new design, the dip was reduced from 80% to only 20% of the full gate current. The clamping activates at 10V and cuts any output current to the gate once the clamping voltage of 11V is reached at 1.2µs in Fig. 9b. In contrast, in Fig. 9a the driver begins to clamp the voltage at 5V / 0.8µs and slows down the whole switching transition until it reaches 10V at 2µs.

Fig. 10 shows the transient behavior of the variable current source output. The gate driver provides a current of 220mA with a rise time of 10ns and a transition to an 20mA low current setting in 15ns. To measure the change in $di/dt$, the voltage $V_{Stray}$ across a parasitic inductance in the current commutation path was measured. This voltage is dependent only on the inductance and the $di/dt$ according to $V_{Stray} = L \cdot di/dt$. An optimized switching transition for a slowed down current transition is shown in Fig. 10a. The current transition $t_{ct}$ (see also Fig. 1) takes place in 400ns, instead of 200ns, with constant high current in Fig. 10b. This results in a reduced voltage spike at the parasitic inductance. With 200mA constant current, a voltage spike of 11.5V can be observed (Fig. 10b). This value is reduced to 7V with the optimized profile. The overshoot of the drain-source voltage $V_{DS}$ is reduced by 5V, which is a significant advantage regarding electromagnetic compatibility (EMC), device stress and required max. ratings of the external power MOSFET.

## IV. Conclusion

A gate driver circuit with highly dynamic output current settings is presented in this paper. This kind of driver offers new opportunities regarding overshoot, device stress and EMC reduction, by employing different gate currents for the separate

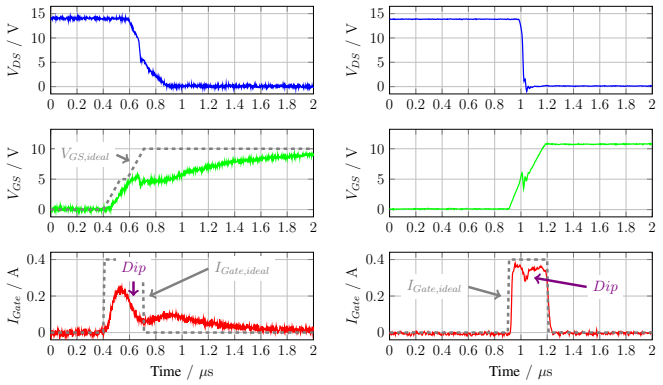


Figure 9: Measured transient behaviour, (a) Current dip without improved output stage; (b) Reduced current dip with new gate driver

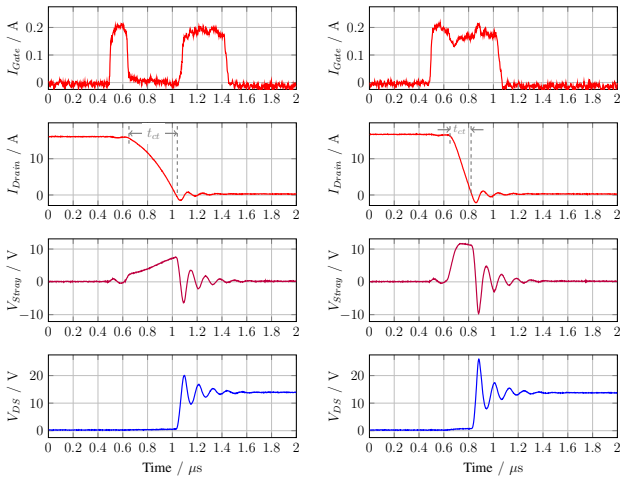


Figure 10: Comparison slow / fast switching, (a) Optimized switching waveform with $t_{ct}$ = 400ns; (b) Switching transition with constant current output and $t_{ct}$ = 200ns

sections of the switching transition. The driver has been implemented in 130nm HV-BiCMOS technology. An output class B buffer enables the very high transition speed of 10ns / 15ns (rising / falling transition) between different output currents, which makes it possible to change the gate current multiple times in one switching action. Reducing the gate current in the current transition phase reduces the voltage overshoot by 20% and the voltage spike across the parasitic inductance by 40%. The new output stage also offers a high immunity against transient coupling on the output current source by an additional cascode device. The dip in gate current was verified to be reduced by 60%. With the proposed driver, it is possible to shape the current and voltage transitions independently in MOSFET bridge applications. Such applications traditionally switch much faster than IGBT output stages, where gate current shaping is already more common.

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