A Fast Short-Circuit Protection Method Using Gate Charge Characteristics of SiC MOSFETs

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***Abstract*—This paper describes a fast protection circuit for silicon carbide metal-oxide semiconductor field-effect transistors (SiC MOSFETs) subjected to hard-switching faults (HSFs). In terms of reliability of power converters, the protection of power semiconductors against short-circuit failures is of great concern.**

The reverse transfer capacitance increases with decreasing drain–source voltage during normal turn-on transient. Under HSF conditions, on the other hand, it hardly changes because the drain–source voltage remains high. As a consequence, quite a significant difference appears in gate charge characteristics between under HSF conditions and normal turn-on operation. Hence, an HSF can be detected by monitoring both the gate–source voltage and the amount of gate charge. The proposed protection circuit has high noise tolerance because it monitors not only the gate-source voltage but also the amount of gate charge.

The validity of the protection circuit is verified by experiment. The proposed protection circuit can detect the HSF within only one microsecond.

I. Introduction

A silicon carbide metal-oxide semiconductor field-effect transistor (SiC MOSFET) is one of the most promising power semiconductor devices for high power density converters because of low conduction and switching losses, high temperature operating capability, and high thermal conductivity. The protection of power semiconductors against failures caused by short circuit is of great concern for reliability of power converters. A fast protection circuit for a hard-switching fault (HSF) is required especially for SiC MOSFETs.

For insulated-gate bipolar transistors (IGBTs), many kinds of protection circuits have been reported [1]–[10]. The collector–emitter-voltage monitoring method (V_{ce}-monitoring method) is one of the conventional protection circuits [1]. Under normal conditions, v_{ce} softly drops toward saturation voltage $V_{ce(sat)}$, so that it takes a long blanking time to detect the HSF in this method. The collector-current monitoring method is also a well-known protection circuit, but it is not a cost-effective method because it needs a current sensor such as a current transformer.

The gate–emitter-voltage monitoring method (V_{ge}-monitoring method) has an advantage in terms of requiring neither a high voltage diode for sensing nor a current sensor [2]–[4]. However, it requires a blanking time to distinguish the HSF from normal turn-on operation.

The V_{ge}-monitoring method combined with the V_{ce}-monitoring method has been reported [5], [6]. It can detect the HSF during a turn-on transient period without setting a blanking time. However, it requires a high-voltage diode for sensing.

The gate-charge monitoring method (Q_g-monitoring method) detects the HSF because the amount of gate charge under HSF conditions is smaller than that under normal turn-on conditions [7]–[9]. This method is affordable, and a fast detection is possible. However, the threshold value of the gate charge for detecting the HSF is not a constant value but a pulse signal which is predefined as a function of the gate–emitter voltage [7]–[9]. In addition, this method generates unnecessary power dissipation because it uses a current mirror circuit.

The fast protection circuit based on a gate charge characteristic has been reported [10]. A gate charge characteristic shows a switching property of power semiconductor devices, so that a significant difference appears in gate charge characteristics between under normal turn-on operating conditions and HSF conditions. Hence, IGBTs can be protected from destruction by monitoring the gate–emitter voltage and the amount of gate charge. Since there is no essential difference between IGBTs and SiC MOSFETs in terms of gate charge characteristic, the HSF detection method based on a gate charge characteristic is applicable to SiC MOSFETs. However, the validity of the method has been verified only for IGBTs. In SiC MOSFETs, the gate–source voltage v_{gs} rises gradually during Miller plateau, so that the reference value of the gate–source voltage to detect the HSF can be set to an arbitrary voltage in Miller plateau. Hence, this protection method is suitable for SiC MOSFETs.

This paper verifies the effectiveness of the proposed protection circuit for SiC MOSFETs subjected to an HSF by experiment.

978-1-4673-7151-3/15/$31.00

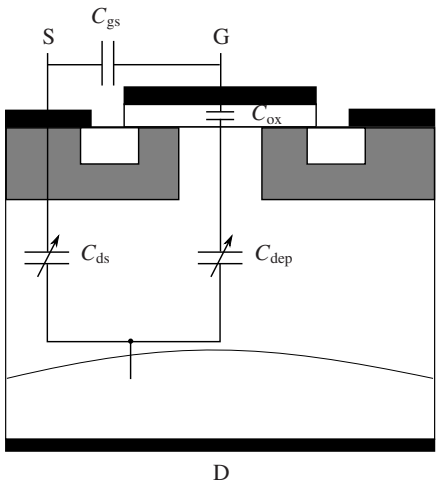

Fig. 1. SiC MOSFET structure and its internal capacitors.

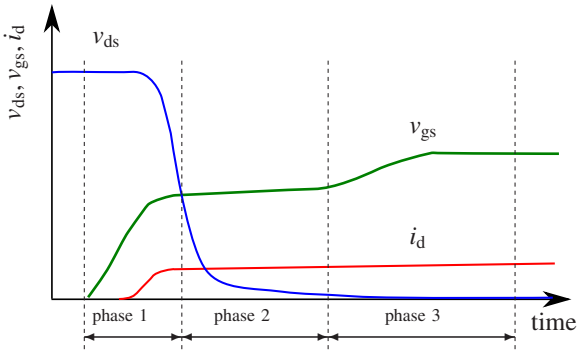

Fig. 2. Typical waveforms under normal conditions.

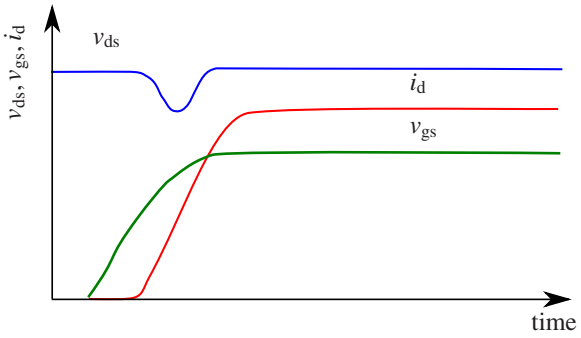

Fig. 3. Typical waveforms under HSF conditions.

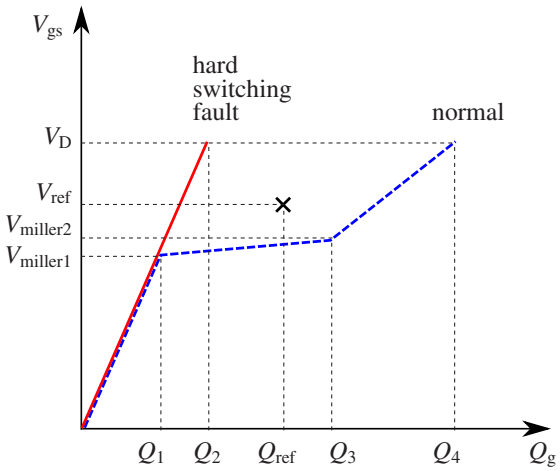

Fig. 4. Gate charge characteristics under normal conditions and HSF conditions.

II. Switching behavior and gate charge characteristics of SiC MOSFETs

A. normal turn-on operation

Fig. 1 shows a structure and internal capacitors of a SiC MOSFET. Drain–gate capacitance C_{dg}, which is referred as reverse transfer capacitance, is the combination of MOS oxide capacitance C_{ox} in series with depletion capacitance C_{dep}. Reverse transfer capacitance C_{dg} is expressed as follows:

$$C_{dg} = \frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}} = \frac{C_{dep}}{1 + C_{dep}/C_{ox}} \quad (1)$$

The gate–source capacitance, the drain–gate capacitance and the drain–source capacitance have voltage dependency. The switching behavior of SiC MOSFETs depends heavily on reverse transfer capacitance C_{dg} because it varies in accordance with the drain–source voltage.

Fig. 2 illustrates typical waveforms of drain–source voltage v_{ds}, drain current i_d and gate–source voltage v_{gs} under normal conditions. There is the period in which the gate–source voltage hardly increases during turn-on transient.

Under normal operating conditions, turn-on process of a SiC MOSFET is as follows.

Phase 1: A SiC MOSFET remains fully saturated due to the high drain–source voltage. In this period, depletion capacitance C_{dep} is much smaller than MOS oxide capacitance C_{ox}, so that reverse transfer capacitance C_{dg} is almost equal to C_{dep}. Besides, reverse transfer capacitance C_{dg} is much smaller than gate–source capacitance C_{gs}. Hence, gate current i_g is flowing only into C_{gs}, and the gate–source voltage is increasing up to the voltage which corresponds to the beginning of the Miller plateau.

Phase 2: The drain–source voltage is dropping toward on-state value $V_{ds(on)}$, and reverse transfer capacitance C_{dg} is being large. Almost of all the gate current is flowing into C_{dg}, and gate–source voltage v_{gs} is slightly increasing. This period is referred as Miller period.

Phase 3: Drain–source voltage v_{ds} has dropped to the voltage where the SiC MOSFET changes from the saturation region to the linear region. The gate–source voltage increases to sustain load current I_d. Gate current i_g is flowing into both C_{gs} and C_{dg}, and gate–source voltage is increasing up to the positive gate control voltage.

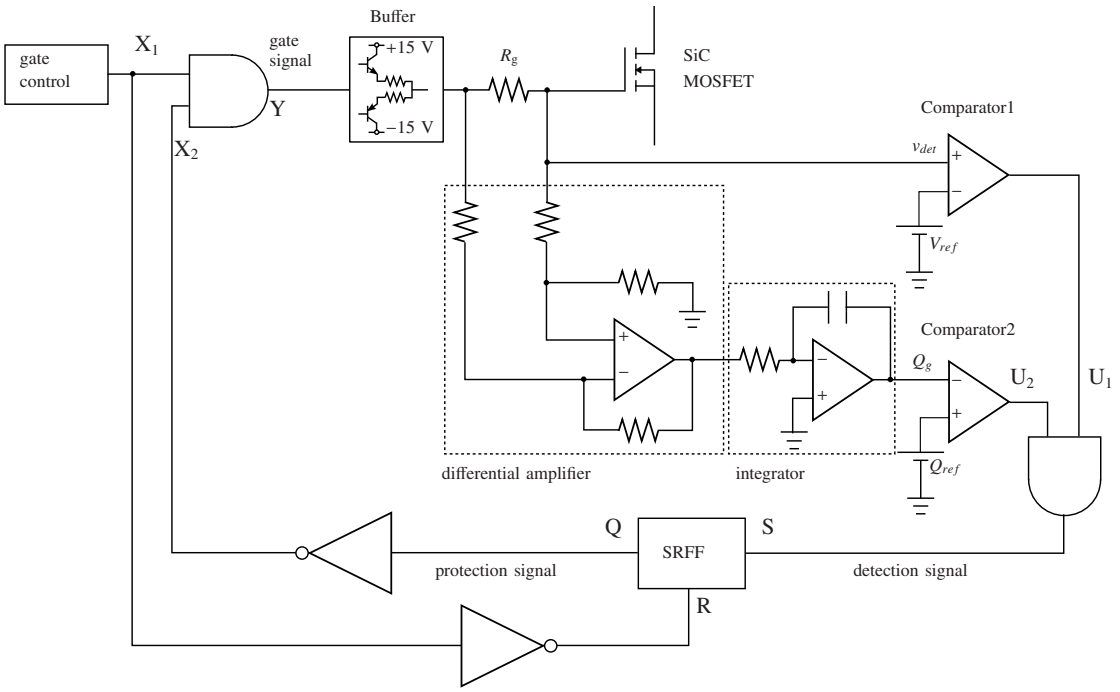

Fig. 5. Outline of the circuit configuration of the proposed HSF detection method.

B. Hard-switching fault

Fig. 3 illustrates typical waveforms under HSF conditions. Drain–source voltage v_{ds} remains high under HSF conditions. Reverse transfer capacitance C_{dg} hardly changes, and the gate current is flowing only into C_{gs}. The gate–source voltage is rapidly rising to the positive gate control voltage, so that Miller plateau does not appear in the gate–source voltage under HSF conditions.

C. Gate charge characteristic

As mentioned above, there is quite a significant difference in gate–source voltage waveforms between under normal conditions and under HSF conditions. As a consequence, a gate charge characteristic under HSF conditions differs from that under normal operating conditions.

Fig. 4 depicts a comparison between gate charge characteristics under normal conditions and HSF conditions. When the gate–source voltage is lower than $V_{miller1}$ which corresponds to the voltage at the beginning of the Miller plateau, no difference is found in gate charge characteristics between normal turn-on conditions and HSF conditions.

Under normal turn-on conditions, gate–source voltage v_{gs} rises gradually from $V_{miller1}$ to $V_{miller2}$ with increasing gate charge from Q_1 to Q_3 during Miller period, and v_{gs} reaches positive gate control voltage V_D. As a consequence, the gate charge characteristic under normal conditions is stepwise.

On the other hand, reverse transfer capacitance C_{dg} remains small under HSF conditions because drain–source voltage v_{ds} remains high. Gate–source voltage v_{gs} reaches rapidly positive gate control voltage V_D, so that no Miller plateau appears. Consequently, the gate charge characteristic is linear under HSF conditions.

III. Methods of short circuit detection and protection

As shown in Fig. 4, the amount of gate charge under normal turn-on conditions is larger than that under HSF conditions when the gate–source voltage is higher than the voltage in Miller plateau. Hence, an HSF can be detected by monitoring both the gate–source voltage and the amount of gate charge.

Reference charge Q_{ref} and reference voltage V_{ref} should be set to the value within the quadrangle area surrounded by the four coordinates (Q_1, $V_{miller1}$), (Q_3, $V_{miller2}$), (Q_4, V_D), and (Q_2, V_D). Since $V_{miller1}$ and $V_{miller2}$ are characterized by the drain current, Q_1 and Q_3 has drain-current dependency. Besides, Q_3 and Q_4 depend on dc-link voltage V_{DC}. As a consequence, the four coordinates are characterized by the drain current and the dc-link voltage.

Under HSF conditions, Q_g is smaller than Q_{ref} when a gate–source voltage is lower than V_{ref}. Under normal turn-on conditions, however, gate charge Q_g is larger than Q_{ref} when a gate–source voltage reaches V_{ref}. Hence, an HSF can be detected as soon as v_{gs} exceeds reference voltage V_{ref}. When V_{ref} is set to a voltage between $V_{miller1}$ and $V_{miller2}$, it can detect the HSF faster than the existing HSF protection circuit.

The proposed protection circuit senses not only the gate-source voltage but also the amount of gate charge. Hence, it has high noise tolerance compared with either V_{ge}-monitoring method or Q_g-monitoring method.

Fig. 5 shows an outline of the protection circuit against HSF conditions. It monitors gate–source voltage v_{gs} and the voltage across gate resistor R_g. The detected voltage across R_g

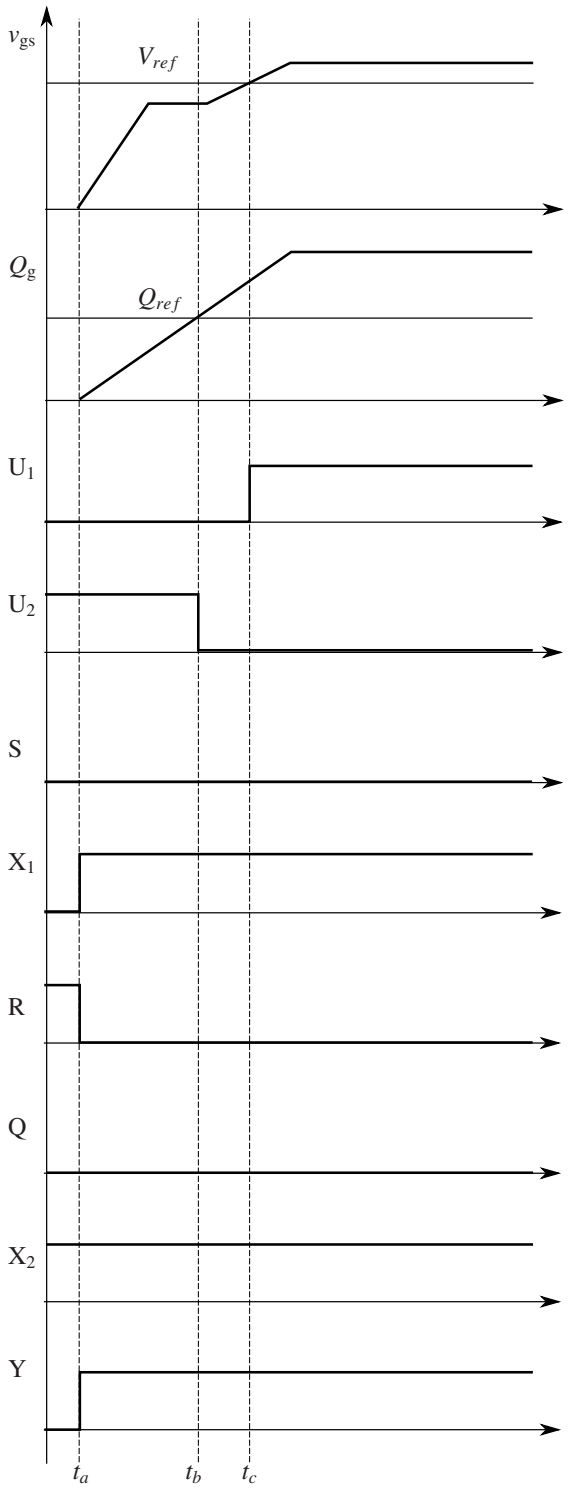

Fig. 6. Timing chart under normal turn-on operations.

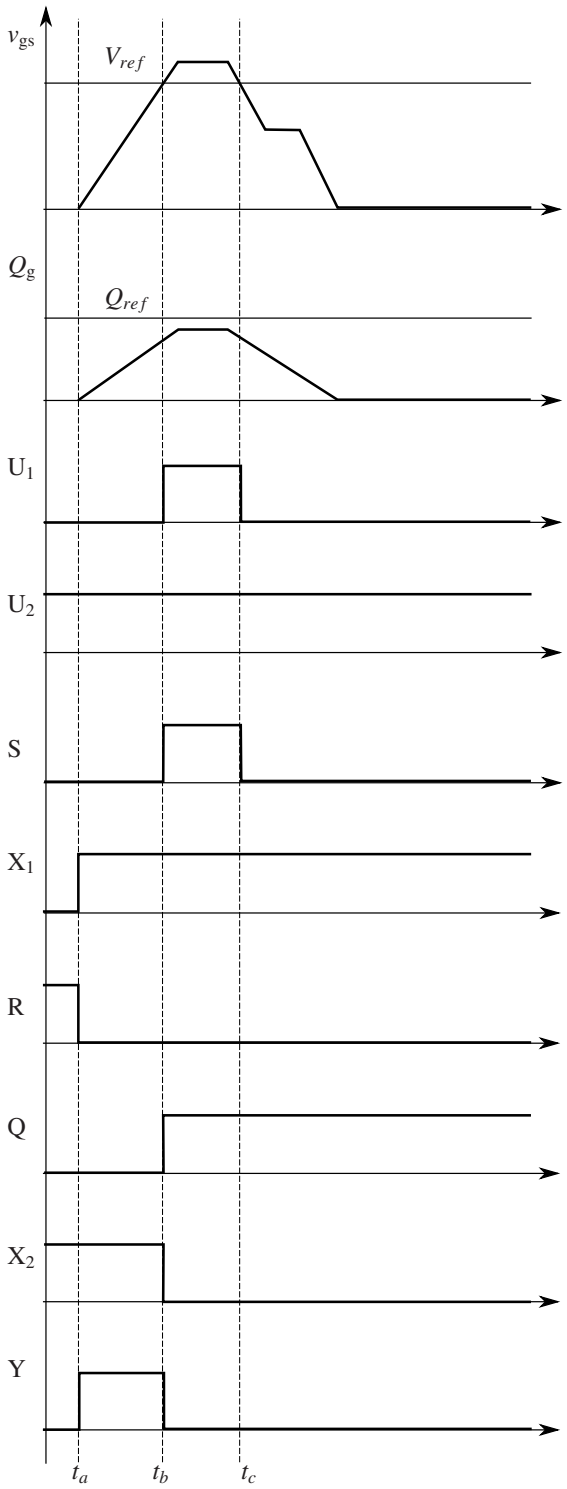

Fig. 7. Timing chart under HSF conditions.

is transferred to a differential amplifier, and gate charge Q_g is calculated with an integrator. Detected gate–source voltage v_{det} and Q_g are compared with reference voltage V_{ref} and Q_{ref}, respectively.

The detection signal is a logical product of the output signals from Comparator1 and Comparator2. The detection signal should be held by using a latch-circuit such as a set-reset flip-flop (SRFF) because v_{gs} decreases after detecting the HSF to protect the SiC MOSFET from destruction. The inverting original gate control signal is transfered to the reset terminal in an SRFF. The final gate signal "Y" is the logical product of the original gate control signal "X_1" and the inverting protection

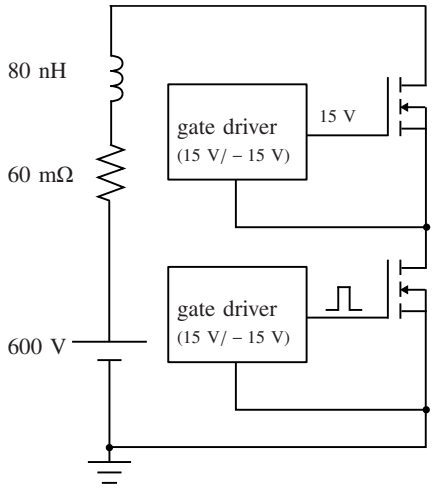

Fig. 8. Test circuit under an HSF condition.

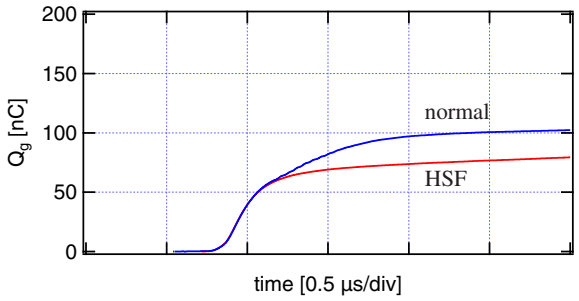

Fig. 9. Comparison of gate charge under the normal condition and the HSF condition.

signal "X_2".

Fig. 6 shows a timing chart of each node in the protection circuit under a normal turn-on operating condition. After $t = t_c$, v_{gs} becomes higher than V_{ref}, whereas Q_g is higher than Q_{ref} after $t = t_b$. Consequently, the detection signal S is always "Low" under a normal turn-on condition.

Fig. 7 shows a timing chart of each node in the protection circuit under an HSF condition. Under HSF conditions, Q_g is always smaller than Q_{ref} because no Miller plateau appears in the v_{gs} waveforms. When V_{ref} is set to the value higher than $V_{miller1}$, the novel protection circuit can detect the fault as soon as v_{gs} exceeds V_{ref}. Hence, the detection signal S shows "High" between t_b and t_c. After detecting the fault, v_{gs} starts decreasing to protect the SiC MOSFET from destruction. Accordingly, v_{gs} becomes lower than V_{ref} at $t = t_c$, and detection signal S changes from "High" to "Low". However, protection signal Q is held "High" after $t = t_c$ by using a latch-circuit such as an SRFF.

IV. Experimental results

Fig. 8 shows the test circuit under an HSF condition. A 1200-V, 24-A SiC MOSFET is used as a test device. The dc-link voltage is set to a voltage of 600 V. Parasitic resistance and

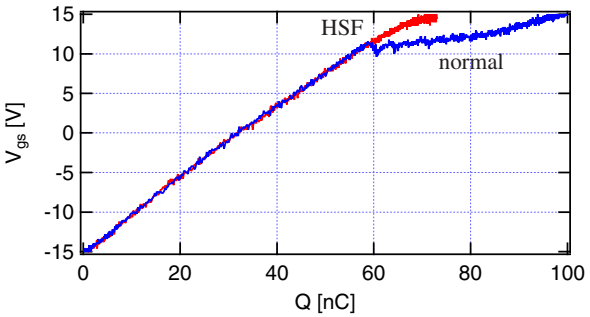

Fig. 10. Comparison of gate charge characteristics under the normal condition and the HSF condition.

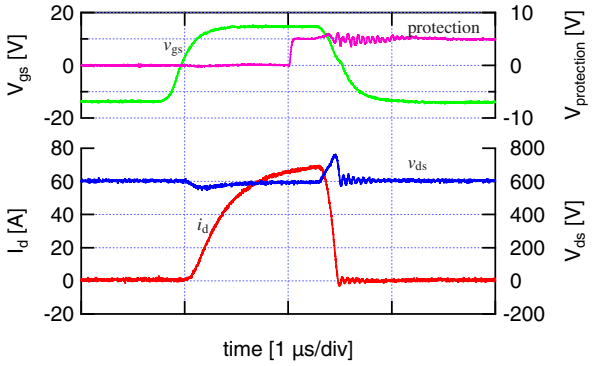

Fig. 11. Experimental waveforms with the protection circuit.

inductance are 60 mΩ and 80 nH, respectively. The positive and negative gate control voltages in the gate driver are +15 V and -15 V, respectively.

The lower-side MOSFET is a switching device, and the pulse signal (±15 V) is applied to the gate terminal. In the upper-side MOSFET, on the other hand, the positive gate control voltage is applied to the gate terminal in order to be kept in the on-state, and no inductive load is connected between the drain and the source terminals.

The proposed protection circuit does not require any blanking time because it detects the HSF as soon as the gate–source voltage exceeds reference voltage V_{ref}. In this experiment, the time constant of the integrator is 300 ns, and the delay time from the detection to the forced turn-off is about 200 ns.

Fig. 9 indicates a comparison of the gate charge under the normal turn-on condition and the HSF condition. The amount of gate charge under HSF conditions is smaller than that under normal turn-on condition.

Fig. 10 shows experimental results of the gate charge characteristics under the normal turn-on condition and the HSF condition. As shown in Fig. 10, the voltage in Miller plateau is about 11 V, so that the reference gate–source voltage was set to the voltage of 14 V in the experiment. The total amount of gate charge under the normal tun-on condition and the HSF condition were about 100 nC and 70 nC, respectively. As a

consequence, the reference value of gate charge was set to the voltage which corresponds to 90 nC.

Fig. 11 shows the experimental waveforms under the HSF condition with the protection circuit. The HSF was detected as soon as the gate–source voltage exceeds 14 V.

As shown in Fig. 11, the drain–source voltage was almost equal to the dc-link voltage, and the drain current reached 70 A, which is about three times as high as its rated current. The gate–source voltage rapidly increased to the positive gate control voltage, and no Miller plateau appeared during turn on transient. The HSF detection time was within about 1 μs after the collector current started flowing through the SiC MOSFET.

The experimental results verify the validity of the protection circuit based on a gate charge characteristic.

V. Conclusion

This paper has presented a fast protection circuit for SiC MOSFETs subjected to HSF conditions. It detects an HSF by monitoring both the gate–source voltage and the amount of gate charge during turn-on transient. No blanking time is required, and the reference gate–source voltage can be set to a voltage in Miller plateau. Hence, it protects SiC MOSFETs from destruction more rapidly than the conventional protection circuits.

Experiment has confirmed that the proposed circuit can detect the HSF within only 1 μs. It is fast enough to detect the HSF from a practical point of view. Moreover, it is a cost-effective method because it requires neither a high voltage diode for sensing nor a current sensor.

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