SmarResearch
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HART Modem
HT2012
DataSheet

HART®
Fieldbus
Profibus
Intrinsic Safety
Configuration Tools
Semiconductors
Training
Custom Design

Features

- Operates at the Bell 202 Standard Forward Bit Rate (1200 bits/ second)
- Uses 1200 Hz and 2200 Hz Bell 202 Shift Frequencies
- Low Power Consumption (typically 40 uA)
- Accurate Carrier Detect Logic
- Single Chip Frequency Shift Keying (FSK)
- 1200 Baud Transmit and Receive Modulation
- 3 to 5 Volt Power Supply
- CMOS and TTL I/O compatible
- Optimized for Intrinsically Safe Applications
- Uses reliable CMOS technology
- Available in 16 pin DIP or 28 pin PLCC packages

General Description

The HT2012 HART ® (Highway Addressable Remote Transducer) is a single chip CMOS low power FSK modem which operates at the Bell 202 standard. It is designed to provide HART® communication capabilities in process control instrumentation and other low power equipment, and provides a low cost, reliable single chip modem capability conforming to the HART® Physical Layer.

The HT2012 is ideal for factory automation, process control, and other applications that require low power such as intrinsically safe environments. The modem circuitry is digital, and includes both modulating and demodulating functions. The HT2012 is designed for use with external circuits that amplify, filter, and shape the media signals, operates from a single 3.3 to 5.0 Volts power supply, and requires an externally generated clock of 460.8 kHz.

The HT2012's operation is half duplex, with the modulator and demodulator controlled by the INRTS pin. It operates at the Bell 202 standard upper (forward) bit rate of 1200 bits per second, and uses Bell 202 standard nominal shift frequencies of 1200 Hz and 2200 Hz. An active low carrier detect output and 19.2 kHz clock output are provided in either a 16 pin Dual In-line (DIP) or 28 pin Plastic Leaded Chip Carrier (PLCC) package *(See Figure 1).* With proper media conditioning, the HT2012 can communicate with other commercial Bell 202 modem without either external adjustments or special biasing.

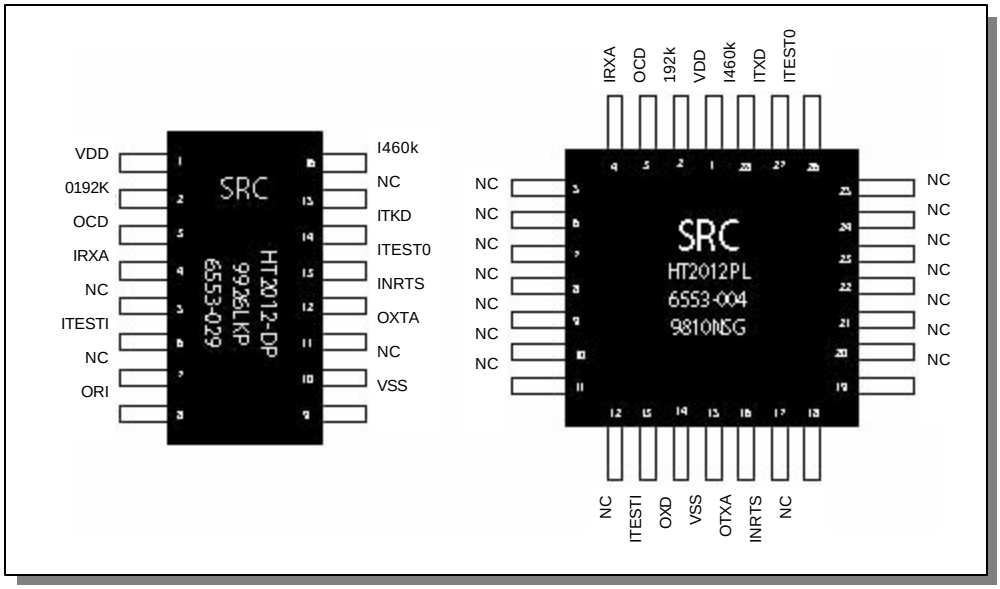

Figure 1 - Pin Out Packages

Table 1 - Pin Descriptions

Signal	Type	DIP Pin	PLCC Pin	Description
VDD	*	1	1	+3.3 to 5.0 Vdc power supply.
019_2k	Output	2	2	User Clock (16x bit rate. Nominally 19.2 kHz).
OCD	Output	3	3	Carrier Detect (Low (0) when carrier present).
IRXA	Input	4	4	Demodulator Input (accepts 1200 or 2200 Hz square wave modulated carrier).
NC	*	5	5-12	No internal connection
Input TEST1	Input	6	13	Test Input One (Must be connected to VSS during normal operation).
NC	*	7	*	No internal connection
ORXD	Output	8	14	Demodulator Output. Provides a logical 1 in response to a 1200 Hz FSK square wave signal at IRXA; a logical 0 to 2200 Hz. Demodulation only takes place when $\overline{\text{INRTS}}$ is high (1). ORXD output is undefined when $\overline{\text{INRTS}}$ is low (0).
VSS	*	9	15	Power Supply Ground.
NC	*	10	*	No internal connection
OTXA	Output	11	16	Modulated Output. Provides a 1200 Hz square wave FSK output in response to a logical (1); 2200 Hz in response to a logical (0). Active when $\overline{\text{INRTS}}$ is low (0). Goes to high impedance state when $\overline{\text{INRTS}}$ is high (1).
$\overline{\text{INRTS}}$	Input	12	17	Request To Send. Selects operation of modulator when low (0); demodulator when high (1). Causes OTXA to go to high impedance state when high (1).
Input TEST0	Input	13	26	Test Input Zero. Must be connected to VSS during normal operation.
ITXD	Input	14	27	Modulator Input. Accepts input data (logical 0 or 1) for carrier output modulation at OTXA.
NC	*	15	18-25	No internal connection
I460k	Input	16	28	Input Clock. Clocks modem circuits. Frequency is nominally 460.8 kHz.

Functional Description

The HT2012 has four major function blocks: carrier detect, clock/ timing, modulation, and demodulation. The nominal bit rate is 1200 bits per second. The HT2012 uses shift frequencies of nominally 1200 Hz (mark = binary 1) and 2200 Hz (space = binary 0).

Clocks

A digital input frequency of 460.8 kHz is accepted from an external source, and is used to generate several internal clocks. All circuit operations can be performed with a master clock frequency of 460.8 kHz. This frequency is significantly lower than clock frequencies used by other single chip modems and results far lower power requirements. Power consumption is further reduced by various sections of the modem being shut down (not clocked) when not in use.

One internal clock at a nominal frequency of 19.2 kHz is brought to an output pin, enabling reconstruction of the data in external circuits.

Demodulator

The demodulator accepts an FSK signal at its IRXA input and reproduces the original modulating signal at the ORXD output. Both input and output signals are digital.

Modulator

Digital data in NRZ form is accepted at the ITXD input. An FSK modulated signal is generated at the OTXA output. The modulator provides phase continuous modulation. The phase angle of the modulated signal is preserved when switching between shift frequencies.

Carrier Detect

The nominal bit rate is 1200 bits per second. The HT2012 uses shift frequencies of nominally 1200 Hz (mark) and 2200 Hz (space).

If the measured interval time falls outside these limits for a period of time after the carrier has been detected carrier detect output is not asserted.

Modem Characteristics

The HT2012 incorporates a Bell 202 compatible 1200 baud modem which implements Frequency Shift Keying (FSK) techniques used to transfer data. A 1200 Hz tone represents a mark while a 2200 Hz tone represents a space. The half duplex operation permits data rates up to 1200 bits per second in both transmit and receive modulation modes.

The HT2012 HART® modem has four main subsections: carrier detect, clock/timing, modulation, and demodulation.

Carrier Detect

The carrier detect output is active low whenever a valid carrier tone between 1000 and 2575 Hz (inclusive) is detected. Detection occurs when timed transitions remain within the band of the 1200 and 2200 Hz periods for 40 nannoseconds to 1 Bit time.

A loss of carrier for 1 millisecond or more causes the carrier detect line to go inactive high (1).

Carrier Detect Frequency Range:

1000 Hz to 2575 Hz

The range of frequencies applied at IRXA over which OCD must go low (0).

Time from Carrier Input to Carrier Detect:

40 nannoseconds (Minimum)
1 bit time (Maximum)

The time from the start of a valid carrier signal at IRXA until OCD goes to logical low (0).

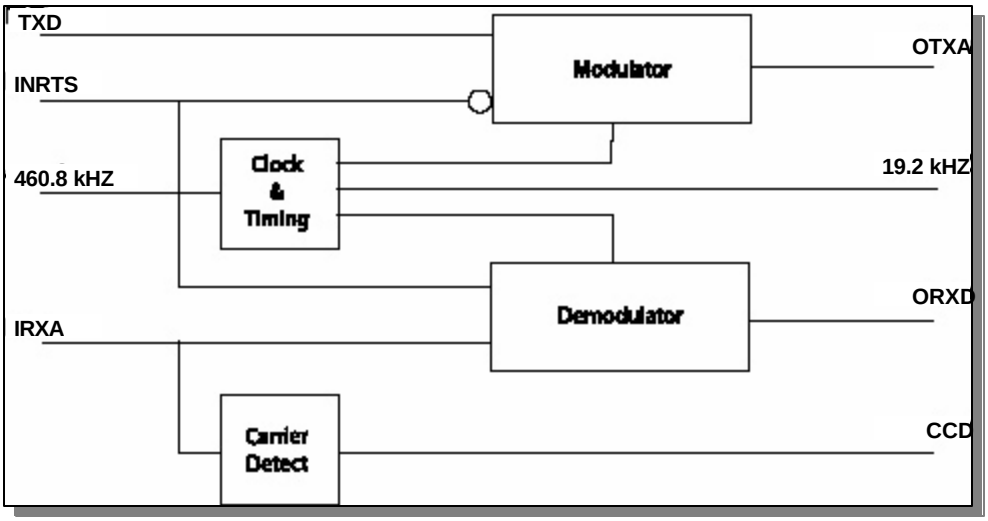

Figure 2 - Modem Characteristics

Time From Carrier Loss to Carrier Undetect:

1.68 milliseconds (Maximum)

The time from the lose of a valid carrier signal at IRXA until OCD goes to a logical high (1).

Conditions:

1. Clock frequency of 460.8 kHz +/- 0.1%
2. Input (IRXA) asymmetry maximum of 5.0%

Clocking and Timing:

The HT2012 requires a 460.8 kHz clock to generate all internal and external timing and control signals. Internal clocks are turned off when a section is not being used to minimize power requirements. The 460.8 kHz input frequency further reduces power requirements compared to most other modem chips that require higher input clock frequencies.

A 19.2 kHz signal is brought outside the HT2012 to support reconstructing data external to the chip. This is the same signal used internally to synchronize operations and is useful for designers who want to preserve that synchronization externally.

The 460.8 kHz clock is divided to generate 1200 and 2200 Hz mark and space frequencies. Dividing by 3 generates 153.6 kHz and dividing by 5.5 generates 83.8 kHz. A common divide by 70 then yields 2194.3 and 1196.9 Hz respectively, resulting in a small phase error of 9.5 degrees and 5.2 degrees *(See Figure 2).*

User Clock Frequency:

Nominal 19.2 kHz
Proportional to the 460.8 kHz clock at I460K

Modulator

The modulator takes data to transmit and modulates it as either 1200 Hz (mark) a 2200 Hz (space). The input signal to transmit is applied to the ITXD pin as an NRZ digital signal. The output

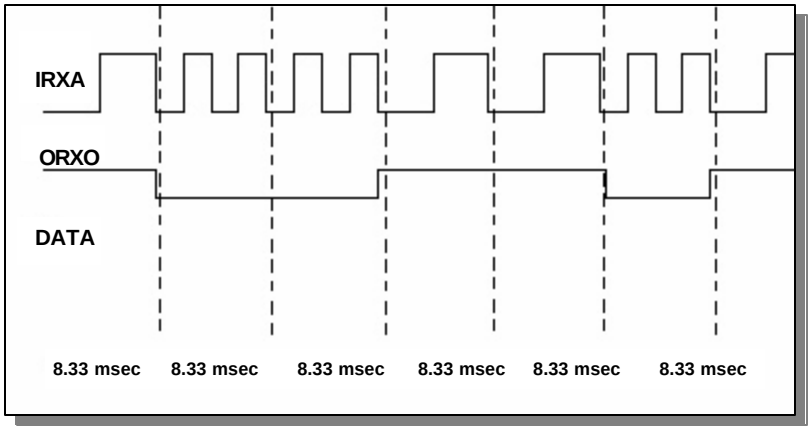

Figure 3 - Typical Demodulator Signal

on the OTXA pin is the FSK modulated signal and is ready to be connected by the line driver and cable interface circuitry.

An important feature of the modulator is its preservation of the phase integrity of each frequency when switching between frequencies. This enables accurate reconstruction of the original modulating signal at the output of the demodulator *(See Figure 4)*.

The clock/timing section generates timing and reference frequencies for the modulator. Output transitions are examined as to when they occur, limiting the maximum accumulated timing error to 12 microseconds, the period of the slower modulation frequency.

Modulator Output Frequency (at OTXA pin):

2194.3 Hz - Nominal High Frequency (space).
1196.9 Hz - Nominal Low Frequency (mark).

Modulator output frequencies are proportional to the input clock frequency.

Modulator Phase Continuity Error:
Maximum +/- 10 degrees

Demodulator

The input signal from the IRXA pin is a digital pulse train consisting of the FSK modulated square waves. The demodulated data stream is buffered at the ORXD pin as a digital output signal *(See Figure 3)*.

Maximum Demodulator Jitter:

+/- 12% of one bit time

Conditions:

1. Input frequencies at 1200 Hz +/- 10 Hz; 2200 Hz +/- 20 Hz
2. Clock frequency of 460.8 kHz +/- 0.1%
3. Input (IRXA) asymmetry = 0

Electrical Characteristics

Table 2 - Electrical Characteristics

Parameter	Symbol	Min.	Max.	Unit
Storage temperature	TSTG	-65	+150	0^C
Operating free-air temperature	TA	-40	+85	0^C
Supply voltage (non-operating)	VDD		7	V

Table 3 - AC Characteristics

Clock frequency	480.8 kHz +/- 0.1%
Clock pulse widths	150 nanoseconds min. (high and low levels)
Clock rise and fall time	10 nanoseconds (max.)
IRXA input rise and fall time	200 nanoseconds (max.)
Other inputs rise and fall time	50 nanoseconds (max.)
Output rise and fall time	10 nanoseconds (max.)

Notes:

1. *All conditions apply over the full operating temperature range with 5.0 volt supply voltage.*
2. *Power should be disconnected before inserting or removing device.*
3. *Store device in conductive foam with all pins shunted to avoid damage from electrostatic discharge.*
4. *Avoid application of voltage or stresses over the maximum ratings.*

Table 4 - Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Condition
VDD	Supply voltage	3.0	5.5	V	
VIN	Input voltage	VSS - 0.3	VDD +0 .3	V	
VIH	Logical 1 input voltage	2.0	VDD + 0.3	V	
VIL	Logical 0 input voltage	VSS - 0.3	0.8	V	
VOL	Output low voltage		0.4	V	Output sink current (4.0mA)
VCH	Output high voltage	2.4	VDD - 0.3	V	Output source current (4.0mA)
IDD*	Supply current during demodulation (typical)	40		µA	@ 5.0v
IDD*	Supply current during modulation (typical)	80		µA	@ 5.0v
IIN	Input leakage current		+/- 1	µA	typical
ITO	High impedance output leakage current		+/- 10	µA	typical
ICIN	Input capacitance		10	pF	typical

* 50pF load to all outputs; all input rise and fall times satisfied; clock frequency = 460.8 kHz +/- 0.1%

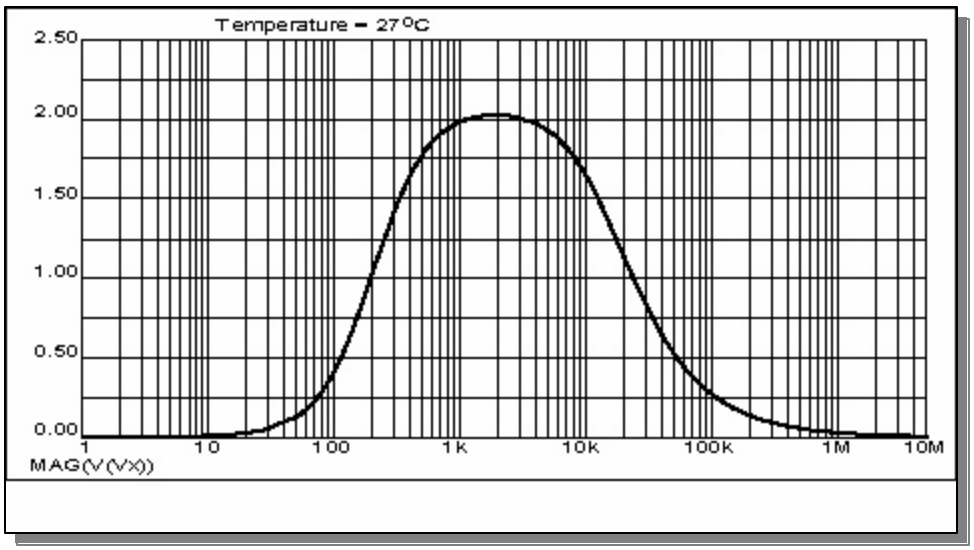

Figure 4 - Gain Vs. Frequency Curve

The HT2012 is designed for use as a peripheral device to a local microprocessor or microcontroller. All interface lines are digital and can directly connect to CMOS or TTL level components. The HT2012 requires two interfaces; one to the local microprocessor or microcontroller, and a second to the medium *(See Figure 5)*.

Microprocessor Interfacing

In its simplest form, the HT2012 is either in the transmit mode or the receive mode depending on the state of the $\overline{\text{INRTS}}$ control signal from the local microprocessor.

If $\overline{\text{INRTS}}$ is logic 0, the modulator is enabled and transmit data is modulated and output on the OXTA pin. The demodulator section is turned off to save power.

If $\overline{\text{INRTS}}$ is logic 1, the demodulator is enabled and the demodulated data from the IRXA pin is output to the ORXD pin. The modulator is turned off to save power.

When the demodulator is active, the carrier detect line (OCD pin) is active low when a valid carrier is present, and inputting demodulated data can begin.

Note:
When the HT2012 is in transmit mode ($\overline{\text{INRTS}}$ = 0) the OCD carrier detect pin is active low because it is still sensing the activity of the carrier being transmitted. In this case, even though the carrier detect is active low, no modulated data is available from the ORXD pin.

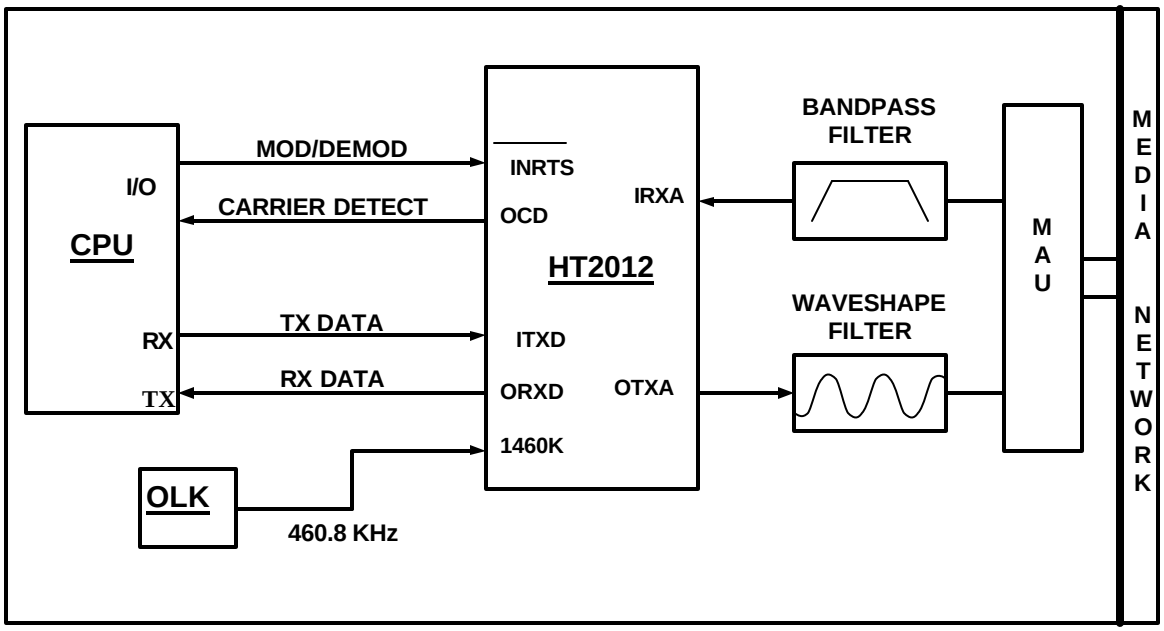

Figure 5 - Typical Hardware Design

Medium Interfacing

A typical application will send transmitted data over a signal medium and receive data over the same medium in a half duplex mode. The signal medium interface will vary and in most cases will contain an input bandpass filter as well as an output wave shaping filter *(See Figure 6).*

The input filter consists of a bandpass filter and a square wave shaper to regenerate the digital square waves to the HT2012. The square wave shaper is a comparator which functions as a zero cross detector. The comparator has a threshold set at half signal level, squaring the input signals and regenerating the sharp edges required by digital circuits. The timing characteristics of the originally transmitted signal are preserved for the accurate decoding of Manchester data.

The bandpass filter is used to reduce induced noise on the received signal, and is needed to smooth sharp transitions and eliminate high frequency components of the input signal. The pass band starts at around 1200 Hz and cuts off at around 2200 Hz. Depending on the signal medium and transmit signal levels, front end gain might be required before applying the signal to the bandpass filter.

The output wave shaping filter functions as a current to voltage modulator and smoothes transition edges to minimize spurious frequencies and harmonics over the transmission lines. This helps eliminate false triggers at the remote receiver due to noise centered on the transition threshold. A simple integrator can be used, depending on the medium interface. In some applications an output filter is not required if the transmission medium can accept square waves directly without inducing or radiating unacceptable levels of noise.

An important characteristic of both filter designs is that they exhibit relatively constant phase delays over the operating bandwidth. This helps assure accurate timing characteristics for the regenerated demodulated signal *(See Figure 7)*.

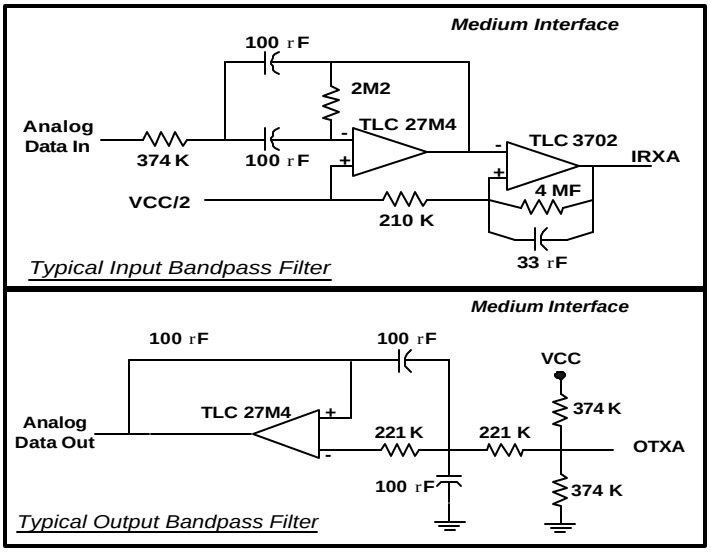

Figure 6 - Typical Bandpass Filter and Output Wave Shape Filters

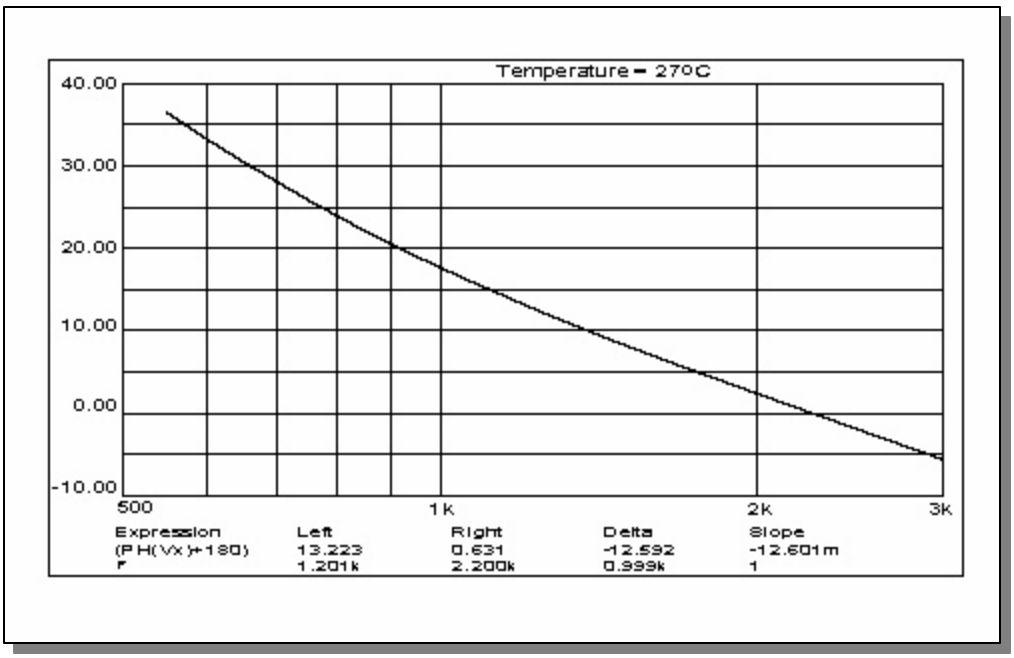

Figure 7 - Phase Shift Vs. Frequency Curve

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