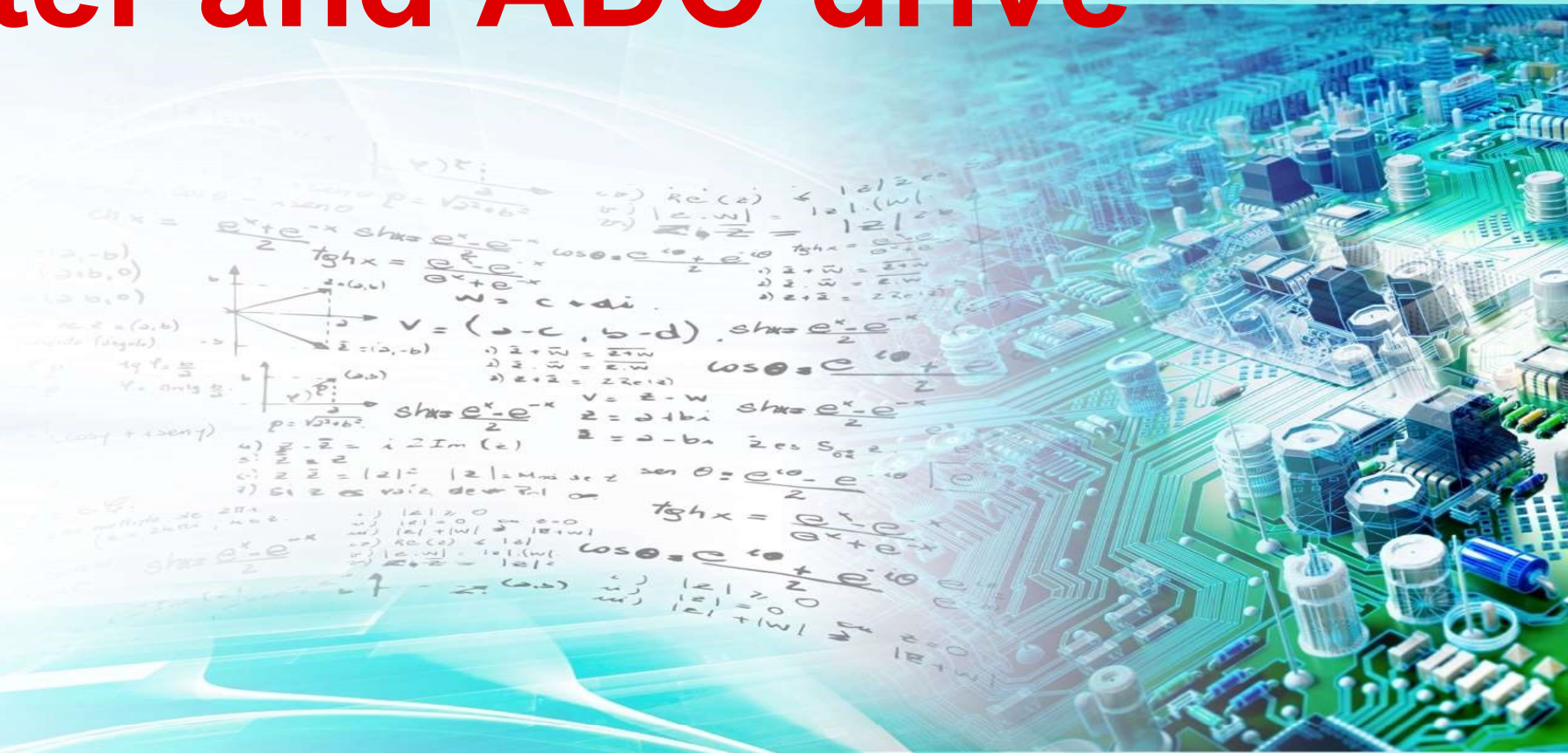
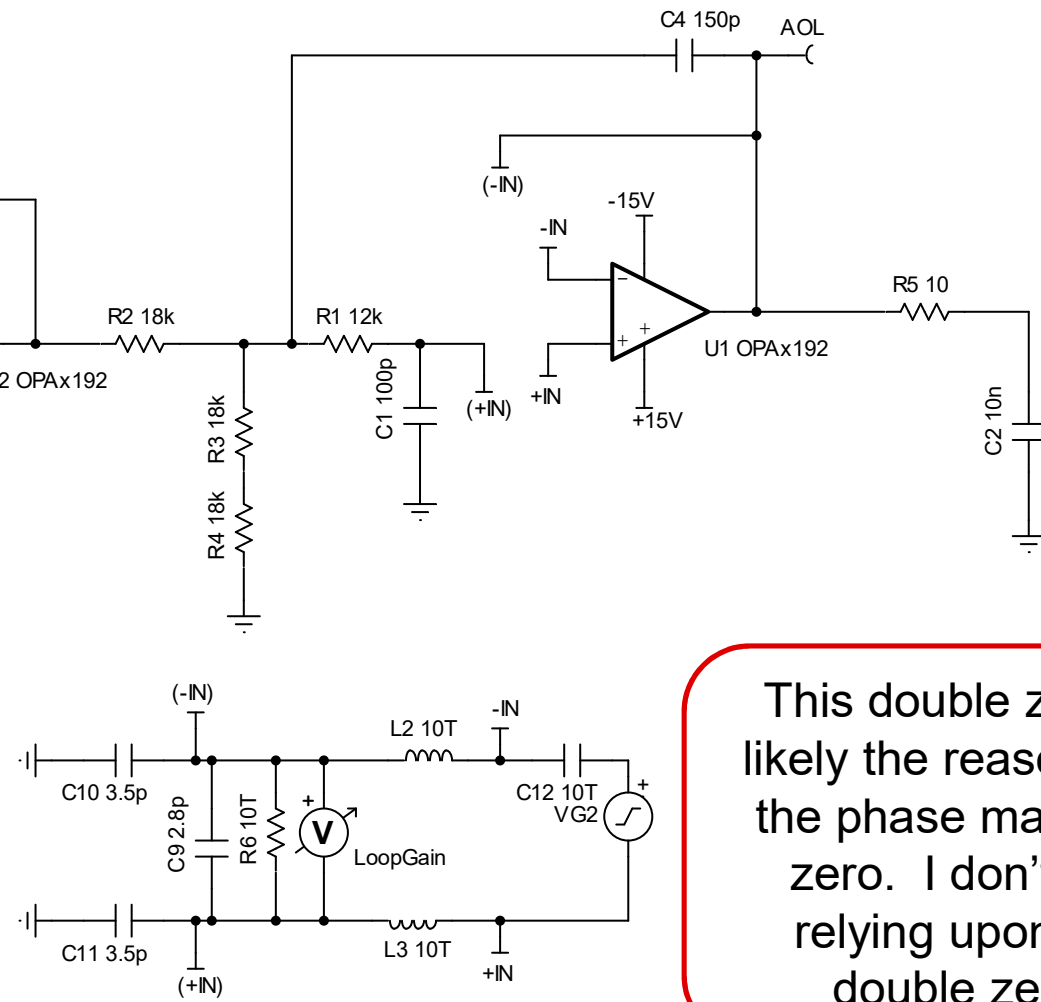


Low pass filter and ADC drive

new values

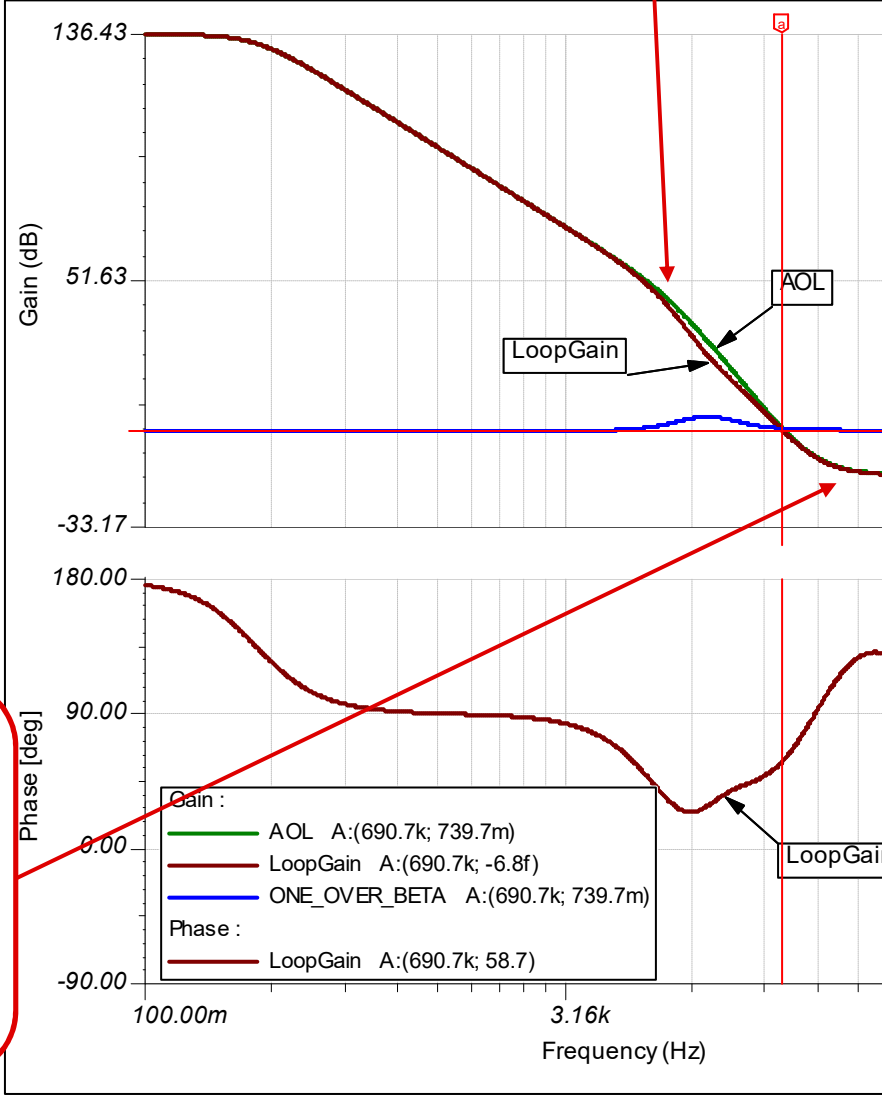


nal circuit

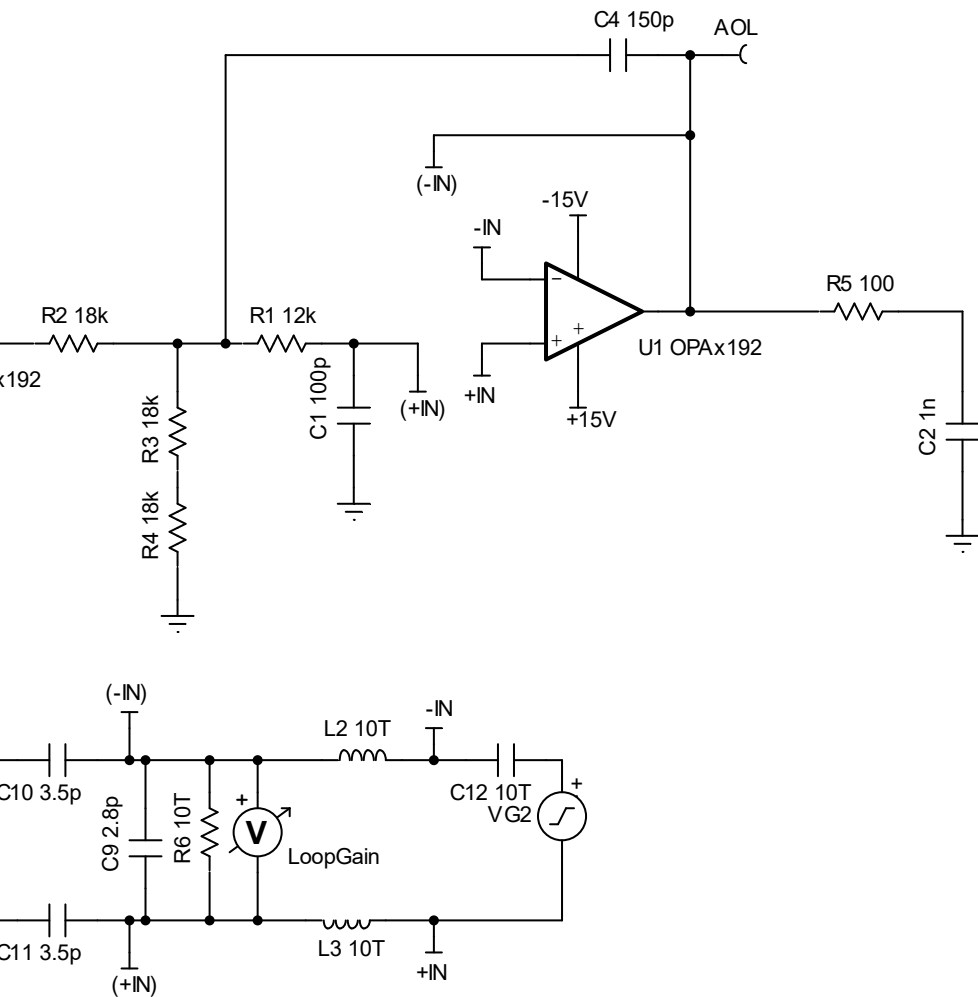


This double zero is likely the reason why the phase margin is zero. I don't like relying upon the double zero.

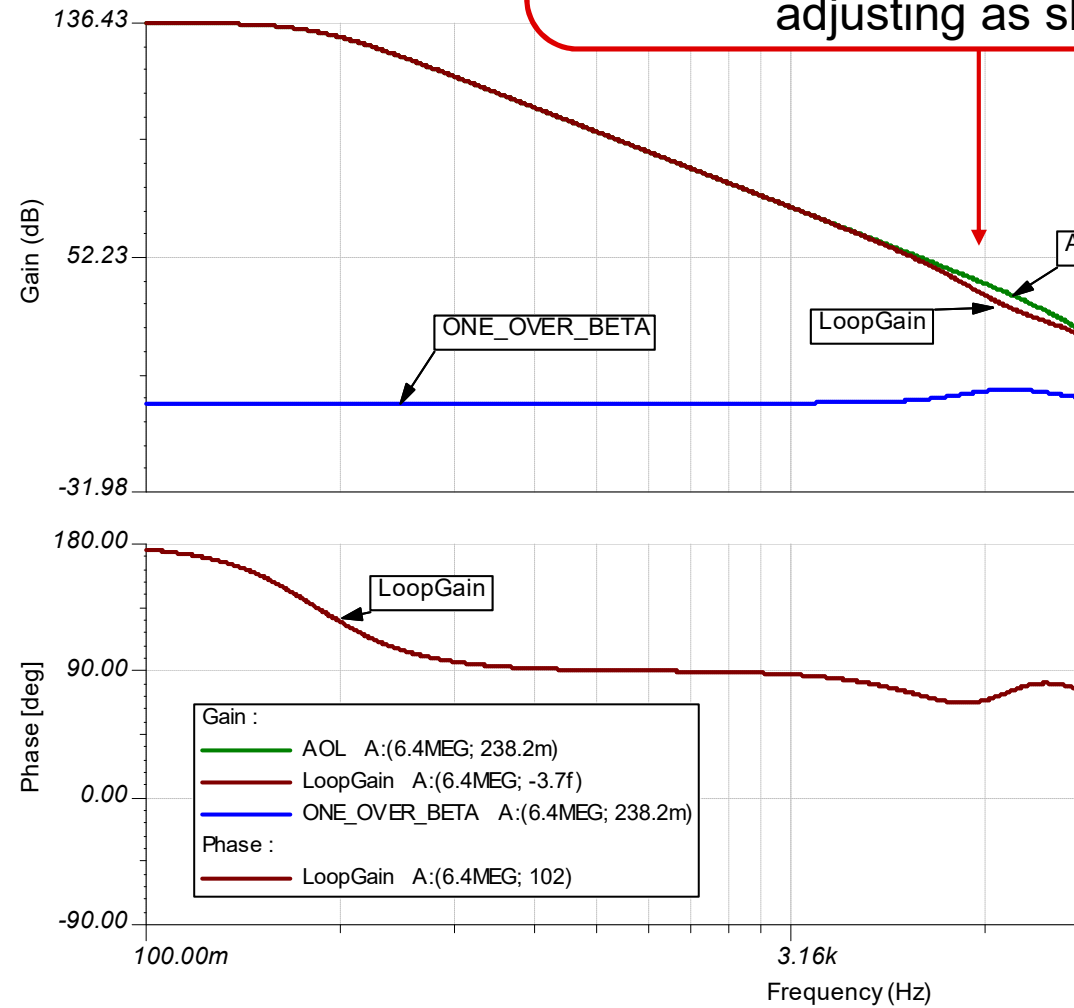
The phase margin is 58.7. However, this second pole makes the rate of closure 40. This condition normally makes the circuit unstable.



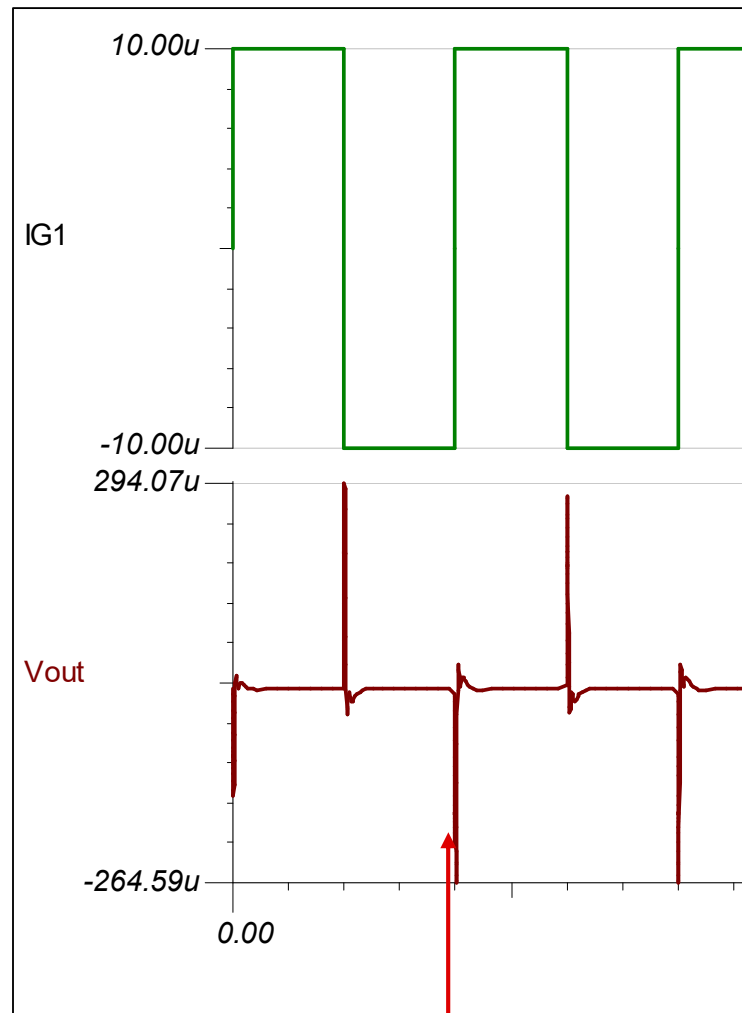
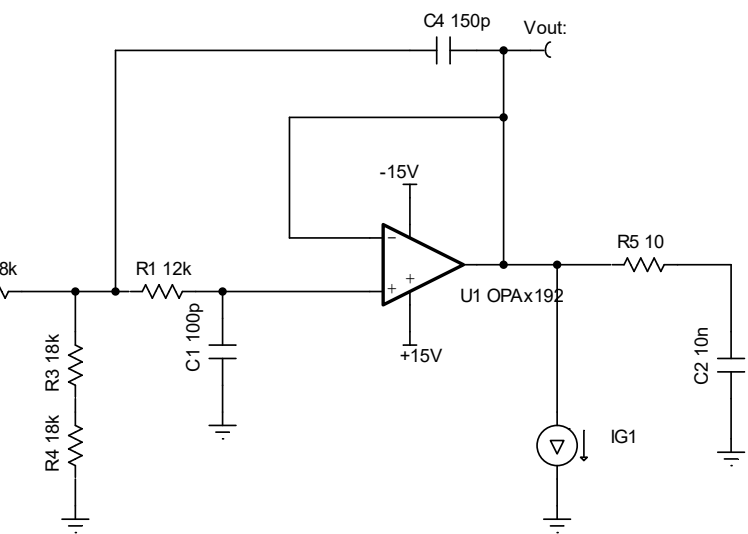
Output filter



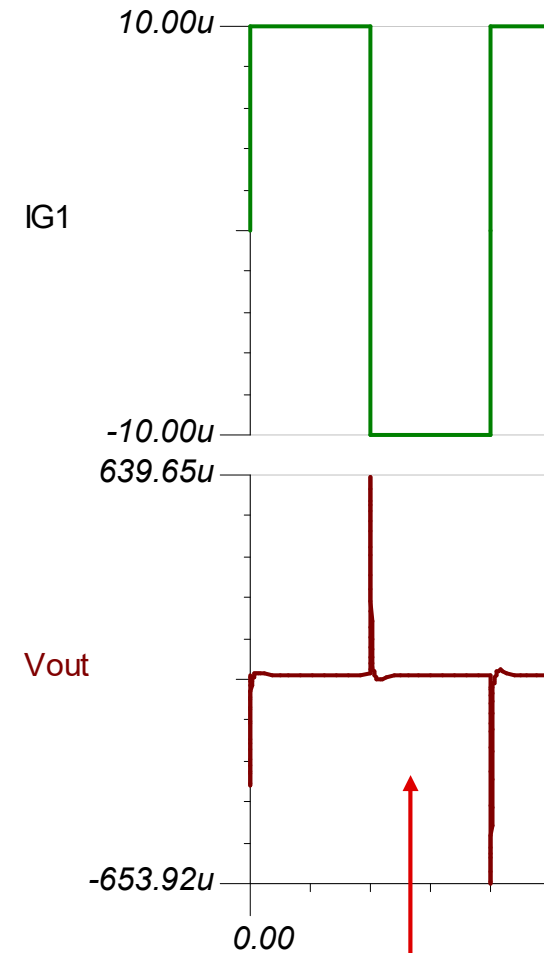
Adjusting the filter eli
40dB/decade rate of c
though the previous ve
good phase margin I w
adjusting as s



ient test

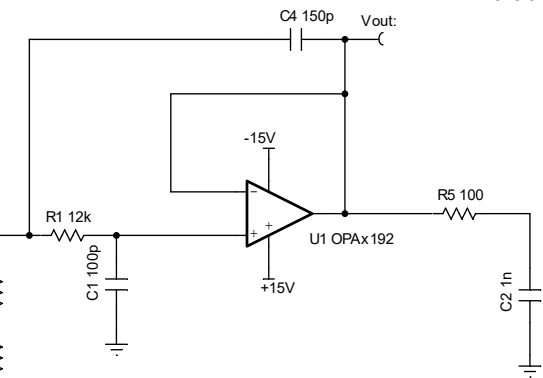
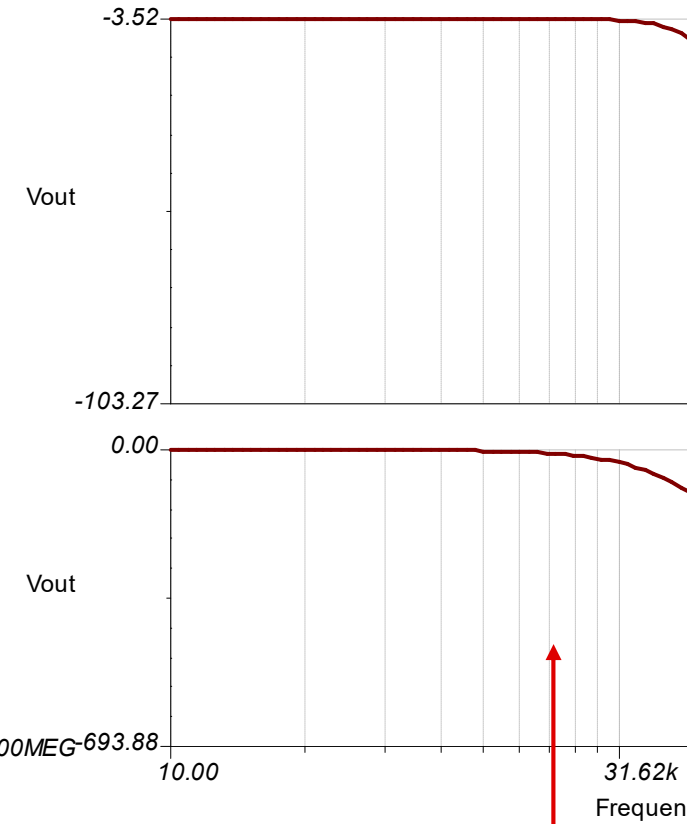
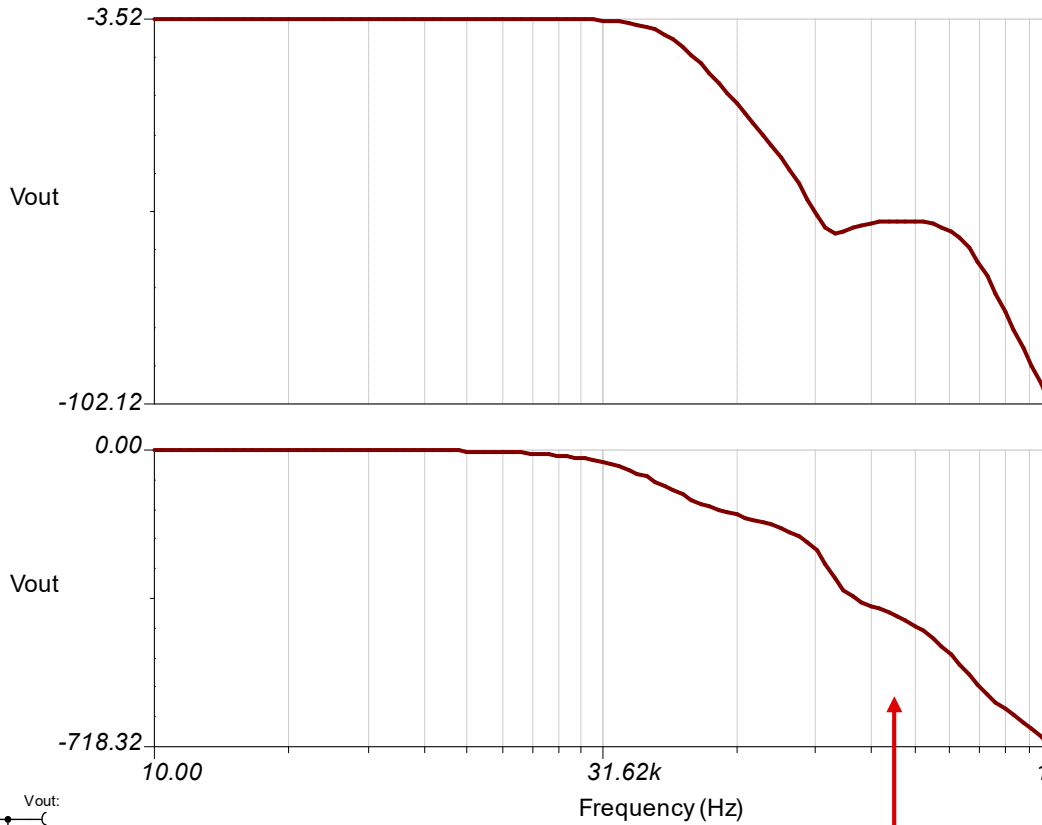


10 x 10nF filter



100 x 1nF filter

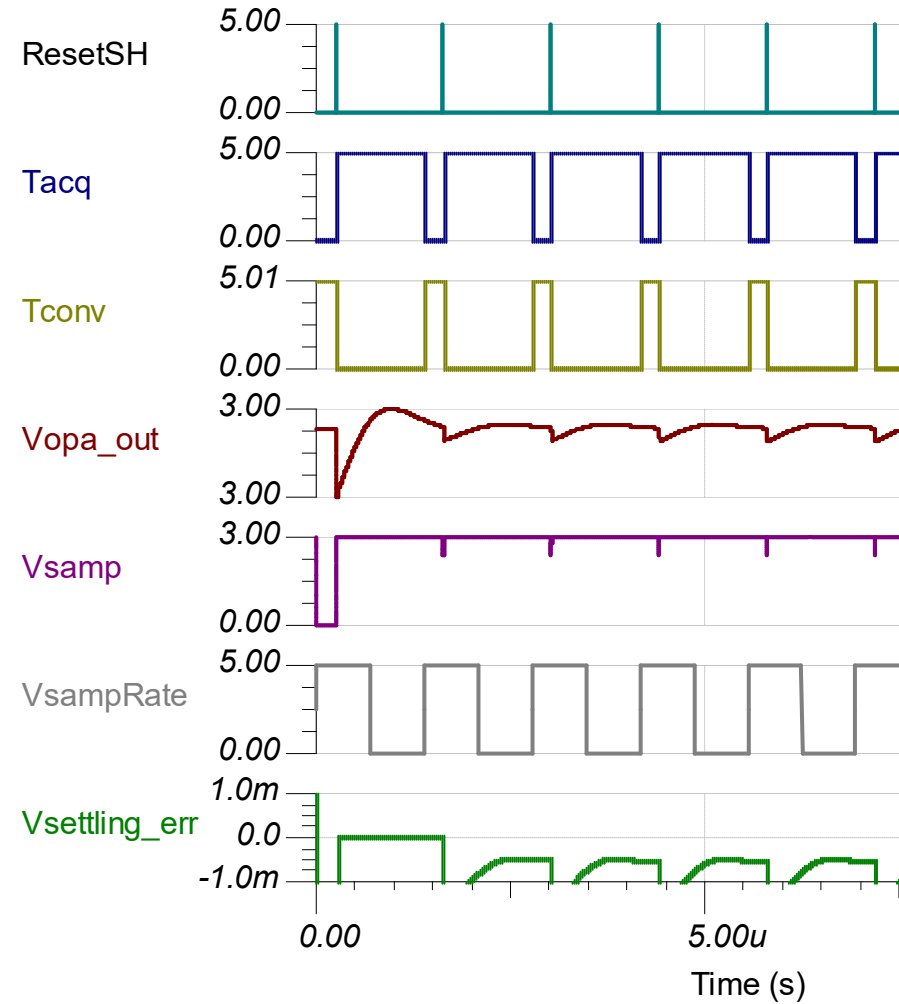
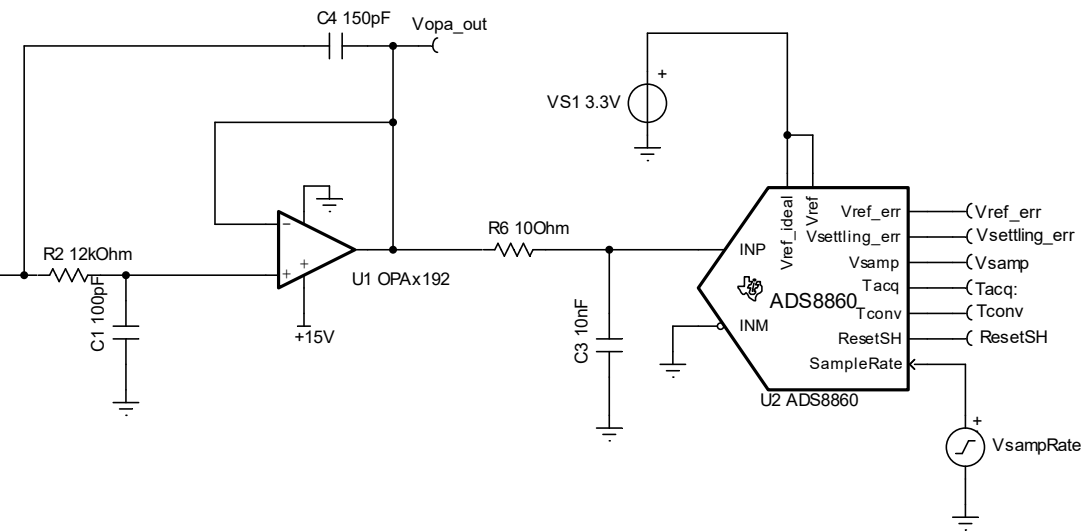
Breaking test



10 x 10nF filter

100 x 1nF filter

drive – original filter 10 x 10n



drive – new filter 10 x 10n

