TI Designs

Reference Design for Reinforced Isolation Three-Phase Inverter With Current, Voltage, and Temp Protection

TEXAS INSTRUMENTS

Design Overview

This design provides a reference solution for a three-phase inverter rated up to 10 kW, designed using reinforced isolated dual IGBT gate driver UCC21520, reinforced isolated amplifier AMC1301, and MCU TMS320F28027. Lower system cost is achieved by using the AMC1301 to measure motor current interfaced with internal ADC of MCU and use of bootstrap power supply for IGBT gate drivers. The inverter is designed to have protection against overload, short circuit, ground fault, DC bus undervoltage and overvoltage, and IGBT module over temperature.

Design Resources

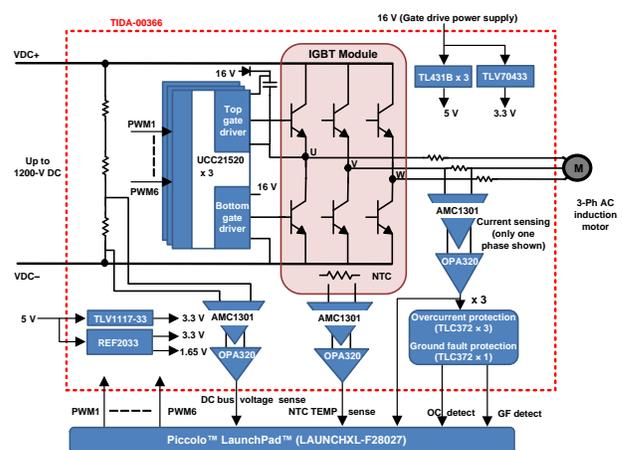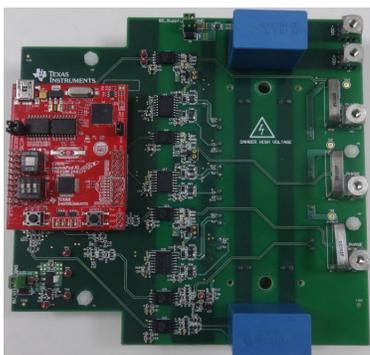|	
TIDA-00366	Design Folder
UCC21520	Product Folder
AMC1301	Product Folder
OPA320	Product Folder
TLC372	Product Folder
TLV1117-33	Product Folder
TLV70433	Product Folder
REF2033	Product Folder
TL431B	Product Folder
SN74LVC1G10	Product Folder
LAUNCHXL-F28027	Tools Folder
TIDA-00195	Tools Folder

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Design Features

- Reinforced Isolated Inverter Suited for 200-V to 690-V AC Drives Rated up to 10 kW
- Simple Yet Effective Gate Driver With 4-A Source, 6-A Sink Output Current Capability
- 250-kHz Isolated Amplifier for Inverter Current, DC Bus Voltage and IGBT Module Temperature Measurement; Enables Use of Internal ADC of MCU
- Calibrated Current Measurement Accuracy of ±0.5% Across Temperature Range From –25°C to 85°C
- Protection Against DC Bus Undervoltage, Overvoltage, Overload, Ground Fault, and Over-Temperature
- Bootstrap Based Power Supply for High-Side Gate Driver Reduces Overall Cost for Power Supply Requirements
- 19-ns (Typical) Propagation Delay Optimizes Dead Band Distortion

Featured Applications

- Variable Speed AC Drives
- Three-Phase UPS
- Industrial Power Supplies
- Solar Inverters

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Reference Design for Reinforced Isolation Three-Phase Inverter With Current, Voltage, and Temp Protection

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1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION
DC bus input voltage	400 to 1200 V
Gate driver supply voltage	16 V for low-side IGBT gate-driver, 15 V (bootstrapped) for high-side IGBT gate-driver
IGBT power module	Voltage rating: 1200 V Current rating: 50 A or more
Rated power capacity	10 kW
Inverter switching frequency	15 kHz (default); adjustable through software
Isolation	Reinforced (IEC61800-5)
Microcontroller	TMS320F28027
Operating ambient temperature	−25°C to 85°C
Motor	Three-phase 400-V AC induction motor
Power supply specification for MCU	3.3 V ± 5%
Feedbacks	Current sensing, DC link bus voltage sensing, IGBT module temperature sensing
Protections	Overload, overvoltage, undervoltage, ground-fault, over-temperature
PCB	160 × 156 mm, 4 layers, 2-oz. copper

2   System Description

Insulated gate bipolar transistors (IGBTs) are mostly used in three-phase inverters that have numerous applications like variable-frequency drives that control the speed of AC motors, uninterruptible power supply, solar inverters, and other similar inverter applications. IGBTs have advantages such as high input impedance as the gate is insulated, a rapid response ability, good thermal stability, simple driving circuit, good ability to withstand high voltage, snubber-less operation, and controllability of switching behavior to provide reliable short-circuit protection. The IGBT is a voltage-controlled device, which gives it the ability to turn on and off very quickly.

A typical application of a three-phase inverter using six isolated gate drivers is shown in Figure 1. Note that each phase uses a high-side and a low-side IGBT switch to apply positive and negative high-voltage DC pulses to the motor coils in an alternating mode. The output voltage to the motor is controlled by pulse width modulation (PWM). The output voltage is an average of the peak or maximum voltage and the amount of time the transistor is turned on or off.
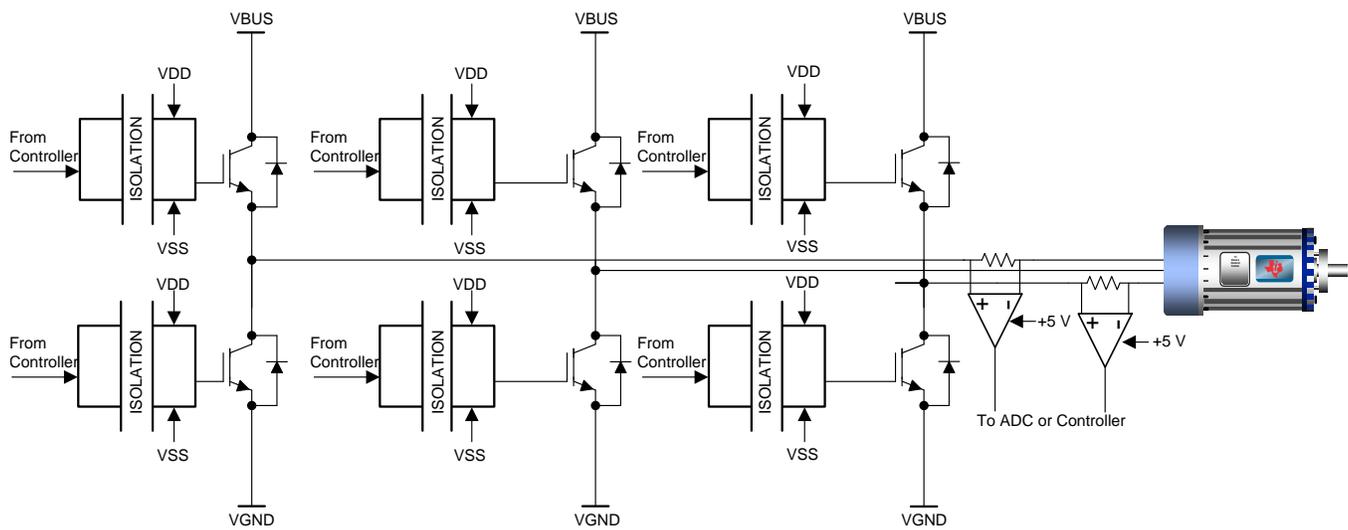
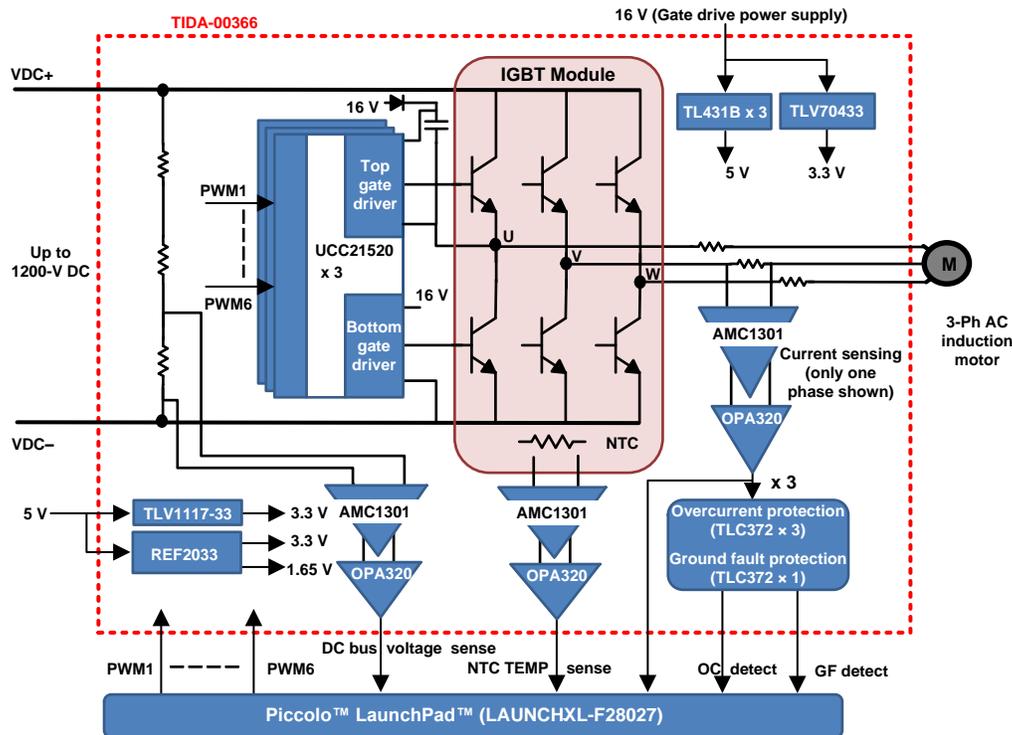Copyright © 2016, Texas Instruments Incorporated

Figure 1. Three-Phase Inverter With Isolated Gate Drive

Apart from isolated gate-drivers for IGBTs, the three-phase inverters include DC bus voltage sensing, inverter current sensing, IGBT protection (like over-temperature, overload, ground fault, and so on).

There are many end applications such as HVAC, solar pumps, and appliances where cost is major concern without compromising the performance. High-end three-phase inverters use $\Sigma\Delta$ modulators for current sensing, which also asks for using expensive controllers with built-in SINC filters. Using an isolated amplifier enables interfacing with low-cost M4 core MCU or TI's Piccolo with a built-in SAR analog-to-digital converter (ADC). The overload protection can be implemented in external hardware, which reduces software complexity. The isolated gate drivers need different supplies for both high-side and low-side gate drivers. Instead of using expensive isolated supplies for powering the gate drivers, using a bootstrap power supply reduces BOM cost on the power supply and also reduces the board space.

3 Block Diagram

Figure 2 shows the system level block diagram for the TIDA-00366.

Figure 2. System Level Block Diagram for TIDA-00366

This design provides a reference solution for a three-phase inverter rated up to 10 kW. As shown in Figure 2, the design uses three reinforced isolated dual IGBT gate drivers (UCC21520) to drive six IGBTs. The IGBTs are integrated into a module along with a temperature sensor (NTC). The IGBTs inside the module are configured in half-bridge configurations. Each half-bridge is driven by two IGBT gate-drivers—top (high-side) and bottom (low-side). The design is interfaced with TI's Piccolo LaunchPad, LAUNCHXL-F28027 through two 20-pin connectors. The complementary PWM signals are generated from the LaunchPad. The three mid-points of IGBT half-bridges are connected to motor terminals. The board is designed to operate up to 1200-V DC for the inverter DC bus voltage.

Accurate phase current sensing with three-phase brushless motors is critical for motor drive performance, efficiency, and protection. This design uses in-phase current sensing using three 5-mΩ shunts and three reinforced isolated amplifiers (AMC1301). The benefits of using in-phase current sensing are:

1. constant motor current flowing through the shunt, independent of IGBT switching, and
2. easy detection of terminal-to-terminal short and terminal to GND short.

The voltage generated across the shunt is amplified using the reinforced isolated amplifier AMC1301. The output of the AMC1301 is signal conditioned and converted to a single-ended signal using the OPA320. Outputs of all the three channels are fed into microcontroller (MCU).

The inverter is designed to protect against overload, short circuit, ground fault, DC bus undervoltage and overvoltage, and IGBT module over-temperature. The DC bus voltage is dropped down using the resistor divider and fed to one more AMC1301 for sensing. The under- and overvoltage are programmed in the MCU using the sensed signal. Similarly, the signal from NTC (integrated into IGBT module) is sensed using the AMC1301, and the sensed signal is fed to the MCU for over-temperature protection. The overload, short-circuit, and ground fault protections are implemented using comparators TLC372, which use the current sensed from the three shunts.

The board is powered through two external power supplies: one 16 V and the other 5 V. The low-side IGBT gate-drivers are powered using 16 V, and high-side IGBT gate-drivers are powered using a bootstrapped supply generated from 16 V. The MCU, op amps, and comparators are powered using 3.3 V generated from a 5-V supply using the TLV1117-33. The design uses the TLV70433, TL431B, and REF2033 to generate other rails and references on the board.

Lower system cost is achieved by using the AMC1301 to measure motor current interfaced with an internal ADC of the MCU and using the bootstrap power supply for IGBT gate drivers.

3.1 Highlighted Products

3.1.1 UCC21520

The UCC21520 is an isolated dual-channel gate driver with a 4-A source and a 6-A sink peak current. It is designed to drive power MOSFETs, IGBTs, and SiC MOSFETs up to 5 MHz with a best-in-class propagation delay and pulse-width distortion. The input side is isolated from the two output drivers by a 5.7-kV$_{RMS}$ reinforced isolation barrier, with a minimum of 100-V/ns common-mode transient immunity (CMTI). Internal functional isolation between the two secondary-side drivers allows a working voltage of up to 1500-V DC. A disable pin shuts down both outputs simultaneously when it is set high and allows normal operation when left floating or grounded. The device accepts VDD supply voltages up to 25 V. A wide input VCCI range from 3 to 18 V makes the driver suitable for interfacing with both analog and digital controllers.

3.1.2 AMC1301

The AMC1301 is a precision isolation amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. The input of the AMC1301 is optimized for direct connection to shunt resistors or other low voltage level signal sources. The excellent performance of the device supports accurate current control resulting in system level power saving and, especially in motor control applications, lower torque ripple.

3.1.3 OPA320

The OPA320 is precision, low-power, single-supply op amp optimized for very low noise. Operated from a voltage range from 1.8 to 5.5 V, the device is well-suited for driving ADCs. With a typical offset voltage of 40 µV and very low drift over temperature (1.5 µV/°C typical), it is very well suited for applications like control loop and current sensing in motor control.

3.1.4 TLC372 (Q-Version)

The TLC372 consists of two independent voltage comparators, each designed to operate from a single power supply (3- to 16-V range). The outputs are open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The TLC372Q is characterized for operation from –40°C to 125°C. The typical response time of comparators for the switching is 200 ns.

3.1.5 TLV1117-33 (I-Version)

The TLV1117 is a positive low-dropout voltage regulator designed to provide up to 800 mA of output current. The internal circuitry is designed to operate down to 1-V input-to-output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA, decreasing at lower load currents. With excellent line and load regulations, the device is available in multiple packages and works for a temperature range from –40°C to 125°C.

3.1.6 TLV70433

The TLV70433 is a 3.3-V LDO with ultralow quiescent current and operates over a wide operating input voltage of 2.5 to 24 V. The device is an excellent choice for industrial applications that undergo large line transients. The TLV70433 is available in a 3-mm×3-mm SOT23-5 package, which is ideal for cost-effective board manufacturing.

3.1.7 REF2033

The REF2033 offers excellent temperature drift (8 ppm/°C, max) and initial accuracy (0.05%) on both the V_{REF} and V_{BIAS} outputs while operating at a quiescent current less than 430 μA. In addition, the V_{REF} and V_{BIAS} outputs track each other with a precision of 6 ppm/°C (max) across the temperature range of –40°C to 85°C. All these features increase the precision of the signal chain and decrease board space, while reducing the cost of the system as compared to a discrete solution. Extremely low dropout voltage of only 10 mV allows operation from very low input voltages.

3.1.8 TL431B (Q-Version)

The TL431 is a three-terminal adjustable shunt regulator with specified ranges for thermal stability over temperature. The output voltage can be set to any value between V_{REF} (approximately 2.5 V) and 36 V, with two external resistors. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications. The "B-grade" version comes with initial tolerances (at 25°C) of 0.5% and TL431BQ devices are characterized for operation from –40°C to 125°C.

3.1.9 SN74LVC1G10

The SN74LVC1G10 performs the Boolean function $Y = !(A \times B \times C)$ or $Y = !A + !B + !C$ in positive logic. With a supply range from 1.65 to 5.5 V and availability in multiple packages, this NAND gate is characterized for operation from –40°C to 125°C.

4   System Design Theory

4.1   DC Bus Voltage Input

The TIDA-00366 is designed to operate for a DC bus voltage up to 1200 V. The DC bus voltage can be applied to the TIDA-00366 at terminals J9 (VDC+) and J8 (VDC−). To keep the board compact and cost optimized, the bulk capacitors are not provided on the board. Most of the ripple current is expected to be sourced from external capacitors. Nevertheless, two polyester capacitors (C111 and C112 with value of 3 μF/1300 V each) are used across the DC bus to suppress high frequency noise as shown in Figure 3.

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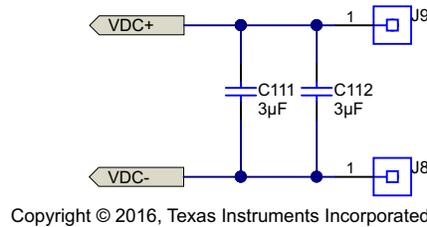
Figure 3. DC Input

4.1.1   Bleeder Resistors

As shown in Figure 4, a series combination of five 100-kΩ resistors is connected across the DC bus terminals. The purpose of these bleeder resistors is to discharge the electric charge stored in the filter capacitors when the DC bus voltage is turned off for safety reasons. It eliminates the possibility of a leftover charge causing electric shock. The total current taken by these bleeder resistor when DC bus voltage is connected is 1200 V/500 kΩ = 2.4 mA.

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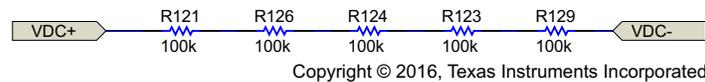
Figure 4. Bleeder Resistors

4.2   Inverter Stage

The three-phase inverter is designed to operate from the DC bus voltage up to 1200 V. This design uses an IGBT module instead of discrete IGBTs.

4.2.1   IGBT Module

This reference design is intended to support various makes of IGBT modules so a commonly used footprint of IGBT module is selected. The power stage is designed to deliver up to 10 kW. The power stage is supplied with 800-V DC replicating high DC bus voltage during regeneration. Considering the safety factor and switching spikes, IGBTs were selected with the voltage rating equal to 1200 V. The current rating of the IGBT depends on the peak winding current. The three-phase inverter bridge is switched such that the sinusoidal current is injected into the motor windings.

- Motor rating (P_{OUT}) = 10 kW
- Line-to-line voltage (V_{LL}) = 415-V AC
- Power factor considered = 0.9
- Typical motor efficiency η_{MOTOR} = 85%

The current through the winding is calculated using Equation 1.

$$I_{LL(RMS)} = \frac{P_{OUT}}{\eta_{MOTOR} \times V_{LL} \times \sqrt{3} \times \cos\Phi} = \frac{10 \text{ kW}}{0.85 \times 415 \times \sqrt{3} \times 0.9} = 18.18 \text{ A}_{RMS}$$

(1)

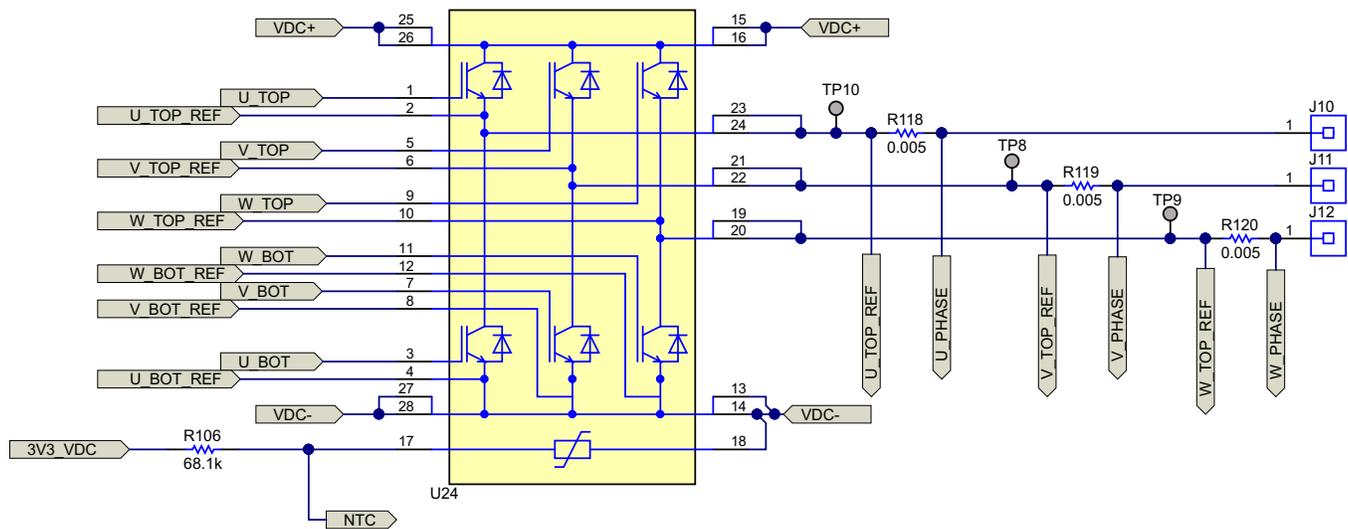The peak value of the winding current is calculated in Equation 2.

$$\sqrt{2} \times I_{LL(RMS)} = \sqrt{2} \times 18.18 = 25.7 \ A_{PEAK}$$

(2)

Considering an overloading of 200%, the peak winding current would be ~51 A. For this reference design, the following IGBT module is used. It has a continuous collector current carrying capacity of 75 A at TC = 25°C and a peak current capacity of 100 A.

The selection of IGBT module with a built-in NTC Thermistor is preferred to avoid thermal breakdown of the IGBT. This IGBT temperature rise information is routed to the MCU to take necessary action.

Figure 5 shows the connections for IGBT module and shunts connected in-phase for current sensing.

Note that the design uses the MG1250H-XN2MM (from Littlefuse Inc.). Other modules with the same layout footprint and similar specifications can also be used.

Figure 5. IGBT Module Connections

Figure 6 shows the grounding scheme used in the design. The reference points (U_BOT_REF, V_BOT_REF, and W_BOT_REF) are connected together to VDC- through 0-Ω resistors R132, R133, and R134, respectively. They are also connected with the GND1 (ground for a 16-V gate-drive power supply) through one more 0-Ω resistor R135. The placements of these shorting links are important in the layout. Figure 86 and Figure 87 show the placements in the layout.
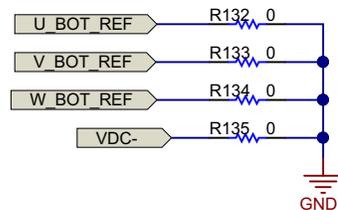
Figure 6. Grounding Scheme

4.3 Isolated IGBT Gate Driver

> **NOTE:** The TIDA-00366 is designed for a three-phase inverter, but this section explains the circuits and components for one channel (U-Phase) only. The same explanation is applicable to two other channels (V-Phase and W-Phase).

A three-phase inverter application uses six power switches (IGBTs in this case). To drive these switches, six totally independent gate drivers are required. Also, with a high-voltage operation, it is necessary to have enough isolation between primary and secondary side of the gate-driver. The UCC21520 is an isolated dual-channel gate driver with a 4-A source and a 6-A sink peak current. It is designed to drive power MOSFETs, IGBTs, and SiC MOSFETs up to 5 MHz with best-in-class propagation delay and pulse width distortion. The input side is isolated from the two output drivers by a 5.7-kV$_{RMS}$ reinforced isolation barrier, with a minimum of 100-V/ns CMTI. Internal functional isolation between the two secondary-side drivers allows a working voltage of up to 1500-V DC. The internal structure of the UCC21520 is shown in Figure 7.
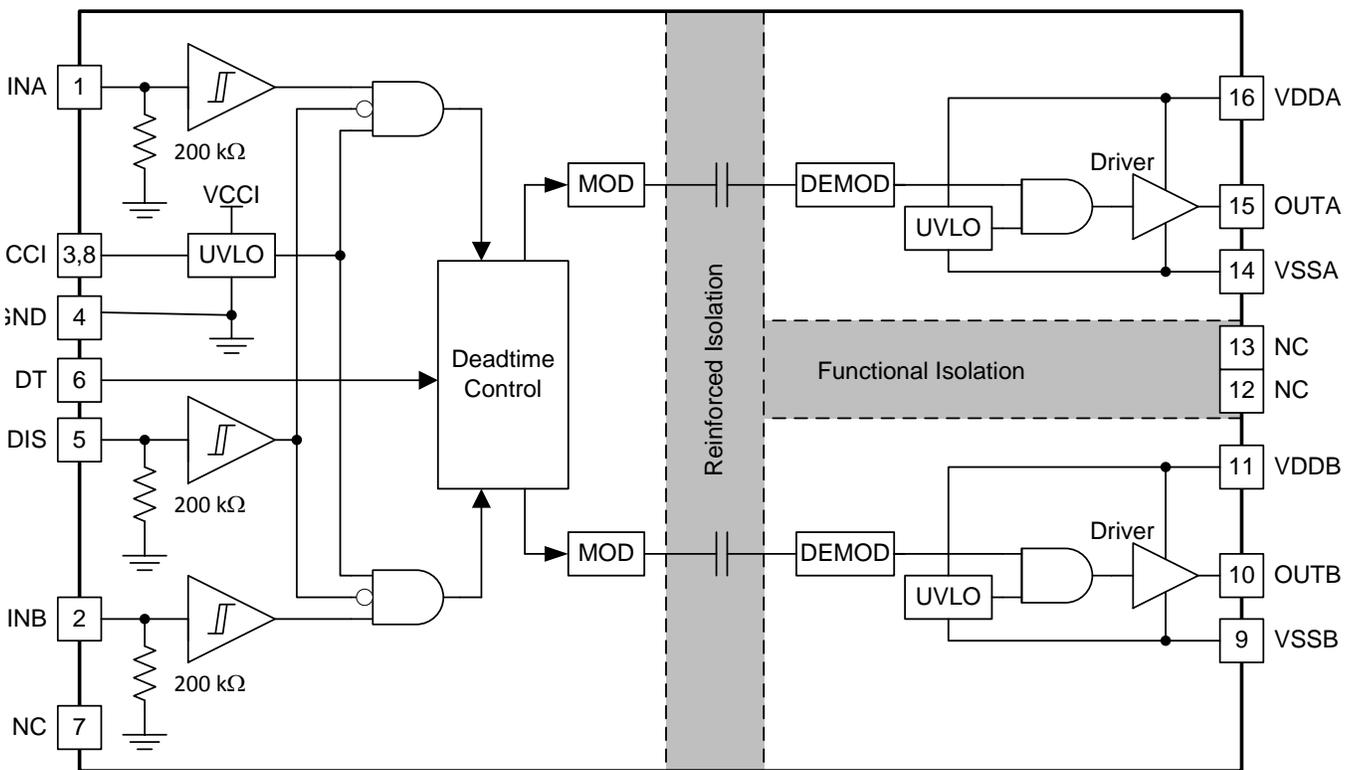
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Figure 7. Functional Block Diagram of UCC21520

This driver can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver with programmable dead time (DT). A disable pin shuts down both outputs simultaneously when it is set high and allows normal operation when left floating or grounded. As a fail-safe measure, primary-side logic failures force both outputs low. The device accepts VDD supply voltages up to 25 V. A wide input VCCI range from 3 to 18 V makes the driver suitable for interfacing with both analog and digital controllers. All the supply voltage pins have undervoltage lockout (UVLO) protection. With all these advanced features, the UCC21520 enables high efficiency, high power density, and robustness in a wide variety of power applications. Figure 8 shows the circuit for the UCC21520 and associated components implemented for half-bridge configuration for a three-phase inverter.

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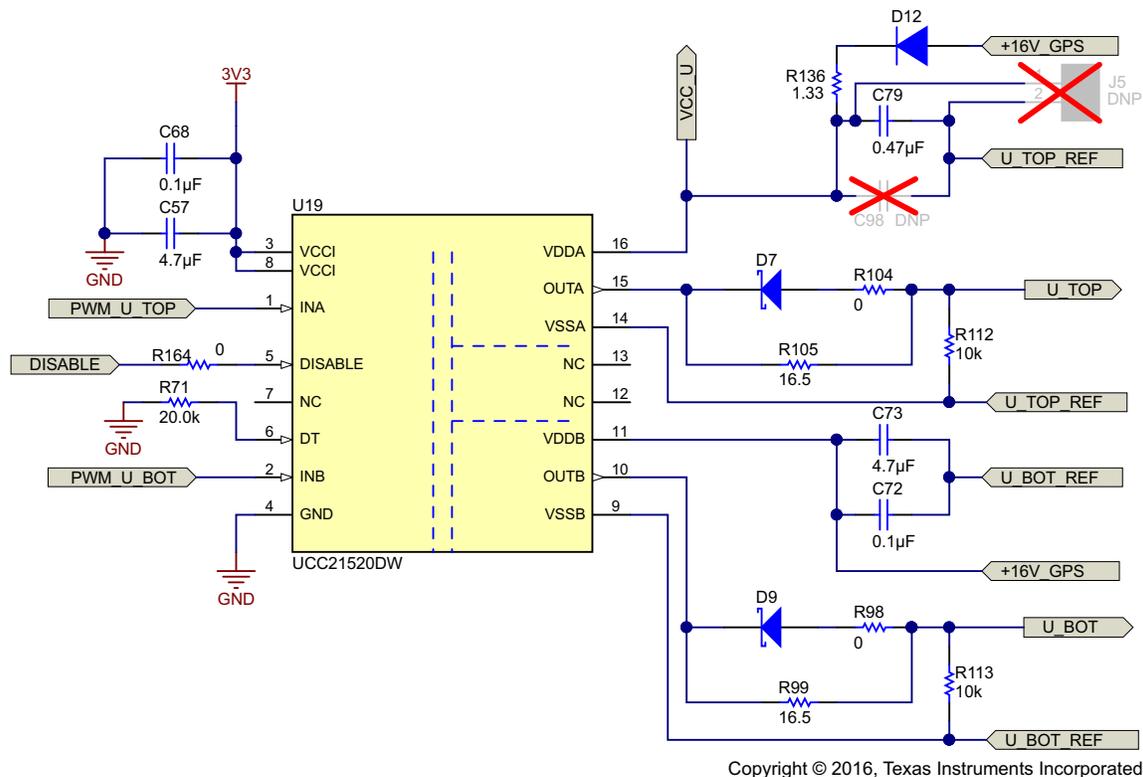
Figure 8. Gate Driver UCC21520 and Related Components and Circuits

4.3.1   Control Supply for Primary Side

VCCI pins (Pin 3 and Pin 8) are supplied with 3.3 V generated using the TLV1117-33 (as explained in Section 4.11.1). C57 (4.7 μF) and C68 (0.1 μF) are used as local decoupling capacitors for VCCI pins.

4.3.2   PWM Inputs

The PWM signals "PWM_U_TOP" and "PWM_U_BOT" are generated from LaunchPad with a dead time of 1.4 μs.

4.3.3 Dead Time Control

The UCC21520 has a programmable dead time function using the DT pin. Tying DT to VCCI allows the outputs to overlap. Leaving DT floating sets the dead time to <15 ns. Placing a 500-Ω to 500-kΩ resistor between DT and GND adjusts dead time according to Equation 3.

$$DT\left(in\ ns\right) = 10 \times R_{DT}\left(in\ k\Omega\right)$$

(3)

A 20-kΩ resistor is connected between DT pin and GND pin sets the dead time to 200 ns as per Equation 3. This resistor must be selected for 1% tolerance to prevent any drift in the dead time. For the TIDA-00366, the dead time is controlled using MCU.

4.3.4 DISABLE Signal for Gate Drivers

The DISBALE pin is used to disable the gate drivers. It disables both driver outputs if asserted high and enables if set low or left open. This pin is pulled low internally if left open or floating. Tie this pin to ground if it is not used to achieve better noise immunity. For the TIDA-00366, the DISABLE pin is generated using a three-input NAND gate as explained in Section 4.9.

4.3.5 Supply for Low-Side Gate Drivers

The low-side gate drivers for all three channels are powered using 16V_GPS, which is supplied externally from connector J4 as shown in Figure 9. Diode D8 is used for reverse-polarity protection for this supply and C93 (10 μF) is used as decoupling capacitor for the same. R111 is used as shorting link for connecting the GND1 (ground for 16V_GPS) and VDC−. The placement of this shorting link in layout is shown in Figure 89.
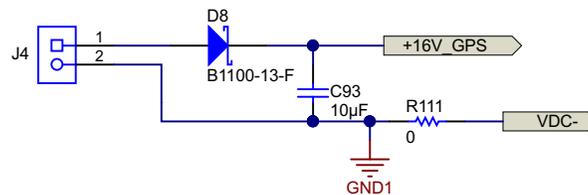
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Figure 9. Gate Driver Power Supply

As shown in Figure 8, VDDB is secondary-side power for driver B. It is supplied with 16V_GPS and locally decoupled to VSSB using low ESR/ESL capacitors C72 (0.1 μF) and C73 (4.7 μF) located as close to the device as possible. VSSB is ground for secondary-side driver B and ground reference for secondary side B channel.

4.3.6 Bootstrap Power Supply for High-Side Gate Drivers

One of the most widely used methods to supply power to the high-side drive circuitry of a gate driver IC is the bootstrap power supply. The bootstrap power supply consists of a bootstrap diode and a bootstrap capacitor (with an optional series resistor). This method has the advantage of being both simple and low cost. The maximum voltage that the bootstrap capacitor (V_{BS}) can reach is dependent on the elements of the bootstrap circuit. Consider the voltage drop across R_{BOOT}, V_F of the bootstrap diode, and the drop across the low-side switch ($V_{CE(ON)}$ or V_{FP}, depending on the direction of current flow through the switch).

4.3.6.1 Selection of Bootstrap Capacitor (C_BOOT)

The bootstrap capacitor must be sized to have more than enough energy to drive the gate of the IGBT high without depleting the bootstrap capacitor more than 10%. A good guideline is to size C_{BOOT} to be at least ten times as large as the equivalent IGBT gate capacitance (C_g). C_g must be calculated based on the voltage driving the high-side gate of the IGBT (V_{GE}) and the gate charge of the IGBT (Q_g). V_{GE} is approximately the bias voltage supplied to VDD after subtracting the forward voltage drop of the bootstrap diode D12 (V_{DBOOT}). In this design example, the estimated V_{GE} is approximately V, as Equation 4 shows.

$$V_{GE} \approx V_{DD} - V_{DBOOT} = 16\ V - 1\ V = 15\ V$$

(4)

The IGBT module in this reference design has a specified Q_g of 0.47 µC. The equivalent gate capacitance of the IGBT can be calculated as Equation 5 shows.

$$C_g = \frac{Q_g}{V_{GE}} = \frac{0.47\ \mu C}{15} = 0.0313\ \mu F \tag{5}$$

After estimating the value for C_g, C_{BOOT} must be sized to at least ten times larger than C_g, as Equation 6 shows.

$$C_{BOOT} \geq 10 \times C_g = 10 \times 0.0313\ \mu F = 0.313\ \mu F \tag{6}$$

For this reference design, a 0.47-µF capacitor has been chosen for the bootstrap capacitor.

4.3.6.2 Selection of Bootstrap Diode

The voltage that the bootstrap diode encounters is the same as the full DC bus voltage (in this case a maximum of 1200-V DC). The bootstrap diode voltage rating must be greater than the DC bus rail voltage. The bootstrap diode must be a fast recovery diode to minimize the recovery charge and thereby the charge that feeds from the bootstrap capacitor to the 16-V supply. The diode must be able to carry a pulsed peak current of 11.28 A (as per Equation 11). However, the average current is much smaller and depends on the switching frequency and the gate charge requirement of the high-side IGBT. This TIDA-00366 reference design uses a 1300-V, 1-A, fast recovery diode BYG23T-M3.

The bootstrap diode power dissipation (P_{DBOOT}) can be estimated based on the switching frequency, diode forward voltage drop, and the switching frequency of the PWM signal (f_{SW}). In this reference design, the switching frequency has been set to 15 kHz. Equation 7 calculates the estimated power loss for the bootstrap diode.

$$P_{DBOOT} = \frac{1}{2} \times Q_g \times f_{SW} \times V_{DBOOT} = \frac{1}{2} \times 0.47\ \mu C \times 15\ kHz \times 1\ V = 3.525\ mW \tag{7}$$

4.3.6.3 Selection of Current Limiting Resistor for Bootstrap Diode

Considering that having a 2-V(p-p) ripple on the bootstrap capacitor, the charge on the 0.47-µF capacitor is:

$$Q = C \times V = 0.47\ \mu \times 2 = 0.94\ \mu C \tag{8}$$

For a capacitor charging period of 1.25 µs, the same charge is also represented as Equation 9.

$$Q = 0.94\ \mu C = I_{CH} \times 1.25\ \mu \tag{9}$$

This gives I_{CH} = 0.752 A.

With a voltage drop across diode being 1 V, the R_{BOOT} is calculated as:

$$R_{BOOT} = \frac{V_{DBOOT}}{I_{CH}} = \frac{1}{0.752} = 1.329\ \Omega \tag{10}$$

The TIDA-00366 uses R_{BOOT} value of 1.33 Ω.

With R_{BOOT} = 1.33 Ω, the bootstrap diode current is calculated as Equation 11.

$$I_{DBOOT(pk)} = \frac{V_{DD} - V_{DBOOT}}{R_{BOOT}} = \frac{16 - 1}{1.33} = 11.28\ A \tag{11}$$

The power dissipation capability of the bootstrap resistor is important. The bootstrap resistor must be able to withstand the short period of high power dissipation during the initial charging sequence of the bootstrap capacitor.

4.3.7 Gate Resistors

The gate current and the appropriate power of the voltage supply depend on the operating frequency, bias control voltages, and total gate charge. The total gate charge is published in IGBT datasheets, depending on gate control voltage. The gate charge necessary for switching is very important to establish the switching performance of IGBT. The lower the charge, the lower is the gate-drive current needed for a given switching time. The gate current can be controlled using external gate resistor between driver output and gate of IGBT. The value of the gate resistor determines the peak charge and discharge currents. The most classical way to influence the switching behavior of an IGBT is by selecting the gate resistors. The gate resistors can be different for the on and off switching process. In such cases, the turn-on gate resistor is denominated with R_{Gon} and turning off with $R_{G(off)}$ as shown in Figure 10. The effective values of gate resistors become:

- Effective $R_{G(on)} = R_{Gon}$
- Effective $R_{G(off)} = R_{Gon} \mathbin{/\mkern-5mu/} R_{Goff}$
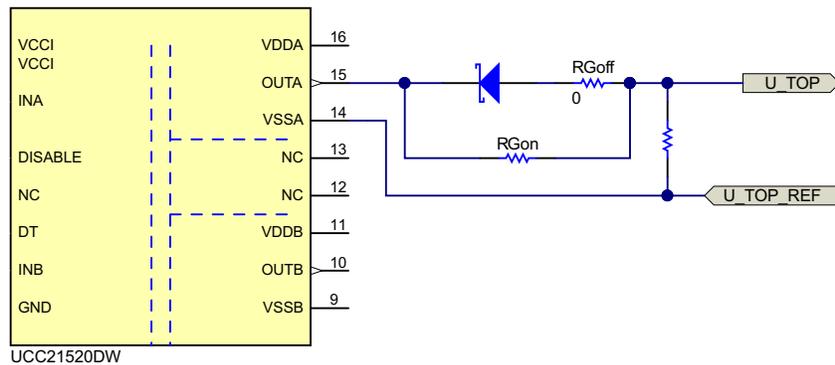
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Figure 10. Gate Resistors

Depending on the gate resistor, both the voltage gradient (dv/dt) as well as the current gradient (di/dt) is modified. The higher the resistance of $R_{G(on)}$, the softer the switching of the IGBT (and correspondingly, the turn-off of the free-wheeling diode). As a consequence, however, the turn-on losses of the IGBT increase (and the recovery losses of free-wheeling diode decrease).

For the TIDA-00366, $R_{G(on)} = 16.5\ \Omega$ and $R_{G(off)} = 0\ \Omega$. With the internal gate resistance of 4 Ω, the gate currents are calculated as:

- Source current = 16 V / (16.5 + 4) Ω = 780 mA
- Sink current = 16 V / 4 Ω = 4 A approximately (considering zero on-resistance of diode)

Another important point to highlight is that Figure 8 shows 10-kΩ resistors across the gate and emitter terminals of the IGBTs. These resistors are a safety precaution and are placed across these nodes to ensure that the IGBTs are not turned on if the UCC21520 is not in place or not properly soldered on the circuit board.

4.4 *Isolated Current Sensing Circuit*

> **NOTE:** The TIDA-00366 is designed for a three-phase inverter, but this section explains the circuits and components for one channel (U-Phase) only. The same explanation is applicable to other two channels (V-Phase and W-Phase).

The current sensing is done using three shunts in-phase with the inverter outputs. Section 4.4.1 explains the selection of shunt value.

4.4.1 Selection of Shunt Resistor for Inverter

As explained in Section 4.2.1, the peak winding current can go up to 51 A. Considering 50 A as the peak current (with some margin), the shunt value can be calculated as given in Equation 12.

$$R_{SHUNT} = \frac{\pm 250 \text{ mV}}{\pm 50 \text{ A}} = 5 \text{ m}\Omega \tag{12}$$

where ±250 mV is the input voltage range for the AMC1301.

4.4.2 Reinforced Isolated Amplifier AMC1301

The AMC1301 is a precision isolation amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. The input of the AMC1301 is optimized for direct connection to shunt resistors. Figure 11 shows the circuit and components related to the AMC1301.

VDD1 is the power supply and GND1 is ground for the hot side of the circuit, where the inputs VINP and VINN are coming directly from the 5-mΩ shunt resistor. VDD1 generation from the bootstrap supply is explained in Section 4.4.2.1. GND1 is connected to "U_TOP_REF" terminal, which is the mid-point of the connection between the top and bottom IGBT of the half-bridge. The capacitors C80 (4.7 μF) and C87 (0.1 μF) are used to decouple the VDD1 supply and must be kept very close to the VDD1 pin of the AMC1301 in the layout. For any noise filtering required by the user, a differential RC filter is provided (R86, R85, and C83). To test the TIDA-00366 no filtering is used so R85 = R86 = 0 Ω and C83 = DNP.

On the cold side, VDD2 is generated from an LDO TLV1117-33 as explained in Section 4.11.1. The capacitors C59 (4.7 μF) and C65 (0.1 μF) are used to decouple the VDD2 supply and must be kept very close to the VDD2 pin of the AMC1301 in the layout. The output of the AMC1301 is available on Pins VOUTP and VOUTN. A differential filter with a cutoff frequency of 95 kHz is connected at the output using R30 (4.7 kΩ), R28 (4.7 kΩ) and C29 (180 pF).
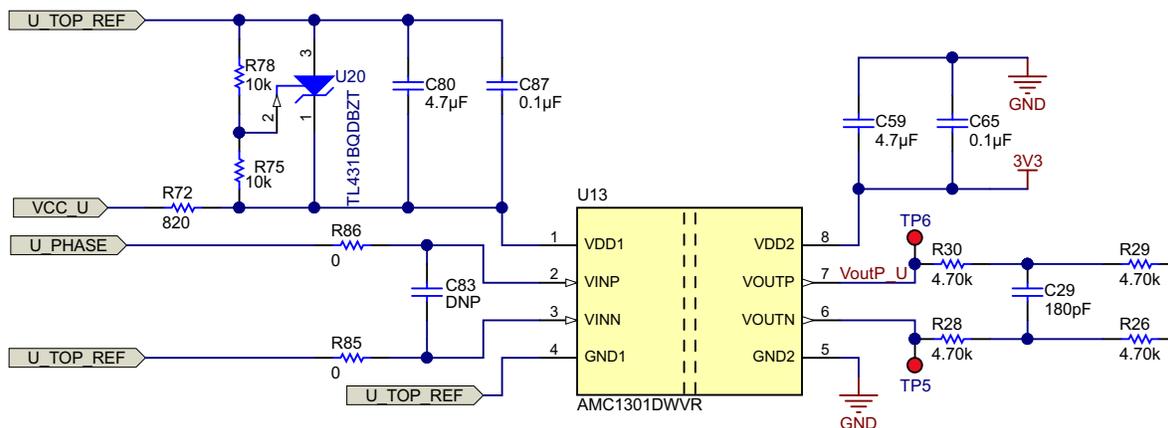
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Figure 11. Reinforced Isolated Amplifier AMC1301

4.4.2.1 Primary-Side Supply Generation Using TL431B

The power supply for a high-side gate-driver is generated using the bootstrap circuit. The reference point for the high-side IGBT gate driver and related circuitry is "U_TOP_REF". The same reference is used for the current sensing circuit, and that is why it is necessary that the power supply for VDD1 for the AMC1301 is also generated from the same bootstrap supply. Figure 12 shows the power supply generation for VDD1 of the AMC1301 using the TL431B shunt regulator. The internal reference value for the TL431B is 2.5 V, which helps decide the output voltage.
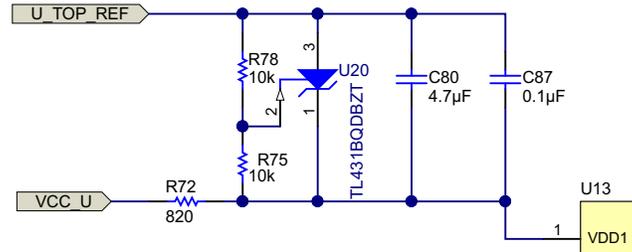
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Figure 12. Power Supply Generation Using TL431B

4.4.3 Differential-to-Single-Ended Conversion Using OPA320

The output of the AMC1301 is differential and has a common-mode voltage of 1.4 V. To interface it with the MCU, the output of the AMC1301 needs to be converted to a single-ended form and must range between 0 to 3.3 V (because of the limitations from the MCU power supply).

4.4.3.1 Selection of Op Amp

The op-amp selection is an integral part of the signal chain for measuring the current, DC link voltage, and IGBT module temperature. For the op amp, consider the following parameters:

- *Offset voltage*: The offset voltage specification for the op amp adds into the overall measurement accuracy, so the lowest offset voltage is preferred for the op amp.
- *Offset voltage drift*: The signal chain accuracy is measured from a temperature range of –25°C to 85°C. The offset voltage drift must be low so as to get lowest error through the specified temperature range. If available, zero drift op-amps are preferred.
- *Rail-to-rail input and output*: The input and output of the op amp must go to both rails so as to use the full range of 1.65 V on both positive and negative cycles (when the output is interfaced with the MCU).
- *Input common-mode range*: The input of op-amp must be able to take a common-mode voltage of VDD/2, which equals 1.65 V for this application.
- *Common-mode rejection ratio (CMRR)*: The switching frequency of typical three-phase industrial inverter goes up to 16 to 20 kHz. The CMRR greater than 80 dB at 100 kHz (approximately five times the switching frequency of inverter) is generally preferred for such applications.

With these specifications, the cost of the op amp should be as low as possible. This design uses the OPA320 with the specifications shown in Table 2.

Table 2. Key Specifications for OPA320

PARAMETER	VALUE
Supply voltage (V)	1.8 to 5.5 V
I_Q/GBW ratio	1. 2 mA/20 MHz 60 µA/MHz
Noise at 1 kHz (nV/rtHz)	8 nV/rtHz
Rail-to-rail	RRIO Input extend ±100-mV beyond rail V_{OUT} to ±10 mV
Zero crossover	Yes
Input bias max (pA)	1 pA max.
Offset voltage (mV)	100 µV, max.
Offset drift	0.5 µV/°C
Packaging	SOT23-5, SOT23-6

Note that five single op amps are used to simplify the component placement in the PCB layout. Using the OPA320 ensures high precision and excellent signal linearity over the entire input common-mode range, making it ideal for driving sampling ADCs.

4.4.3.2 Calculation of Gain for the Amplifier

The AMC1301 datasheet has a "specified linear full-scale range (VINP – VINN)" of –250 to 250 mV. With a nominal gain of 8.2, the V_{OUT} range is –2.05 to 2.05 V. So, $V_{OUT(p-p)}$ for the AMC1301 = 4.10 V.

$V_{OUT(p-p)}$ required from the OPA320 = 3.24 V (the voltage output swing can go up to 30 mV close to both rails). This means the op amp must have a gain of 0.79 as calculated in Equation 13.

$$\text{Op amp gain} = \frac{3.24}{4.10} = 0.79 \text{ V/V}$$

(13)

4.4.3.3   Component Selections

The output of the AMC1301 is filtered using a differential filter (a combination of R30, R28, and C29) with a cutoff frequency of approximately 94 kHz.

The gain for the differential amplifier is calculated in Equation 14.

$$\text{Differential amplifier gain} = \frac{R_F}{R_{IN}} = \frac{7.5 \text{ k}\Omega}{4.7 \text{ k}\Omega + 4.7 \text{ k}\Omega} = 0.7978 \text{ V/V} \tag{14}$$

Figure 13 shows the circuit for the differential amplifier to convert the differential output of the AMC1301 to single-ended to feed into the MCU. The output of the differential amplifier is routed through two paths—one going to the MCU pin (I_U) with an RC filter (cutoff frequency > 1 MHz and time delay of 150 ns) and the other going to the comparator for overload protection. Note that I_U also goes to the ground fault comparator as explained in Section 4.8.

If the delay created by the op-amp circuit is too high, then a bypass path is also given through the DNP resistor R22 to send the current sense signal to the comparator directly.
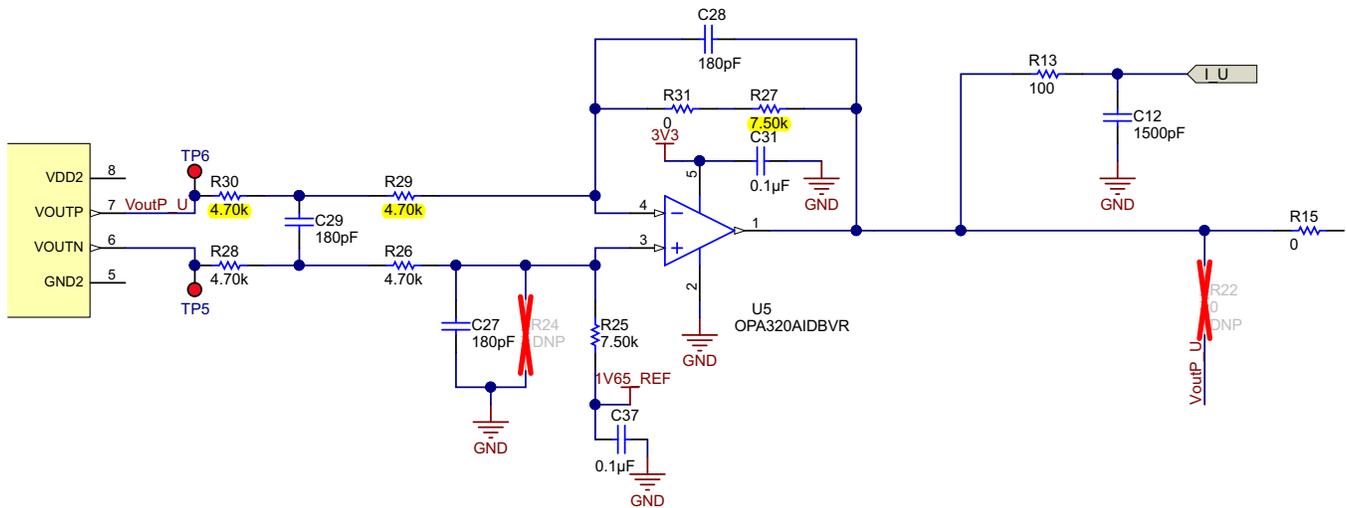
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Figure 13. Differential-to-Single Ended Signal Conversion

4.5 DC Bus Voltage Sensing Circuit

The design implements undervoltage and overvoltage protections on the DC bus by measuring DC bus voltage. The DC bus input voltage is scaled down and fed to the MCU using the AMC1301 reinforced isolation amplifier, and op amp OPA320. The output of the OPA320 can directly drive an ADC input or can be further filtered before processed by the ADC.

To scale down the DC bus voltage, a resistor divider network is chosen considering the maximum voltage for the MCU ADC input as 3.3 V and the maximum DC bus voltage to be measured as 1200 V.

To achieve better linearity and noise performance of the device, the allowable input voltage between the amplifier pin VINP and VINN is ±250 mV. The voltage divider resistor is selected such that input voltage to the amplifier is less than ±250 mV at maximum DC bus condition.

As shown in Figure 14, six 1-MΩ resistors and a 3.01-kΩ resistor are used to drop the VDC signal. The VINN pin of the AMC1301 is fed with an offset voltage created using R81 (31.9 kΩ) and R107 (3.16 kΩ). This helps in using the entire ±250-mV range of the AMC1301 input.

The sensed signal is filtered using a differential filter at the input of the AMC1301. The filter uses R83 (39 Ω), R82 (39 Ω), and C81 (0.01 μF) and has a cutoff frequency of 204 kHz.

NOTE: The undervoltage for this design can be set at 400-V DC, hence anything below 400 V should not be measured. In that case, use two 200-V Zener diodes (currently DNP) connected in parallel with two 1-MΩ resistors.
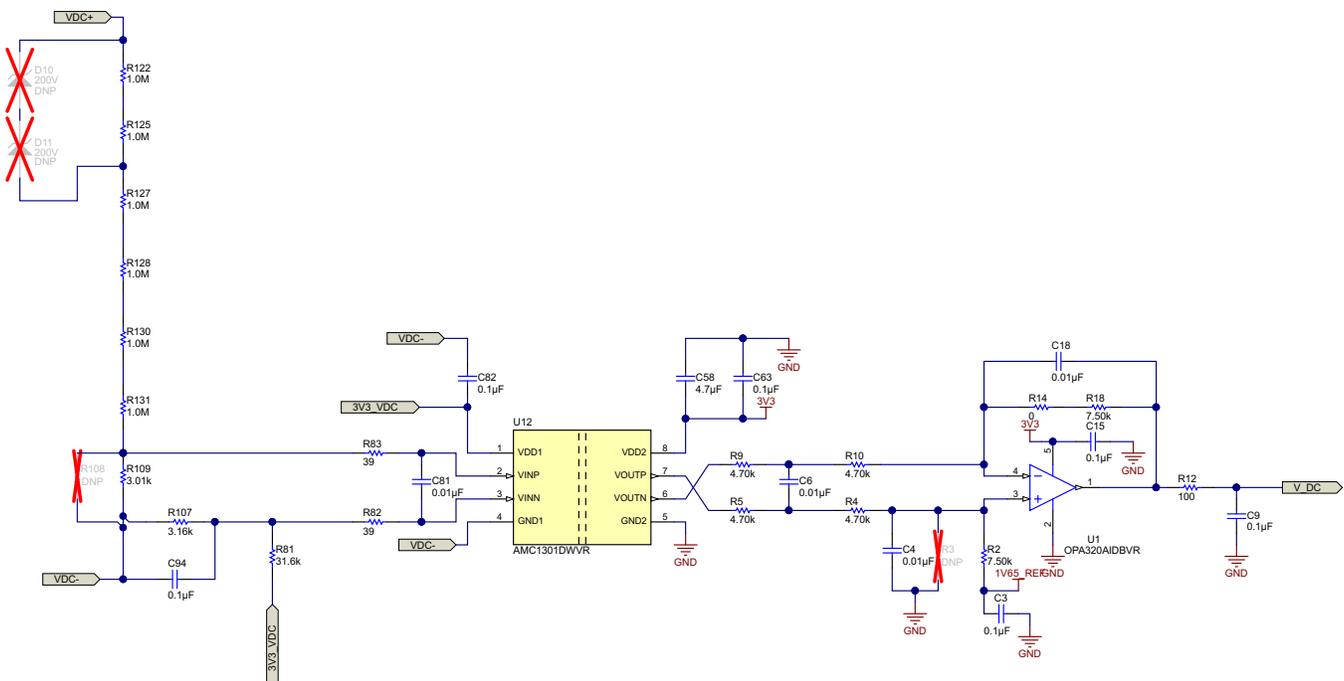
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Figure 14. DC Bus Voltage Sensing Circuit

The spacing for the resistors and Zener diodes are important due to high voltage operation. See the layout for these components in Figure 88.

4.6 NTC Temperature Sensing Circuit

The IGBT module used in this design has an integrated NTC thermistor. The characteristics of this NTC are shown in Figure 15.
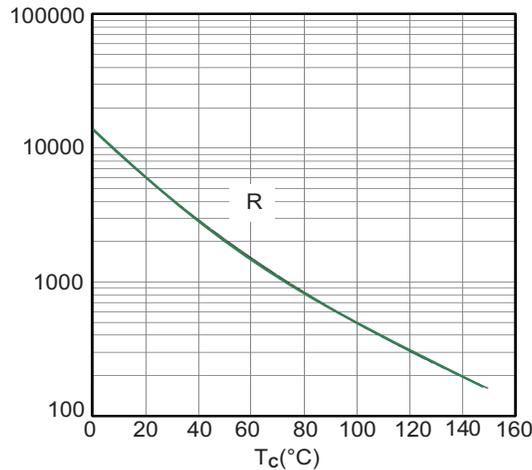
Figure 15. NTC Characteristics

The design implements over-temperature protection by sensing the NTC voltage and providing the signal to the MCU for shutting off the PWMs. The NTC is biased using one resistor R106 (68.1 kΩ) as shown in Figure 5. The biased signal is given to the VINP pin of the AMC1301 as shown in Figure 16. The VINN pin of the AMC1301 is fed with an offset voltage created using R90 (90.9 kΩ) and R91 (5.76 kΩ). This helps in using the entire ±250-mV range of the AMC1301 input. The sensed signal is filtered using a differential filter at the input of the AMC1301. The filter uses R83 (39 Ω), R82 (39 Ω) and C81 (0.01 μF) and has a cutoff frequency of 204 kHz. The differential output of the AMC1301 is filtered and converted to single-ended signal by the OPA320 with the gain of 0.79. The output of the OPA320 is filtered using an RC filter (cutoff frequency = 16 kHz and RC delay = 10 μs) and fed to the MCU as a "MODULE_TEMP" signal.
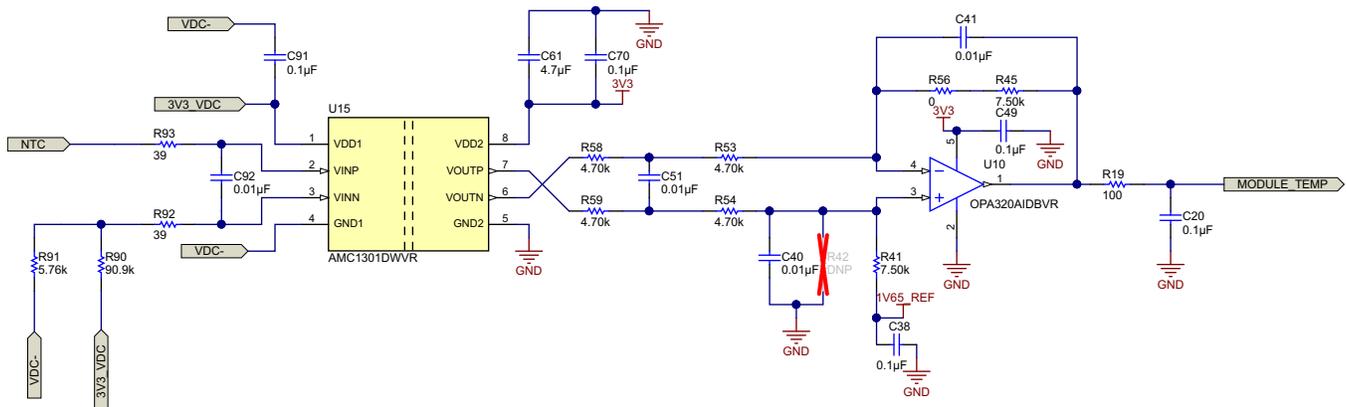
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Figure 16. NTC Temperature Sensing Circuit

4.7 Overload (or Overcurrent) Protection

NOTE: The TIDA-00366 is designed for a three-phase inverter, but this section explains the circuits and components for one channel (U-Phase) only. The same explanation is applicable to two other channels (V-Phase and W-Phase).

4.7.1 Selection of Comparators

A typical industrial drive needs to have overload protection to operate within 300 to 500 ns. The TLC372 helps reach this goal. The TLC372 is very low cost and a dual-channel comparator. It operates from a supply range from 3 to 16 V and has a typical response time of 200 ns.

4.7.2 Calculation of Threshold Levels

Considering 50 A_{PEAK} as the threshold for ground fault condition (which is ~200% of rated current), Table 3 shows the calculations that are used to select the resistors for setting the threshold on the comparators.

- $I_{SENSE(RMS)}$ = 35.4 A
- $I_{SENSE(PEAK)}$ = 50 A
- R_{SHUNT} = 5 mΩ

Table 3. Calculations of Threshold Levels for Overload Protection

PARAMETER	EQUATION	CALCULATED VALUE	UNIT
Input to AMC1301 (peak)	$I_{SENSE(PEAK)} \times R_{SHUNT}$	250	mV
Output of AMC1301 (peak)	Input to AMC1301 × 8.2	2.05	V
Output of op-amp stage (peak)	Output of AMC1301 × 0.7978	1.63549	V
With VDD for TLC372 = 3.3 V, the reference mid-point value is (3.3 V/2) = 1.65 V			
High threshold	1.65 V + Output of op-amp stage (peak)	3.28549	V
Low threshold	1.65 V – Output of op-amp stage (peak)	0.01451	V

4.7.3 Calculation of Resistors for Setting the Threshold

The high threshold is set by resistors R20 and R23, whereas the low threshold is set by resistors R23 and R21 as shown in Figure 17. Assuming R20 = R21 = 100 Ω, R23 is calculated as R23 = 10.7 kΩ.

As shown in Figure 17, the input signal for the comparators (which is compared with threshold) is coming from the output of the op-amp stage. The TLC372 is open-drain output comparator, which needs a pullup resistor at the output. R11 serves that purpose. C13 (0.1 μF) is used as decoupling capacitor for the TLC372. C23 (0.1 μF) is used as local decoupling for the threshold generating resistor divider network.

The OVERLOAD signal generated from all the three channels is combined together. It is given to the MCU as well as to the DISABLE logic gate input for further processing.

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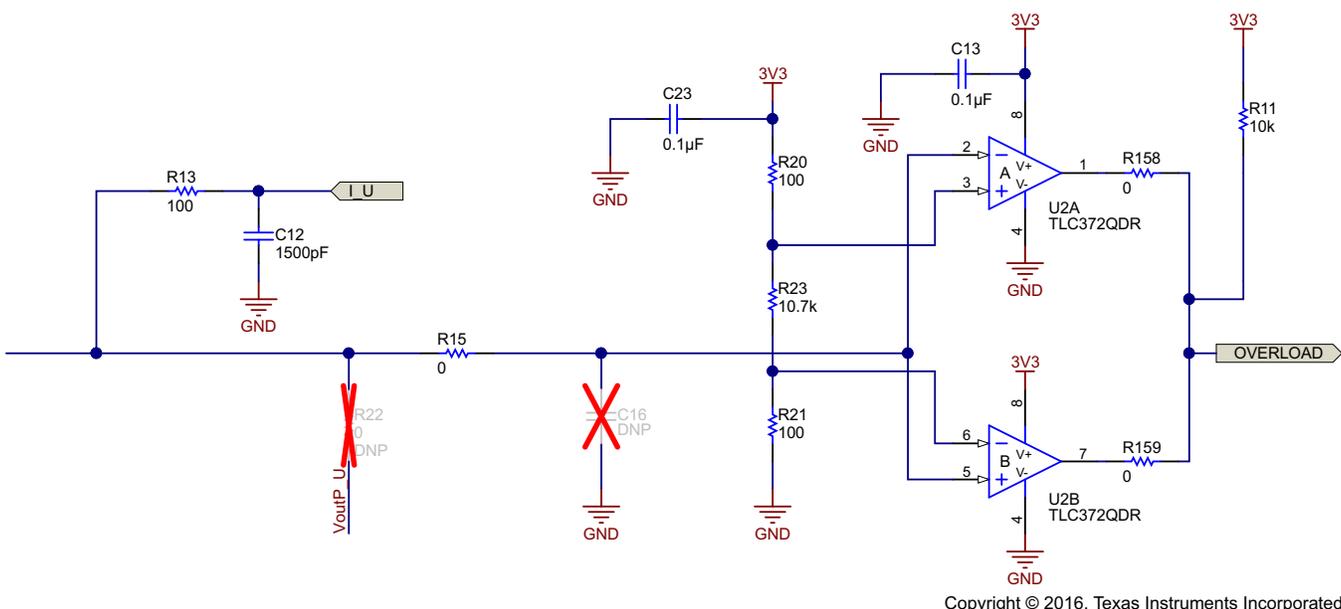
Figure 17. Overload Protection Circuit

4.8 Ground Fault Protection

4.8.1 Selection of Comparator

A typical industrial drive needs to have ground fault protection to operate within 300 to 500 ns. To reach this goal, the TLC372 is selected. The TLC372 is very low-cost and dual channel comparator. It operates from a supply range from 3 to 16 V and has typical response time of 200 ns.

4.8.2 Calculation of Threshold Levels

Considering 5 A_{PEAK} as threshold for ground fault condition (which is ~20% imbalance), the following calculations are used to select the resistors for setting the threshold on the comparators.

- $I_{SENSE(RMS)}$ = 3.54 A
- $I_{SENSE(PEAK)}$ = 5 A
- R_{SHUNT} = 5 mΩ

Table 4. Calculations of Threshold Levels for Ground Fault Protection

PARAMETER	EQUATION	CALCULATED VALUE	UNIT
Input to AMC1301 (peak)		25	mV
Output of AMC1301 (peak)	Input to AMC1301 × 8.2	205	mV
Output of op-amp stage (peak)	Output of AMC1301 × 0.7978	163.549	mV
With VDD for TLC372 = 3.3 V, the reference mid-point value is (3.3 V/2) = 1.65 V			
High threshold	1.65 V + Output of op-amp stage(peak)	1.813549	V
Low threshold	1.65 V – Output of op-amp stage(peak)	1.486451	V

4.8.3 Calculation of Resistors for Setting the Threshold

The high threshold is set by resistors R145, R147, and R146 as shown in Figure 18. Assuming R146 = 10 kΩ, the other two resistors are calculated as R145 + R147 = 8.2 kΩ.

The final values used in the schematic are R145 = 0 Ω, R146 = 8.2 kΩ, and R146 = 10 kΩ.

The low threshold is set by resistors R157, R156, and R155 as shown in Figure 18. Assuming R155 = 10 kΩ, the other two resistors are calculated as R157 + R156 = 12.2 kΩ.

The final values used in the schematic are R157 = 200 Ω, R156 = 12 kΩ, and R155 = 10 kΩ.
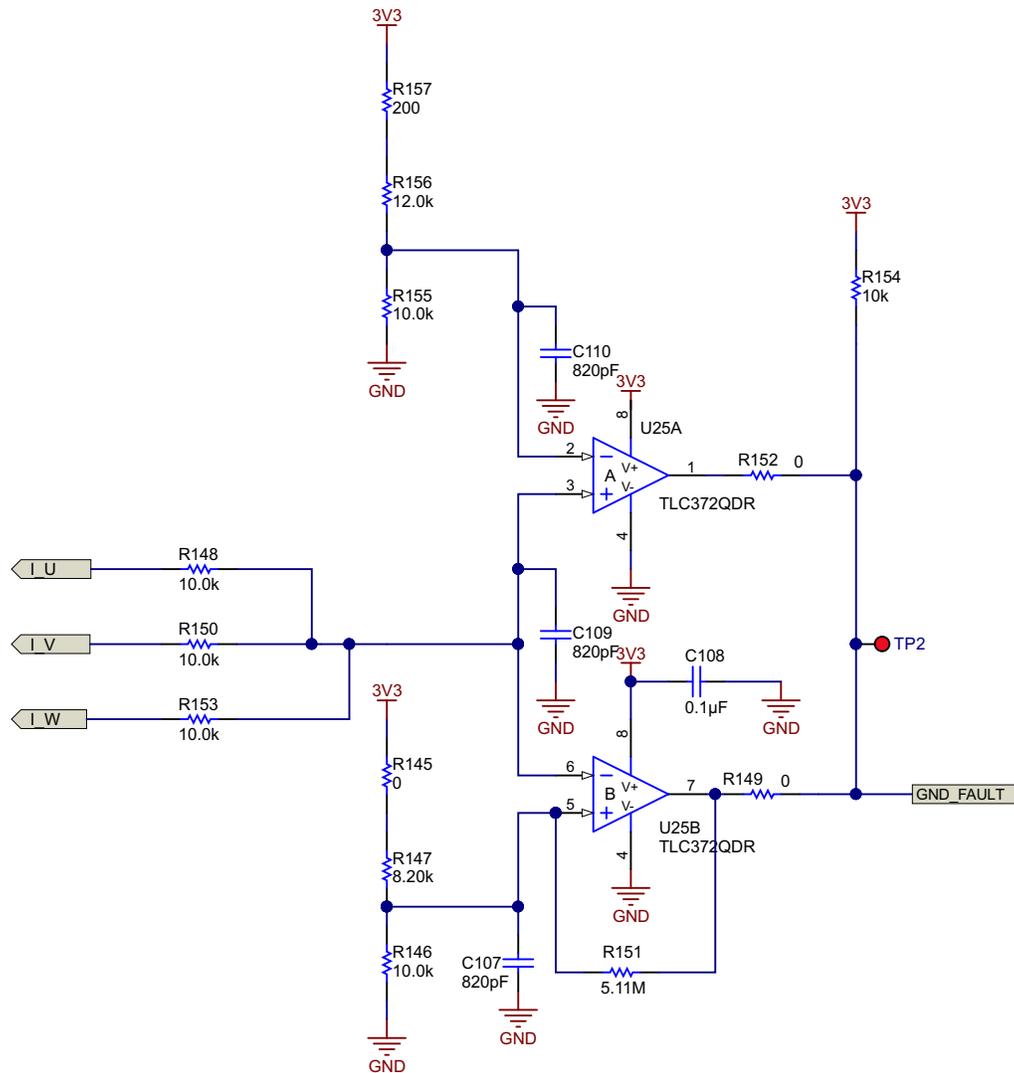
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Figure 18. Ground Fault Detection Circuit

As shown in Figure 18, the input signal for the comparators (which is compared with threshold) is coming from the output of three op-amp stages and summed together using three 10-kΩ resistors. The TLC372 is an open-drain output comparator, which needs a pullup resistor at the output. R154 serves that purpose. C108 (0.1 μF) is used as decoupling capacitor for the TLC372. C107, C109, and C110 (all equal to 820 pF) are used as local decoupling for the threshold generating resistor divider networks and input signal.

The GND_FAULT signal generated from comparators is given to the MCU as well as to the DISABLE logic gate input for further processing.

4.9 Gate Logic for DISABLE Signal

The DISABLE signal for IGBT gate drivers disable both the driver outputs if asserted high, and enabled if set low or left open. This pin is pulled low internally if left open or floating. The disable signal for IGBT gate-drivers used on TIDA-00366 design is generated for the occurrence of following conditions:

1. If any of the three channels have overload condition (that is, OVERLOAD = LOW) OR

2. If earth fault condition has occurred (that is, GND_FAULT = LOW) OR

3. If "TRIP" signal is generated from the microcontroller by user (that is, TRIP = HIGH).

At the PWM startup, a sequence is required that can make the low-side IGBT turn on first so that the bootstrap configuration works properly. This also uses the TRIP signal as explained in Section 6.3. The logic truth table for generating the DISABLE signal is shown in Table 5.

Table 5. Truth Table for Disable Logic

STATE	TRIP (A)	GND_FAULT (B)	OVERLOAD (C)	DISABLE (Y)
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

To fulfill all these conditions, the circuit shown in Figure 19 is used to implement the DISABLE logic.
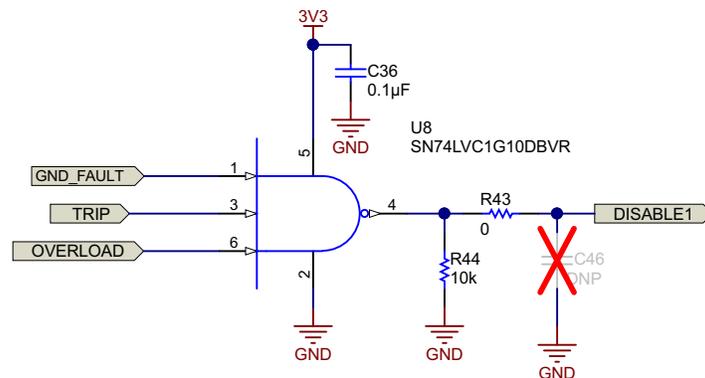
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Figure 19. DISABLE Logic Generation

R44 (10 kΩ) is a pulldown resistor for the output of the NAND gate just to make it connected to ground when not driven with the inputs. Also, the RC filter (R43 and C46) is used to set up a delay, required by the user.

> **NOTE:** The DISABLE1 signal is connected to the MCU pin through a 1-kΩ resistor (R167) as shown in Figure 20. This is required to set the startup sequence of the PWM switching.

When the board is powered up and PWM is not turned on, the "OVERLOAD" and "GND_FAULT" signals will be active low, which will make the DISABLE1 (and also DISABLE) to go high as per Table 5. If the DISABLE signal is high, the gate-drivers are disabled. To come out of this situation, the DISABLE signal is pulled "Low" by changing the GPIO state from input to output for a short duration of time. The 1-kΩ resistor limits the current into the GPIO during this time.

Reference Design for Reinforced Isolation Three-Phase Inverter With Current, Voltage, and Temp Protection

4.10 Connectors to Connect C2000 Piccolo LaunchPad

Table 6 shows the pinout for C2000 Piccolo LaunchPad. The highlighted pins are used for connecting the TIDA-00366 board.

Table 6. C2000 LaunchPad Pinout

MUX VALUE				J1 PIN	J5 PIN	MUX VALUE			
3	2	1	0			0	1	2	3
			3.3 V	1	1	5 V			
			ADCINA6	2	2	GND			
TZ2	SDAA	SCIRXDA	GPIO28	3	3	ADCINA7			
TZ3	SCLA	SCITXDA	GPIO29	4	4	ADCINA3			
RSVD	RSVD	COMP2OUT	GPIO34	5	5	ADCINA1			
			ADCINA4	6	6	ADCINA0			
	SCITXDA	SPICLK	GPIO18	7	7	ADCINB1			
			ADCINA2	8	8	ADCINB3			
			ADCINB2	9	9	ADCINB7			
			ADCINB4	10	10	NC			
MUX VALUE				J6 PIN	J2 PIN	MUX VALUE			
3	2	1	0			0	1	2	3
RSVD	RSVD	EPWM1A	GPIO0	1	1	GND			
COMP1OUT	RSVD	EPWM1B	GPIO1	2	2	GPIO19	SPISTEA	SCIRXDA	ECAP1
RSVD	RSVD	EPWM2A	GPIO2	3	3	GPIO12	TZ1	SCITXDA	RSVD
COMP2OUT	RSVD	EPWM2B	GPIO3	4	4	NC			
RSVD	RSVD	EPWM3A	GPIO4	5	5	RESET number			
ECAP1	RSVD	EPWM3B	GPIO5	6	6	GPIO16 and GPIO32	SPISIMOA or SDAA	RSVD or EPWMSYNCI	TZ2 or ADCSOCA
TZ2 or ADCSOCA	RSVD or EPWMSYNCI	SPISIMOA or SDAA	GPIO16 and GPIO32	7	7	GPIO17 and GPIO33	SPISOMIA or SCLA	RSVD or EPWMSYNCO	TZ3 or ADCSOCB
TZ3 or ADCSOCB	RSVD or EPWMSYNCO	SPISOMIA or SCLA	GPIO17 and GPIO33	8	8	GPIO6	EPWM4A	EPWMSYNCI	EPWMSYNCO
			NC	9	9	GPIO7	EPWM4B	SCIRXDA	RSVD
			NC	10	10	ADCINB6			

On the TIDA-00366 board, two 20-pin connectors are used to connect with the C2000 LaunchPad as shown in Figure 20 and Figure 21. The PWM signals for the inverter are generated using the LAUNCHXL-F28027 board. The PWM signals generated from the MCU are filtered using an RC filter with values of R = 100 Ω and C = 10 pF. This corresponds to a cutoff frequency of 159 MHz and an RC time delay of 1 ns. GND_FAULT and OVERLOAD signals are generated from their respective comparators and are connected to the MCU on GPIOs and also connected to a three-input NAND gate as explained in Section 4.9 to generate the DISABLE signal for gate drivers. The TRIP signal is generated from the MCU in case the user wants to interrupt the PWM signals or if the GND_FAULT and OVERLOAD signals need to be latched.

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Figure 20. 20-Pin Connector to Connect With Connectors J6 and J2 on LAUNCHXL-F28027

The 3.3-V supply generated using the TLV1117-33 supplies the LaunchPad as shown in Figure 21. There is also a provision to power the MCU from external 5 V by populating components R7, C10, and C11 on the board. The sensed signals I_U, I_V, I_W, V_DC, and MODULE_TEMP are connected to ADC input pins after the RC filtering (for aliasing). 1V65_REF and 3V3_REF are also provided to ADCs for any ratiometric measurements.
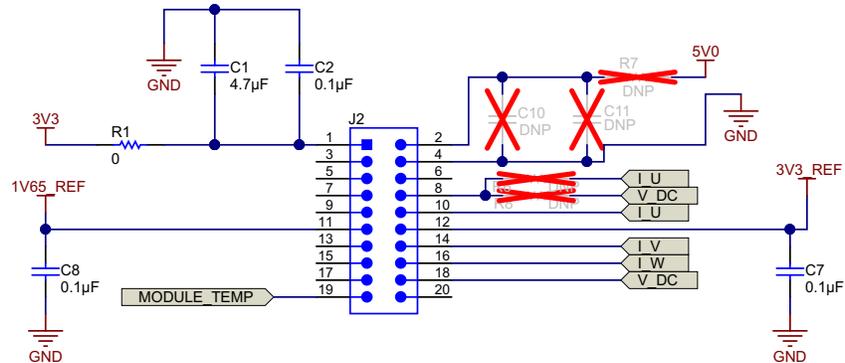
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Figure 21. 20-Pin Connector to Connect With Connectors J1 and J5 on LAUNCHXL-F28027

4.11 Power Supplies

As explained in the system block diagram in Section 3, the design uses two external supplies: 5 V for powering the cold side of the design, and 16 V for powering the isolated gate-drivers (near high-voltage side).

4.11.1 3.3-V Generation Using TLV1117-33

A 3.3-V supply is needed to power:
- VDD2 of AMC1301 (output side) used for all current measurement channels, DC link voltage sensing and temperature sensing circuit
- VCCI of the UCC21520 (input side)
- VDD of the OPA320
- VDD of the TLC372 for overload as well as ground-fault detection circuit
- VCC of the SN74LVC1G10
- 3.3-V supply for LAUNCHXL-F28027 board through connector J2 (Pin 1)

To convert 5 V to 3.3 V, the TLV1117-33 is selected for the following reasons:
1. Input voltage range: 4.7 to 15 V (16-V absolute maximum rating)
2. Output current: up to 800 mA
3. Temperature range: –40°C to 125°C

The total current required to be supplied from the TLV1117-33 is ~205.86 mA (5 × IDD2 of the AMC1301, or 5 × 6 mA = 30 mA; 3 × ICCI of the UCC21520, or 3 × 5 mA = 15 mA; 5 × IDD of the OPA320, or 5 × 1.85 mA = 9.25 mA; 4 × IDD of the TLC372, or 4 × 400 μA = 1.6 mA; ICC of the SN74LVC1G10 = 10 μA; and a supply current of 150 mA for the LAUNCHXL-F28027 board).

Check the thermal stress on the LDO. The total power it has to dissipate is:

$$P_{LDO(max)} = \left(V_{LDO(IN)} - V_{LDO(OUT)} \right) \times i_{LDO(max)} = (5\ V - 3.3\ V) \times 205.86\ mA = 0.349962\ W \tag{15}$$

For package selection,

$$\theta_{JA(max)} = \frac{\left(T_J - T_A \right)}{P_{D(max)}} = \frac{(125°C - 85°C)}{0.349962} = 114.29°C/W \tag{16}$$

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The LDO must have a package with $\theta_{JA} \leq 114.29°C/W$. Looking at Table 7 from the TLV1117-33 datasheet, all packages are suitable. The TIDA-00366 uses DCY package.

Table 7. Thermal Information for TLV1117-33

THERMAL METRIC		TLV1117							UNIT
		PowerFlex							
		KTE (3 PINS)	KTP (3 PINS)	DRJ (8 PINS)	DCY (4 PINS)	KVU (3 PINS)	KCS, KCT (3 PINS)	KTT (3 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.6	19.2	38.3	104.3	50.9	30.1	27.50	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.7	60.6	36.5	53.7	57.9	44.6	43.20	
$R_{\theta JB}$	Junction-to-board thermal resistance	3.2	3.1	60.5	5.7	34.8	1.2	17.30	
φ_{JT}	Junction-to-top characterization parameter	5.9	8.7	0.2	3.1	6.0	5.0	2.80	
φ_{JB}	Junction-to-bottom characterization parameter	3.1	3.0	12.0	5.5	23.7	1.2	9.30	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal parameter	3.0	3.0	4.7	N/A	0.4	0.4	0.30	
$R_{\theta JP}$	Thermal resistance between the die junction and the bottom of the exposed pad.	2.7	1.4	1.78	N/A	N/A	3.0	1.94	

The schematic of 5-V to 3.3-V conversion using the LDO TLV1117-33 is shown in Figure 22. Diode D1 is used for reverse polarity protection. C5 (10 μF) and C14 (0.1 μF) are the input capacitors. C24 (22 μF) and C25 (0.1 μF) are output capacitors. Output capacitor selection is critical for regulator stability. Larger COUT values benefit the regulator by improving transient response and loop stability. This device is designed to be stable with tantalum and aluminum electrolytic output capacitors having an ESR between 0.2 and 10 Ω. Although an input capacitor is not required for stability, a 10-μF capacitor placed between IN and GND counteracts reactive input sources and improves transient and noise performance. Higher value capacitors are necessary if large load transients with fast rise times are anticipated.
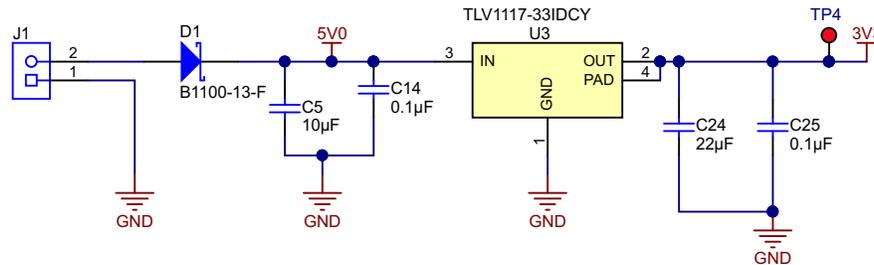
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Figure 22. 3.3-V Generation From 5-V Input

4.11.2 3.3-V Generation Using TLV70433

A 3.3-V supply is needed to power VDD1 of the AMC1301 (input side) used for DC link voltage sensing and temperature sensing circuit.

To convert 16 V to 3.3 V, the TLV70433 is selected for the following reasons:

1. Input voltage range: 2.5 to 24 V
2. Output current: up to 150 mA
3. Temperature range: –40°C to 125°C

The total current required to be supplied from the TLV70433 is ~14 mA (6.5-mA maximum for VDD1 of each AMC1301, used for the DC bus sense circuit and NTC module temperature sensing circuit).

Check the thermal stress on the LDO. The total power it has to dissipate is:

$$P_{LDO(max)} = \left(V_{LDO(IN)} - V_{LDO(OUT)}\right) \times i_{LDO(max)} = \left(16\ V - 3.3\ V\right) \times 14\ mA = 0.1778\ W \tag{17}$$

For package selection,

$$\theta_{JA(max)} = \frac{\left(T_J - T_A\right)}{P_{D(max)}} = \frac{\left(125°C - 85°C\right)}{0.1778} = 224.97°C/W \tag{18}$$

The LDO must have a package with $\theta_{JA} \le 224.97°C/W$. Looking at Table 8 from the TLV70433 datasheet, DBV (SOT-23) package is suitable.

Table 8. Thermal Information for TLV70433

	THERMAL METRIC	TLV704 DBV (5 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	213.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	110.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	97.4	
φ_{JT}	Junction-to-top characterization parameter	22.0	
φ_{JB}	Junction-to-bottom characterization parameter	78.4	

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The schematic of the 16-V to 3.3-V conversion using the LDO TLV70433 is shown in Figure 23. C96 (4.7 μF) and C97 (0.1 μF) are the input capacitors, and C95 (4.7 μF) is output capacitor. Although an input capacitor is not required for stability, when a 0.1-μF or larger capacitor is placed between IN and GND, it counteracts reactive input sources and improves transient and noise performance. Higher value capacitors are necessary if large load transients with fast rise times are anticipated. The TLV704 requires a 1-μF or larger capacitor connected between OUT and GND for stability. Ceramic or tantalum capacitors can be used. Larger value capacitors result in better transient and noise performance.

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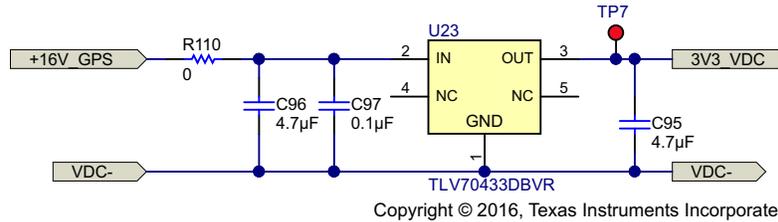
Figure 23. 3.3-V Generation From 16-V Gate Drive Power Supply Input

4.11.3   3.3-V and 1.65-V Reference Generation Using REF2033

Applications with only a positive supply voltage often require additional stable voltage in the middle of the ADC input range to bias input bipolar signals. As explained in Section 4.4.2, the output of the AMC1301 is bipolar; hence the level shifting is required during the differential-to-single-ended op amp stage. The output of the op amp is interfaced with the MCU (which is operating with a 3.3-V power supply), so the level shifting of signal should be done at 1.65 V. Figure 24 shows the reference voltage generation using the REF2033. The 0.1-μF capacitors at input and outputs are for noise filtering.

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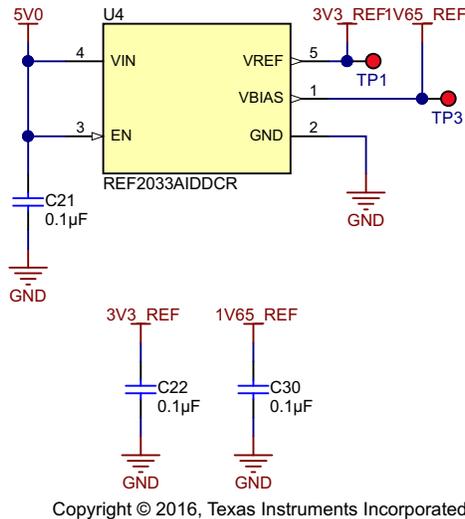
Figure 24. 1.65-V and 3.3-V Reference Generation

5 Getting Started Hardware

This section explains the top and bottom views of the PCB for the TIDA-00366 showing all the different sections. It also explains the power supply requirement and connectors used to connect the external world.

5.1 TIDA-00366 PCB Overview
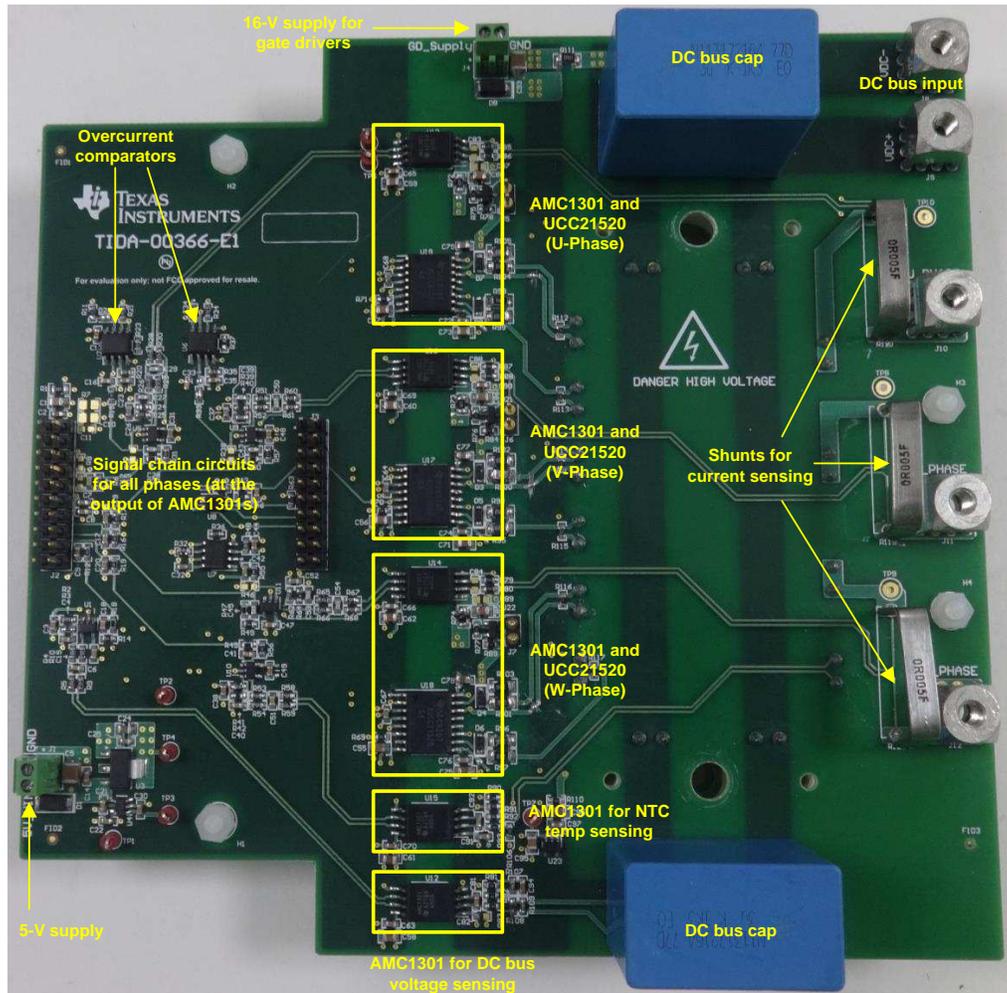
Figure 25. Top View of PCB for TIDA-00366

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Figure 26 shows the bottom view of the TIDA-00366 PCB. The IGBT module is mounted on the bottom layer so it can connect with the heat sink as required by the output power levels.
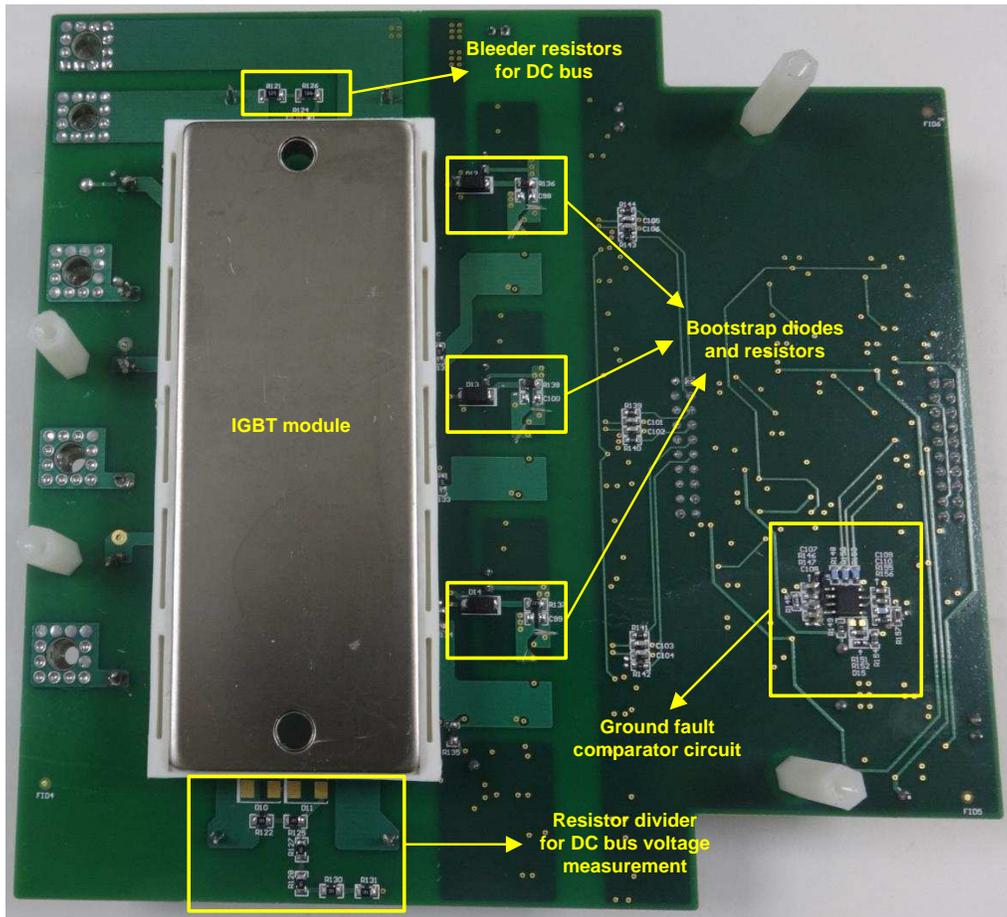
Figure 26. Bottom View of PCB for TIDA-00366

5.2 Connectors

Table 9 shows the connectors used on the TIDA-00366 PCB and their purposes.

Table 9. Connectors

CONNECTOR	PURPOSE
J1	5-V_VIN power supply to power MCU, op amps, low side of AMC1301 and comparators
J2	To connect to J1-J5 of LAUNCHXL-F28027
J3	To connect to J6-J2 of LAUNCHXL-F28027
J4	16-V GD_Supply to power low-side gate drivers
J5	To supply external isolated 16 V for U-Phase low-side gate driver if bootstrap configuration is not used
J6	To supply external isolated 16 V for V-Phase low-side gate driver if bootstrap configuration is not used
J7	To Supply external isolated 16 V for W-Phase low-side gate driver if bootstrap configuration is not used
J8	VDC– input
J9	VDC+ input
J10	U-Phase output for connecting to the motor
J11	V-Phase output for connecting to the motor
J12	W-Phase output for connecting to the motor

Figure 27 shows how the LAUNCHXL-28027 can be mounted on connectors J2 and J3.
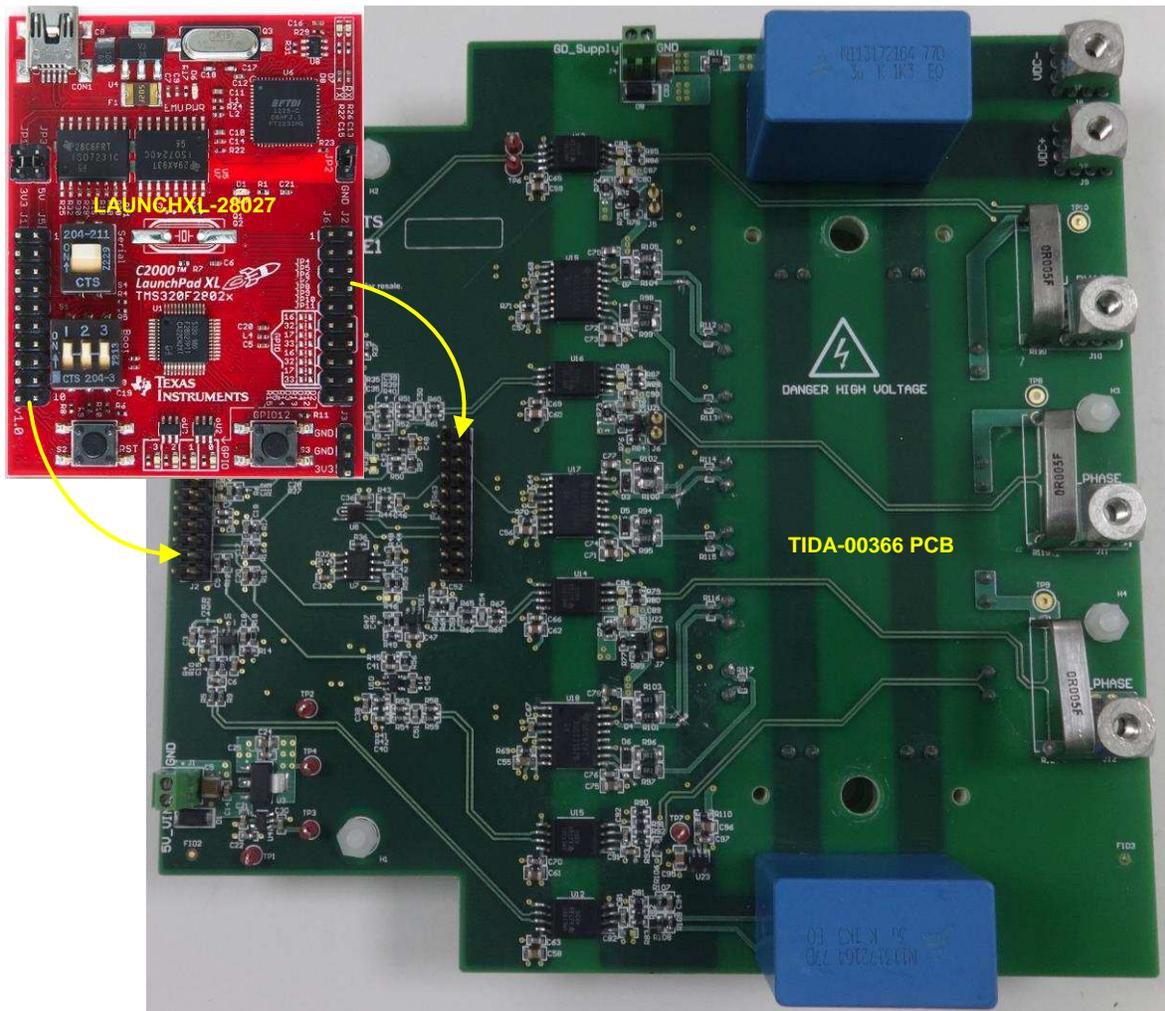
Figure 27. Connecting LAUNCHXL-F28027 Board to TIDA-00366 PCB

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6 Test Data

6.1 Power Supplies

Table 10 shows the measured values of voltage rails on the board.

Table 10. Voltage Rails—Designed and Measured Values

RAIL NAME	FROM DEVICE	DESIGNED VALUE FOR THE RAIL (V)	MEASURED VALUE FOR THE RAIL (V)
3V3 VDC	TLV70433	3.3	3.3117
3V3	TLV1117-33	3.3	3.2997
3V3_REF	REF2033	3.3	3.3
1V65_REF	REF2033	1.65	1.6501
16V GPS	Externally applied (for low-side IGBT gate-drivers)	16	16
VCC_U	Bootstrap supply (for high-side IGBT gate driver)	15	14.9
VCC_V	Bootstrap supply (for high-side IGBT gate driver)	15	14.89
VCC_W	Bootstrap supply (for high-side IGBT gate driver)	15	14.92
Supply for AMC1301	U Phase	5	5.017
	V Phase	5	4.999
	W Phase	5	5.027

6.1.1 Power Supply Rail Generated Using LDOs and References

Figure 28 and Figure 29 show the voltage rail and ripple for 3V3 rail generated using the TLV1117-33. The ripple is much less than 10 mV(p-p).
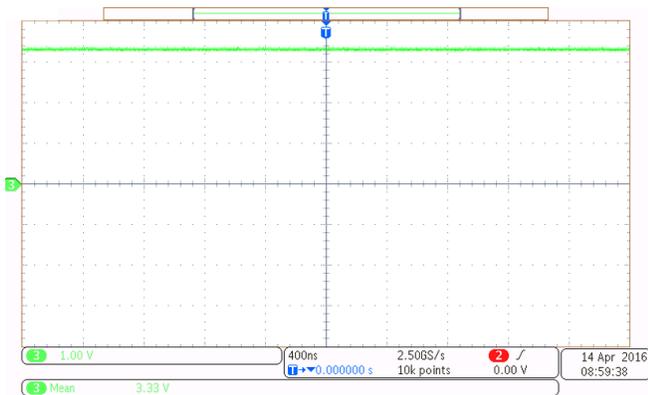
Figure 28. 3.3-V Rail Generated Using TLV1117-33
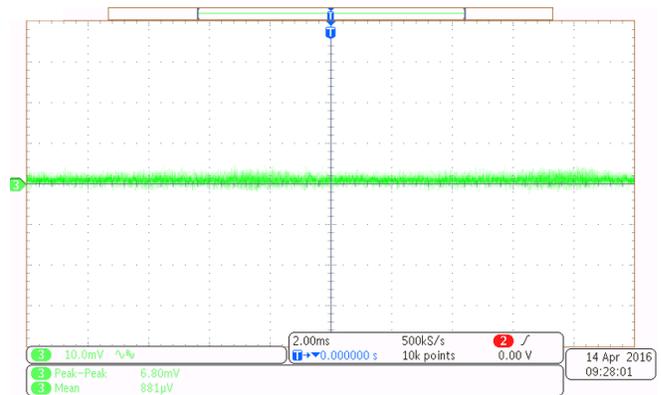
Figure 29. Ripple on 3.3-V Rail Generated Using TLV1117-33

Figure 30 and Figure 31 show the voltage rail and ripple for the 3V3_VDC rail generated using the TLV70433. The ripple is much less than 10 mV(p-p).
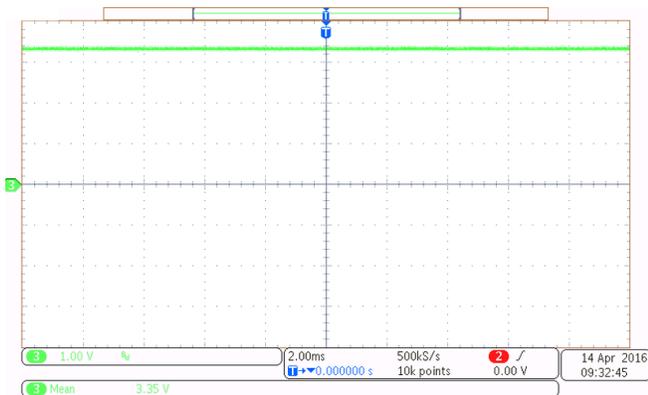
Figure 30. 3.3-V Rail Generated Using TLV70433
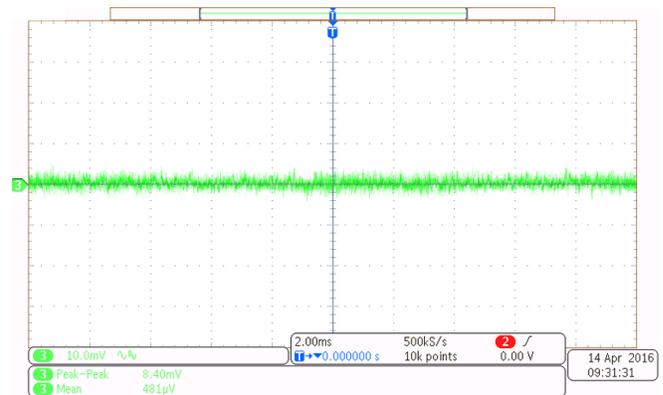
Figure 31. Ripple on 3.3-V Rail Generated Using TLV70433

Figure 32 and Figure 33 show the voltage rails, 3V3 and 1V65 rails, respectively, generated using the REF2033.
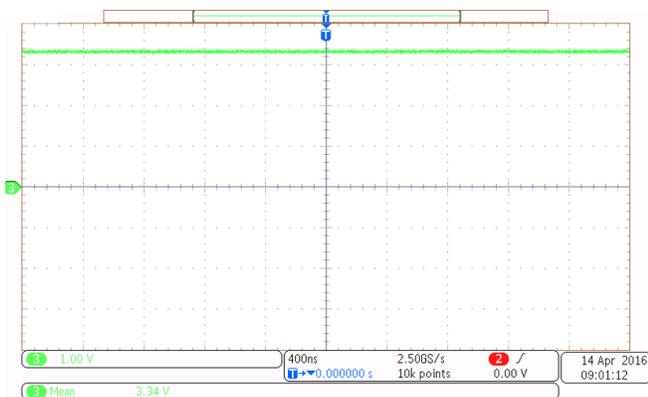
Figure 32. 3.3-V Rail Generated Using REF2033
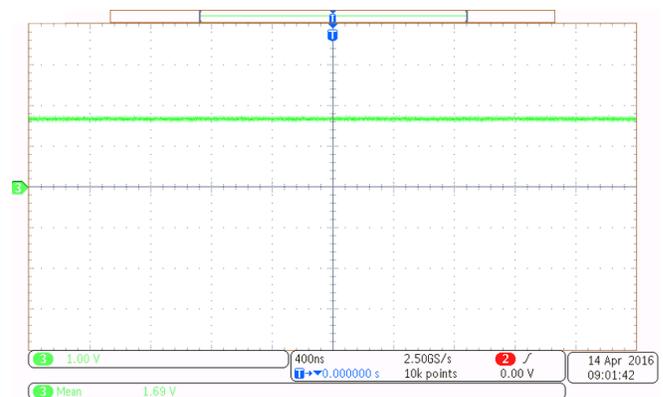
Figure 33. 1.65-V Rail Generated Using REF2033

6.1.2   Power Supply Rail for AMC1301

As explained in Section 4.4.2.1, 5-V rails for the hot side of the AMC1301 are generated from the bootstrap power supply using the TL431B. Figure 34 and Figure 35 show the 5-V rail and ripple on that rail, respectively. The peak-to-peak ripple value is less than 400 mV and the frequency is (1/66.40 μs) = 15.040 kHz, which is exactly the switching frequency of the power stage.
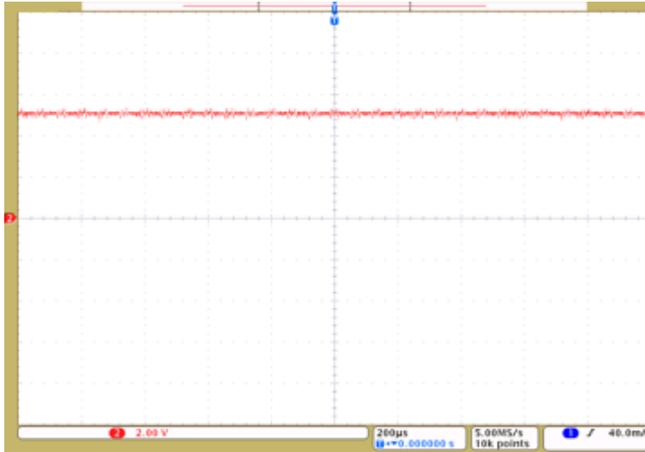
Figure 34. 5 V to Power Hot Side of AMC1301
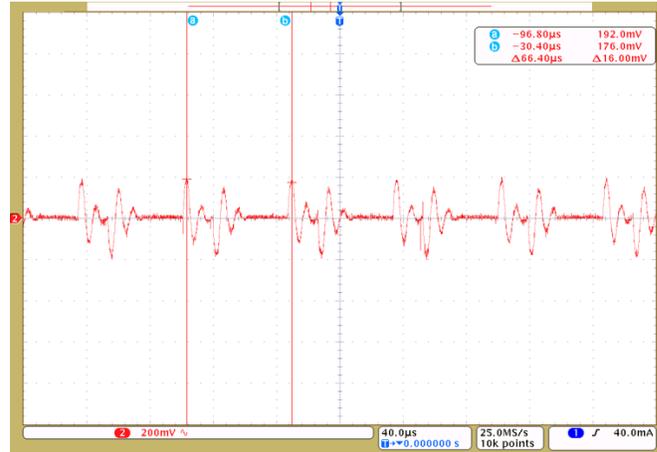
Figure 35. Ripple on 5 V to Power Hot Side of AMC1301

6.1.3   Power Supply Rail for Low-Side Gate Drivers

Figure 36 and Figure 37 show the voltage rail and ripple for the 16-V rail, respectively, for the low-side gate driver. The peak-to-peak ripple value is 80 mV and the frequency is (1/66.80 μs) = 14.97 kHz, which is near to the switching frequency of the power stage.
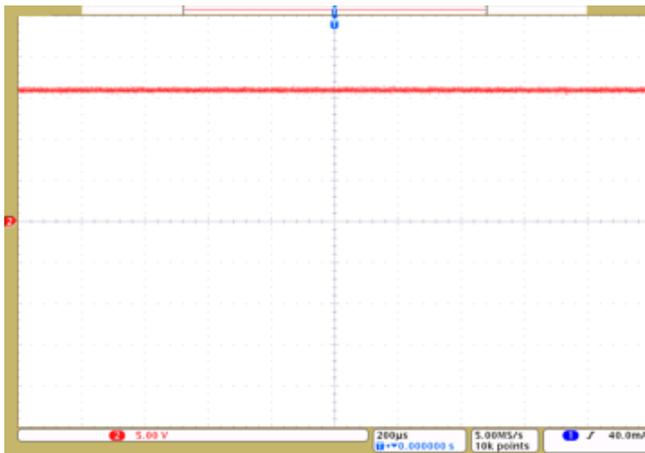
Figure 36. 16-V Rail for Low-Side Gate Driver
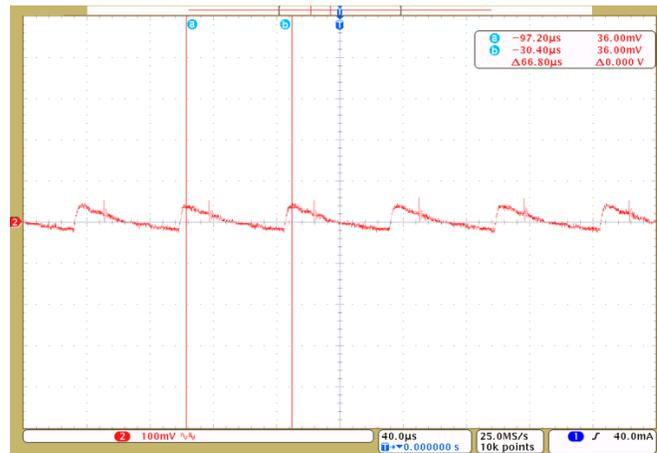
Figure 37. Ripple on 16-V Rail for Low-Side Gate Driver

6.1.4 Power Supply Rail for High-Side Gate Drivers (Bootstrap Supply)

Figure 38 and Figure 39 show the voltage rail and ripple for bootstrap supply, respectively, for the high-side gate driver. The peak-to-peak ripple voltage is 2.3 V while applying a VDC = 800 V on DC Bus.
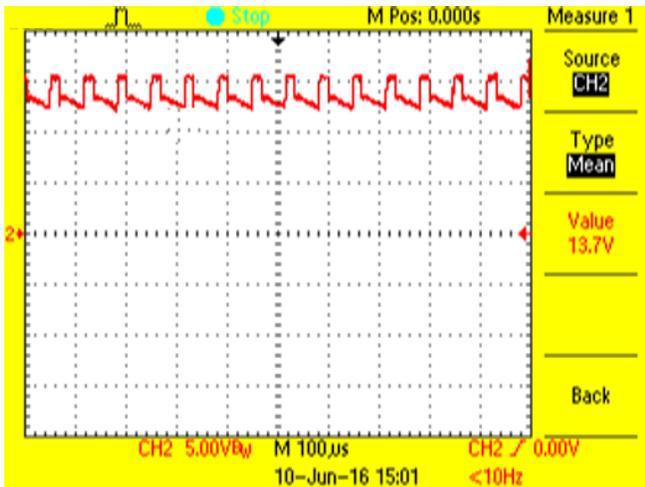
Figure 38. Bootstrap Power Supply for High-Side Gate Driver
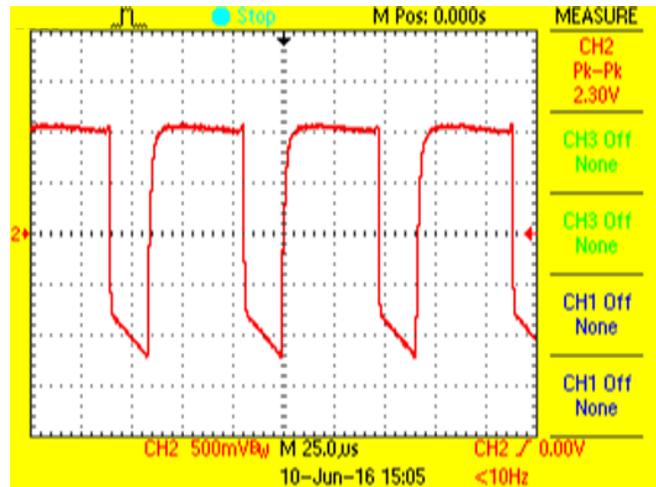
Figure 39. Ripple on Bootstrap Power Supply for High-Side Gate Driver

The bootstrap capacitor value plays a major role in deciding the ripple on the power supply. As an extended test, a bootstrap capacitor value of 1 μF is used and tested for ripple on the supply line. Figure 40 shows the reduced value of ripple with higher capacitance. The peak-to-peak ripple voltage is 1.5 V while applying a VDC = 800 V on the DC Bus.
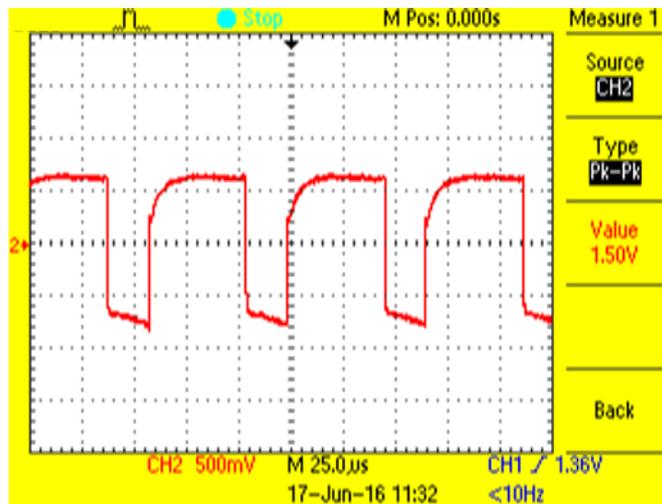
Figure 40. Bootstrap Ripple With 1-μF Capacitor for CBST

6.2   Gate Drive Signals and Waveforms

6.2.1   PWM Waveforms

Figure 41 and Figure 42 show PWM signal generated from the MCU and at the gate of IGBTs, respectively. The PWM frequency is 15 kHz.

NOTE: Blue: High-side PWM signal, Red: Low-side PWM signal
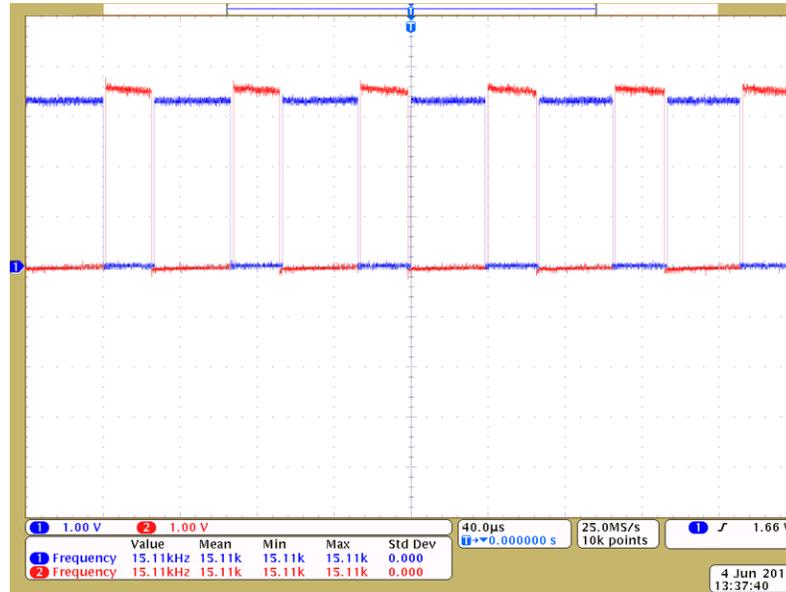
Figure 41. PWM Generated From MCU

NOTE: Blue: High-side PWM signal, Green: Low-side PWM signal
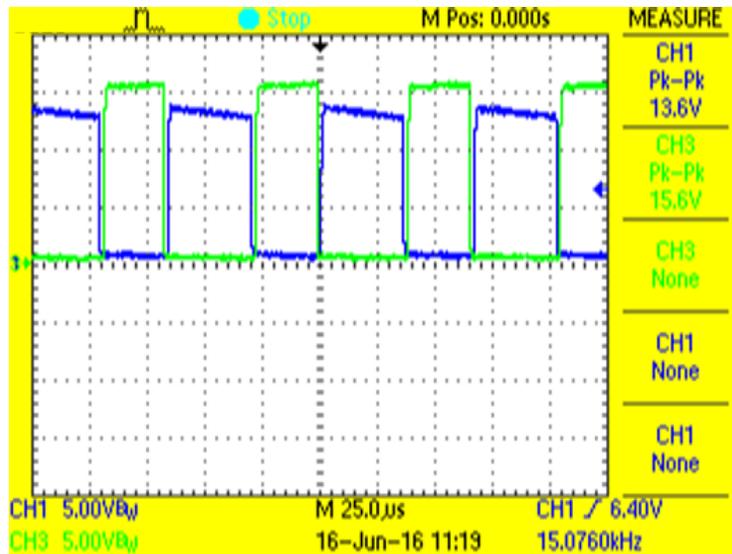
Figure 42. PWM at the Gate Driver Output

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6.2.2 Dead Time Between High-Side and Low-Side PWM

For the PWM waveforms driving both high-side and low-side IGBT gates, it is important to have enough dead time to prevent shoot-through during the switching operation. The dead time is set to ~1.4 μs as shown in Figure 43, Figure 44, Figure 45, and Figure 46.

NOTE: Blue: High-side PWM signal, Red: Low-side PWM signal
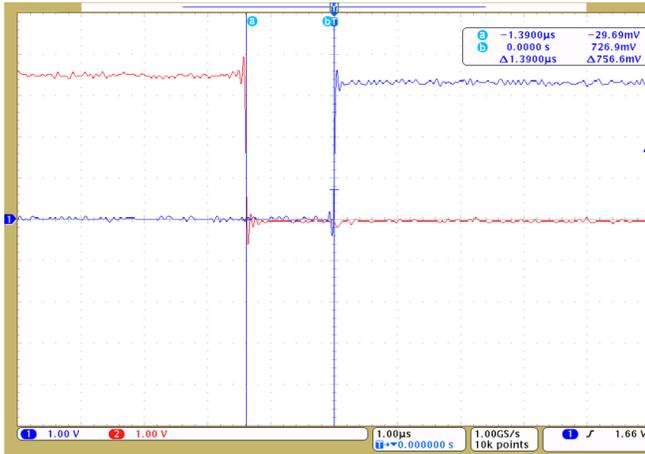
Figure 43. PWM From MCU—Dead Time (Rising Edge)
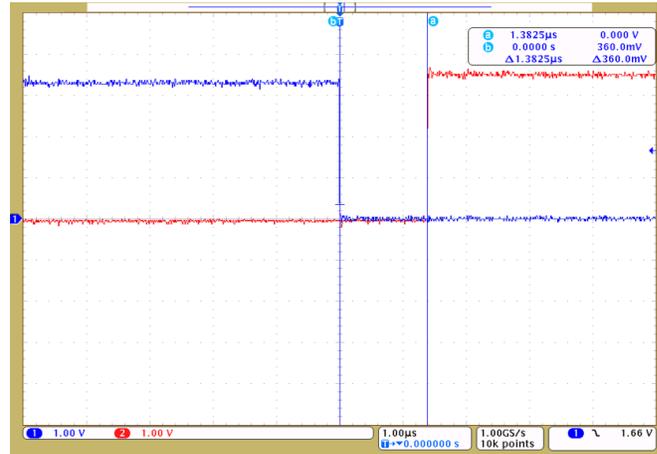
Figure 44. PWM From MCU—Dead Time (Falling Edge)

NOTE: Blue: High-Side PWM Signal, Green: Low-Side PWM Signal
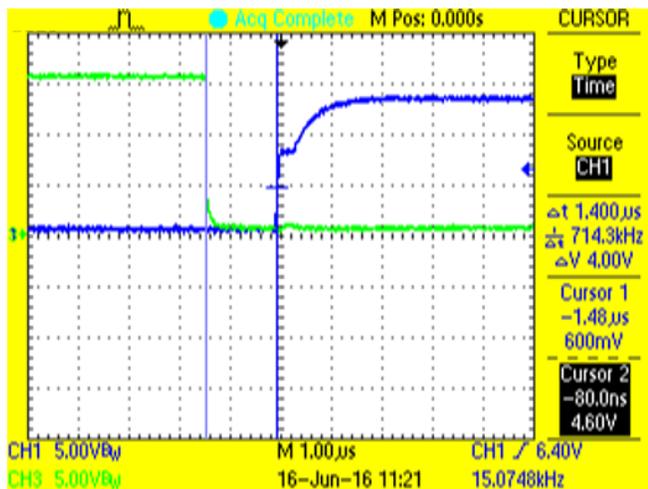
Figure 45. PWM at Gate Driver Output—Dead Time (Rising Edge)
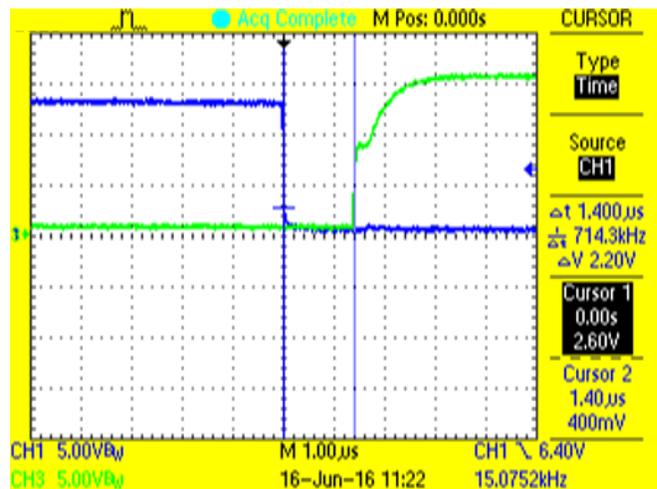
Figure 46. PWM at Gate Driver Output—Dead Time (Rising Edge)

6.2.3 Startup Sequence

As explained in Section 4.3.6.3, the high-side gate drivers are powered using bootstrap configuration. This configuration needs a start-up sequence. When starting the application, the low-side IGBTs of half-bridge should always be turned on first, so that the bootstrap capacitor can recharge to the nominal value of the supply voltage. Otherwise, it may lead to uncontrolled switching and/or error detection. Figure 47 and Figure 48 show the startup sequence where low-side IGBT is turned on first for time of 10 ms and then high-side IGBT is turned on.

NOTE: Blue: High-side PWM signal, Green: Low-side PWM signal
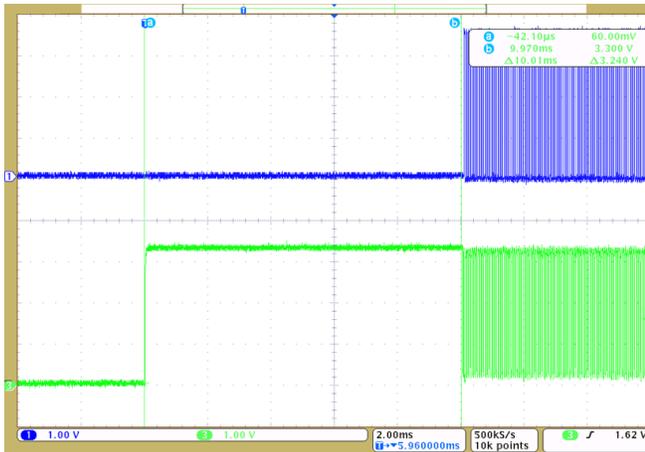
Figure 47. Startup Sequence (PWM From MCU)
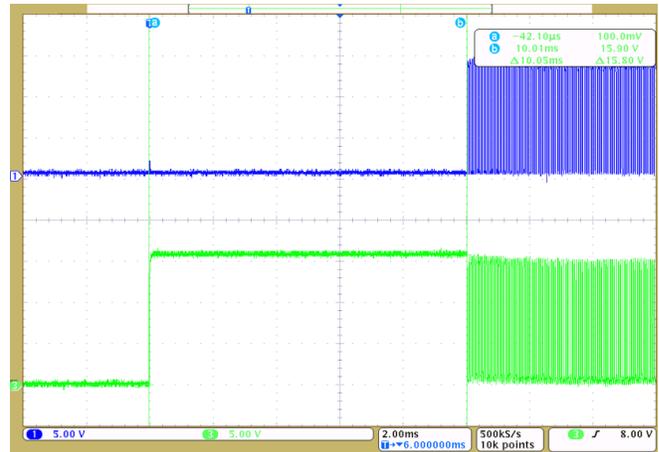
Figure 48. Startup Sequence (PWM at Gate Driver Output)

6.2.4 UVLO for Gate Drivers

Figure 49 and Figure 50 show the undervoltage lockout for the IGBT gate drivers. The output PWM starts only when the power supply of the gate driver reaches a threshold as defined in the UCC21520 datasheet. The UVLO threshold measured during the testing of the TIDA-00366 is 8.4 V (for low-side gate driver) and 8 V (for high-side gate driver).

NOTE: Blue: PWM signal from MCU, Red: VDDB supply, Green: PWM signal at the output of the gate driver
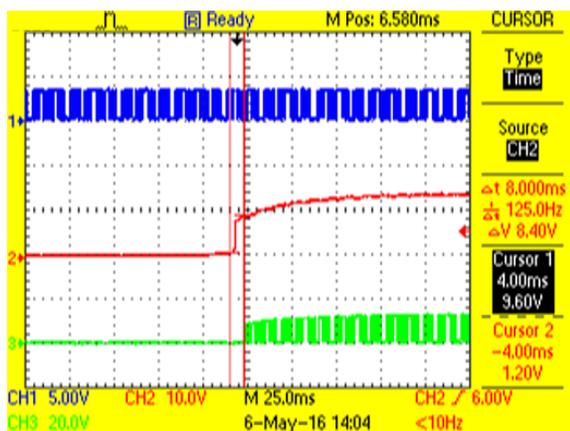
Figure 49. Low-Side Gate Driver UVLO
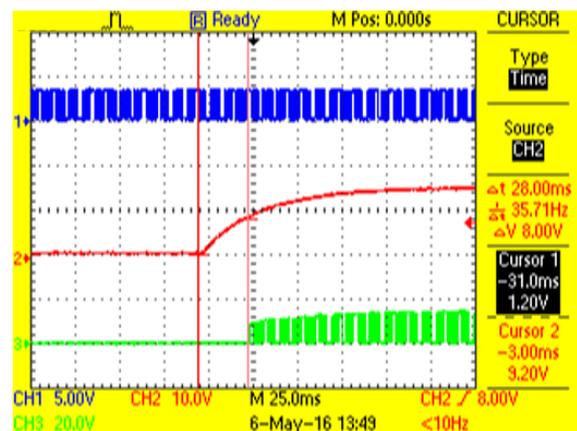
Figure 50. High-Side Gate Driver UVLO

6.2.5 PWM Signal Propagation Delay From Gate Drivers

The user must know the propagation delay of the gate driver. Figure 51 shows the line diagram where the measurements are taken for the propagation delay.
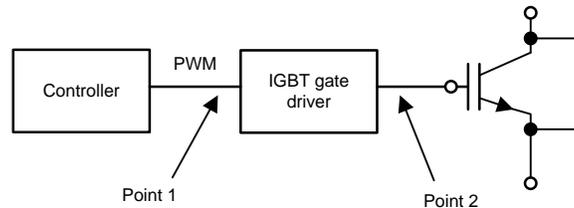
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Figure 51. Propagation Delay Measurement Points

Figure 52, Figure 53, Figure 54, and Figure 55 show the propagation delays measured for the low-side and high-side gate drivers at rising and falling edges. For these figures, the blue waveform is the input of the gate driver and the red waveform is the output of the gate driver. The measured propagation delay is ~19 ns. The UCC21520 datasheet specifies the propagation delay of 19 ns (typical).
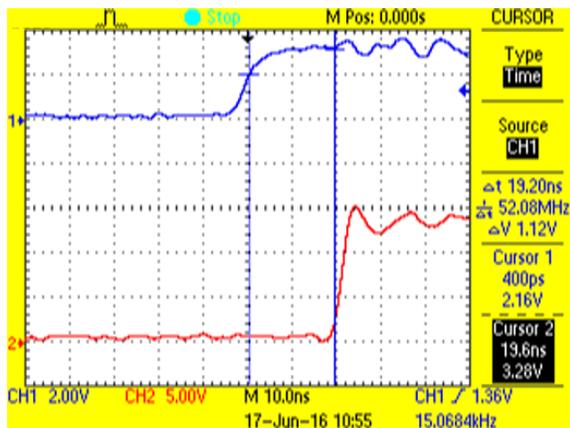
Figure 52. Propagation Delay—Low-Side Gate Driver (Rising Edge)
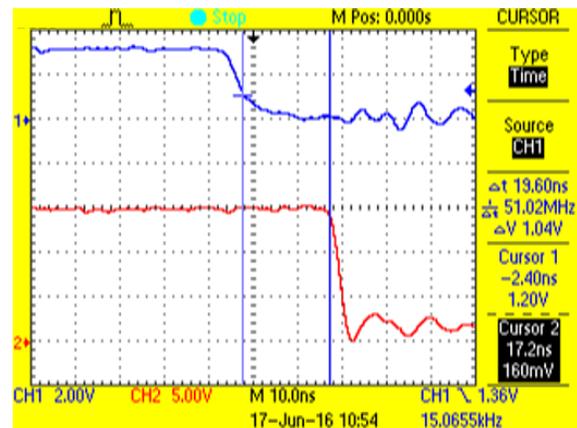
Figure 53. Propagation Delay—Low-Side Gate Driver (Falling Edge)
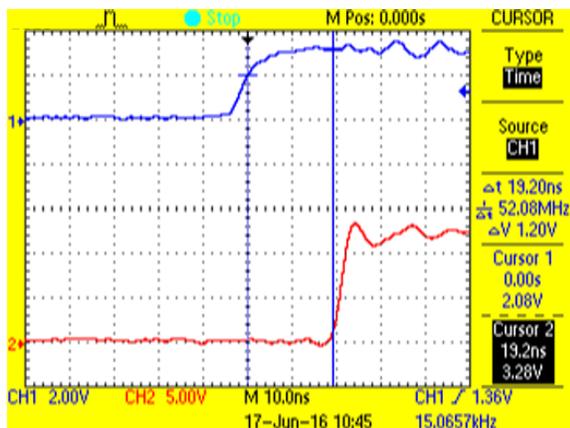
Figure 54. Propagation Delay—High-Side Gate Driver (Rising Edge)
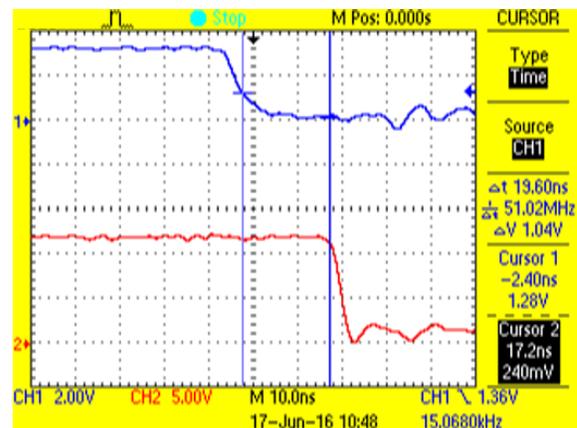
Figure 55. Propagation Delay—High-Side Gate Driver (Falling Edge)

6.2.6   Sink/Source Current From Gate Drivers

Figure 56, Figure 57, and Figure 58 show the source and sink currents delivered by the UCC21520. The test conditions are:

- $R_{G(on)}$ = 16.5 Ω
- $R_{G(off)}$ = 0 Ω
- IGBT module = MG1250H-XN2MM (from Littlefuse Inc.)
- Gate charge (Q_G) = 0.47 μC
- Internal resistance = 4 Ω
- Input capacitance C_{IES} = 3.6 nF

> **NOTE:** For sake of measuring the current, $R_{G(off)}$ is changed to 0.5 Ω. The actual circuit uses $R_{G(off)}$ = 0 Ω only.

> **NOTE:** Blue: Gate driving PWM Waveform, Red: Voltage across gate resistor
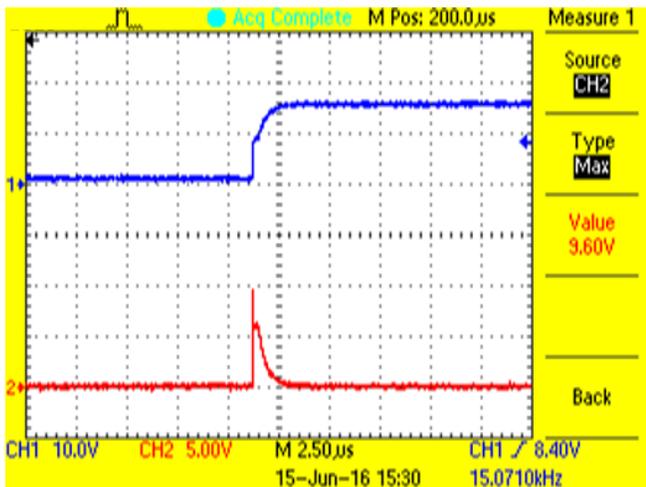
Figure 56. Source Current From Gate Driver
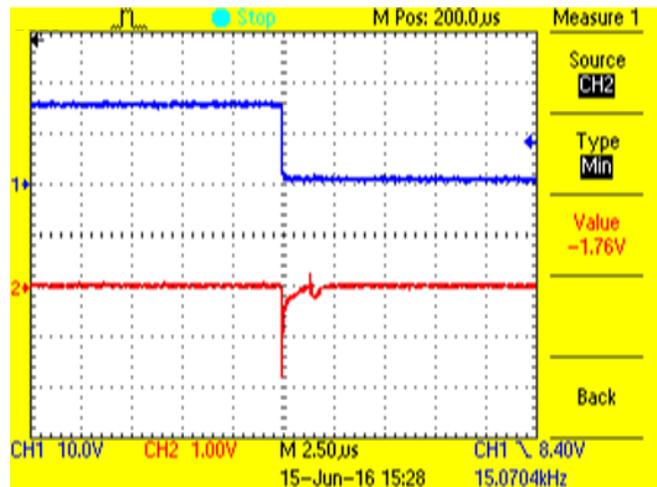
Figure 57. Sink Current to Gate Driver
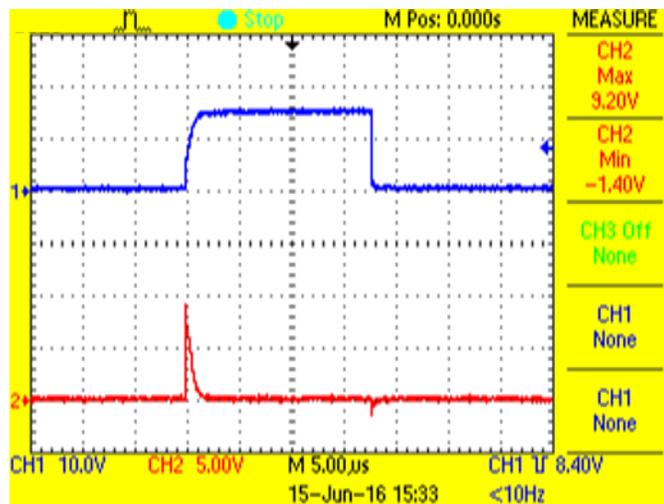
Figure 58. Source and Sink Current

6.2.7   dv/dt Measurement

With the test conditions specified in Section 6.2.6, the measured dv/dt for the falling edge (Figure 59) and rising edge (Figure 60) is 744 V/180 ns = 4.133 kV/µs at VDC = 800 V.
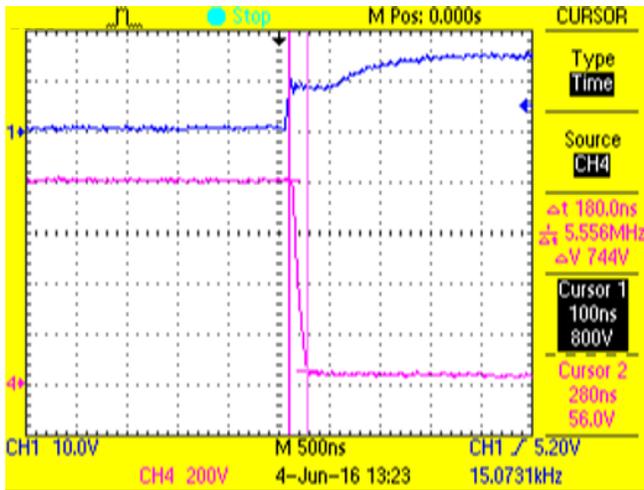
Figure 59. dv/dt During Sourcing   **Figure 60. dv/dt During Sinking**
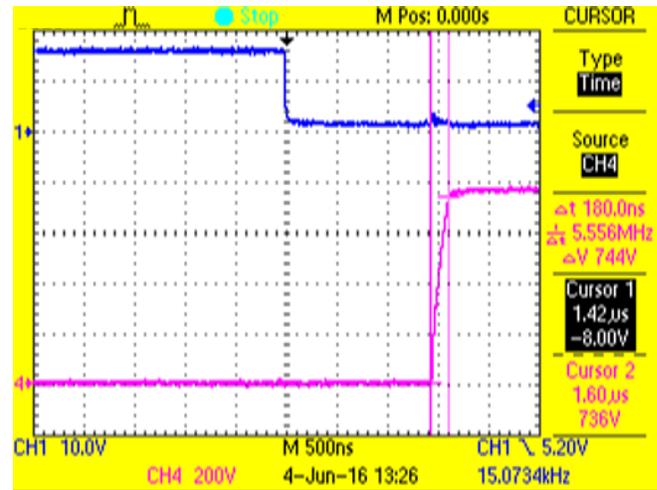
6.3   Verification of DISABLE Logic

As explained in Section 4.9, the DISABLE logic for gate drivers is derived using a three-input NAND gate. The three inputs for the NAND gates are "OVERLOAD", "GND_FAULT", and "TRIP". Figure 61 shows that the DISABLE is active as per the timings explained in Table 11.

NOTE: Blue: GND_FAULT, Red: OVERLOAD, Green: TRIP, Pink: DISABLE for gate drivers
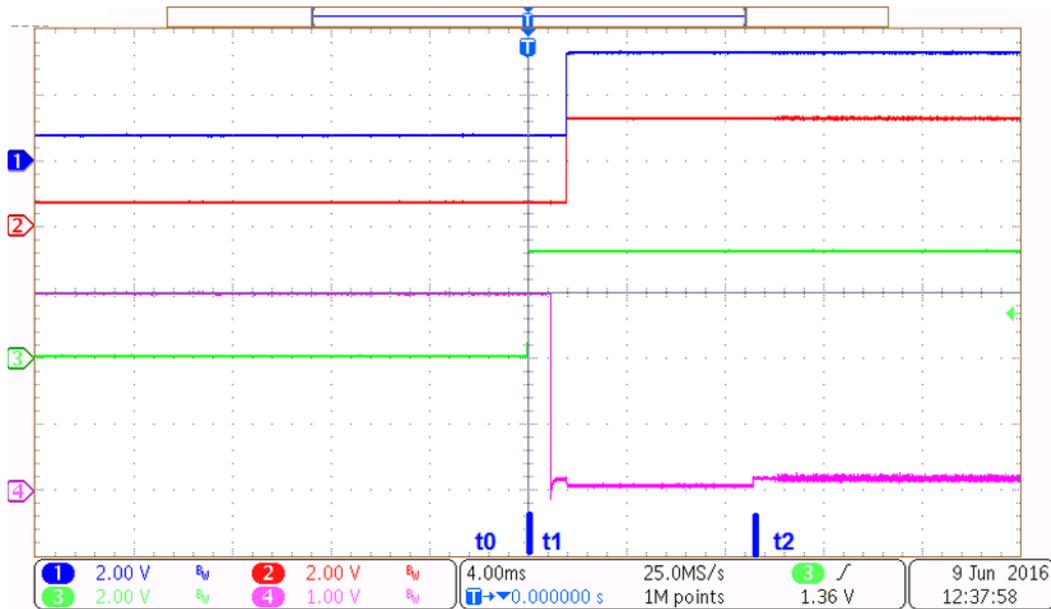
Figure 61. DISABLE Logic for Gate Drivers

Table 11. Timings for DISABLE Logic

STATE	CONDITION	OVERLOAD	GND_FAULT	TRIP	DISABLE
t0	At the power-up (with PWM not yet started)	LOW	LOW	LOW	HIGH
t1	Software makes TRIP signal to go HIGH and DISABLE LOW. Start-up sequence is started by software (All faults are ignored during this time)	LOW or HIGH	LOW or HIGH	HIGH	LOW
t2	The PWMs are running, gate-drivers are enabled. Faults reach their required states	HIGH	HIGH	HIGH	LOW

6.4 *Current Measurement Propagation Delay*

The propagation delay for the current measurement is captured by applying a 250-mV step input to the input of the AMC1301 (after de-soldering the 5-mΩ shunt from the PCB).

As shown in Figure 62, the input of the AMC1301 (blue waveform), the output of the AMC1301 (red waveform), the output of the OPA320 (green waveform), and the output of the comparator TLC372 (pink waveform) are captured to show the step response.

Figure 63 shows the propagation delay from the AMC1301 input to the AMC1301 output. Figure 64 shows the propagation delay from the AMC1301 output to the op amp OPA320 output. Figure 65 shows the propagation delay from the AMC1301 input to the comparator TLV372 output. Table 12 shows the summary of measured delays.

Table 12. Propagation Delays for Signal Chain

PARAMETER	PROPAGATION DELAY (µs)
Propagation delay from AMC1301 input to AMC1301 output	2.0
Propagation delay from AMC1301 output to op-amp OPA320 output	1.6
Propagation delay from AMC1301 input to comparator TLV372 output	4.4
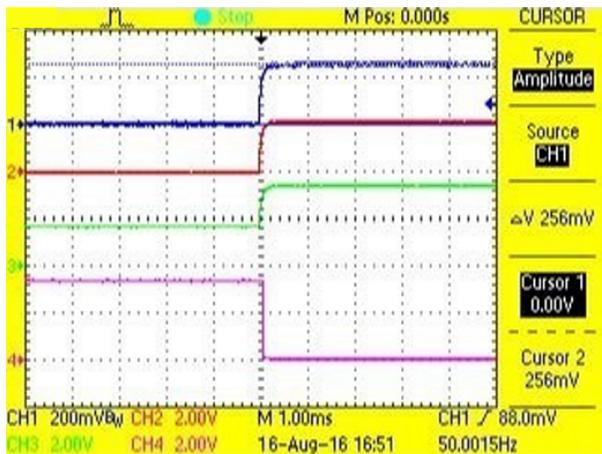
Figure 62. Step Response for Current Measurement Signal Chain
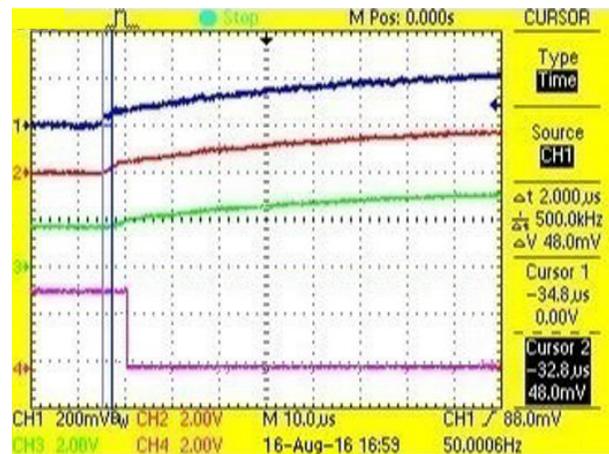
Figure 63. From AMC1301 Input to AMC1301 Output
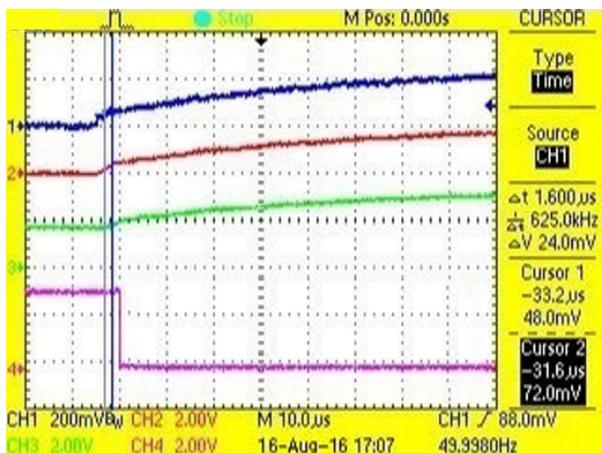
Figure 64. From AMC1301 Output to Op Amp Output
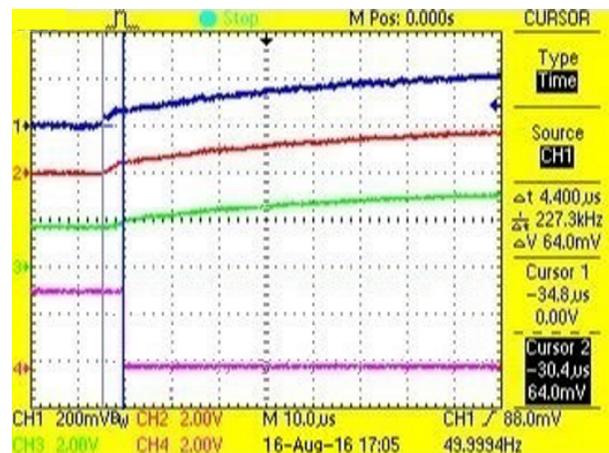
Figure 65. Propagation Delay From AMC1301 Input to Comparator Output

6.5 Current Measurement Accuracy

The current measurement accuracy is shown in Figure 66. The measurement is done from 1 to 35 A_{RMS}, which corresponds to the 50 A_{PEAK}. As observed, the calibrated error is less than ±0.5%.
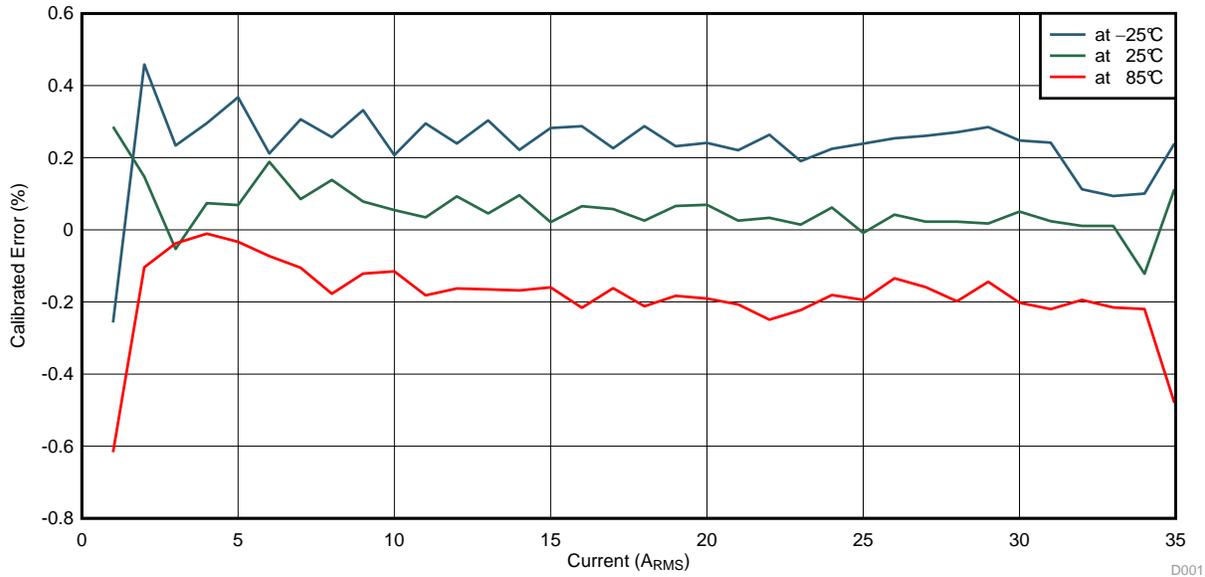
Figure 66. Current Measurement Accuracy

6.6 DC Bus Voltage Measurement

6.6.1 Accuracy of Measurement

The measurement accuracy for the DC bus voltage is shown in Figure 67. The measurement is done from 400-V to 1200-V DC. Figure 67 shows two accuracy graphs. One is DC bus voltage measurement uncalibrated STATIC accuracy, that is the motor is at standstill. Often this is not the only scenario. The accuracy varies if the motor is running. So the other graph shows the uncalibrated accuracy of DC bus voltage while motor is running at a speed of 1480 rpm.
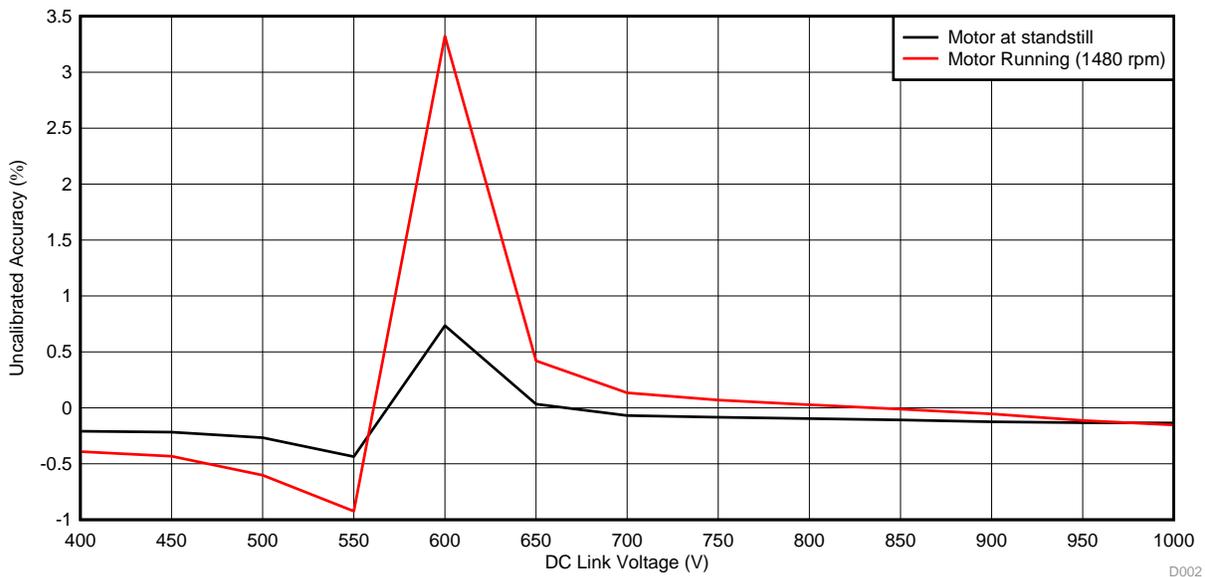
Figure 67. Accuracy of DC Bus Voltage Measurement

6.6.2 Transfer Function

Figure 68 shows the transfer function of the DC bus voltage measurement.
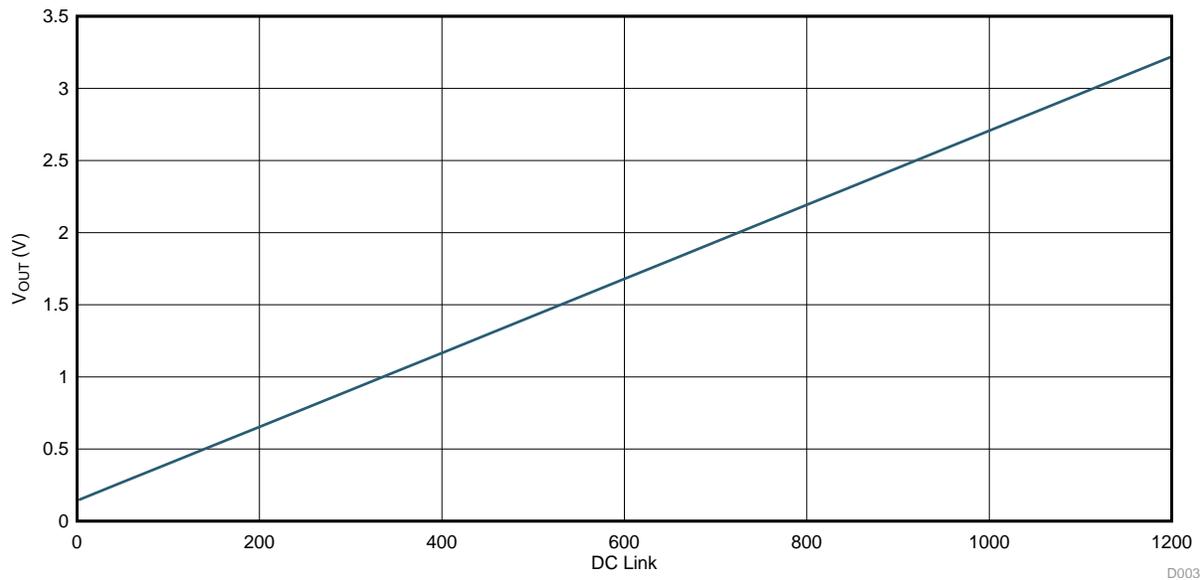
Figure 68. Transfer Function of DC Bus Voltage Measurement

6.7 IGBT Module Temperature Sensing

As explained in Section 4.6, the IGBT module has an internal NTC, and it is characterized for a temperature range of 0°C to 100°C. Figure 69 shows temperature versus the output of the temperature measurement signal chain.
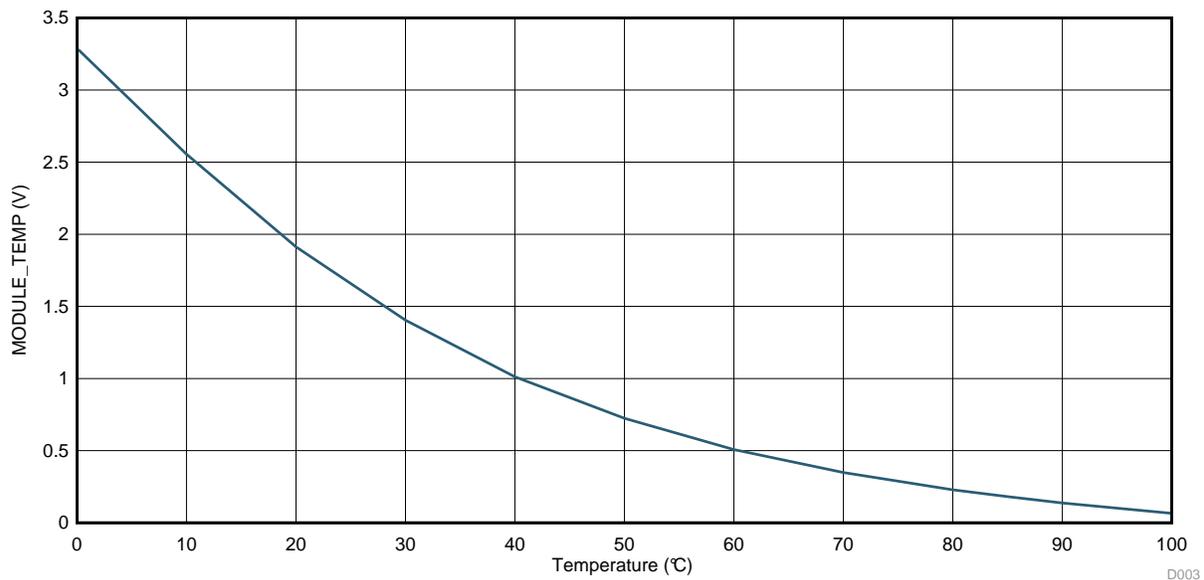
Figure 69. Transfer Function for IGBT Module NTC versus Temperature

6.8 Overload Detection

As explained in Section 4.7, the overload detection is implemented for all three channels, but the outputs of all overload comparators are shorted together to give single "OVERLOAD" signal.

6.8.1 Detection During Positive Half Cycle

Figure 70 shows the overload detection during a positive half cycle. The overload is detected at 49 A_{PEAK}.

NOTE: Blue: Current flowing through shunt, Red: OVERLOAD output from comparator
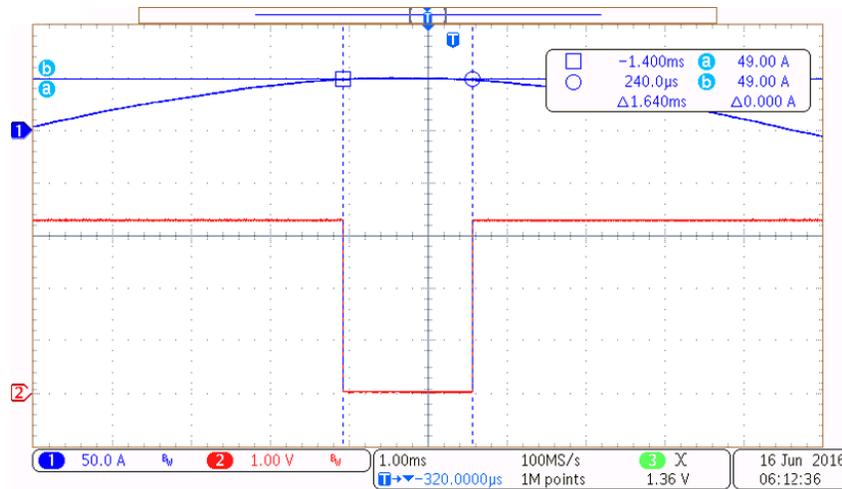
Figure 70. OVERLOAD Detection During Positive Half Cycle

6.8.2 Detection During Negative Half Cycle

Figure 71 shows the overload detection during a negative half cycle. The overload is detected at –49 A_{PEAK}.

NOTE: Blue: Current flowing through shunt, Red: OVERLOAD output from comparator
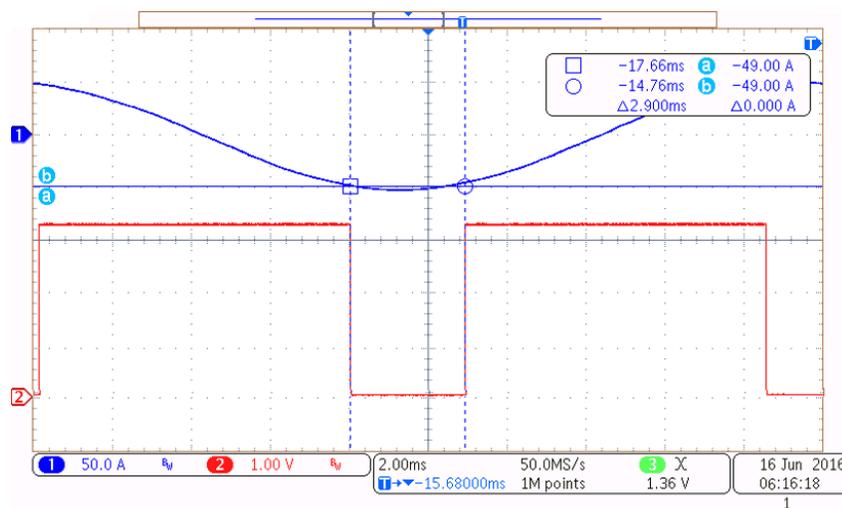
Figure 71. OVERLOAD Detection During Negative Half Cycle

6.8.3 Latching Function on TRIP Pin

The overload detect signal is latched on the TRIP pin as shown in Figure 72.

NOTE: Blue: GND_FAULT, Red: OVERLOAD, Green: TRIP, Pink: DISABLE for gate drivers
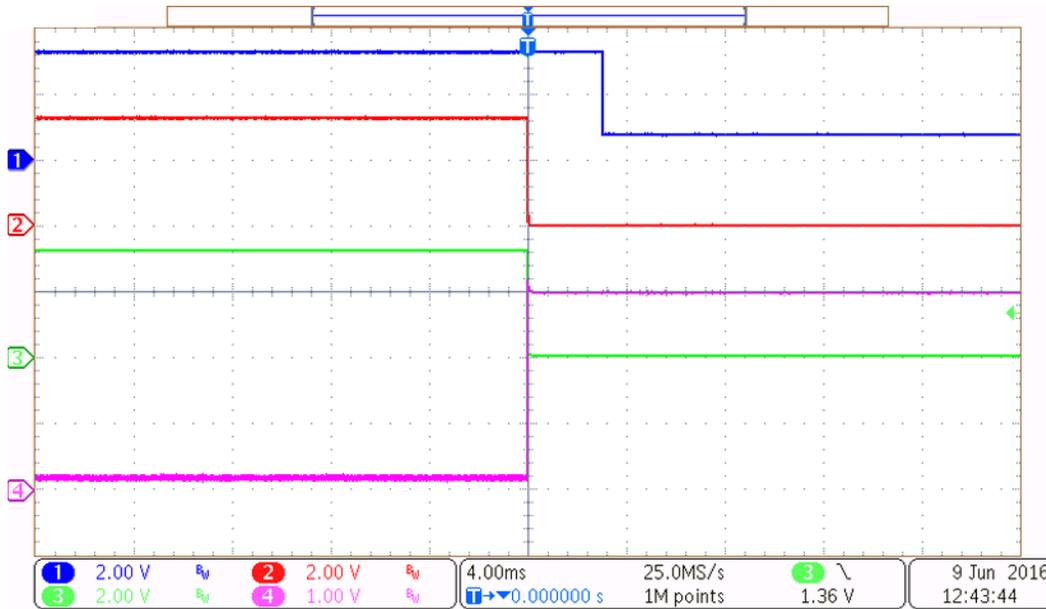
Figure 72. Latching of OVERLOAD Detect Signal on TRIP Pin

6.9 Ground Fault Detection

As explained in Section 4.8, the ground fault detection is implemented by combining the detected current for all three channels. In an ideal condition, when no ground fault has occurred, the "GND_FAULT" signal must be disabled (that is, active high). When ground fault condition occurs in any one channel (or more than one channel), the GND_FAULT detect is enabled (that is, goes low).

For capturing the ground fault occurrence, the current is passed through only one channel (V-channel) and "GND_FAULT" signal is observed.

6.9.1 Detection During Positive Half Cycle

Figure 73 shows the ground fault detection during a positive half cycle. The fault is detected at 5 A_{PEAK}.

NOTE: Blue: Current flowing through shunt, Red: GND_FAULT output from comparator
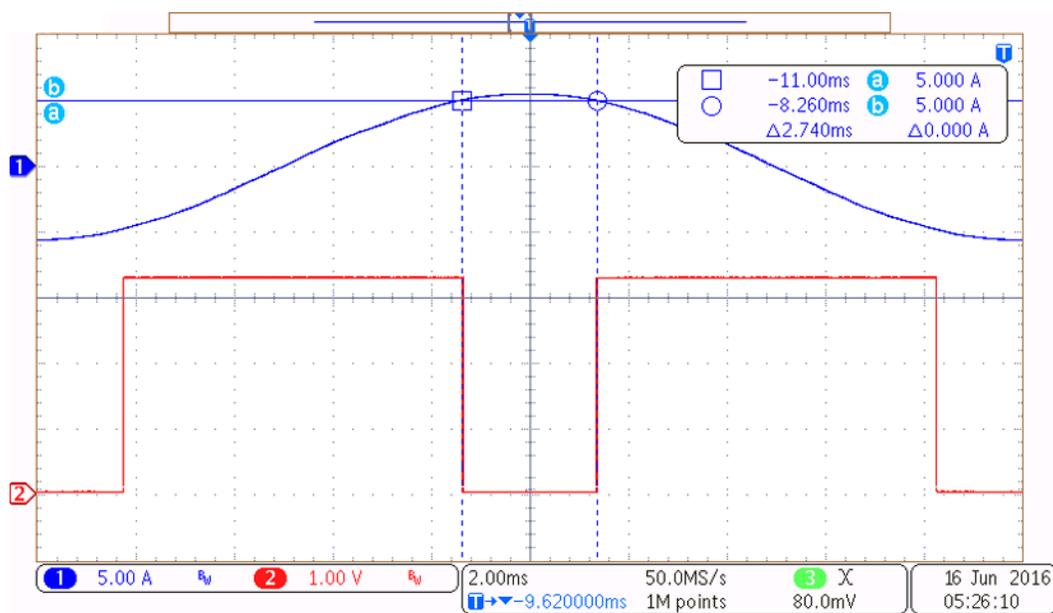
Figure 73. GND_FAULT Detection During Positive Half Cycle

6.9.2 Detection During Negative Half Cycle

Figure 74 shows the ground fault detection during a negative half cycle. The fault is detected at –5 A$_{PEAK}$.

NOTE: Blue: Current flowing through shunt, Red: GND_FAULT output from comparator
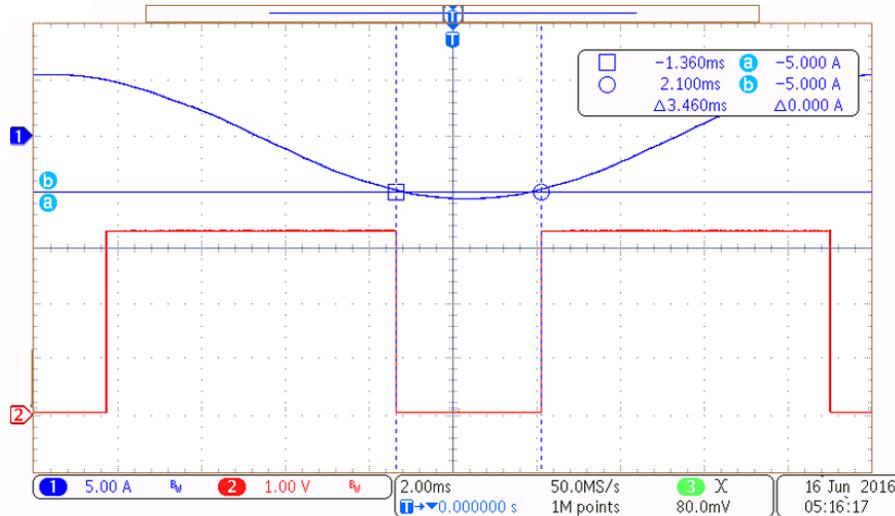
Figure 74. GND_FAULT Detection During Negative Half Cycle

6.9.3 Latching Function on TRIP Pin

The ground fault detect signal is latched on the TRIP pin as shown in Figure 75.

NOTE: Blue: GND_FAULT, Red: OVERLOAD, Green: TRIP, Pink: DISABLE for gate drivers
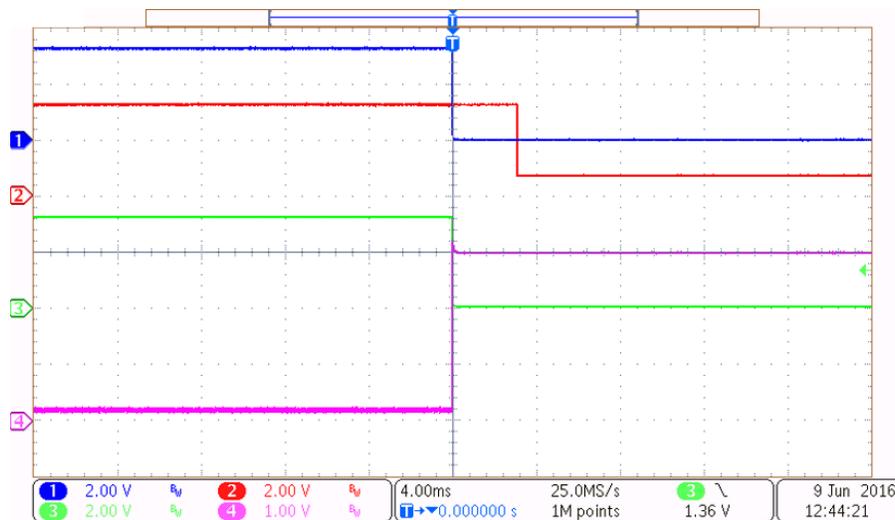
Figure 75. Latching of GND_FAULT Detect Signal on TRIP Pin

6.10   Testing Using Three-Phase AC Induction Motor and Load Setup

NOTE: TI recommends that a proper heatsink must be mounted before connecting the TIDA-00366 board to the motor.

The TIDA-00366 board is connected to the 5HP Three-Phase AC Induction Motor and load setup as shown in Figure 76. The motor is loaded up to 1.2 kW (limited by the load setup) and torque is applied according to the requirement.
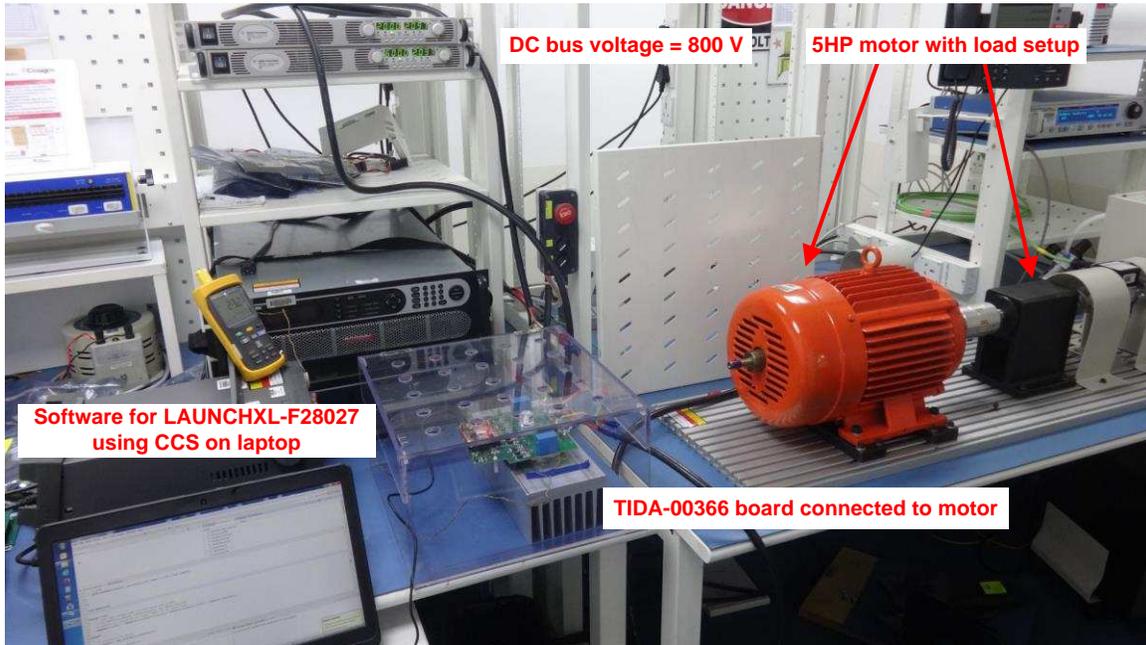
Figure 76. TIDA-00366 Test Using ACIM and Load Setup

Table 13 shows the test results for the load test along with temperature readings observed during the test. The test conditions for the load test are as follows:

- Ambient temperature = 25.4°C
- Air flow = 400 LFM
- Freq of operation = 60 Hz
- Shunt value used for load test = 50 mΩ
- Heatsink connected to the IGBT module

Table 13. Load Test Using Three-Phase AC Induction Motor

MEASURED ON MAGTROL EQUIPMENT			MEASURED ON DC SOURCE		MEASURED ON MULTIMETER	MEASURED ON OSCILLOSCOPE	MEASURED WITH THERMAL CAMERA
TORQUE	SPEED	OUTPUT (W)	VDC	IDC	AC RMS (MEASURED AT THE PHASE)	I_{RMS} (A)	MODULE TEMPERATURE (°C)
0.0	1770	10	757.6	0.425	400.7	1.559	48.7
1.0	1800	203	757.6	0.685	397.7	1.762	52.1
2.0	1800	420	757.6	0.944	395.1	2.074	56.5
3.0	1800	660	757.6	1.212	393.0	2.469	60.6
4.0	1800	860	757.6	1.485	391.3	2.933	64.1
5.0	1800	1070	757.6	1.767	390.2	3.445	68.8
5.6	1800	1220	757.6	1.984	389.5	3.862	73.4

During the load test, the current flowing through the motor terminal (W-Phase) is measured using a current probe, and the same current is observed at the MCU pin. Figure 77 shows the two waveforms for the same.

NOTE: Blue: Motor current measured with current probe, Pink: Voltage measured on MCU pin
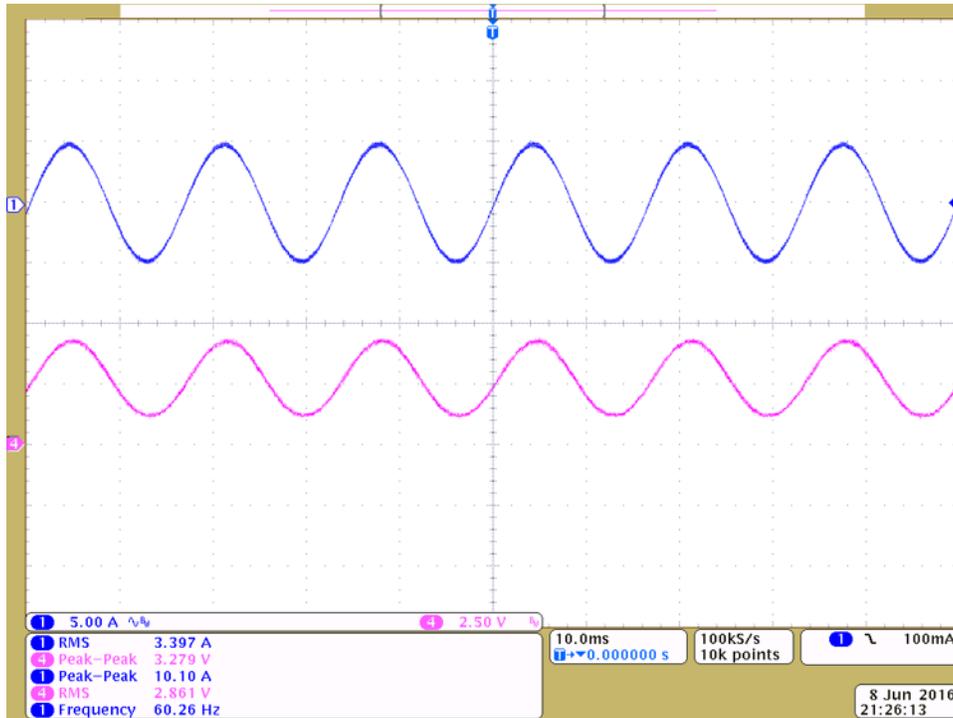
Figure 77. Motor Current Measurement

7   Design Files

7.1   *Schematics*

To download the schematics, see the design files at TIDA-00366.

7.2   *Bill of Materials*

To download the bill of materials (BOM), see the design files at TIDA-00366.

7.3   *PCB Layout Recommendations*

Figure 78 shows the top layer and Figure 79 shows the bottom layer of the PCB. The IGBT module is placed on the bottom layer and all the driving and sensing circuit is on the top layer.
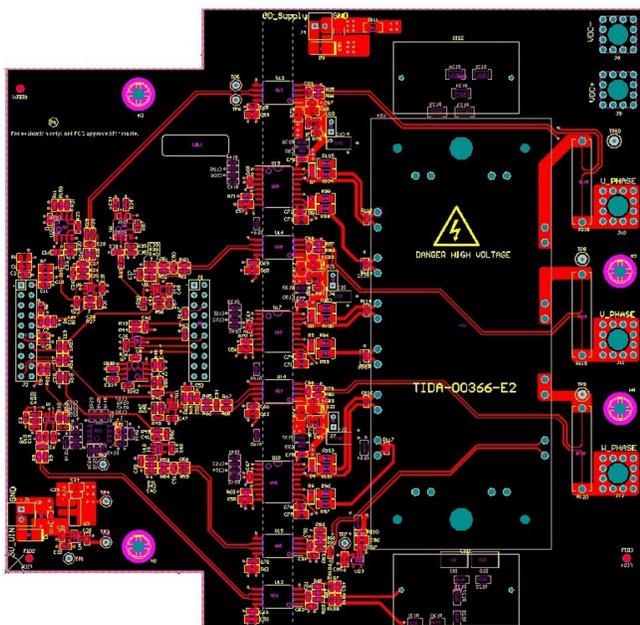
Figure 78. Top Layer
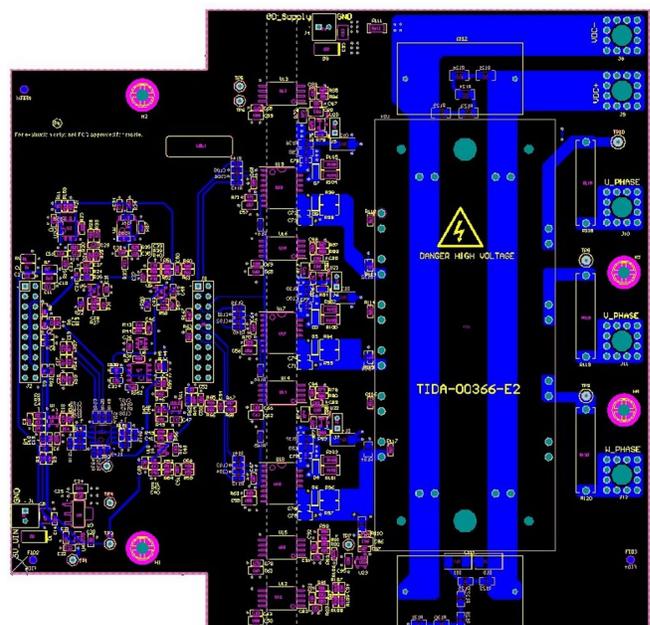
Figure 79. Bottom Layer

Figure 80 shows the ground layer and Figure 81 shows the power layer. The ground plane and power planes are cut wherever there is requirement for isolation from high-voltage side as well as between the low-side and high-side IGBT gate drivers.
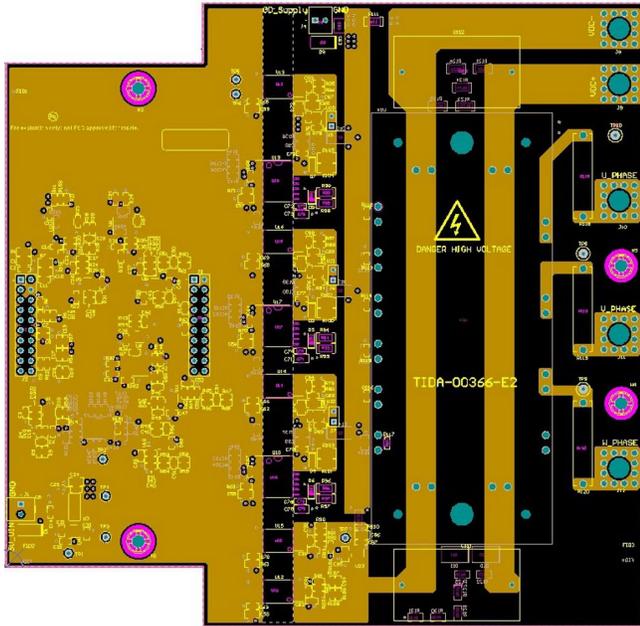
Figure 80. GND Layer
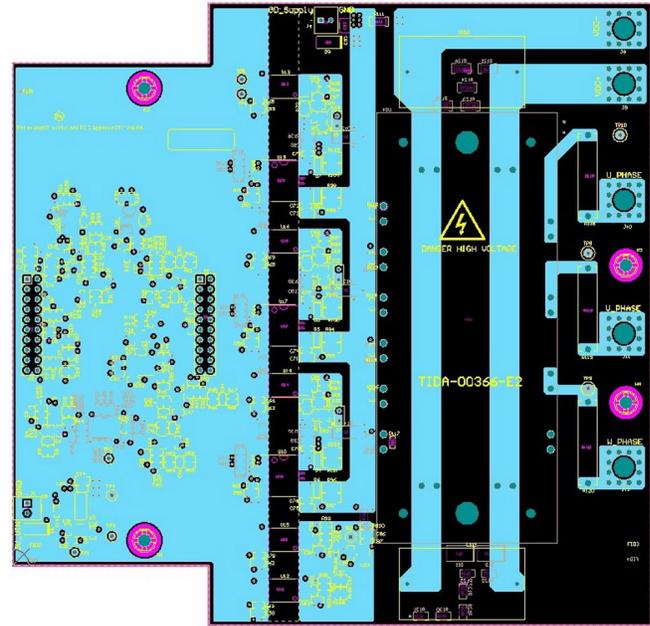
Figure 81. PWR Layer

Figure 82 shows the placement of components for the IGBT gate driver as well as the current sensing circuit. The figure also shows the critical placement of the decoupling capacitors that needs to be placed as close as possible to the AMC1301 while maintaining a differential routing of the input and output signals. To maintain the isolation barrier and the CMTI, keep the distance between the high-side ground (GND1) and the low-side ground (GND2) at a maximum; that is, the entire area underneath the device must be kept free of any conducting materials as shown in Figure 82. For the UCC21520, apart from placing the decoupling capacitors close to the supply pins, have multiple vias for VDD as well as VCCI supply lines. This will minimize the loop inductance of the VDD and VCCI loops.
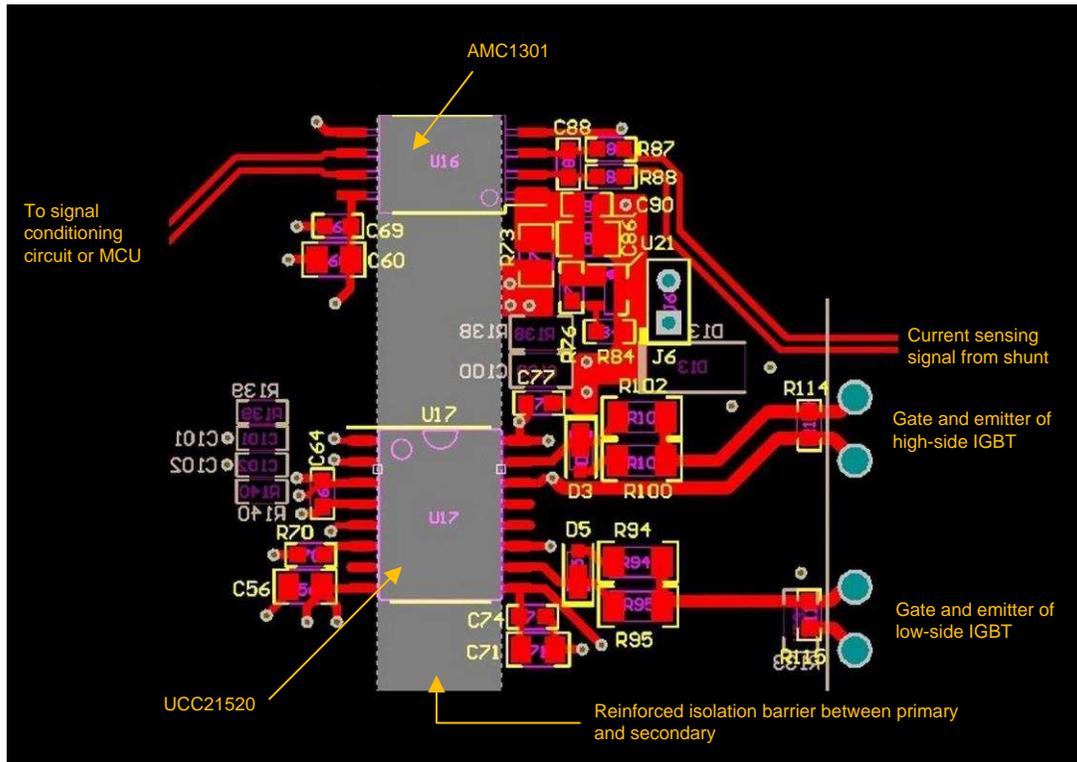
Figure 82. Gate Driver and Current Sensing Circuit

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The grounding and power supply planes for the gate drivers are shown in Figure 83 and Figure 84, respectively. As highlighted in Figure 83, the ground for the 16-V gate drive power supply (for the low-side IGBT gate driver) is isolated from the bootstrapped supply for the high-side IGBT gate-driver. Similarly, the power planes are isolated as shown in Figure 84.
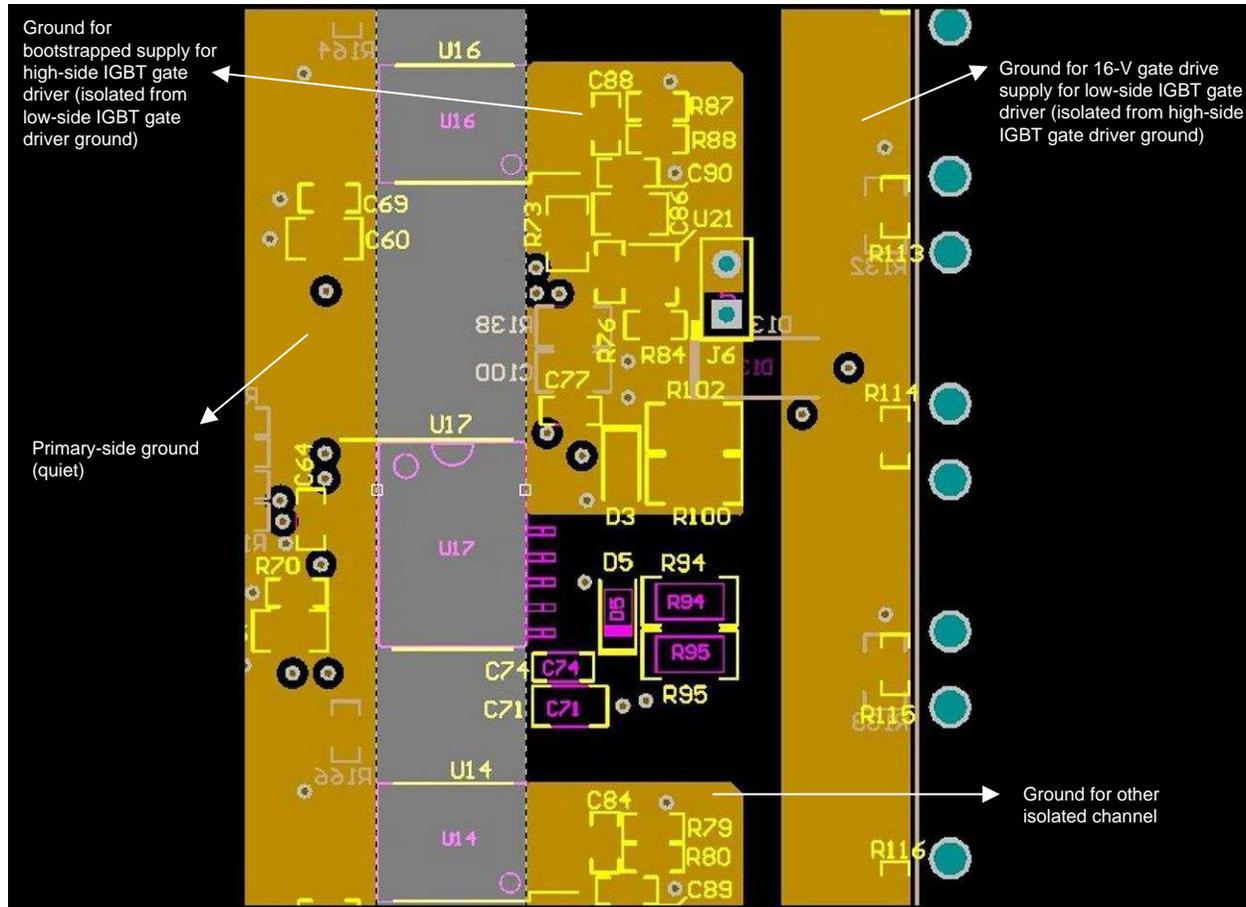
Figure 83. Grounding for High-Side and Low-Side IGBT Gate Drivers
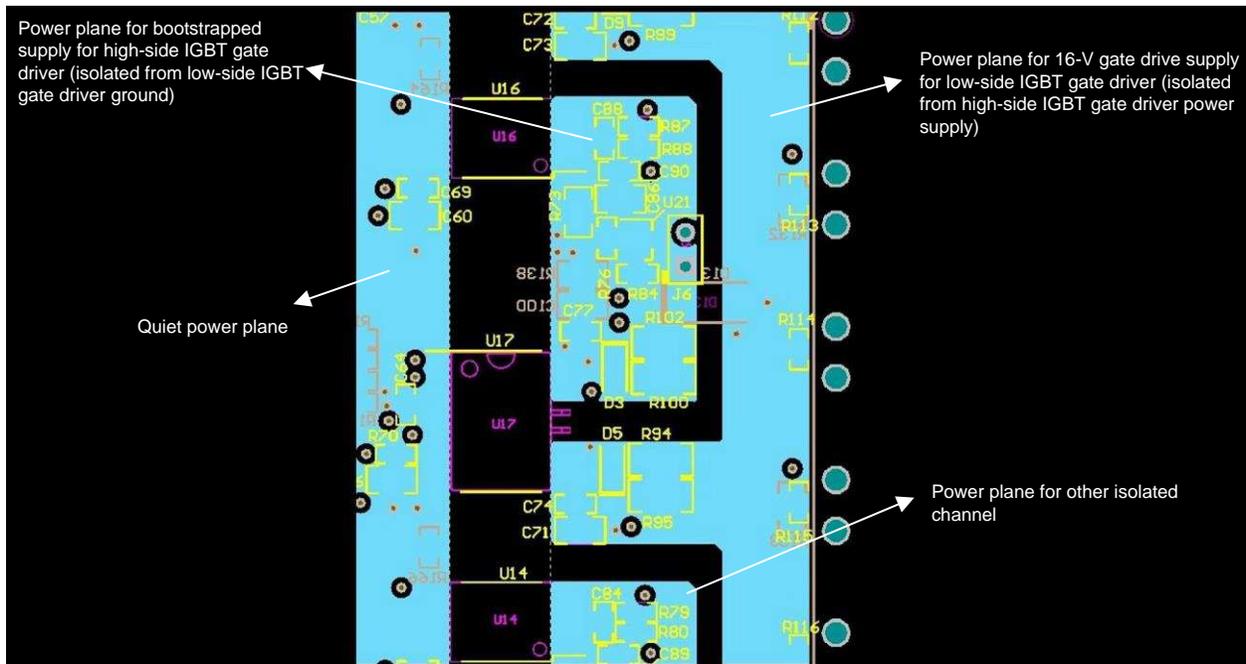
Figure 84. Power Planes for High-Side and Low-Side IGBT Gate-Drivers

Figure 85 shows that the return path for bottom IGBT gate signal is connected in the bottom layer. Also, the bootstrap diode is connected between the 16-V gate drive power supply (for the low-side IGBT gate driver) and the bootstrap power supply for the high-side IGBT gate driver.

Figure 85. Return Path

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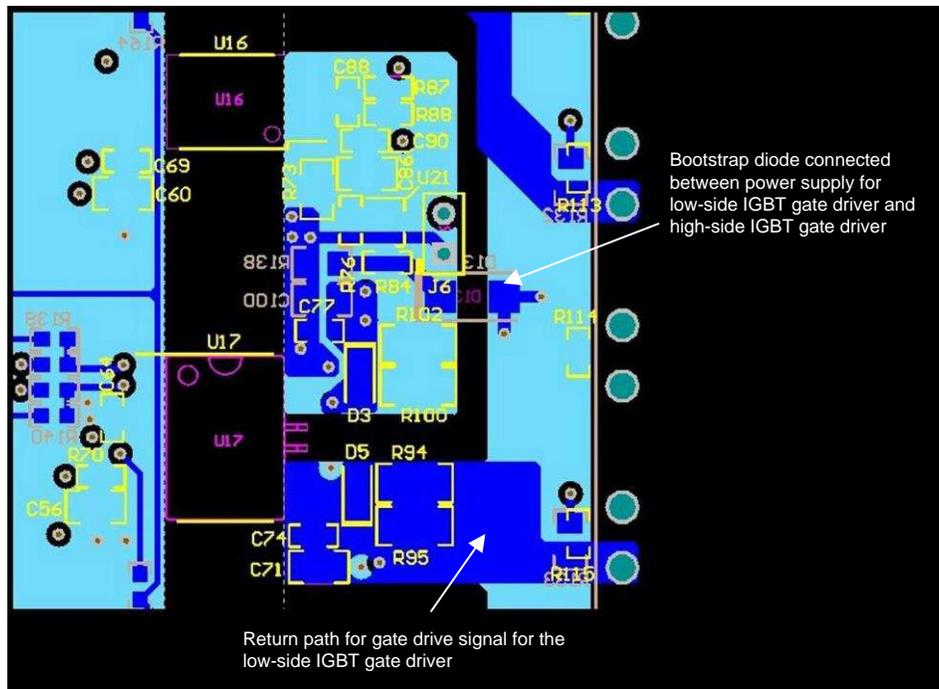
As explained in Section 4.2, the grounds for all the three channels are connected to VDC– through 0-Ω resistors (shorting links). Figure 86 and Figure 87 show the placement of these shorting links on the board.
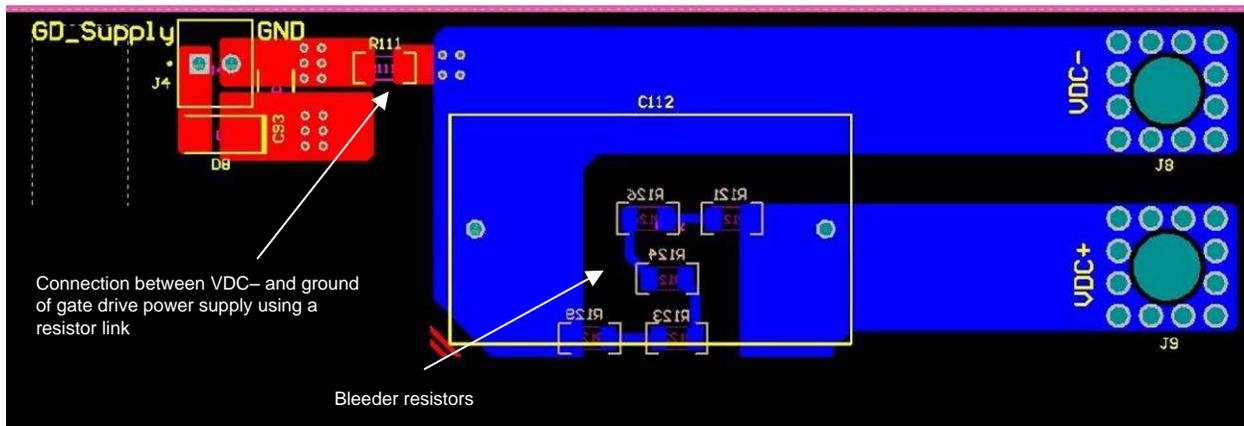
Figure 86. Shorting Link
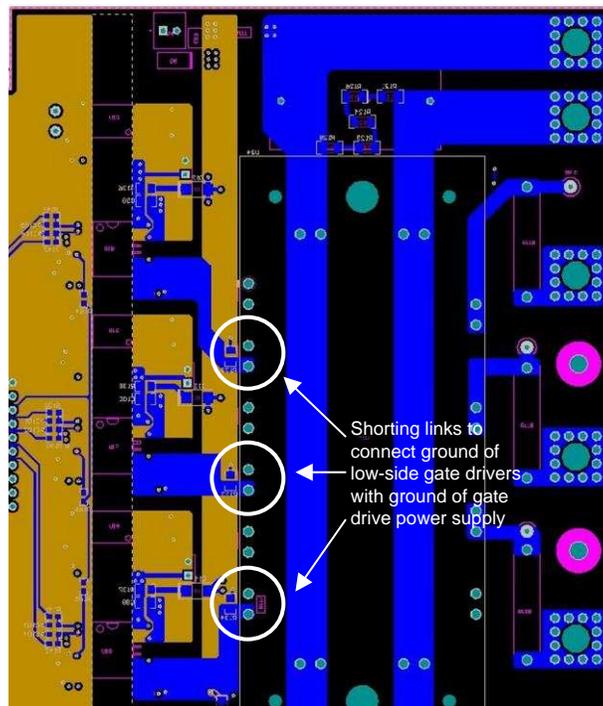
Figure 87. Shorting Links

Figure 88 shows the sensing circuit for DC bus voltage. The voltage sensing is done at the film capacitors as shown in Figure 88.

Figure 88. DC Bus Sensing Section

Since it is a high-voltage PCB, the sensing circuit cannot be in direct contact with the high-voltage planes. The sensing signals are orthogonal in the layout as shown in Figure 89.

Figure 89. Sensing and High-Voltage Planes

7.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00366.
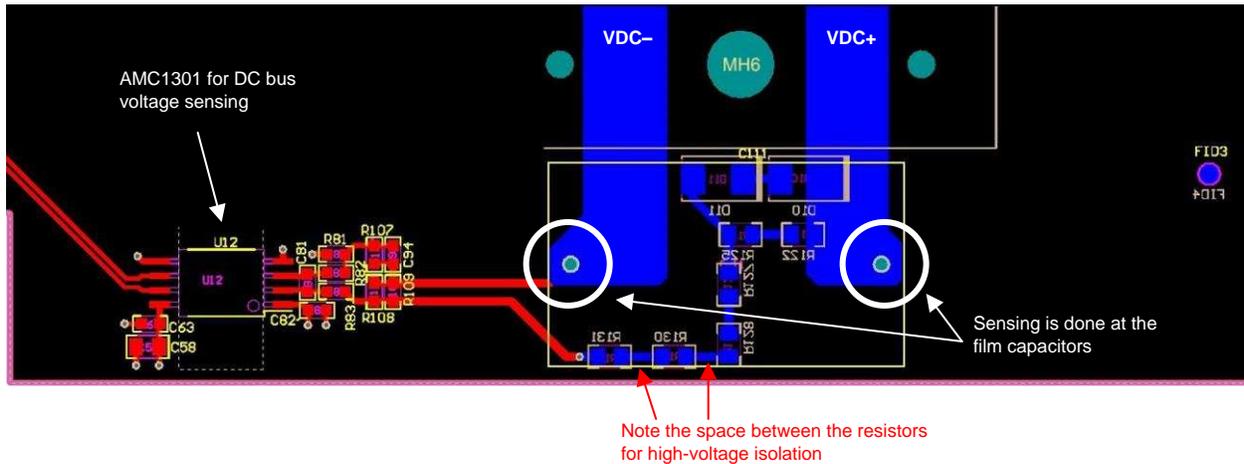
7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00366.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00366.

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00366.

8 References

1. Texas Instruments, *LAUNCHXL-F28027 C2000 Piccolo LaunchPad Experimenter Kit*, LAUNCHXL-F28027 User's Guide (SPRUHH2)

8.1 Trademarks

All trademarks are the property of their respective owners.

9 Terminology

PWM— Pulse width modulation

MCU— Microcontroller unit

IGBT— Insulated bipolar gate transistor

RPM— Rotation per minute

RMS— Root mean square

NTC— Negative temperature coefficient thermistor

10 About the Authors

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Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision A History

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