9601 Monostable Multivibrator

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF
T. I.																SN2960I	J①	N①							
FAIRCHILD																FM960I	D①			F①					
																FC960I	D①	P①		F①					
MOTOROLA																MC960I	L①			F①					
																MC860I	L①	P①		F①					
N. S. C.																DM960I	J①	N①		W①					
																DM860I	J①	N①		W①					
PHILIPS																									
SIGNETICS																									
SIEMENS																									
FUJITSU																									
HITACHI																									
MITSUBISHI																									
NEC																									
TOSHIBA																									

Electrical Characteristics SN2960I

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} (see Notes 1 and 2)	8 V	Operating free-air temperature range	0°C to 75°C
Input voltage	5.5 V	Storage temperature range	−65°C to 150°C
Interemitter voltage (see Note 3)	5.5 V	Steady-state input current range	−30 mA to 5 mA
		Low-level output current	50 mA

recommended operating conditions

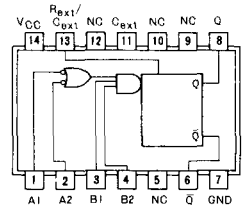
		SN2960I MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20	
	Low logic level			10	
Input data setup time, t_{setup}		40◇			ns
Input data hold time, t_{hold}		40◇			ns
Width of clear pulse, $t_{w(clear)}$		40◇			ns
External timing resistance		5		50	kΩ
External capacitance		No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal				50	pF
Operating free-air temperature, T_A		0		75	°C

electrical characteristics over operating free-air temperature range

PARAMETER *			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −800 μA, See Note 4	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 16 mA, See Note 4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	data inputs	V_{CC} = MAX, V_I = 2.4 V			40	μA
		clear input				80	
I_{IL}	Low-level input current	data inputs	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
		clear input				−3.2	
I_{OS}	Short-circuit output current◆		V_{CC} = MAX, See Note 4	−10		−40	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX, See Notes 5 and 6		23	28	mA
t_{PLH}	from either A input to Q output		V_{CC} = 5 V, T_A = 25°C, C_{ext} = 0, R_{ext} = 5 kΩ, C_L = 15 pF, R_L = 400 Ω		22	33	ns
t_{PLH}	from either B input to Q output				19	28	ns
t_{PHL}	from either A input to $\overline{Q}$ output				30	40	ns
t_{PHL}	from either B input to $\overline{Q}$ output				27	36	ns
$t_{w(min)}$	Minimum width of Q output pulse				45	65	ns
t_w	Width of Q output pulse		V_{CC} = 5 V, T_A = 25°C, C_{ext} = 1000 pF, R_{ext} = 10 kΩ, C_L = 15 pF, R_L = 400 Ω	3.08	3.42	3.76	μs

Pin Assignment (Top View)

①



positive logic: see function table (See Note A)

NC = No internal connection.

Function Table (See Note B)

INPUTS A1	A2	B1	B2	OUTPUTS Q	Q̄
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎎
L	X	H	↑	⎍	⎎
X	L	H	H	L	H
X	L	↑	H	⎍	⎎
X	L	H	↑	⎍	⎎
H	↓	H	H	⎍	⎎
↓	↓	H	H	⎍	⎎
↓	H	H	H	⎍	⎎

NOTES:

1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. The maximum V_{CC} value of 8 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately two forward-biased-diode drops below the V_{CC} voltage, so the primary limit on V_{CC} is that the voltage at any input may not go above 5.5 volts. This effectively limits the system V_{CC} to approximately 7 volts.
3. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies between inputs that go directly into the same AND or NAND gate in the functional block diagram.
4. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
5. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, C_{ext} = 0.02 μF, R_{ext} = 25 kΩ, R_{int} and all outputs open.
6. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, C_{ext} = 0.02 μF, R_{ext} = 25 kΩ, R_{int} and all outputs open.

A. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

B. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎎ = one low-level pulse, X = irrelevant (any input, including transitions).

† For conditions shown as MIN or MAX, use the value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

◆ Not more than one output should be shorted at a time.

* t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.

◇ These conditions are recommended for use at V_{CC} = 5 V, T_A = 25°C.