Functional Safety Information

SN74AHCT32-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the SN74AHCT32-Q1 (N, D, NS, DB, PW, DGV, RGY, and BQA package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

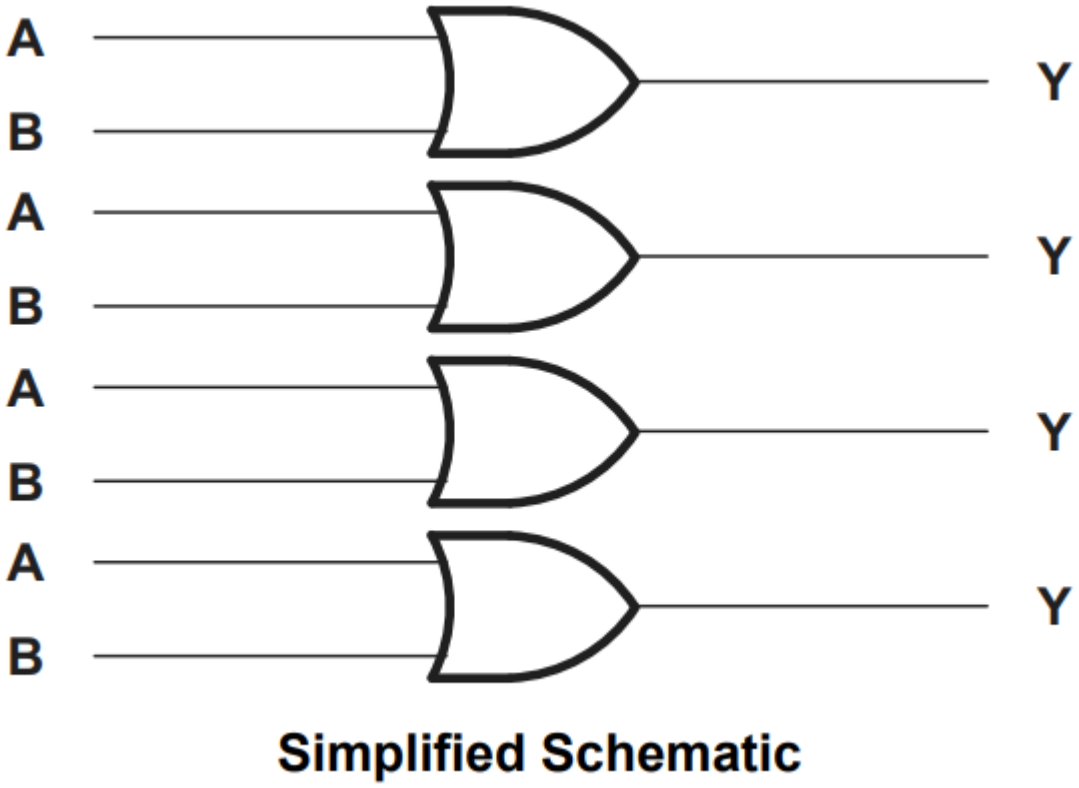

Figure 1-1. Functional Block Diagram

The SN74AHCT32-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

2.1 N, D, NS, DB, PW, DGV, RGY, and BQA Package

This section provides functional safety failure in time (FIT) rates for the N, D, NS, DB, PW, DGV, RGY, and BQA package of the SN74AHCT32-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)							
	N	D	NS	DB	PW	DGV	RGY	BQA
Total component FIT rate	45	17	20	13	11	8	9	6
Die FIT rate	2	2	3	3	3	2	3	2
Package FIT rate	43	15	17	10	8	6	6	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 50 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
3	CMOS, BICMOS Digital, analog, or mixed	5 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74AHCT32-Q1 in comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output stuck-at fault	30%
Output open (HIZ)	25%
Output functional – out of specification timing or voltage	45%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the SN74AHCT32-Q1 (N, D, NS, DB, PW, DGV, RGY, and BQA and PackageType2 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see and .)
- Pin open-circuited (see and)
- Pin short-circuited to an adjacent pin (see and)
- Pin short-circuited to supply (see and)

through also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- External pullup resistor on $\overline{CS}$ to VDD
- RC filter on every analog input, AINx.

  Series resistors are sized to limit the input currents into the analog inputs to <10 mA in all circumstances (for example, in case the device is unpowered and the input signal is applied).
- The device is the only slave on the SPI bus.

4.1 N, D, NS, DB, PW, DGV, RGY, and BQA and TSSOP Package

and show the SN74AHCT32-Q1 pin diagrams for the N, D, NS, DB, PW, DGV, RGY, and BQA and TSSOP package. The following pin FMA tables may be provided as a reference based on each pin type (input, output, GND, VCC, etc.) instead of pin name (A, Y, GND, VCC, etc.). For a detailed description of the device pins and their corresponding pin type, please refer to the *Pin Configuration and Functions* section in the SN74AHCT32-Q1 data sheet.

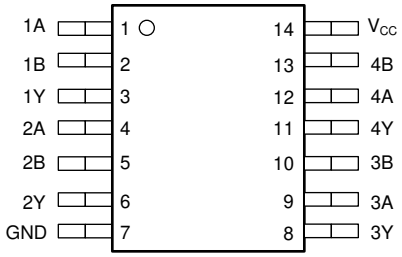

Figure 4-1. Pin Diagram (N, D, NS, DB, PW, DGV, RGY, and BQA) Package

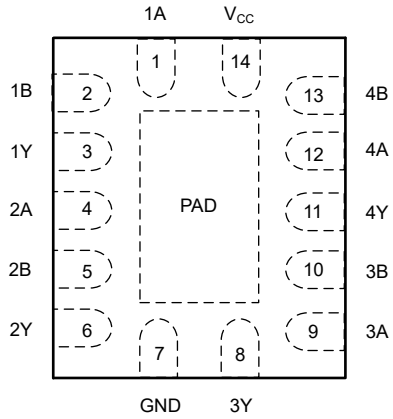

Figure 4-2. Pin Diagram (TSSOP) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1-4A; 1-4B	1, 2, 4, 5, 9, 10, 12, 13	Input pin functionality is defined such as input is LOW - see Device Function Table (for example, if buffer input is GND, output will always be driven LOW).	B
1-4Y	3, 6, 8, 11	Can cause excessive output current, output will not switch (for example, if buffer output is shorted to ground and is attempting to drive to VCC).	A
V_{CC}	14	Device will not be powered, because short is external to device. System level damage may occur in this scenario.	B
GND	7	Normal operation.	D
Thermal Pad	-	Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1-4A; 1-4B	1, 2, 4, 5, 9, 10, 12, 13	Pin is floating, can change output state and cause excessive current from VCC to GND - see Implications of Slow or Floating CMOS Inputs - ti.com/lit/scba004.	A
1-4Y	3, 6, 8, 11	Normal operation.	D
V_{CC}	14	Device will not be powered.	B
GND	7	Device will not be powered.	B
Thermal pad	-	Normal operation.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
1-4A; 1-4B	1-4A; 1-4B	Two inputs shorted together will not cause damage unless there is external bus contention that drives the input such that VIL < Input Voltage < VIH in which case excessive supply current to gnd may cause damage. System level damage may occur in this scenario.	A
1-4A; 1-4B	1-4Y	Can cause excessive output current, output will not switch (for example, if inverter input is shorted to output).	A
1-4A; 1-4B	GND	See response in "Short to GND" table.	A
1-4A; 1-4B	Thermal Pad	When Thermal Pad is tied to GND: See response in "Short to GND" table.	A
1-4A; 1-4B	V_{CC}	See response in "Short to VCC" table.	A
1-4Y	1-4Y	Can cause excessive output current, output will not switch (for example, if one output is driving to VCC and another output is driving to GND).	A
1-4Y	GND	See response in "Short to GND" table	A
1-4Y	Thermal Pad	When Thermal Pad is tied to GND: See response in "Short to GND" table.	A
1-4Y	V_{CC}	See response in "Short to VCC" table	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name		Description of Potential Failure Effect(s)	Failure Effect Class
1-4A; 1-4B	1, 2, 4, 5, 9, 10, 12, 13	Input pin functionality is defined such as input is HIGH - see Device Function Table (for example, if buffer input is VCC, output will always be driven HIGH).	B
1-4Y	3, 6, 8, 11	Can cause excessive output current, output will not switch (for example, if buffer output is shorted to VCC and is attempting to drive to GND).	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name		Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC}	14	Normal operation.	D
GND	7	Device will not be powered, because short is external to device. System level damage may occur in this scenario.	B
Thermal pad	-	Device will not be powered, because short is external to device. System level damage may occur in this scenario.	B

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