DATA BOOK
PACKAGE OUTLINE

DRAFTSMAN: E.REY	DATE: 07/10/2013
DESIGNER: E.REY	DATE: 07/10/2013
CHECKER: J.HOLLOWAY	DATE: 07/10/2013
ENGINEER: E.REY	DATE: 07/10/2013
APPROVED: J.HOLLOWAY	DATE: 07/10/2013
RELEASED: M.MURRAY	DATE: 07/10/2013
TEMPLATE INFO: EDGE# 4218519 REV A	DATE: 03/22/2013

DIMENSIONS IN MILLIMETERS

TEXAS INSTRUMENTS
SEMICONDUCTOR OPERATIONS

CODE IDENTITY NUMBER
01295

ePOD, DGV0056A / TVSOP,
56 PIN, 0.4MM PITCH

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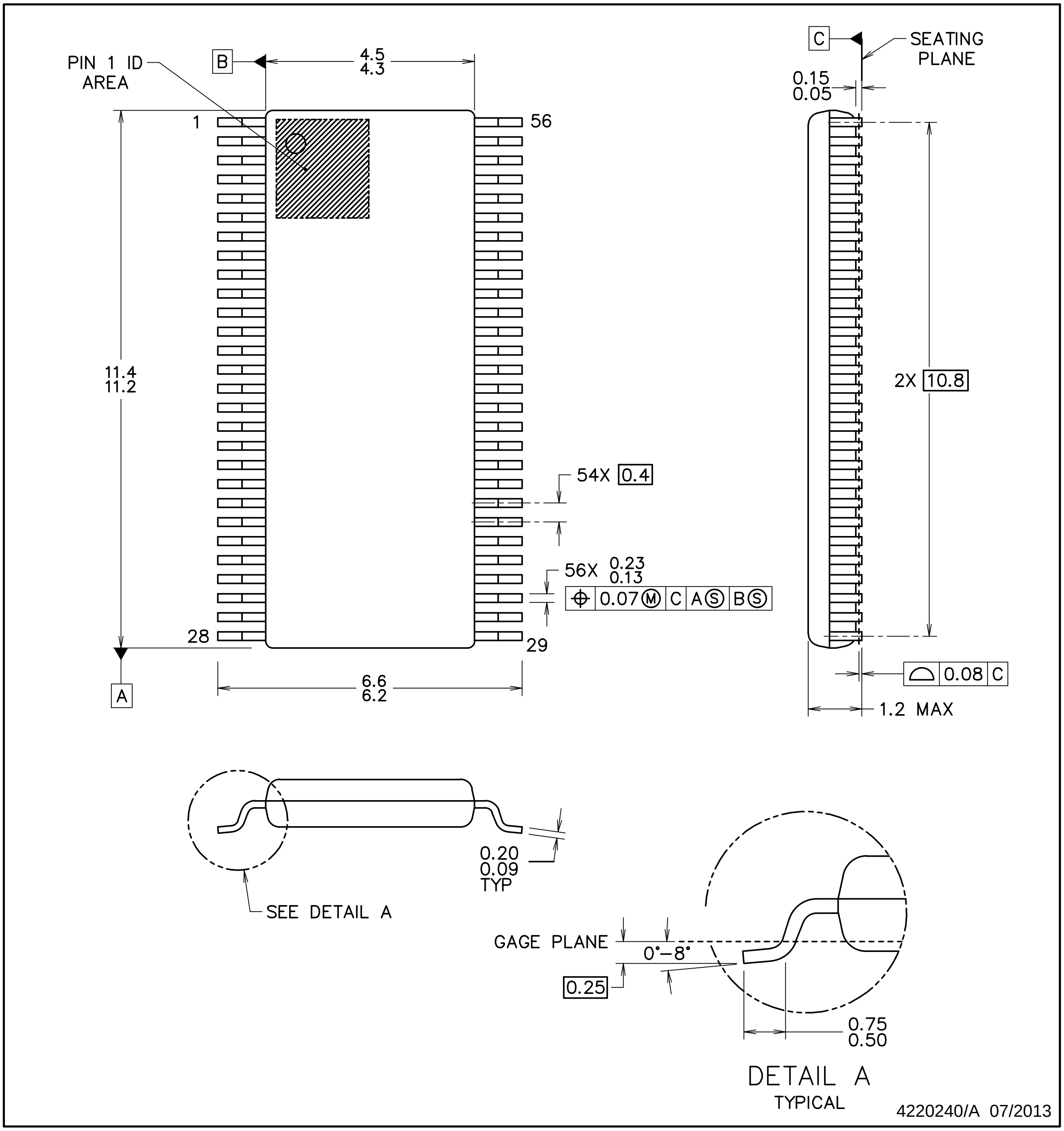
PACKAGE OUTLINE

DGV0056A

TVSOP - 1.2mm max height

TVSOP



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NOTES:

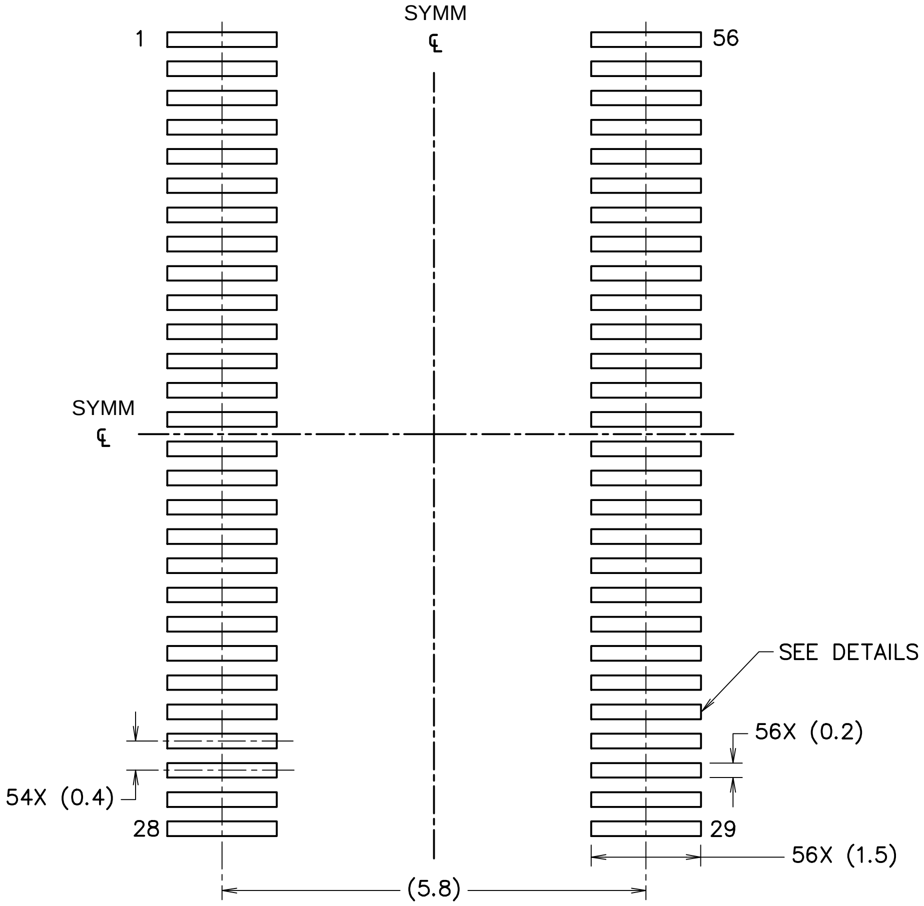
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-194, variation AF.

EXAMPLE BOARD LAYOUT

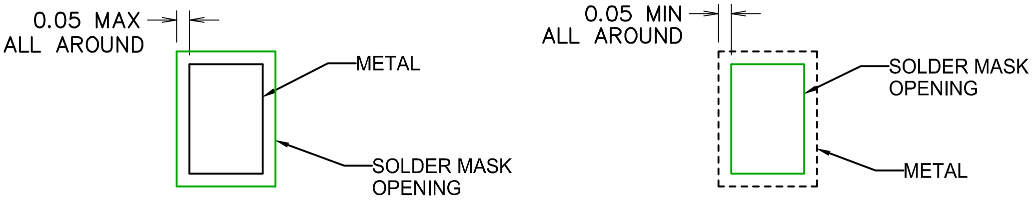
DGV0056A

TVSOP - 1.2mm max height

TVSOP



LAND PATTERN EXAMPLE



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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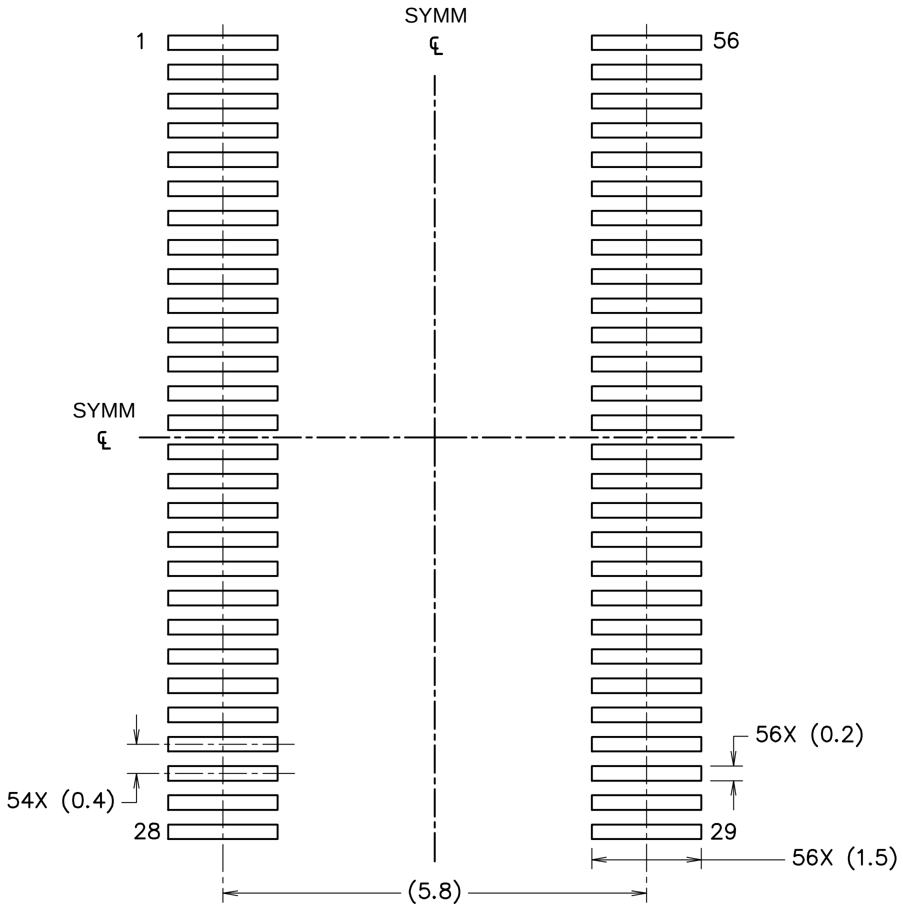
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

TVSOP - 1.2mm max height



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

REVISIONS				
REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2134218	07/10/2013	E.REY

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