F75914

4-bit Bidirectional Level Shifter

July, 2017
V0.13P

F75914 Datasheet Revision History

Version	Date	Revision History
V0.10	May, 2017	Preliminary version
V0.11	June, 2017	Made clarification and correction
V0.12	June, 2017	Made clarification and correction
V0.13	July, 2017	Modify Ordering Information

Table of Contents

1 General Description

The F75914 is a 4 bit bidirectional voltage level shifter with Enable (EN) input.

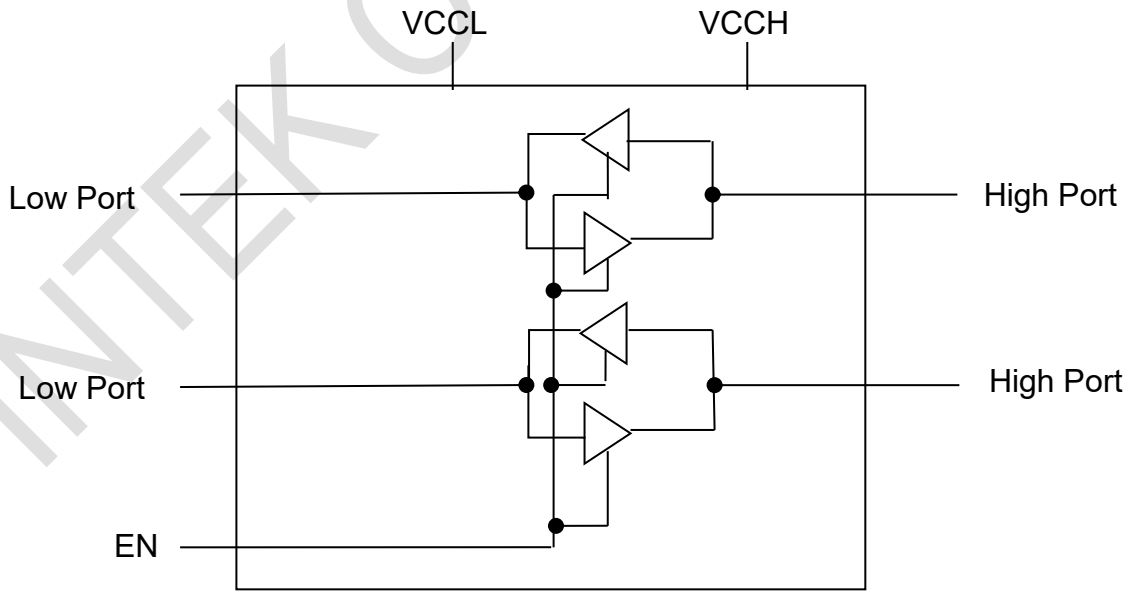
The L port is designed to track VCCL. VCCL accepts any supply voltage from 1.1 V to [VCCH - 0.7 V]. The H port is designed to track VCCH. VCCH accept any supply voltage from 1.8V to 3.3V. This allows for universal low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V and 2.5V voltage nodes. VCCH should exceed VCL over 0.7V.

The F75914 is designed that the EN input circuit is supplied by VCCL. When the Enable (EN) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, EN should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

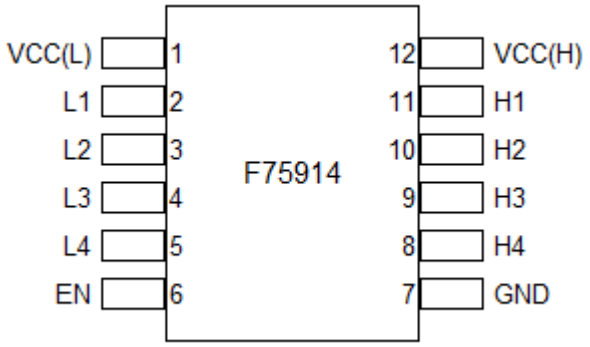
2 Feature

- 4-Bit bidirectional level shifter
- Voltage level shifting from L-Port (1.1V to VCCH -0.7V)
- Voltage level shifting from H-Port (1.8V to 3.3V)
- Max data rates
  - 130 Mbps (Vcc(L) = 2.5V to Vcc(H) = 3.3V)
- High impedance bus pin when Power-off
- EN input circuit referenced to VCCL
- 12-DFN Green Package

3 Block Diagram



4 Pin Configuration



Pin Configuration of F75914

5 Pin Description

Pin	Name	Type	Description
1	VCCL	P	Port L power supply
2	L1	Analog	Input/output port L1 (lower voltage side)
3	L2	Analog	Input/output port L2 (lower voltage side)
4	L3	Analog	Input/output port L3 (lower voltage side)
5	L4	Analog	Input/output port L4 (lower voltage side)
6	EN	IN	Enable input (active high). Referenced to VCCL
7	GND	GND	Ground
8	H4	Analog	Input/output port 4. Referenced to V_{CCH}. Internal pull high 1K**Ω***
9	H3	Analog	Input/output port 3. Referenced to V_{CCH}. Internal pull high 1K**Ω***
10	H2	Analog	Input/output port 2. Referenced to V_{CCH}. Internal pull high 1K**Ω***
11	H1	Analog	Input/output port 1. Referenced to V_{CCH}. Internal pull high 1K**Ω***
12	VCCH	P	Port H power supply

*: Pease note that internal pull high resistor will be a divider with external resistor.

6 Principles and Operation

Power Up

During operation, ensure that VCCL ≤ VCCH at all times. During power-up sequencing, VCCL ≥ VCCH does not damage the device, so any power supply can be ramped up first. The F75914 has circuitry that disables all output ports when either VCC is switched off (VCCL/H = 0 V or VCCH/L = 0 V).

Enable and Disable

The F75914 has an EN input that is used to disable the device by setting EN = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when EN goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after EN is taken high.

Application and Notification on I/O Lines

The F75914 is designed to drive capacitive loads of up to 100 pF. The output drivers of the F75914 do not have low dc drive strength. Pullup or pulldown resistors are not recommended to be connected externally to the data I/Os. For the same reason, the F75914 should not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on bidirectional data I/O.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings*

over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCH}	Supply voltage port High side range		-0.5	+3.6	V
V_{CCL}	Supply voltage port Low side range		-0.5	+3.6	V
$V_{I/O}$	Input/output voltage range	Port low side, enable pin (EN)	-0.5	+3.6	V
		Port high side	-0.5	+5	V
I_O	Continuous output current			16	mA
T_{stg}	Storage temperature range		-55	145	°C
T_{amb}	Ambient temperature(Design Guarantee)	Operating in the free air	-40	85	°C

*Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Static Characteristics

Typical values with VCCL = 1.1V, VCCH = 3.3V, GND = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCH}	Supply voltage port High side		1.8		3.3	V
V_{CCL}	Supply voltage port Low side		1.1		V_{CCH} –0.7	V
I_{CCL}	Supply current port Low side	All port low side static High		0		mA
		All port low side static Low		0		mA
I_{CCH}	Supply current port High side	All port High side static High		0.25		mA

Input and output of port Low side (L1:L4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	Port Low side	0.7 V_{CCL}		V_{CCL}	V
V_{IL}	Low-level input voltage	Port Low side	-0.5		+0.3 V_{CCL}	V
V_{OH}	High-level output voltage	Port Low side; I_{OH} = –20 μA	V_{CCH} – 0.25			V
V_{OL}	Low-level output voltage	Port Low side; I_{OL} = 20 μA			0.25	V
I_{IL}	Input leakage current	V_I=$Vcc_{(L)}$			1	uA
I_{OL}	Output leakage current	V_O= $Vcc_{(L)}$			1	uA
C_{iO}	Input/output capacitance			5		pF

Input and output of port High side (H1:H4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	Port High side	0.7 V_{CCH}		V_{CCH}	V
V_{IL}	Low-level input voltage	Port Low side	-0.5		+0.3 V_{CCH}	V
V_{OH}	High-level output voltage	Port High side I_{OH} = –20 μA	V_{CCL} – 0.4			V
V_{OL}	Low-level output voltage	Port High side I_{OL} = 20 μA			0.25	V
I_{IH}	Input leakage current	V_I=$Vcc_{(H)}$			1	uA
I_{OH}	Output leakage current	V_O= $Vcc_{(H)}$			1	uA
C_{iO}	Input/output capacitance			5		pF

Enable

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		0.7 V_{CCL}		V_{CCH}	V
V_{IL}	Low-level input voltage		-0.5		+0.3 V_{CCL}	V
I_{IH}	High-level input current				1	uA
I_{IL}	Low-level input current				1	uA
C_i	Input capacitance	V_I=3.6V or 0V		4		pF

7.3 Timing Requirements

over recommended operating free-air temperature range, **$V_{CC(L)}$ = 1.1V ± 0.05V** (unless otherwise noted)

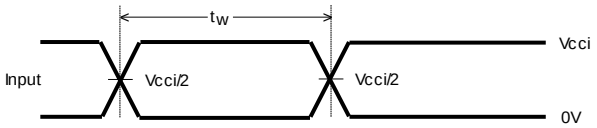
			$V_{CC(H)}$ = 1.8V		$V_{CC(H)}$ = 2.5V		$V_{CC(H)}$ = 3.3V		Unit
			Min	Max	Min	Max	Min	Max	
	Data rate			80		80		80	Mbps
t_w	Pulse duration	Data inputs	12.5		12.5		12.5		ns

over recommended operating free-air temperature range, **$V_{CC(L)}$ = 1.8V ± 0.1V** (unless otherwise noted)

			$V_{CC(H)}$ = 2.5V		$V_{CC(H)}$ = 3.3V		Unit
			Min	Max	Min	Max	
	Data rate			120		110	Mbps
t_w	Pulse duration	Data inputs	8.3		9		ns

over recommended operating free-air temperature range, **$V_{CC(L)}$ = 2.5V ± 0.1V** (unless otherwise noted)

			$V_{CC(H)}$ = 3.3V		Unit
			Min	Max	
	Data rate			130	Mbps
t_w	Pulse duration	Data inputs	7.8		ns



Vcci is the Vcc associated with the input port.

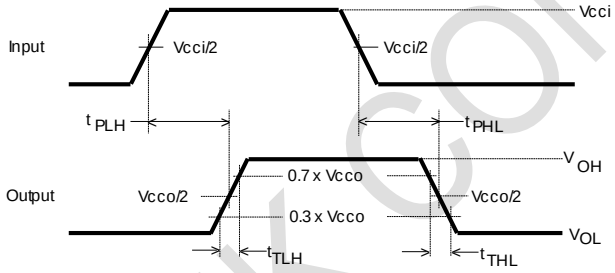
Figure. Voltage Waveforms Pulse Duration

7.4 Dynamic Characteristics

over recommended operating free-air temperature range, **$V_{CC(L)}$ = 1.8V; $V_{CC(H)}$ = 3.3V** (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	Low to High propagation delay	Port H to port L(1)	0.9	1.65	2.5	ns
t_{PHL}	High to Low propagation delay		1.0	1.9	2.9	
t_{PLH}	Low to High propagation delay	Port L to port H(1)	1.3	2.5	3.8	ns
t_{PHL}	High to Low propagation delay		1.5	2.8	4.3	
t_{TLH}	Low to High output transition time	Port L(1)	1.0	1.9	2.9	ns
t_{THL}	High to Low output transition time		1.0	1.8	2.8	
t_{TLH}	Low to High output transition time	Port H(1)	0.9	1.7	2.6	ns
t_{THL}	High to Low output transition time		0.9	1.7	2.6	
t_{en}	Enable time	EN high before enable condition	1.4	2.7	4.1	ns
t_{dis}	Disable time	EN low after disable condition	1.4	2.7	4.1	ns
$t_{SK(O)}$	Channel-to-channel skew		-0.8	0	0.8	ns
Max data rate					110	Mbps
Max clock rate					55(2)	MHz

(1) Load capacitance = 20 pF.
(2) Duty rate = 50%



A. Vcci is the Vcc associated with the input port.
B. Vcco is the Vcc associated with the output port.

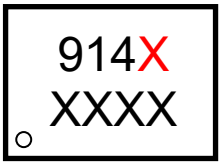
Figure. Voltage Waveforms Propagation Delay times

8 Ordering Information

Part Number	Package Type
F75914V	DFN-12

9 Top Marking Specification

DFN-12



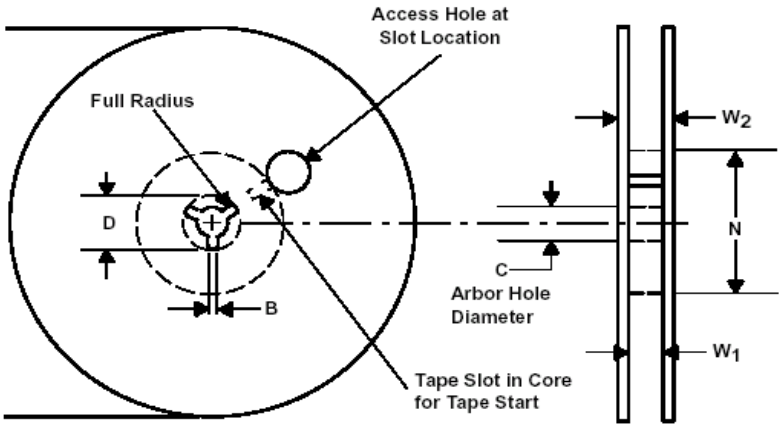
1st Line: Device Name (914) + IC Version (X) where A means version A, B means version B, …

2nd Line: Fintek Internal Trace Code (XXXX)

◯ : Pin 1 Identifier

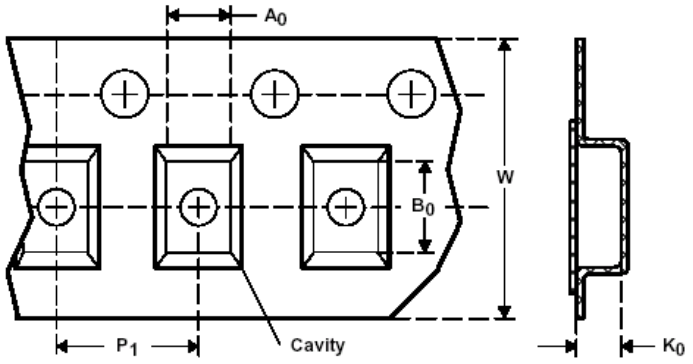
10 Tape and Reel Information

10.1 Reel Dimensions



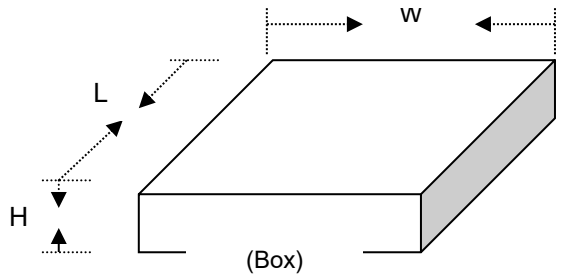
Tape Width	R (mm)	C (mm)	N (mm)	W1 (mm)
8	178+1.0/-1.0	20.2	62±0.5	8.4±0.2

10.2 Tape Dimensions



PKG	Body size	W (mm)	P1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)
DFN	2.5x2.5 mm^2	8	4.0	2.75	2.75	1.05

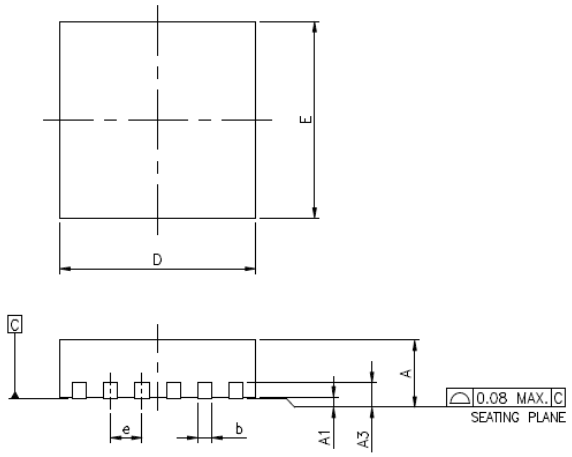
10.3 Tape and Reel Box Dimensions

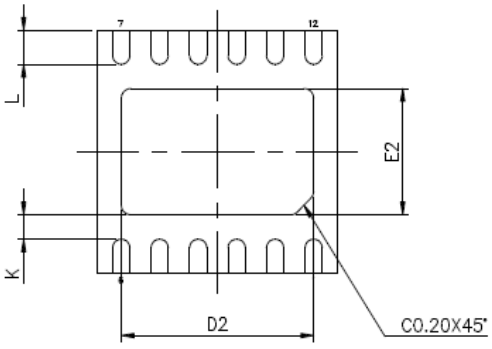


Reel Diameter	L (mm)	W (mm)	H (mm)
178mm	185	185	78

11 Package Dimension

DFN-12 Package





It's unnecessary to solder directly to the thermal pad on the bottom of the IC.

Unit: mm	PACKAGE TYPE		
PKG CODE	DFN		
SYMBOLS	MIN.	MON.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.13	0.18	0.23
D	2.50 BSC		
E	2.50 BSC		
e	0.40 BSC		
L	0.30	0.35	0.40
K	0.20	-	-

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
57X91 MIL	1.95	2.00	2.05	1.25	1.30	1.35	V	X	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

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12 Typical Application Circuit

The F75914 can be used in level-translation applications between devices or systems operating at different supply voltages. See below figure for a typical operating circuit using the F75914.

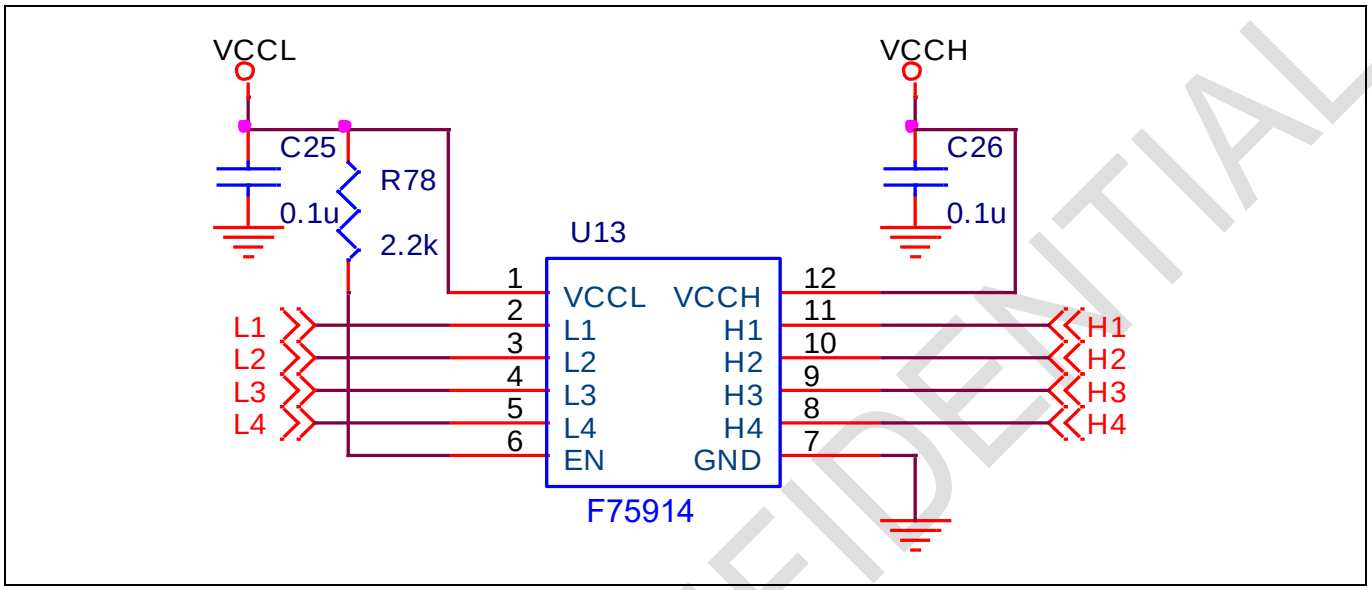

Figure. Typical operating circuit