Functional Safety Information

SN74HC08-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the SN74HC08-Q1 (D package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

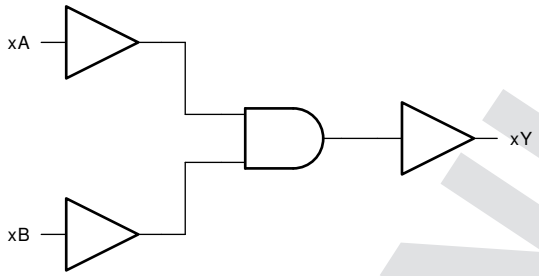

Figure 1-1. Functional Block Diagram

The SN74HC08-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the SN74HC08-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) - TSSOP (PW)	FIT (Failures Per 10^9 Hours) - SOIC (D)
Total component FIT rate	6	20
Die FIT rate	2	4
Package FIT rate	4	16

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 25 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
3	CMOS Logic FCT, HC, LV, LVC, ALVC, VHC, and so forth	5 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74HC08-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output stuck-at fault	30%
Output open (HIZ)	25%
Output functional – out of specification timing or voltage	45%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the SN74HC08-Q1 (D and PW packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5-1)
- Pin open-circuited (see Table 5-2)
- Pin short-circuited to an adjacent pin (see Table 5-3)
- Pin short-circuited to V_{CC} (see Table 5-4)

Table 5-1 through Table 5-4 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

5 D and PW Package

shows the SN74HC08-Q1 pin diagram for the D and PW packages. For a detailed description of the device pins and their corresponding pin type, please refer to the *Pin Configuration and Functions* section in the SN74HC08-Q1 data sheet. **Thermal Thermal Pad should be tied directly to GND plane to avoid potential failures that can cause excessive current.**

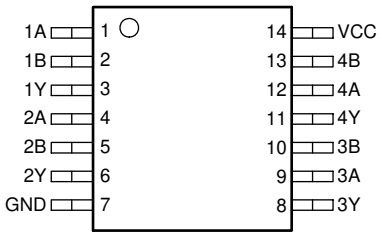

Figure 5-1. Pin Diagram (D & PW) Package

Table 5-1. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A, B	1, 2, 4, 5, 9, 10, 12, 13	Input pin functionality is defined such as input is low – see *Device Function Table* (for example, if the buffer input is GND, output will always be driven low).	B
GND	7	Normal operation.	D
Y	3, 6, 8, 11	Can cause excessive output current; output will not switch (for example, if buffer output is shorted to ground and is attempting to drive to V_{CC}).	A
V_{CC}	14	Device will not be powered, because short is external to the device. System level damage may occur in this scenario.	B

Table 5-2. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A, B	1, 2, 4, 5, 9, 10, 12, 13	Pin is floating, can change output state and cause excessive current from V_{CC} to GND See Implications of Slow or Floating CMOS Inputs.	A
GND	7	Device will not be powered.	B
Y	3, 6, 8, 11	Normal operation.	D
V_{CC}	14	Device will not be powered.	B

Table 5-3. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
A, B	1, 2, 4, 5, 9, 10, 12, 13	A, B	Two inputs shorted together will not cause damage unless there is external bus contention that drives the input such that V_{IL} < Input Voltage < V_{IH} in which case excessive supply current to gnd may cause damage System level damage may occur in this scenario.	A
A, B	1, 2, 4, 5, 9, 10, 12, 13	Y	Can cause excessive output current; output will not switch (for example, if inverter input is shorted to output).	A
A, B	1, 2, 4, 5, 9, 10, 12, 13	GND	Input pin functionality is defined such as input is low – see *Device Function Table* (for example, if the buffer input is GND, output will always be driven low).	B
A, B	1, 2, 4, 5, 9, 10, 12, 13	V_{CC}	Input pin functionality is defined such as input is HIGH – see Device Function Table (for example, if buffer input is V_{CC}, output will always be driven HIGH).	B
Y	3, 6, 8, 11	GND	Can cause excessive output current; output will not switch (for example, if buffer output is shorted to ground and is attempting to drive to V_{CC}).	A
Y	3, 6, 8, 11	V_{CC}	Can cause excessive output current; output will not switch (for example, if buffer output is shorted to V_{CC} and is attempting to drive to GND).	A

Table 5-4. Pin FMA for Device Pins Short-Circuited to V_{CC}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A, B	1, 2, 4, 5, 9, 10, 12, 13	Input pin functionality is defined such as input is HIGH – see Device Function Table (for example, if buffer input is V_{CC}, output will always be driven HIGH).	B
GND	7	Device will not be powered, because short is external to device. System level damage may occur in this scenario.	B
Y	3, 6, 8, 11	Can cause excessive output current; output will not switch (for example, if buffer output is shorted to V_{CC} and is attempting to drive to GND).	A
V_{CC}	14	Normal operation.	D

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