

LSF010x Waveform With Different Pull Up Resistors

Ting Ye

Test Configuration

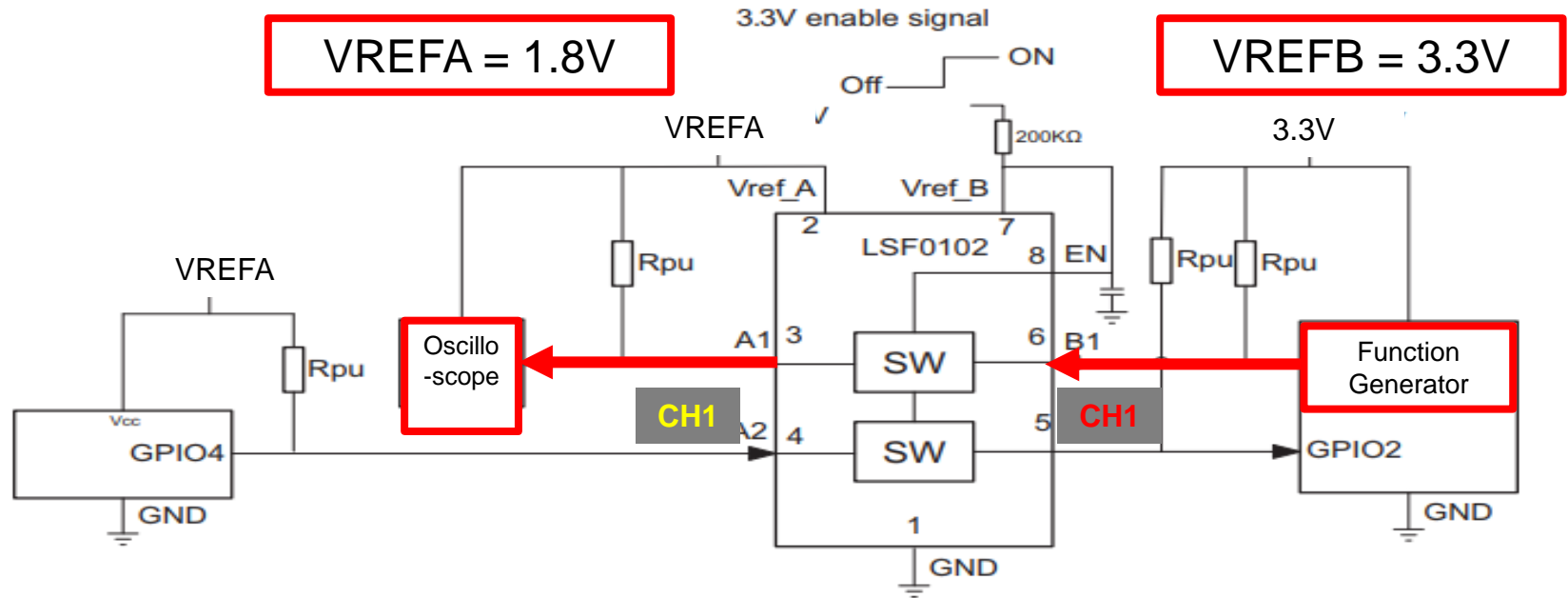
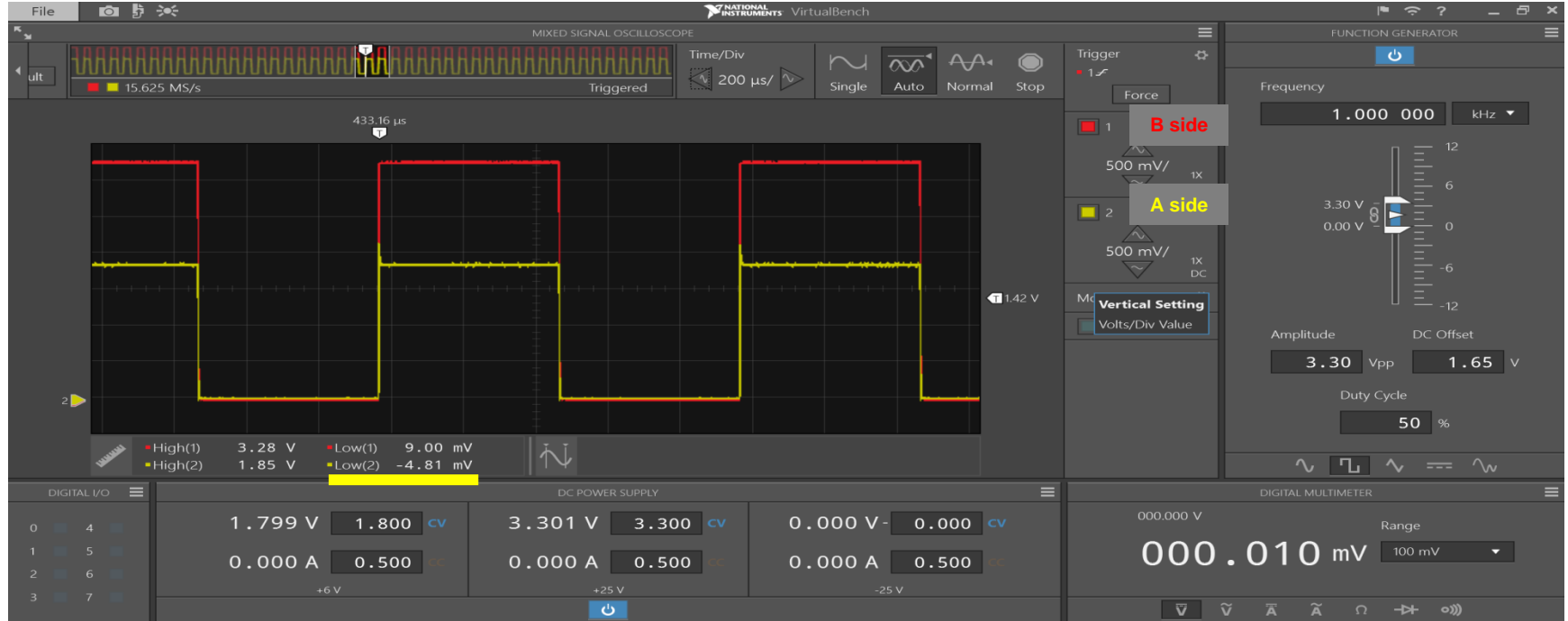
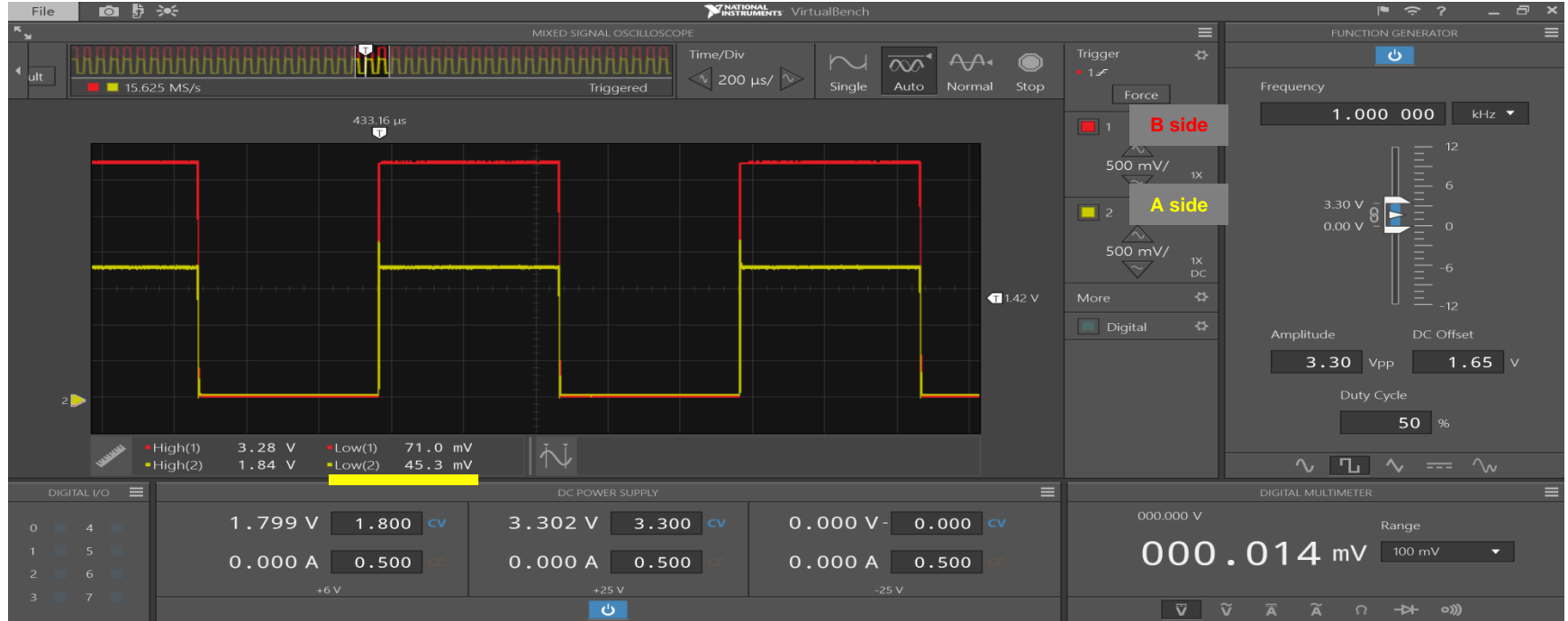


Figure 6. Bidirectional Translation to Multiple Voltage Levels

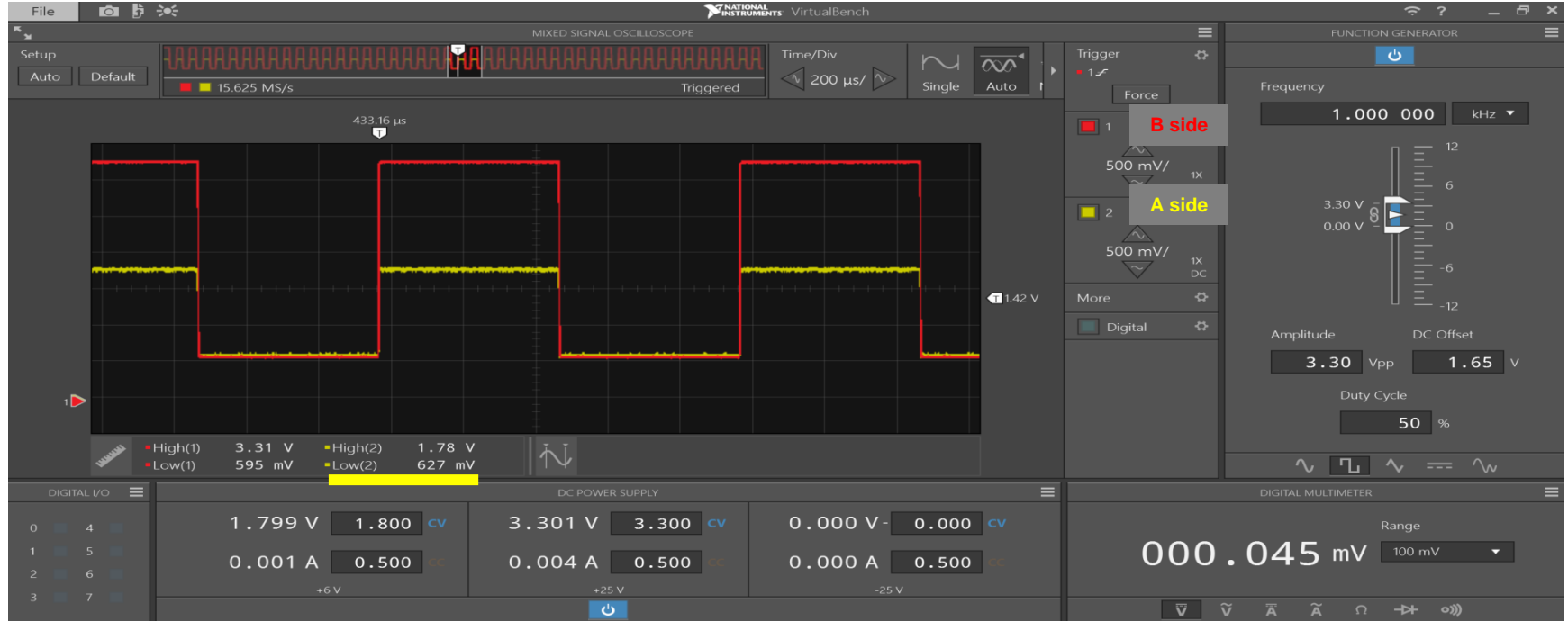
Input signal frequency = 1kHz
R_{pu} = 47k-ohm



Input signal frequency = 1kHz
R_{pu} = 4.7k-ohm



Input signal frequency = 1kHz
 $R_{pu} = 0.3\text{k-ohm}$



<https://training.ti.com/tlm-lsf-up>

Email

Inside the LSF

THE LOGIC MINUTE

The diagram illustrates the internal structure of the LSF (Logic Sense Function) block. It features a differential pair of transistors, labeled B1 and A1, connected to a common source resistor. The input signal is a differential voltage V_B , which is applied to the gates of the transistors. The output signal is a differential voltage V_A , which is taken from the drains of the transistors. The circuit includes resistors R_{B1} and R_{A1} , and capacitors C_{B1} and C_{A1} . A bias voltage V_{bias} is applied to the gates of the transistors. The current I_B is shown flowing through the source resistor, and the current $I_A + I_B$ is shown flowing through the output node. The diagram is labeled "LSF" and "B1", "A1".

1:37 / 5:39

ASIX INSTRUMENTS

Application Note to Explain Receiver I_{SINK} and Level Shifter V_{OL}

- Effects of External Pullup and Pulldown Resistors on TXS and TXB Devices

<http://www.ti.com/lit/an/scea054/scea054.pdf>

- Factors Affecting V_{OL} for TXS and LSF Auto-bidirectional Translation Devices

<http://www.ti.com/lit/an/scea056/scea056.pdf>