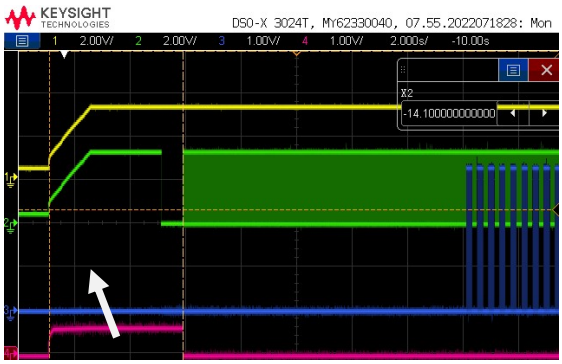
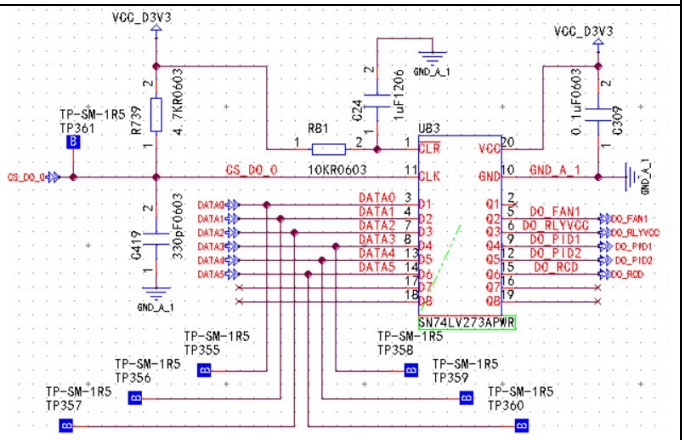
SN74LV273PWRQn output is abnormal during power-up

Issue：SN74LV273PWRQn output is abnormal during power-up

一、Test waveforms

测试波形	原理图
 CH1:CLR;CH2:CLK;CH3:Pin 8(DATA3) CH4::Pin 9(DO_PID1) Fig. 1	

1. When VCC rise is slow (about 3.3v/2s) during power-up,both Vclk and Vclr ris are also slow because VCC rise is slow. Q4(pin9) outputs occasionally is not kept low even CLR is already high(shown as above Fig. 1).
2. Change Vcc rise speed from low to high, so Vclk and Vclr rise speed is also fast. The Q4 output can be always kept low during power up(shown as below fig.2).

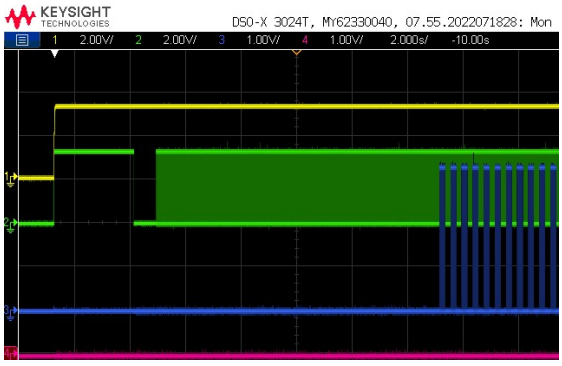


Fig. 2 CH1:CLR;CH2:CLK;CH3:Pin 8(DATA3);CH4::Pin 9(DO_PID1)

Questions:

1. Are there any rise/fall speed requirement for both CLK and CLR of SN74LV273?
2. Above issue, is it caused by rise speed of CLK and CLR?