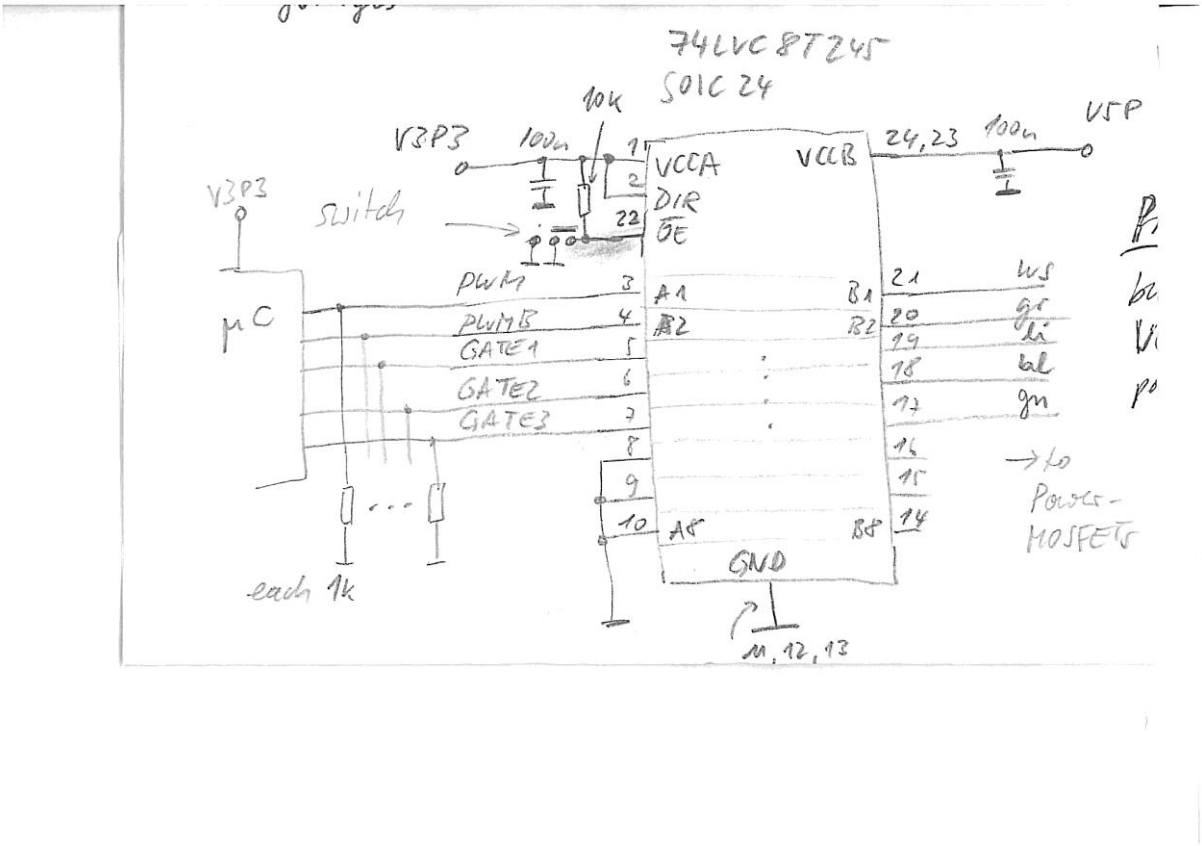
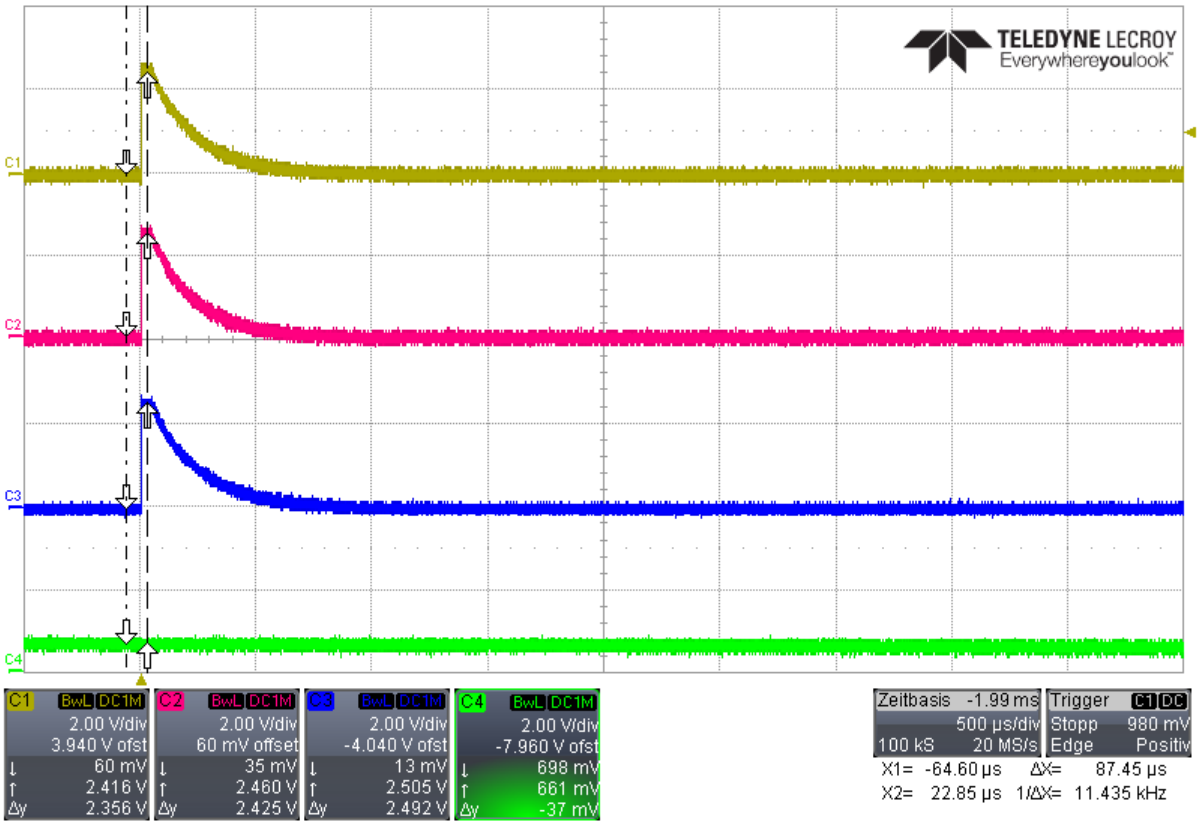
During the switching-off period there is a moment when VCCA = ca. 0,7V (and /OE is pullup-up to it) at which for 50% of the trials is an output glitch at the Bn signals. They must stay low in our circuitry because else the following power MOSFETs will switch partially on and so will get damaged.



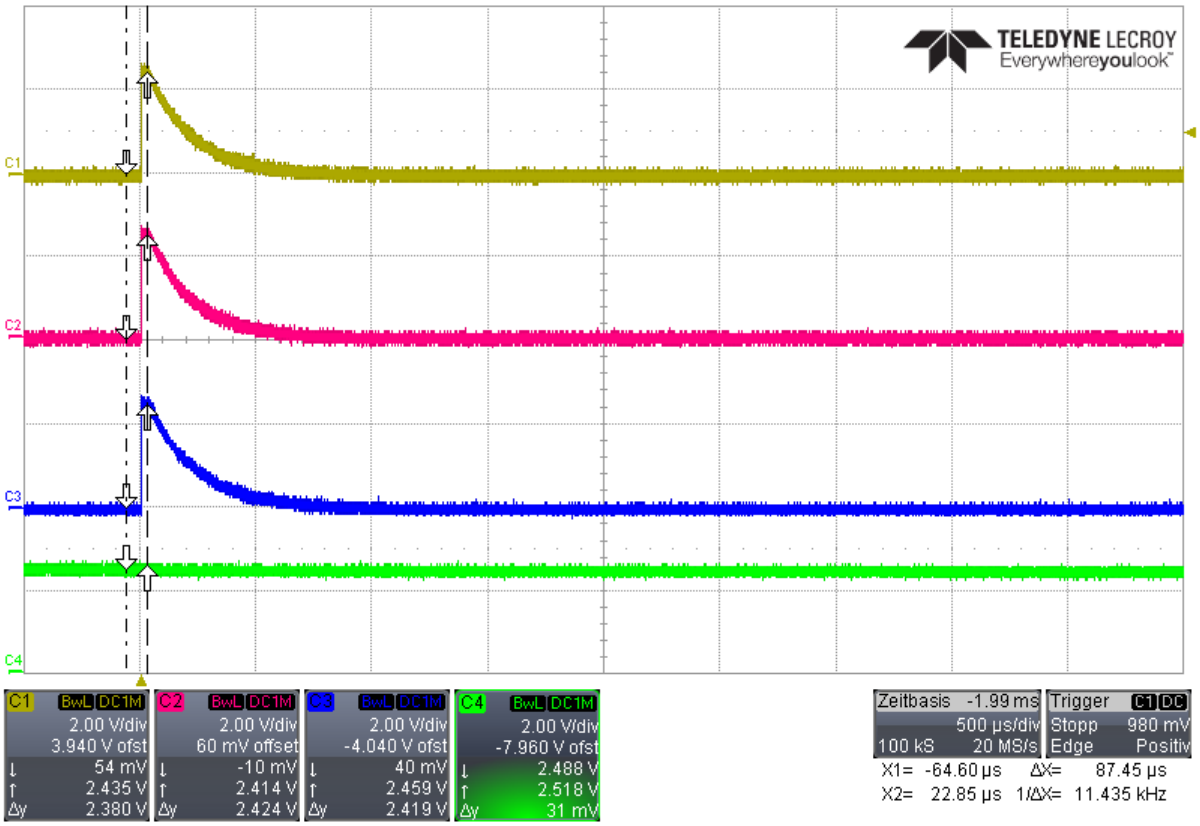
Schematic of part with latch SN74LVC8T245

There is a switch for the /OE signal because it is not yet controlled by the microcontroller. DIR has no pull-up R but is directly connected.

Please see the following two scope measurements showing Bn and VCCA [B]. The An signals are pulled low and keep logic low during switch-off (I checked this of course), the microcontroller switches with this undervoltage all outputs to inputs.



Ch1 .. Ch3 = Bn
Ch4 = VCCA



Ch1 .. Ch3 = Bn
Ch4 = VCCB