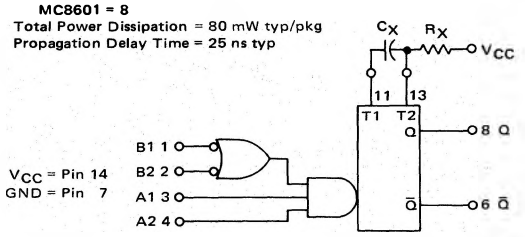
RETRIGGERABLE
MONOSTABLE
MULTIVIBRATOR

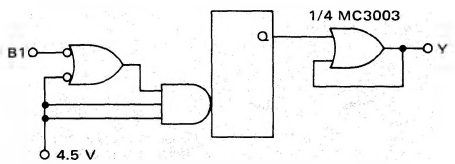
MC9601F, L*
MC8601F, L, P*

Input Loading Factor = 1
Output Loading Factor:
MC9601 = 6
MC8601 = 8
Total Power Dissipation = 80 mW typ/pkg
Propagation Delay Time = 25 ns typ



The MC9601/8601 monostable multivibrator may be triggered from either edge of an input pulse and will produce accurate output pulse over a wide range of widths. The duration and accuracy of the complementary output pulses are determined by the external timing components, R_X and C_X. Each time the input conditions for triggering are met the external timing capacitor, C_X, is discharged, starting a new output pulse. The output goes to the high state while C_X is being discharged and remains there until the capacitor recharges through R_X, to a threshold determined by an internal comparator. Input pulses applied during the active state again discharge the capacitor, thus adding another full timing cycle to the output pulse width. This retriggering feature can be inhibited if not required.

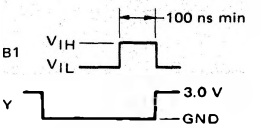
FUNCTIONAL TEST



SEQUENCE

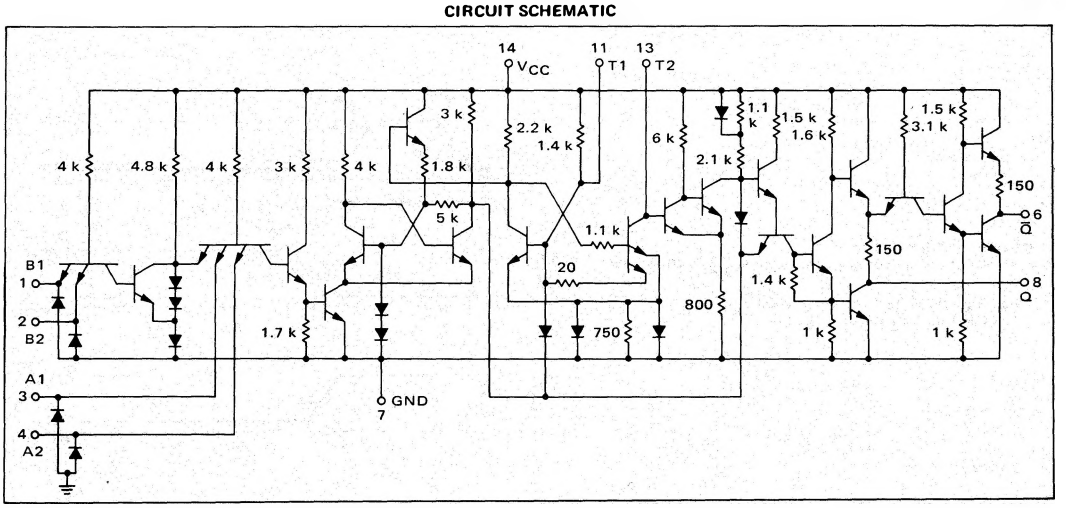
1. Apply V_{IL} to B1.
2. Momentarily ground Y.
3. Apply V_{IH} to B1.
4. Apply V_{IL} to B1.
5. Check Y for logical "1" level.

TIMING DIAGRAM



Device	Temperature	V_{IL}	V_{IH}
MC9601	-55	0.85	2.0
	+25	0.9	1.7
	+125	0.85	1.4
MC8601	0	0.85	1.9
	+25	0.85	1.8
	+75	0.85	1.6

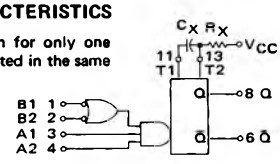
CIRCUIT SCHEMATIC



*F suffix = TO-86 ceramic flat package (Case 607).
L suffix = TO-116 ceramic dual in-line package (Case 632).
P suffix = TO-116 plastic dual in-line package (Case 605).

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input. Other inputs are tested in the same manner.

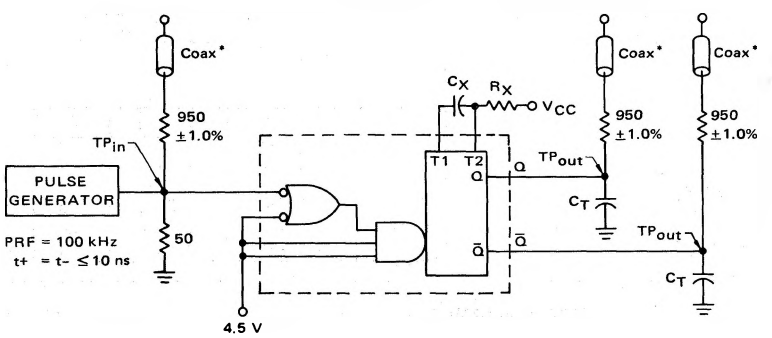


	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES (1) mA I_{OL}	I_{OH}	I_D	Volts V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}
MC9601	−55°C	10.0	-0.72	-	0.4	4.5	-	4.5	5.5
	+25°C	10.0	-0.72	-10	0.4	4.5	5.0	4.5	5.5
	+125°C	10.0	-0.72	-	0.4	4.5	-	4.5	5.5
MC8601	0°C	12.8	-0.96	-	0.45	4.5	-	4.75	5.25
	+25°C	12.8	-0.96	-10	0.45	4.5	5.0	4.75	5.25
	+75°C	12.8	-0.96	-	0.45	4.5	-	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC9601 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC8601 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_D	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																									
Forward Current	I_F	1	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-1.6	-	-1.6	-	-1.6	mAdc	-	-	-	1	-	-	-	14	7
Leakage Current	I_R	1	-	-	-	60	-	60	μAdc	-	-	-	60	-	60	μAdc	-	-	-	-	1	-	-	14	7
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	Vdc	-	-	-	-1.5	-	-	Vdc	-	-	1	-	-	-	14	-	7
Output																									
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	Vdc	-	0.45	-	0.45	-	0.45	Vdc	6	-	-	-	-	-	14	-	7,11
		8	-	0.4	-	0.4	-	0.4	Vdc	-	0.45	-	0.45	-	0.45	Vdc	8	-	-	-	-	-	14	-	7
	V_{OH}	6	2.4	-	2.4	-	2.4	-	Vdc	2.4	-	2.4	-	2.4	-	Vdc	-	6	-	-	-	-	14	-	7
		8	2.4	-	2.4	-	2.4	-	Vdc	2.4	-	2.4	-	2.4	-	Vdc	-	8	-	-	-	-	14	-	7,11
Short-Circuit Current	I_{SC}	6	-	-	-10	-40	-	-	mAdc	-	-	-10	-40	-	-	mAdc	-	-	-	-	-	14	-	-	6,7
		8	-	-	-10	-40	-	-	mAdc	-	-	-10	-40	-	-	mAdc	-	-	-	-	-	14	-	-	7,8,11
Power Requirements																									
Power Supply Drain	I_{PD}	14	-	25	-	25	-	25	mAdc	-	25	-	25	-	25	mAdc	-	-	-	-	-	-	-	14	7

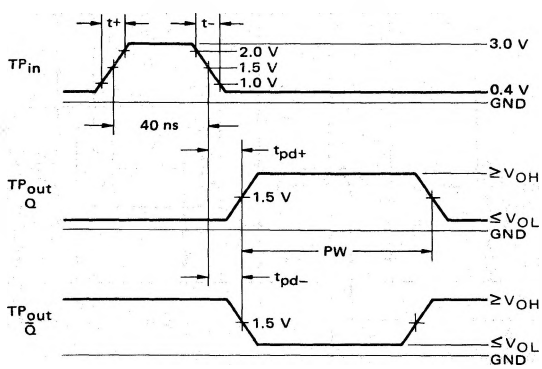
(1) A 10-kilohm resistor (R_X) is placed between Pin 13 and V_{CC} for all tests unless otherwise noted.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.



When R_X = 5.0 kΩ, C_X = 0:
PW = 65 ns max, t_{pd+} = 40 ns max, t_{pd-} = 40 ns max

When R_X = 10 kΩ ± 1.0%, C_X = 1000 pF:
PW = 3.08 μs min, 3.76 μs max

TYPICAL CHARACTERISTICS

FIGURE 1 – INPUT LOAD CURRENT versus INPUT VOLTAGE

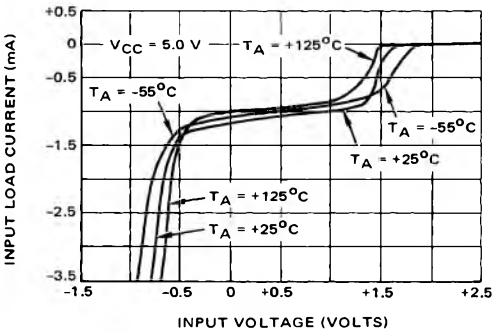


FIGURE 2 – INPUT LEAKAGE CURRENT versus INPUT VOLTAGE

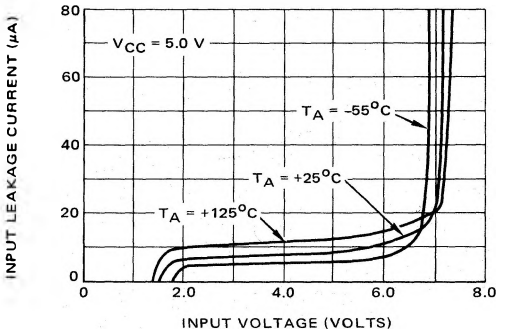


FIGURE 3 – OUTPUT CURRENT versus OUTPUT VOLTAGE (LOW STATE)

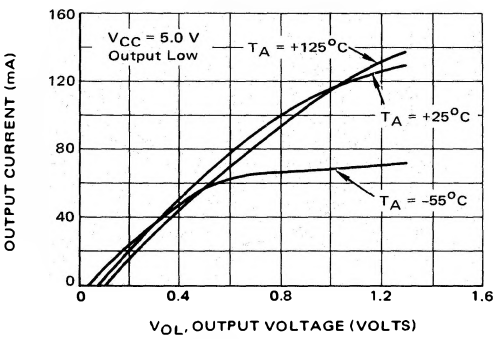


FIGURE 4 – OUTPUT CURRENT versus OUTPUT VOLTAGE (HIGH STATE)

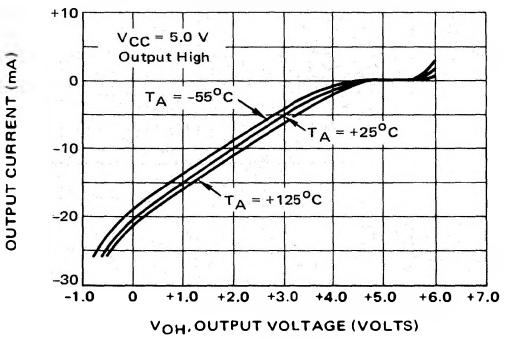


FIGURE 5 – POWER DISSIPATION versus AMBIENT TEMPERATURE and SUPPLY VOLTAGE

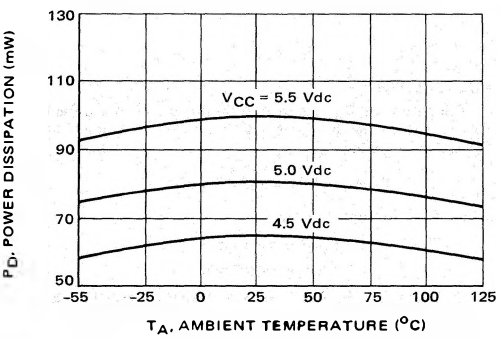
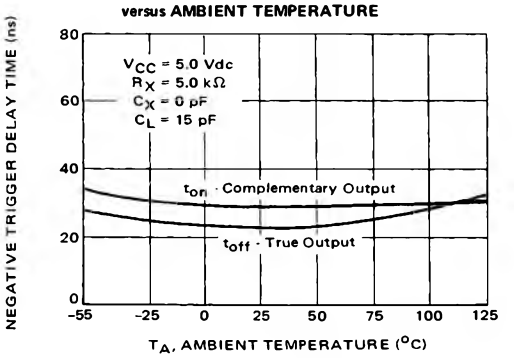


FIGURE 6 – NEGATIVE TRIGGER DELAY TIME versus AMBIENT TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – NORMALIZED OUTPUT PULSE WIDTH versus AMBIENT TEMPERATURE

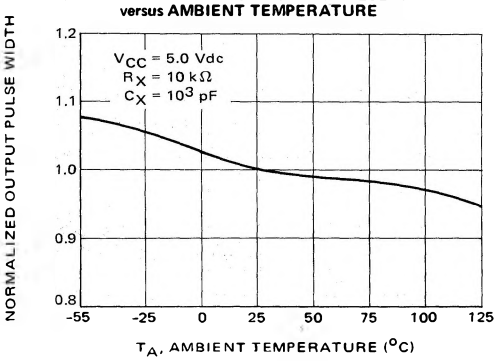


FIGURE 8 – NORMALIZED OUTPUT PULSE WIDTH versus SUPPLY VOLTAGE

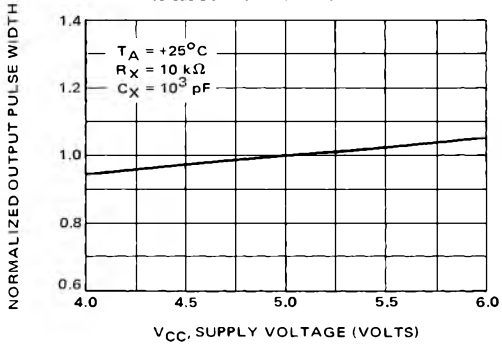


FIGURE 9 – NORMALIZED OUTPUT PULSE WIDTH versus OPERATING DUTY CYCLE

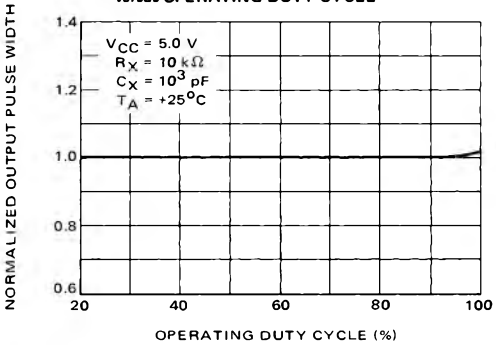
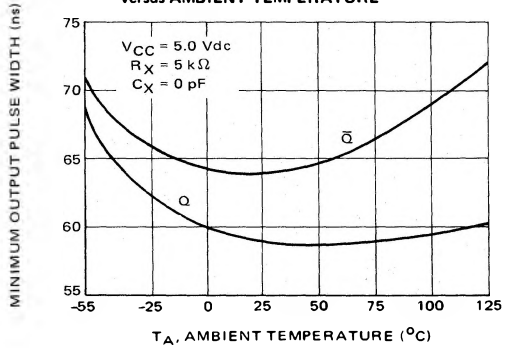


FIGURE 10 – OUTPUT PULSE WIDTH versus AMBIENT TEMPERATURE



OPERATING CHARACTERISTICS

PULSE WIDTH

For values of C_X less than 1000 pF, the output pulse width, PW, is defined by the curves of Figure 11. For larger values of C_X use the equation:

$$PW = 0.32\ R_X C_X \{1 + (0.7/R_X)\}$$

where PW is in nanoseconds,

R_X is in kilohms,

C_X is in picofarads.

Values of R_X may vary from 5.0 kilohms to 50 kilohms for 0° to +75°C operation of the MC8601, and from 5.0 kilohms to 25 kilohms for -55° to +125°C operation of the MC9601. The range of capacitance values is unlimited, hence maximum pulse width is limited only by the values of available capacitors.

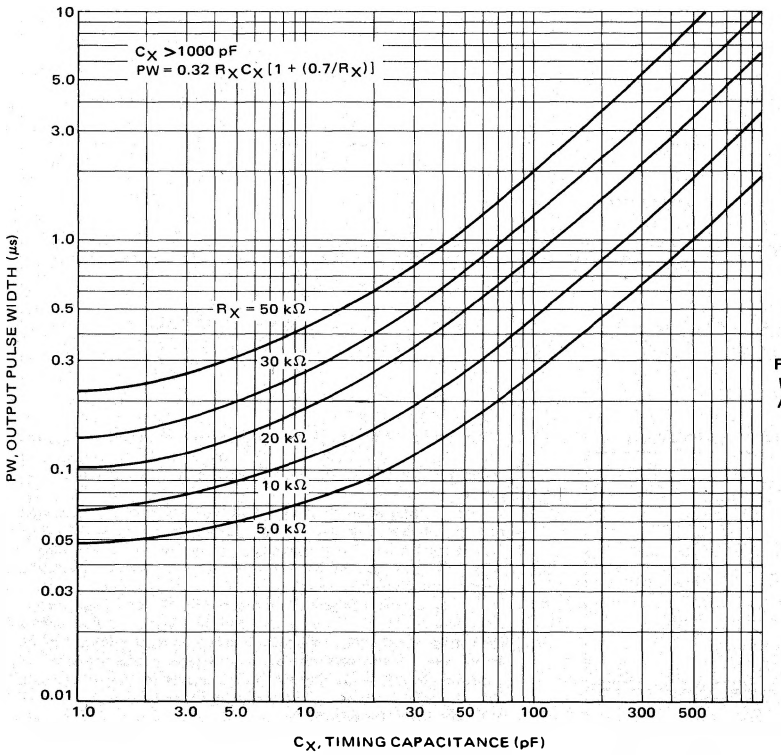


FIGURE 11 – OUTPUT PULSE WIDTH versus TIMING RESISTANCE AND CAPACITANCE

PULSE INITIATION

Output pulses are initiated by any combination of inputs satisfying the logic expression A1 • A2 • (B1 + B2); A1 and A2 must be high and either B1 or B2 must be low. Output pulses are generated by transitions from low to high on A1 or A2, and by transitions from high to low on B1 or B2. Leading edge triggering may be accomplished by either of the methods shown in Figure 12.

Similarly, trailing edge triggering may be accomplished by either of the methods shown in Figure 13.

FIGURE 12 – LEADING EDGE TRIGGERING

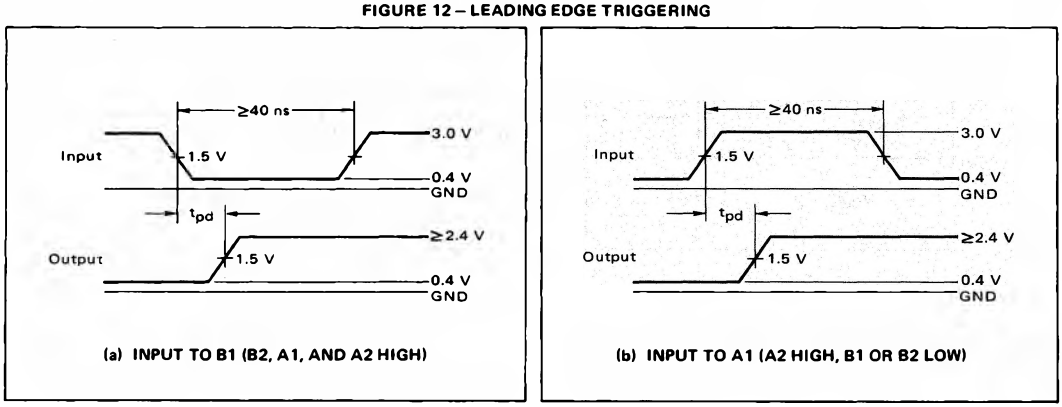


FIGURE 13 – TRAILING EDGE TRIGGERING

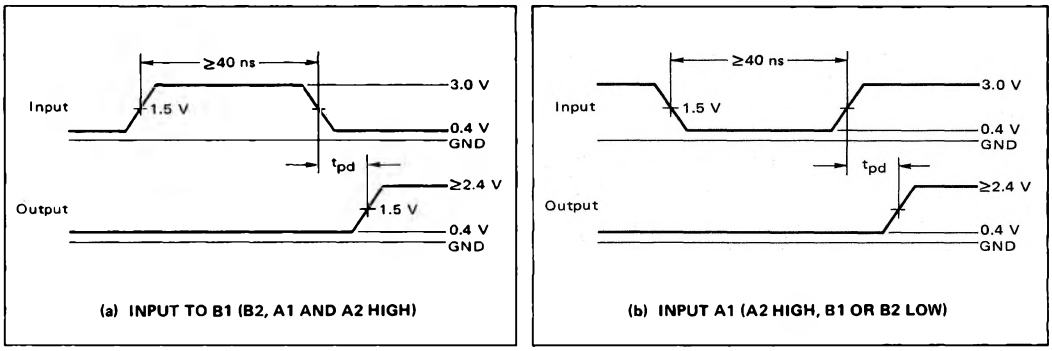
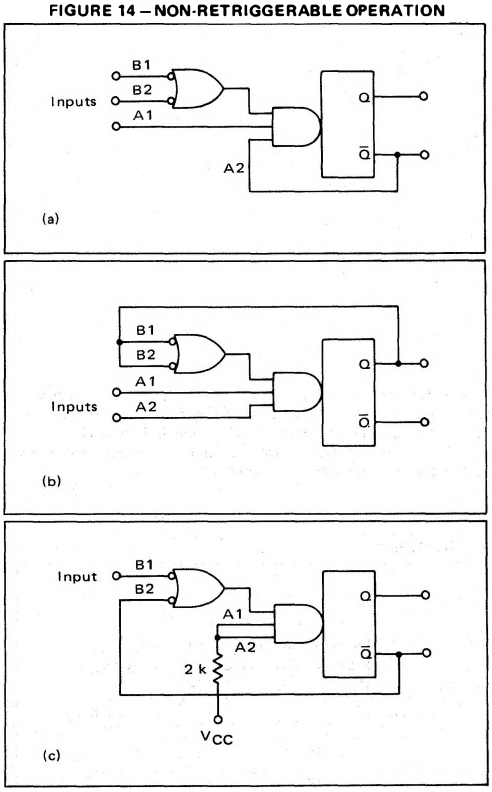


FIGURE 14 – NON-RETRIGGERABLE OPERATION



RETRIGGER INHIBIT

For applications where retriggering is not required, appropriate feedback from the outputs will inhibit trigger signals arriving during the active timing cycle. Figure 14 illustrates three methods for doing this.

In Figure 14(a), A2 is held low by the $\overline{Q}$ output during the active state. Since both A inputs must be high for triggering to occur, this configuration inhibits retriggering at all of the remaining inputs.

The configuration of Figure 14(b) will be triggered active on the trailing edge of a negative going pulse applied to either A1 or A2. B2 and B1 are then held high by the Q output. Since either B1 or B2 must be low for triggering to occur, further triggering during a timing cycle is inhibited.

The feedback arrangement of Figure 14(c) holds B2 low during the active timing cycle. Since this keeps the output of the inverted OR gating circuitry high, subsequent input signals to B1 during the active state do not retrigger the monostable. Noise immunity is improved by returning unused "high" inputs to V_{CC} through a 2.0 kilohm resistor instead of leaving them open (see A1 and A2 of Figure 14(c), for example.)

ASTABLE OPERATION

Astable applications requiring adjustable duty cycles may be accomplished by the conventional method of cascading two one-shots as shown in Figure 15. In applications where narrow output pulses are satisfactory, a single monostable may be used. One method for doing this is illustrated in Figure 16, monostable A. The clock generation for a simple pulse generator is accomplished by connecting the $\overline{Q}$ output of the "A" monostable back to an AND input. The period of oscillation, or pulse repetition frequency, PRF, is determined by the external timing components, R_{XA} and C_{XA}. At the end of each timing cycle, the $\overline{Q}_A$ output generates a low-to-high transition at the AND input and thus triggers another cycle. The nominal output pulse width is approximately 30 ns, and is determined by the propagation time through the gating and discharge circuitry. The maximum PRF is approximately 15 MHz, obtained with C_{XA} = 0 pF and R_{XA} = 5.0 kΩ. The variable delay feature is controlled by the timing components of monostable "B", C_{XB} and R_{XB}. The output pulse width is determined by C_{XC} and R_{XC}, the timing components of monostable "C".

ELECTROLYTIC CAPACITOR PROTECTION

If electrolytic capacitors are used they should be protected from reverse voltage; either of the methods indicated in Figure 16 may be used. Any silicon switching diode, such as the 1N4001 shown for monostable "B", is adequate. The transistor method of monostable "C" requires a silicon transistor with gain at low currents.

This figure also illustrates the preferred method of using remotely located variable timing components. Noise pickup will be minimized by locating R_X and C_X physically close to the device. Stray capacitance at pins 11 and 13 should be 50 pF or less.

FIGURE 15 – ASTABLE OPERATION – ADJUSTABLE DUTY CYCLE

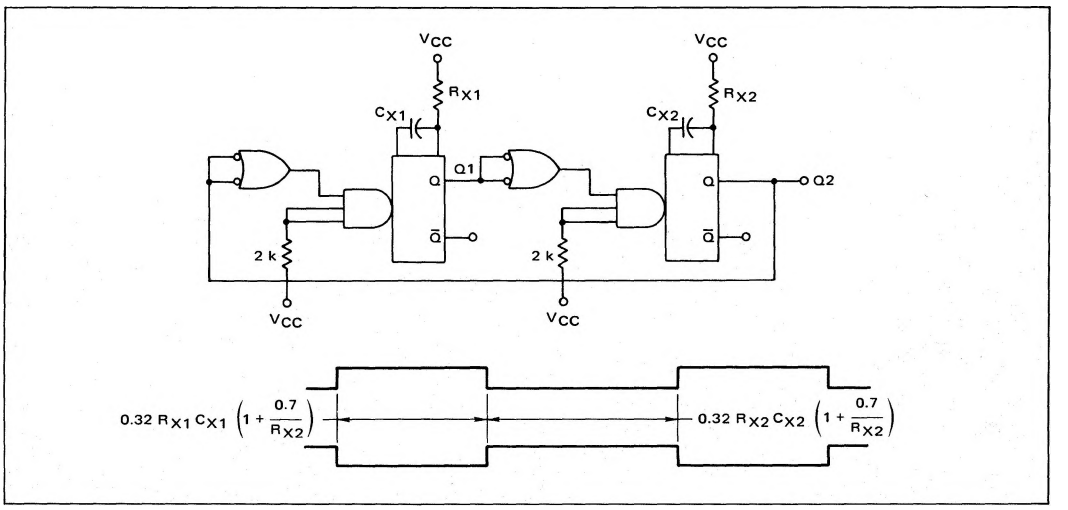


FIGURE 16 – PULSE GENERATOR