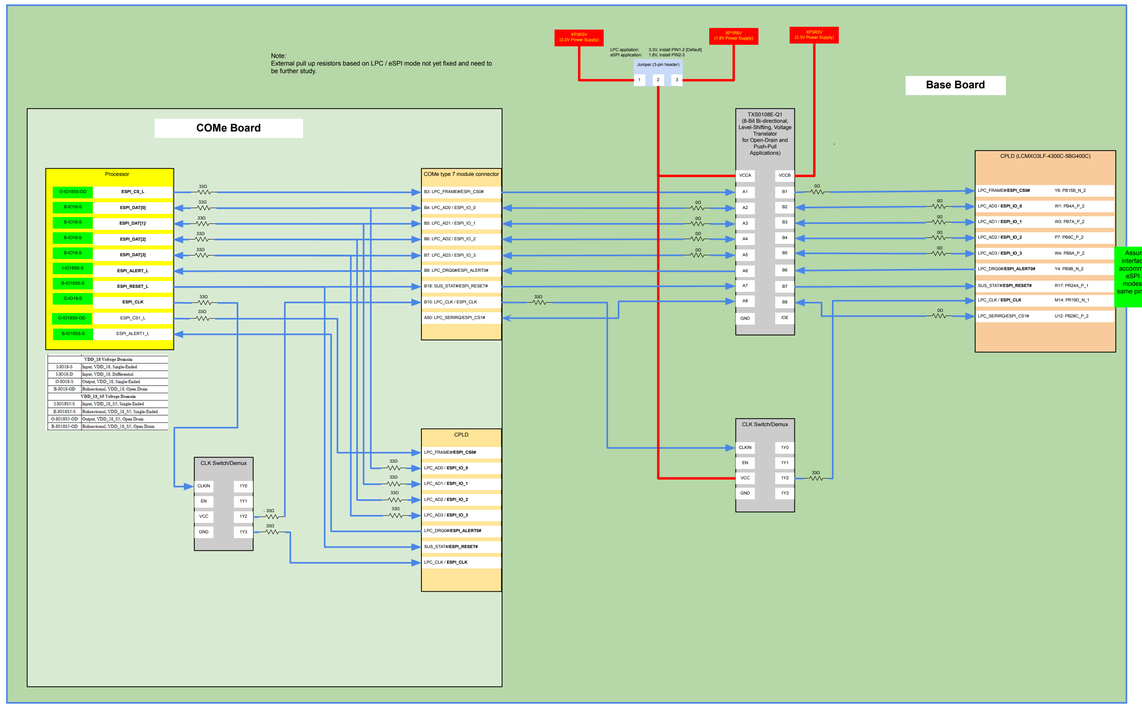
Processor Design Guide

Table 56. Miscellaneous Signals Quick Reference (continued)

Group	Signal Name	Connection	Termination[1]	Termination Voltage
ESPI/SPI ROM Signals	ESPI_ALERT_L/AGPI5027	Is a 10 kΩ pull-up resistor to 1.8V. This signal must remain at a logic high through the boot process. It is not recommended to use this signal as a GPIO unless it can meet this condition.	10 kΩ	VDD_18_S5
	ESPI_RESET_L/CBEST_L/AGPI5021	Connected to ESPI Device RESET#	10 kΩ	VDD_18_S5
	SPI1_CLK/ESPI_CLK/EGPI5077	Clock of SPI/ESPI device 1	10Ω series resistor Implementation Dependent	–
	SPI1_CS1_L/EGPI5074	Chip Select 1 of SPI/ESPI device 1	10 kΩ	VDD_18
	SPI1_CS2_L/EGPI5078	Chip Select 2 of SPI/ESPI device 1	10 kΩ	VDD_18
	SPI1_CS3_L/EGPI5079	Chip Select 3 of SPI/ESPI device 1	10 kΩ	VDD_18
	SPI1_DAT[0]/ESPI_DAT[0]/EGPI5081	DQ0 on SPI/ESPI device 1	10 kΩ	VDD_18
	SPI1_DAT[1]/ESPI_DAT[1]/EGPI5080	DQ1 on SPI/ESPI device 1	10 kΩ	VDD_18
	SPI1_DAT[2]/ESPI_DAT[2]/AGPI5068	DQ2 on SPI/ESPI device 1	10 kΩ	VDD_18
	SPI1_DAT[3]/ESPI_DAT[3]/AGPI5069	DQ3 on SPI/ESPI device 1	10 kΩ	VDD_18
	SPI2_CLK/EGPI5070	Clock of SPI device 2	10Ω series resistor Implementation Dependent	–
	SPI2_CS1_L/EGPI5075	Chip Select of SPI device 2	10 kΩ	VDD_18
	SPI2_DAT[0]/EGPI5104	DQ0 on SPI device 2	10 kΩ	VDD_18
	SPI2_DAT[1]/EGPI5105	DQ1 on SPI device 2	10 kΩ	VDD_18
	SPI2_DAT[2]/EGPI5106	DQ2 on SPI device 2	10 kΩ	VDD_18
	SPI2_DAT[3]/EGPI5107	DQ3 on SPI device 2	10 kΩ	VDD_18
	SPI_CLK/ESPI_CLK	Clock of multi-I/O SPI or ESPI device.	10Ω series resistor Implementation Dependent	–
	SPI_CS1_L	Chip Select#1 of SPI or ESPI device	10 kΩ	VDD_18_S5
	SPI_CS2_L/ESPI_CS_L/AGPI5030	Chip Select#2 of SPI or ESPI device	10 kΩ	VDD_18_S5



eSPI Spec

Operating Specification

8 Operating Specification

8.1 Electrical Specification

NOTE: The electrical specification defined in this section is preliminary and it is subjected to change.

Table 21: Electrical Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Vcc	eSPI I/O voltage		1.71	1.8	1.89	V
R_{ON}	Output driver impedance	V_{out} = Vcc/2	15	25	35	Ohm
V_{IL}	Input low voltage				0.3*Vcc	V
V_{IH}	Input high voltage		0.7*Vcc			V
V_{HYS}	Input hysteresis voltage		0.1*Vcc			V
$R^1_{reset-PU}$	Weak pull-up impedance	V_{out} = 0.7*Vcc	10k		30k	Ohm
$R^1_{reset-PD}$	Weak pull-down impedance	V_{out} = 0.3*Vcc	10k		30k	Ohm
$R_{alert-PU}$	Weak pull-up impedance for Alert# pin	V_{out} = 0.7*Vcc		4.7k[3]		Ohm
C_{in}	Input capacitance				5	pF
C_L[2]	Load capacitance			10		pF
I_{IL}	Input leakage current	0 < V_{in} < Vcc			±10	uA

NOTES:

1. Weak pull-up on eSPI data and Chip Select# pins (except Alert# pin) and weak pull-down on eSPI clock must be implemented as an integral part of the eSPI master buffer or on the board.
2. C_L is the test load defined for AC timing measurement.
3. The weak pull-up impedance value is defined for a typical eSPI bus loading when Alert# pin is configured as open-drain. Platform is required to adjust this value accordingly such that when Alert# pin is asserted, the assertion of the CS# for the shortest possible transaction (which causes the slave to tri-state the Alert# pin), is able to pull the Alert# pin high fast enough to the deasserted value before or by the last failing edge of the serial clock at the end of the transaction.

3.3 Pin Descriptions

eSPI uses the existing SPI I/O buffer. The electrical specification for this new interface is the same as SPI.

eSPI Reset# is typically driven from eSPI master to eSPI slaves. The exception is when eSPI Reset# is generated by eSPI slave, which drives the eSPI Reset# to the eSPI master. eSPI Reset# is the reset to the eSPI interface on both sides.

eSPI master and eSPI slaves must tri-state the interface pins when their respective eSPI Reset# is asserted. The Chip Select# and I/O[n:0] pins require weak pull-up to be enabled on these pins whereas the Serial Clock requires a weak pull-down. When functions as a driven output, Alert# pin does not require a weak pull-up to be enabled on the pin unless for the purpose of terminating the pin to inactive when it is not used. When functions as an open-drain output, Alert# pin requires a weak pull-up to be enabled on the pin.

The weak pull-up/pull-down should be implemented either as an integral part of the eSPI master buffer or on the board. eSPI slaves must not implement the weak pull-up/pull-down. For Alert# pin configured as open-drain, it is recommended that the weak pull-up be implemented on the board such that its impedance value could be adjusted accordingly when needed.

Refer to Section 8.1 - Electrical Specification for the value of the weak pull-up/pull-down resistor.

After eSPI Reset# is deasserted on the eSPI master, the eSPI master begins driving Chip Select# and Serial Clock pins to their idle state appropriately. The weak pull-up on the Chip Select# and the weak pull-down on the Serial Clock are allowed to be disabled after the eSPI Reset# deassertion. However, I/O[n:0] and Alert# pin (open-drain) continue to have the weak pull-up enabled for the proper operation of the eSPI bus.

LPC Spec

10.4 Signal Pull-Up Requirements

The LAD[3:0] signals require pull-up resistors to maintain their state during the turnaround (TAR) periods of a cycle.

The LDRQ[1:0] signals require pull-ups if they are not connected to a LPC peripheral device. This will keep them in the inactive state.

See Table 24 below for recommended pull-up values. Some host devices will incorporate these pull-ups internally. Other signals may or may not require pull-up resistors, dependent on the specific system implementation.

Table 24: Recommended Pull-Up Values

Signal Name	Pull-Up
LAD[3:0]	15k - 100k ohm
LDRQ[1:0]#	15k - 100k ohm