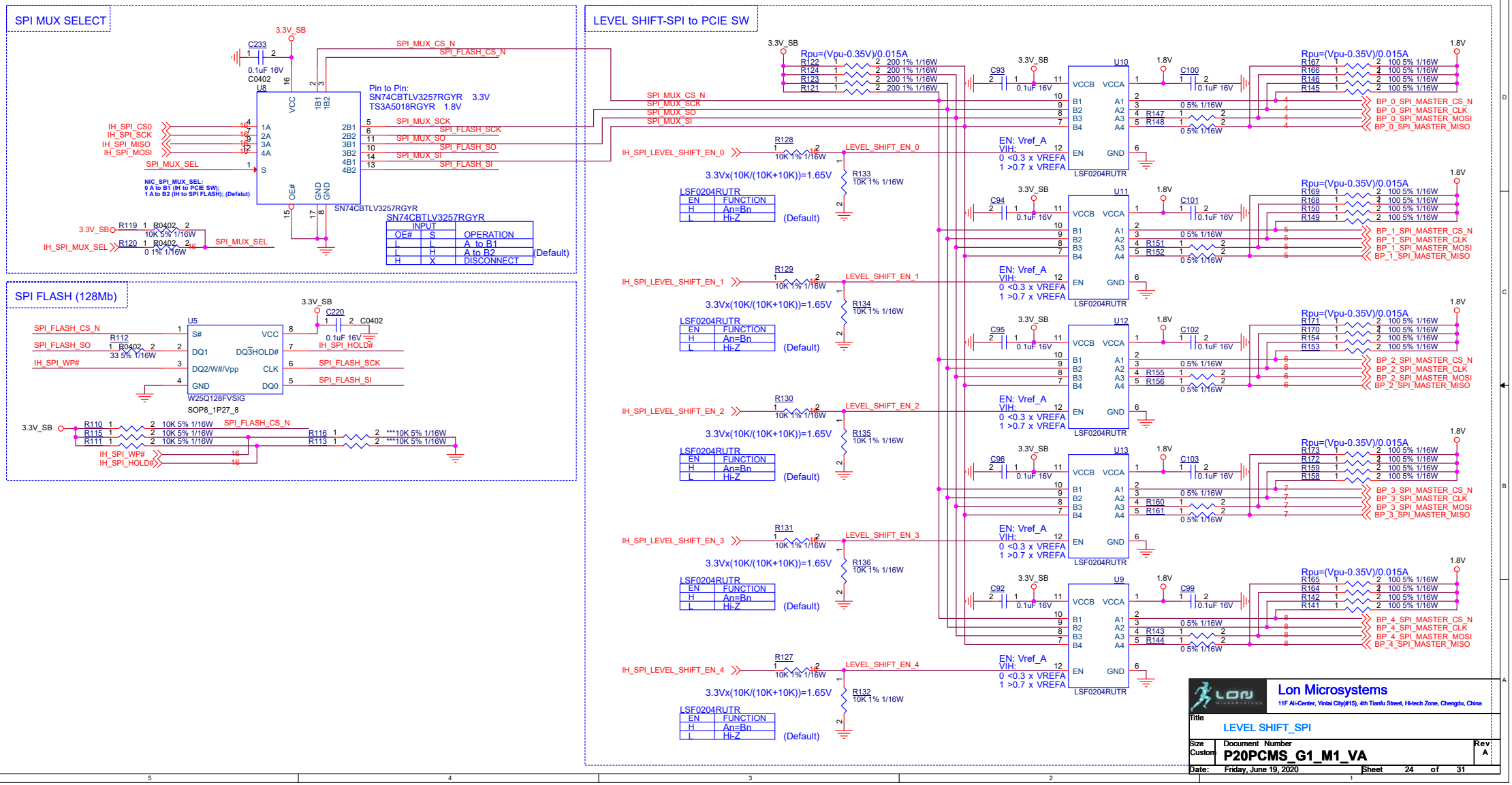
SPI MUX SELECT
Pin to Pin:
SN74CBTLV3257RGYR 3.3V
TS3A5018RGYR 1.8V
NIC_SPI_MUX_SEL:
0 A to B1 (IH to PCIE SW);
1 A to B2 (IH to SPI FLASH); (Defalut)
SN74CBTLV3257RGYR
INPUT
OE# S OPERATION
L L A to B1
L H A to B2 (Default)
H X DISCONNECT
SPI FLASH (128Mb)
W25Q128FVSIG
SOP8_1P27_8
LEVEL SHIFT-SPI to PCIE SW
Rpu=(Vpu-0.35V)/0.015A
3.3Vx(10K/(10K+10K))=1.65V
LSF0204RUTR
EN FUNCTION
H An=Bn
L Hi-Z
(Default)
EN: Vref_A
VIH:
0 <0.3 x VREFA
1 >0.7 x VREFA
Lon Microsystems
11F Ali-Center, Yintai City(#15), 4th Tianfu Street, Hi-tech Zone, Chengdu, China
Title
LEVEL SHIFT_SPI
Size Custom
Document Number
P20PCMS_G1_M1_VA
Rev A
Date: Friday, June 19, 2020
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