

TEXAS INSTRUMENTS
FIELD PROGRAMMABLE LOGIC DEPARTMENT
PROGRAMMING ALGORITHM SPECIFICATION

DEVICE FAMILY TICPAL22V10Z
DEVICES TICPAL22V10Z(TURBO), TICPAL22V10Z(ZERO PWR)
INCLUDED


ARRAY PROGRAMMING PROCEDURE:

Array FAMOS transistors are programmed by executing the following programming sequence. Each FAMOS transistor can be programmed by selecting the appropriate Inputs Line(s), (1 of 45), and Product Lines(s), (1 of 17). The levels for selecting Input Lines and Product Lines are shown in Tables 1-3 and 1-4.

- Step 1. Raise Pin 24 to 5V and Pin 13 to V_{IH} .
- Step 2. Raise Pin 1 to V_{IHH} .
- Step 3. Address the first location.
- Step 4. Place the data to be programmed on I/O pins.
- Step 5. $X = 0$
- Step 6. Program one 1.0 ms pulse by pulsing Pin 13 to a V_{IHH} level.
- Step 7. $X = X + 1$
- Step 8. If $X = 10$, then GOTO Step 10.
- Step 9. Verify the data by taking Pin 13 to V_{IL} . If incorrect, repeat Steps 6 through 8
- Step 10. Program one pulse of duration $4 * X * 1.0$ ms.
- Step 11. Reverify data. If incorrect, device fails (END).
- Step 12. Repeat Steps 4 through 11 until all addresses are programmed.
- Step 13. Verify array at 5V.
- Step 14. Lower Pin 1 to 0V.
- Step 15. Lower Pin 24 to 0V.

SECURITY FUSE PROGRAMMING PROCEDURES: (See Figure 3)

- Step 1. Raise Pin 24 to 5V.
- Step 2. Address the device per Tables 1-3 and 1-4.
- Step 3. Raise Pin 1 to a V_{IHH} .
- Step 4. Raise Pin 3 to a V_{IHH} .
- Step 5. Program the Security Fuse by pulsing Pin 13 to a V_{IHH} .

| | | | | | |
|-------------------------------------|--|------------------|--|----------|----------------------|
| PREPARED BY B. Cole PAL24C-1.DWG | | DATE 10/28/88 |  TEXAS INSTRUMENTS | | |
| CHECKED BY <i>M. Haddige</i> | | DATE 7/17/90 | TITLE ALGORITHM SPECIFICATION TICPAL22V10Z | | |
| ENGINEER <i>Jim Fournier</i> | | DATE 7/19/90 | | | |
| APPROVED BY <i>[Signature]</i> | | DATE 7/19/90 | REVISION B | A | PAL24010 |
| RELEASED BY <i>[Signature]</i> | | DATE 7/17/90 | LETTER | SIZE | |
| | | | | | SHEET 1 10 |

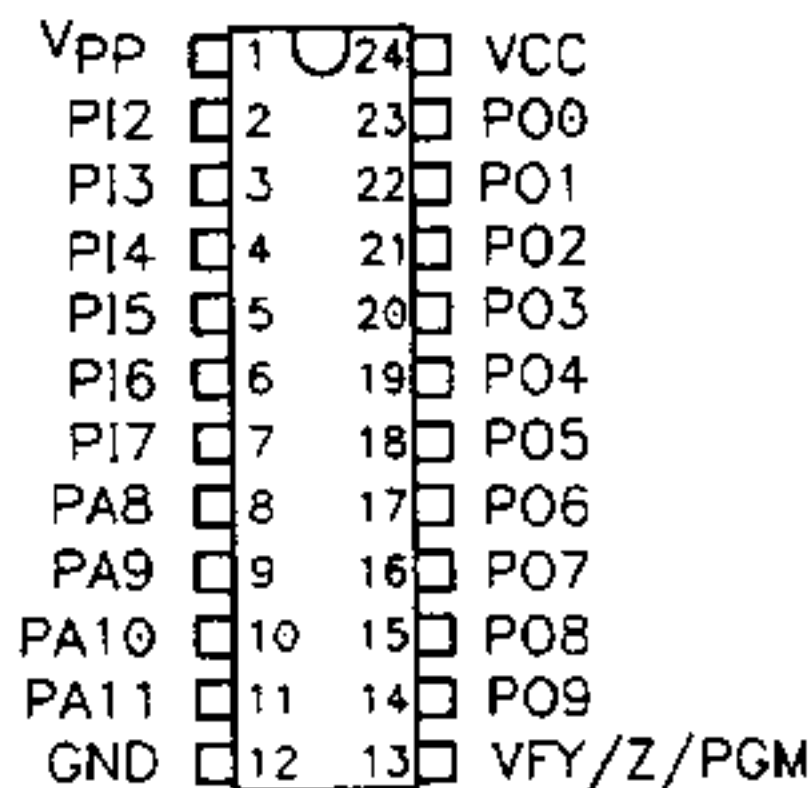
SECURITY FUSE VERIFY PROCEDURES: (See Figure 3)

- Step 1. Raise Pin 24 to 5V.
- Step 2. Raise Pin 1 to a V_{IH} .
- Step 3. Raise Pin 4 to V_{IH} .
- Step 4. Address the device per Tables 1-3 and 1-4 for Security Fuse Verify. With Pin 13 at V_{IL} , Pin 3 will act as an output under these conditions and will be a logical "0" if the Security Fuse is not programmed, and a logical "1" if the Security Fuse is programmed.

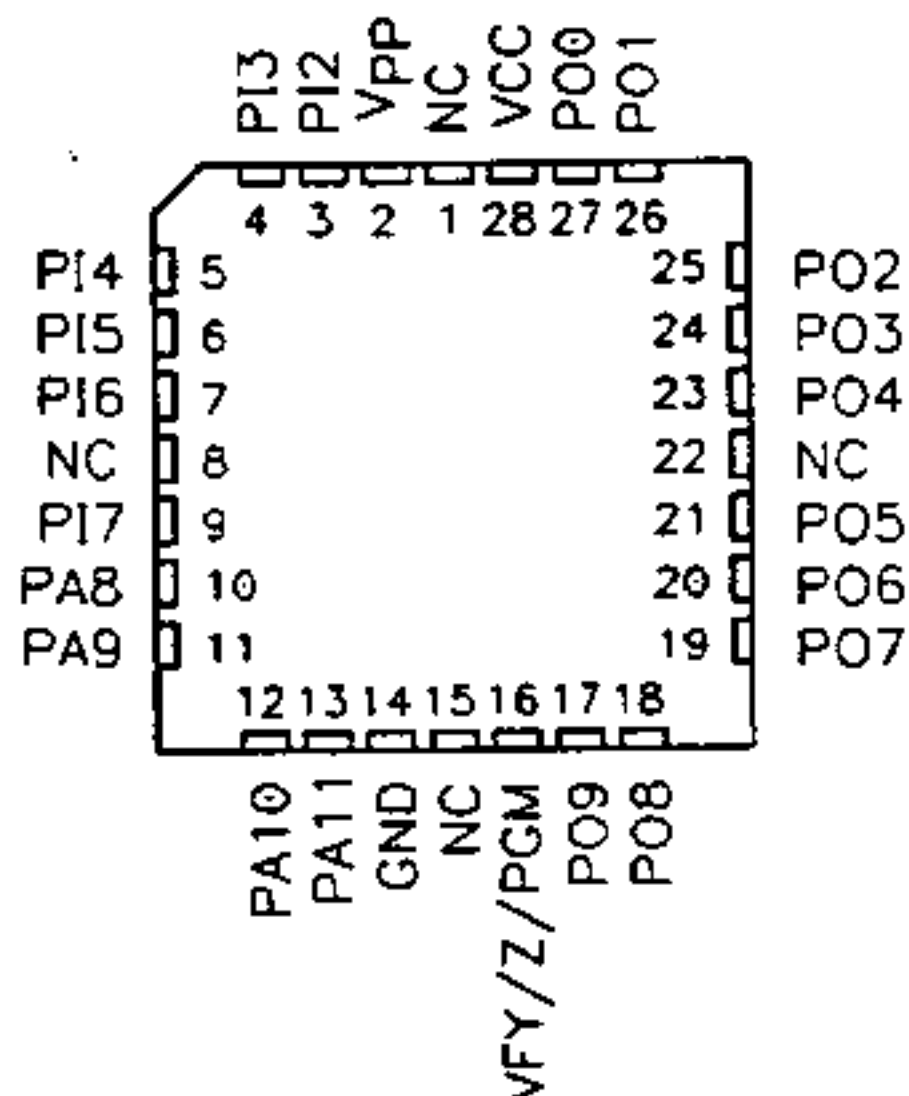
NOTE: Pin 13 should always be at V_{IH} , when changing a device address.

pin assignments in programming mode

JD OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



TURBO-BIT PROGRAMMING

Treat the C22V10Z as two separate devices and create two algorithms --- one for the TURBO mode, and one for the ZERO POWER mode. The two devices will be listed in the programmer's menu and device lists as follows:

C22V10Z(TURBO) and C22V10Z(ZERO PWR). These names may need to be shortened, i.e. 'T' = TURBO and 'ZP' = ZERO PWR. For programmer manufacturers who use family pinout codes, two separate codes must be assigned.

JEDEC FILE

The only JEDEC file needed will be a standard 22V10 file with 5828 bits numbered 0...5827. The TURBO-Bit shall not be a part of the JEDEC file. Any requirement to modify the standard JEDEC file to include the TURBO-Bit will not be supported by TI.

CHECKSUM

The TURBO-Bit will not be used to compute a logic code's checksum.

LOADING MASTERS

A blank device's logic code shall be loadable, without error, using either of the algorithms.

The two algorithms will be 100% JEDEC compatible.

VERIFICATION AND PROGRAMMING

When using the C22V10Z(ZERO PWR) algorithm to program a device, the TURBO-Bit shall be verified just like any other bit. If the TURBO-Bit shows to be programmed, the programmer shall give a "VERIFY" error.

When using the C22V10Z(TURBO) algorithm to program a device, the TURBO-Bit shall always be programmed and verified. If there is a preprogramming blank check routine, and the TURBO-Bit has already been programmed, then the programmer shall give a "NON-BLANK DEVICE" warning. Otherwise, the programming shall continue without interruption.

TABLE 1-2, Programming Parameters, $T_A = 25^\circ \text{C}$

| PARAM | DESCRIPTION | MIN | NOM | MAX | UNIT |
|--------------------|----------------------------------|-------|-------|----------|---------------|
| V_{CCP} | Supply Voltage – Programming | 4.75 | 5.00 | 5.25 | V |
| V_{IHH} | Programming Voltage | 13.00 | 13.50 | 14.00 | V |
| V_{IH} | High Level Input Voltage | 3.00 | | V_{CC} | V |
| V_{IL} | Low Level Input Voltage | 0.00 | | 0.40 | V |
| V_{OH} | Voltage Out – High | 2.40 | | | V |
| V_{OL} | Voltage Out – Low | | | 0.40 | V |
| I_{PP} | Supply Current – Programming | | | 90 | mA |
| t_p | Delay to Programming Voltage | 20 | | | μs |
| t_{prime} | Programming Pulse Width | 0.95 | | 1.05 | ms |
| t_{final} | Programming Pulse Width | 3.8 | | 42 | ms |
| t_{dp} | Delay to Program | 1 | | | μs |
| t_r, t_f | V_{IHH} Rise/Fall Time | 50 | | | ns |
| t_{r1}, t_{f1} | V_{IHH} Rise/Fall Time PGM/VFY | 20 | | | ns |
| t_{as} | Address Set-up Time | 1 | | | μs |
| t_{ah} | Address Hold Time | 1 | | | μs |
| t_{hp} | Hold from Program or Verify | 1 | | | μs |
| t_{ds} | Data Set-up Time | 1 | | | μs |
| t_{dh} | Data Hold Time | 1 | | | μs |
| t_{scty} | Programming PW for Security | 50 | | | ms |
| t_{dv} | Delay from Program to Verify | 2 | | | μs |
| t_{vd} | Delay to Data Out | | | 1 | μs |
| t_{vp} | Verify Pulse Width | 2 | | | μs |
| t_{dz} | Verify to High Z | | | 1 | μs |

TABLE 1-3, INPUT LINE ADDRESSING

| INPUT LINE NUMBER | INPUT LINE NUMBER-ADDRESS PIN STATES | | | | | |
|----------------------|--------------------------------------|-----|-----|-----|--------|-----|
| | P17 | P16 | P15 | P14 | P13 | P12 |
| 00 | L | L | L | L | L | L |
| 01 | L | L | L | L | L | H |
| 02 | L | L | L | L | H | H |
| 03 | L | L | L | L | H | H |
| 04 | L | L | L | H | L | H |
| 05 | L | L | L | H | L | H |
| 06 | L | L | L | H | H | L |
| 07 | L | L | L | H | H | L |
| 08 | L | L | H | L | L | L |
| 09 | L | L | H | L | L | H |
| 10 | L | L | H | L | H | L |
| 11 | L | L | H | L | H | H |
| 12 | L | L | H | H | L | L |
| 13 | L | L | H | H | L | H |
| 14 | L | L | H | H | H | L |
| 15 | L | L | H | H | H | H |
| 16 | L | H | L | L | L | L |
| 17 | L | H | L | L | L | H |
| 18 | L | H | L | L | H | L |
| 19 | L | H | L | L | H | H |
| 20 | L | H | L | H | L | L |
| 21 | L | H | L | H | L | H |
| 22 | L | H | L | H | H | L |
| 23 | L | H | L | H | H | H |
| 24 | L | H | H | L | L | L |
| 25 | L | H | H | L | L | H |
| 26 | L | H | H | L | H | L |
| 27 | L | H | H | L | H | H |
| 28 | L | H | H | H | L | L |
| 29 | L | H | H | H | L | H |
| 30 | L | H | H | H | H | L |
| 31 | L | H | H | H | H | H |
| 32 | H | L | L | L | L | L |
| 33 | H | L | L | L | L | H |
| 34 | H | L | L | L | H | L |
| 35 | H | L | L | L | H | H |
| 36 | H | L | L | L | L | L |
| 37 | H | L | L | H | L | H |
| 38 | H | L | L | H | H | L |
| 39 | H | L | L | H | H | H |
| 40 | H | L | H | L | L | L |
| 41 | H | L | H | L | L | H |
| 42 | H | L | H | L | H | L |
| 43 | H | L | H | L | H | H |
| ARCH S0/S1 | H | H | H | H | H | H |
| TURBO | H | H | H | H | H | H |
| SF PROG | L | L | L | L | HH | L |
| SF VERIFY | L | L | L | HH | OUTPUT | L |

ARCH S0 - ARCHITECTURE POLARITY FUSE

SF - SECURITY FUSE

ARCH S1 - ARCHITECTURE REGISTER/LOGIC FUSE

TABLE 1-4, PRODUCT TERM ADDRESSING

| PRODUCT TERM | | | | | | | | | | PRODUCT TERM SELECT ADDRESS PIN STATES | | | |
|----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|--|------|-----|-----|
| P00 | P01 | P02 | P03 | P04 | P05 | P06 | P07 | P08 | P09 | PA11 | PA10 | PA9 | PA8 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | L | L | L | L |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | L | L | L | H |
| 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | L | L | H | L |
| 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | L | L | H | H |
| 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | L | H | L | L |
| 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | L | H | L | H |
| 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | L | H | H | L |
| 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 | L | H | H | H |
| | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | | H | L | L | L |
| | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | | H | L | L | H |
| | | 10 | 10 | 10 | 10 | 10 | 10 | | | H | L | H | L |
| | | 11 | 11 | 11 | 11 | 11 | 11 | | | H | L | H | H |
| | | | 12 | 12 | 12 | 12 | | | | H | H | L | L |
| | | | 13 | 13 | 13 | 13 | | | | H | H | L | H |
| | | | | 14 | 14 | | | | | H | H | H | L |
| | | | | 15 | 15 | | | | | H | H | H | H |
| OE | OE | OE | OE | OE | OE | OE | OE | OE | OE | HH | H | H | H |
| | | | AR | | | | | | | H | H | H | H |
| | | | | | | SP | | | | H | H | H | H |
| S0 | S0 | S0 | S0 | S0 | S0 | S0 | S0 | S0 | S0 | HH | L | L | L |
| S1 | S1 | S1 | S1 | S1 | S1 | S1 | S1 | S1 | S1 | HH | L | H | L |
| | | | | | | | TB | | | HH | H | H | L |
| SF PROG/VERIFY | | | | | | | | | | L | L | L | L |

OE - OUTPUT ENABLE

AR - ASYNCHRONOUS RESET

SP - SYNCHRONOUS PRESET

S0 - ARCHITECTURE POLARITY FUSE

S1 - ARCHITECTURE REGISTER/LOGIC FUSE

TB - TURBO-BIT

- DATA IS PIN 20

- DATA IS PIN 17

- OUTPUT POLARITY

- OUTPUT REGISTER/LOGIC

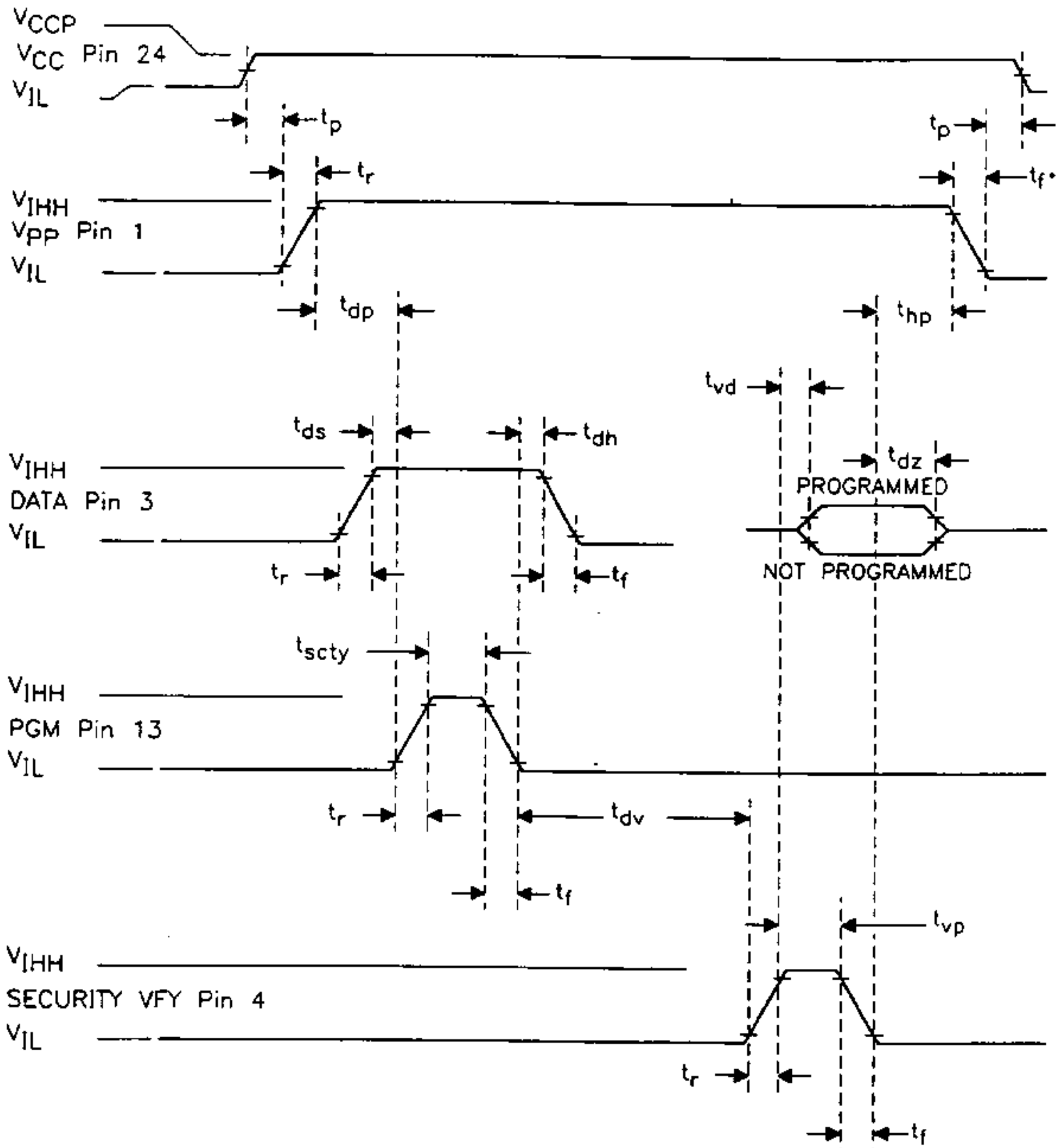
- DATA IS PIN 16



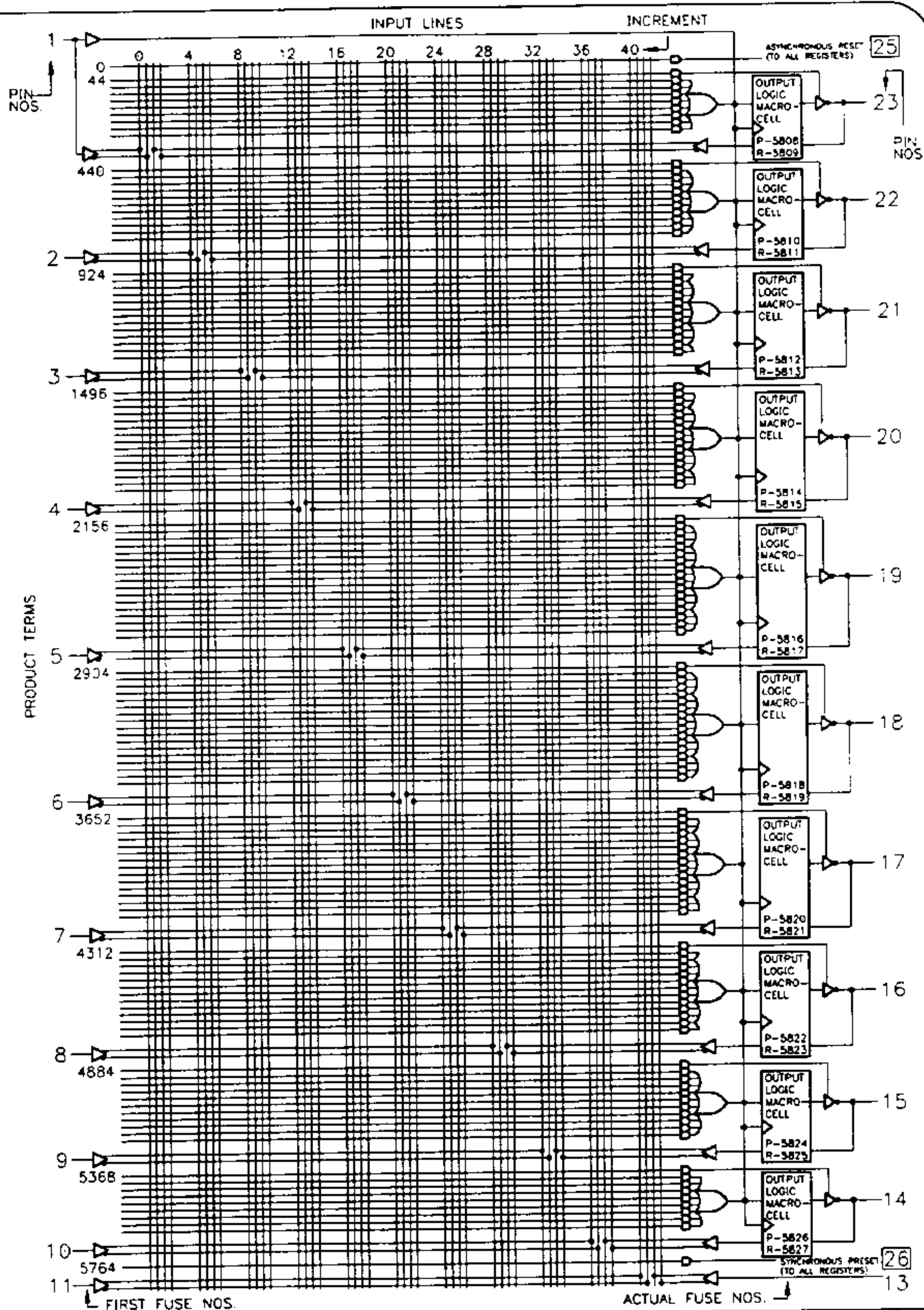
1. Pin 1 & Pin 24 should not be cycled for each program/verify cycle, but may remain static during programming.
2. For programming \overline{OE} Product Terms & Architecture bits, Pin 11 must go to V_{IH} and satisfy t_{as} and t_{ah} .

FIGURE 3

Programming Waveforms Security Fuse



NOTE: Inside each Macrocell, the 'P' fuse No. is the polarity fuse, and the 'R' fuse No. is the register fuse.



REVISION HISTORY

| REVISION LTR. | DATE | ENGINEER | DESCRIPTION OF CHANGES |
|---------------|-------|----------|---|
| A | 10-89 | Thomas | Added a page to explain how the C22V10Z TURBO and ZERO PWR modes are programmed. Removed fuse t-5828 from the fuse map. |
| B | 06-90 | Lippens | Sh 6: Table 1-4. Added TB - TURBO BIT - Data is pin 16. |