

TEXAS INSTRUMENTS
FIELD PROGRAMMABLE LOGIC DEPARTMENT
PROGRAMMING ALGORITHM SPECIFICATION

DEVICE FAMILY PAL20XXA
DEVICES PAL20L8A, PAL20R4A, PAL20R6A, PAL20R8A
INCLUDED

PROGRAMMING PROCEDURE:

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (1 of 40) Input Line and then pulsing the correct (1 of 64) Product Line. The levels for selecting Input Lines and Product Lines are shown in Table 1-2.

- Step 1: Raise PGM ENABLE to V_{IHH}
- Step 2: Select an Input Line by applying appropriate levels to L/R and PI pins. Apply V_{IL} or V_{IH} to selected PI pin (See Table 1-2).
- Step 3: Select Product Line by applying appropriate levels to PA pins (See Table 1-2).
- Step 4: Raise V_{CC} to V_{IHH} .
- Step 5: Blow the fuse by pulsing the appropriate PO pin to V_{IHH} .
- Step 6: Return V_{CC} to 5 volts and pulse PGM VERIFY. The PO pin will exhibit a low output if the fuse is blown.

Four fuse locations can be verified simultaneously, however, fuses should be addressed and blown sequentially.

If the fuse is still intact, steps 4 thru 6 may be repeated until the fuse is successfully blown, not to exceed 4 retries. Do not apply additional pulses to a fuse once it is correctly programmed.

For Input and Product Line selection see Table 1-2.

For programming waveforms see Figure 1-1.

To prevent further verification, two security fuses may be blown by raising PGM ENABLE and PGM VERIFY to 16 volts. V_{CC} must be at 0 volts during this operation (See Figure 1-2).

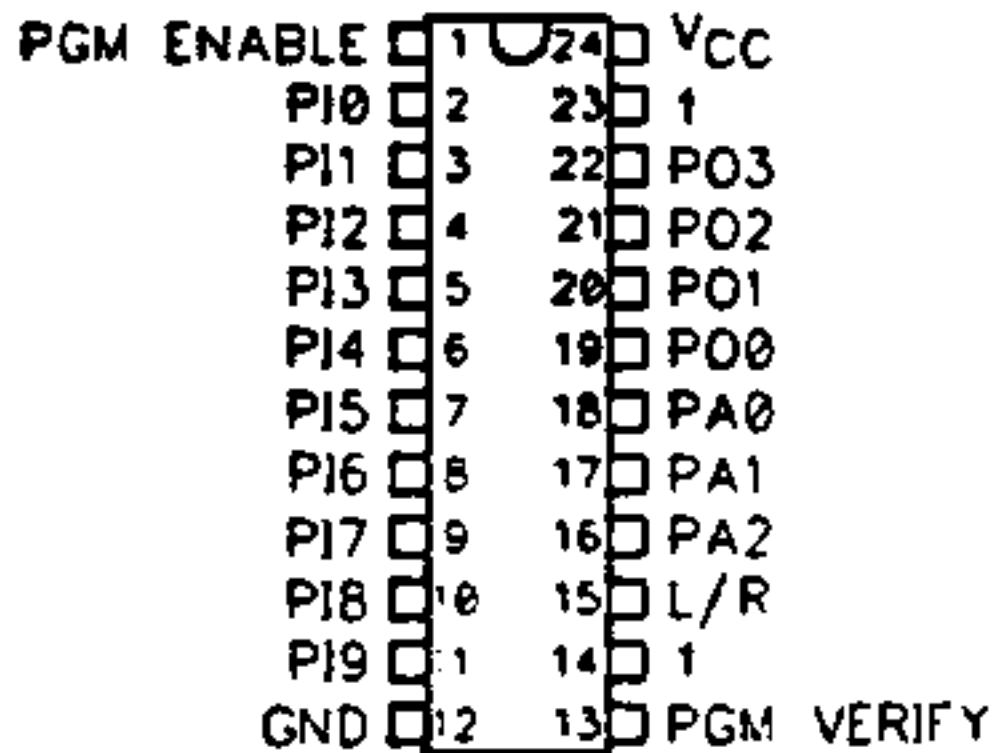
PREPARED BY B. Cole PAL20-1.DWG		DATE 10/15/86		TEXAS INSTRUMENTS	
CHECKED BY <i>Donald B. Jones</i>		DATE 04/12/88		TITLE: ALGORITHM SPECIFICATION PAL20XXA	
ENGINEER Jim Giddings		DATE 10/15/86			
APPROVED BY <i>Donald B. Jones</i>		DATE 04/29/88		REVISION C	SIZE A
RELEASED BY 		DATE / /		LETTER	PAL24002
					SHEET 1 11

PIN ASSIGNMENTS IN PROGRAMMING MODE

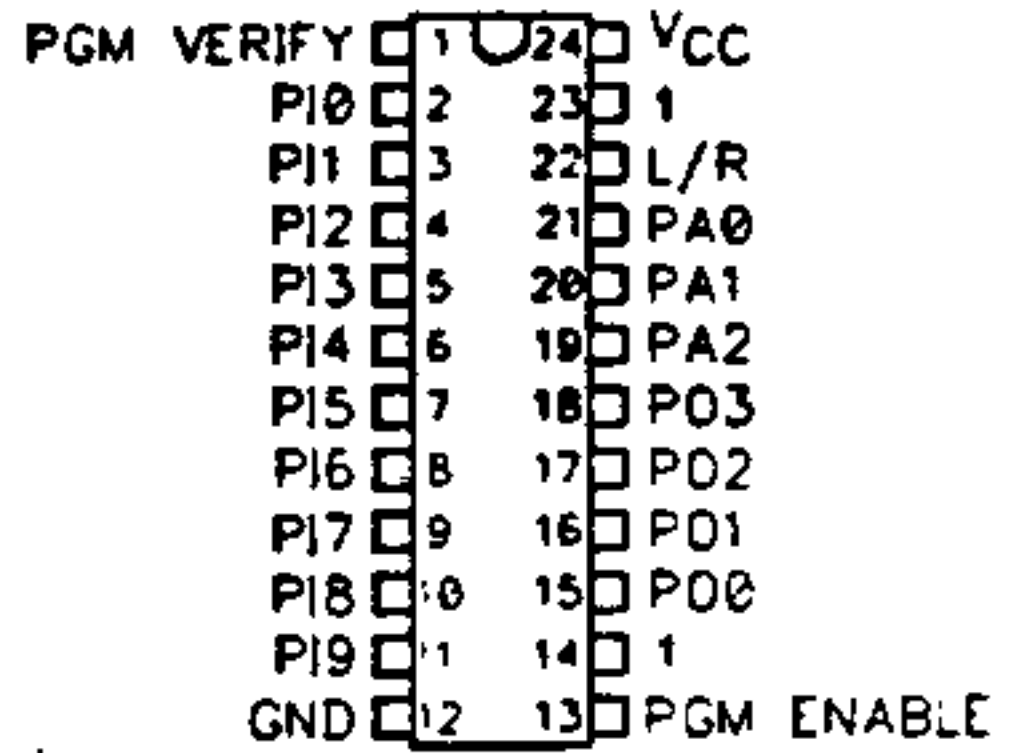
PRODUCT TERMS 0 THRU 31

PRODUCT TERMS 32 THRU 63

(TOP VIEW)

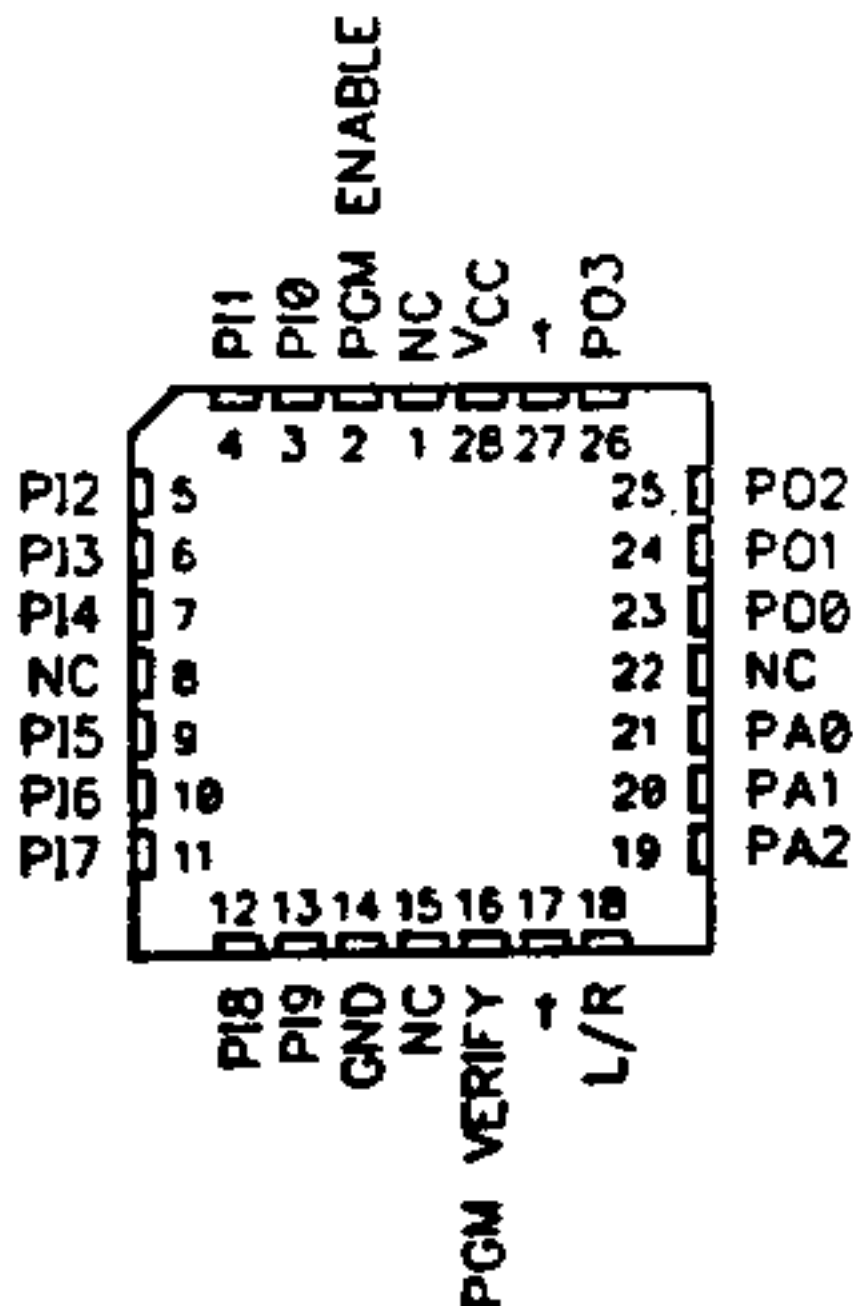


(TOP VIEW)



¹ Pins 14 and 23 have no programming function. Make no connection.

(TOP VIEW)



(TOP VIEW)

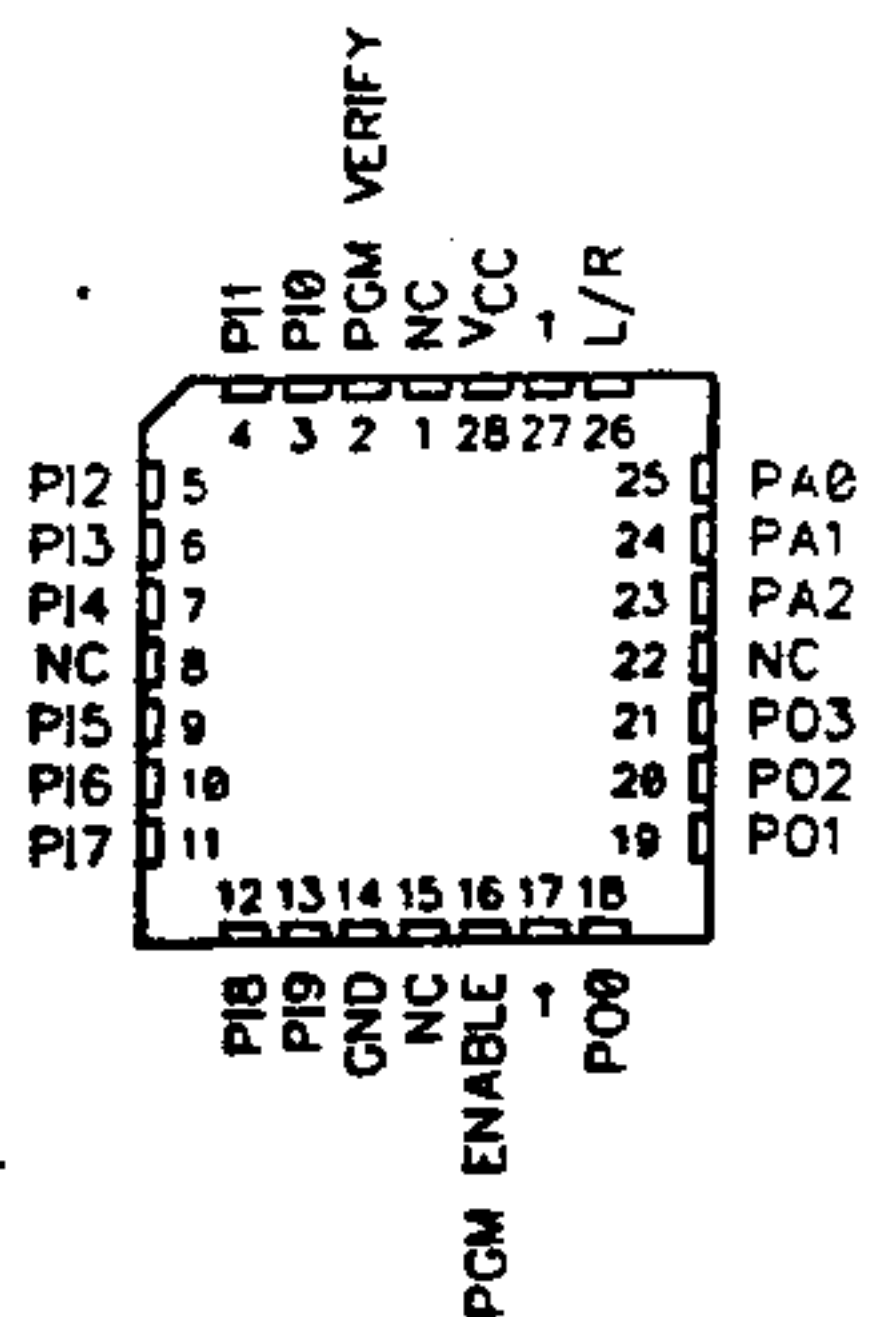


TABLE 1-1. PROGRAMMING PARAMETERS. TA = 25°C

PARAM	DESCRIPTION	MIN	NOM	MAX	UNIT
V _{CC}	Verify-level supply voltage	4.75	5.00	5.25	V
V _{IH}	High-Level input voltage	2.40		5.50	V
V _{IL}	Low-level input voltage			0.50	V
V _{IHH}	Program-pulse voltage	10.25	10.50	10.75	V
I _{IHH}	Program-pulse PO		20	50	Ma
	current PGM ENA, L/R		10	25	Ma
	PI, PA		1.5	5	Ma
	I _{CC}		250	400	Ma
t _{w1}	Program-pulse duration at PO	10		50	uS
	Prog.-pulse duty cycle, PO, V _{CC}			25	%
t _{w2}	Pulse duration at PGM VERIFY	100			nS
t _{su}	Set-up time	100			nS
t _h	Hold time	100			nS
t _{d1}	Delay time from V _{CC} to 5V to PGM VERIFY	100			uS
t _{d2}	Delay time from PGM VERIFY pulse to valid output	200			nS
	Voltage at pins 1 and 11 to open verify-protect (security) fuse		16		V
	Current to open security fuse			400	Ma
	Security fuse pulse duration	20		50	uS
t _{w3}	V _{CC} during security fusing		0	0.40	V

TABLE 1-2. INPUT/PRODUCT LINE SELECT

TABLE 1 - INPUT LINE SELECT

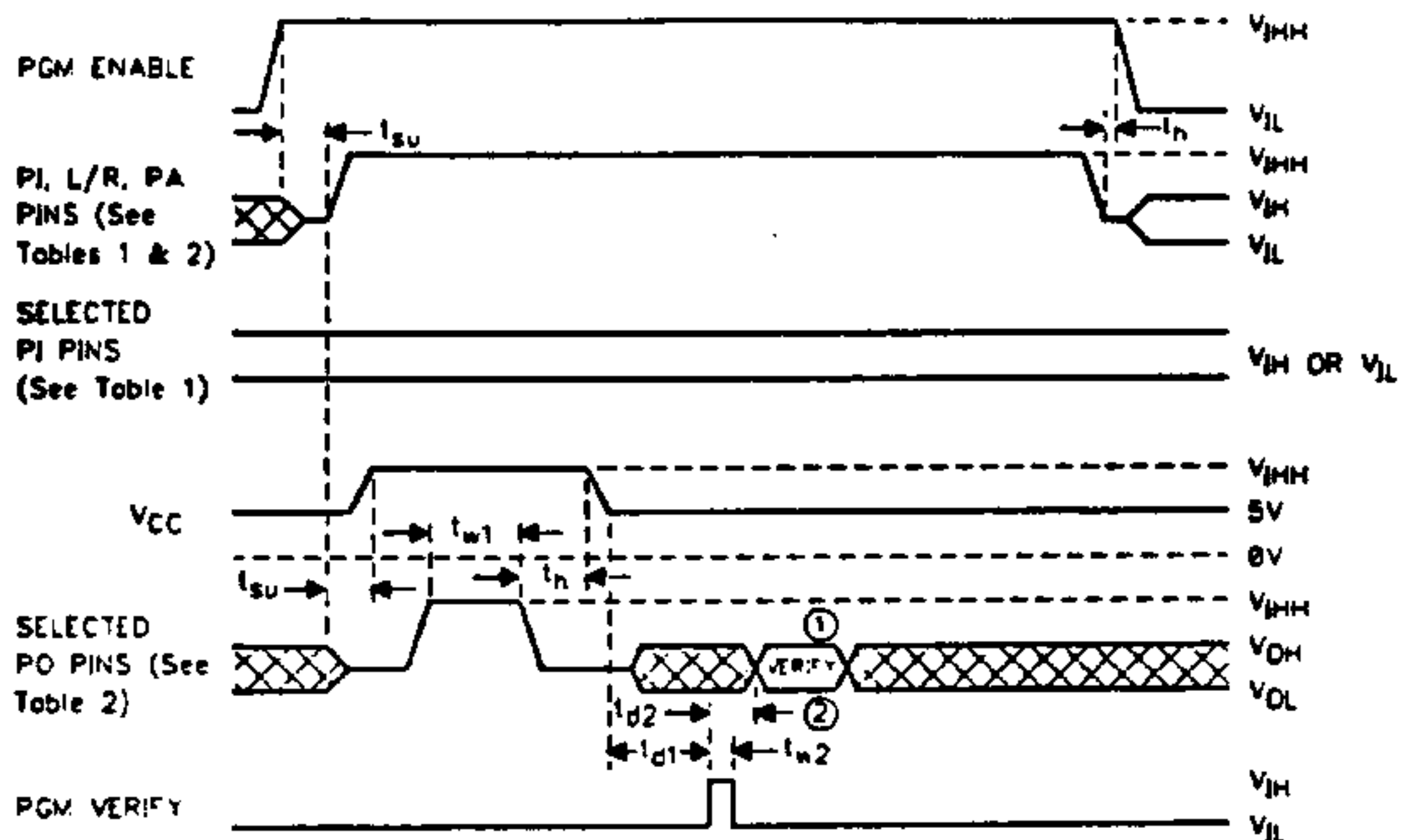
TABLE 2 - PRODUCT LINE SELECT

INPUT LINE NO.	PIN NAME									
	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L HH	HH
7	HH	HH	HH	HH	HH	HH	HH	H HH	H HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

PROD. LINE NO.	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0,32	Z	Z	Z	HH	Z	Z	Z
1,33	Z	Z	Z	HH	Z	Z	HH
2,34	Z	Z	Z	HH	Z	HH	Z
3,35	Z	Z	Z	HH	Z	HH	HH
4,36	Z	Z	Z	HH	HH	Z	Z
5,37	Z	Z	Z	HH	HH	Z	HH
6,38	Z	Z	Z	HH	HH	HH	Z
7,39	Z	Z	Z	HH	HH	HH	HH
8,40	Z	Z	HH	Z	Z	Z	Z
9,41	Z	Z	HH	Z	Z	Z	HH
10,42	Z	Z	HH	Z	Z	HH	Z
11,43	Z	Z	HH	Z	Z	HH	HH
12,44	Z	Z	HH	Z	HH	Z	Z
13,45	Z	Z	HH	Z	HH	Z	HH
14,46	Z	Z	HH	Z	HH	HH	Z
15,47	Z	Z	HH	Z	HH	HH	HH
16,48	Z	HH	Z	Z	Z	Z	Z
17,49	Z	HH	Z	Z	Z	Z	HH
18,50	Z	HH	Z	Z	Z	HH	Z
19,51	Z	HH	Z	Z	Z	HH	HH
20,52	Z	HH	Z	Z	HH	Z	Z
21,53	Z	HH	Z	Z	HH	Z	HH
22,54	Z	HH	Z	Z	HH	HH	Z
23,55	Z	HH	Z	Z	HH	HH	HH
24,56	HH	Z	Z	Z	Z	Z	Z
25,57	HH	Z	Z	Z	Z	Z	HH
26,58	HH	Z	Z	Z	Z	HH	Z
27,59	HH	Z	Z	Z	Z	HH	HH
28,60	HH	Z	Z	Z	HH	Z	Z
29,61	HH	Z	Z	Z	HH	Z	HH
30,62	HH	Z	Z	Z	HH	HH	Z
31,63	HH	Z	Z	Z	HH	HH	HH

L = V_{IL} , H = V_{IH} , HH = V_{IHH} , Z = high impedance (e.g. 10 k Ω to GND except for pin being verified = 10 k Ω to 5V).

FIGURE 1-1. PROGRAMMING WAVEFORMS



- ① A high level during the verify interval indicates that programming has not been successful.
 ② A low level during the verify interval indicates that programming has been successful.

FIGURE 1-2. SECURITY FUSE WAVEFORMS

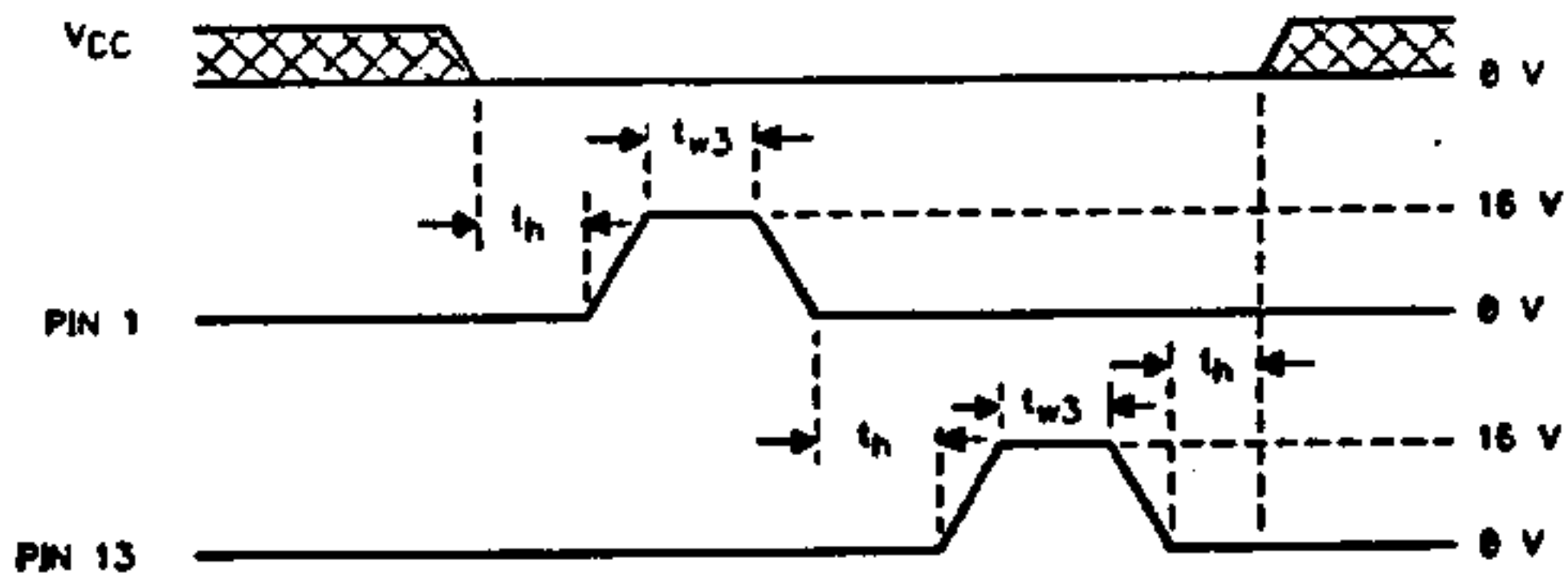


FIGURE 1-3. PRELOAD PROCEDURES

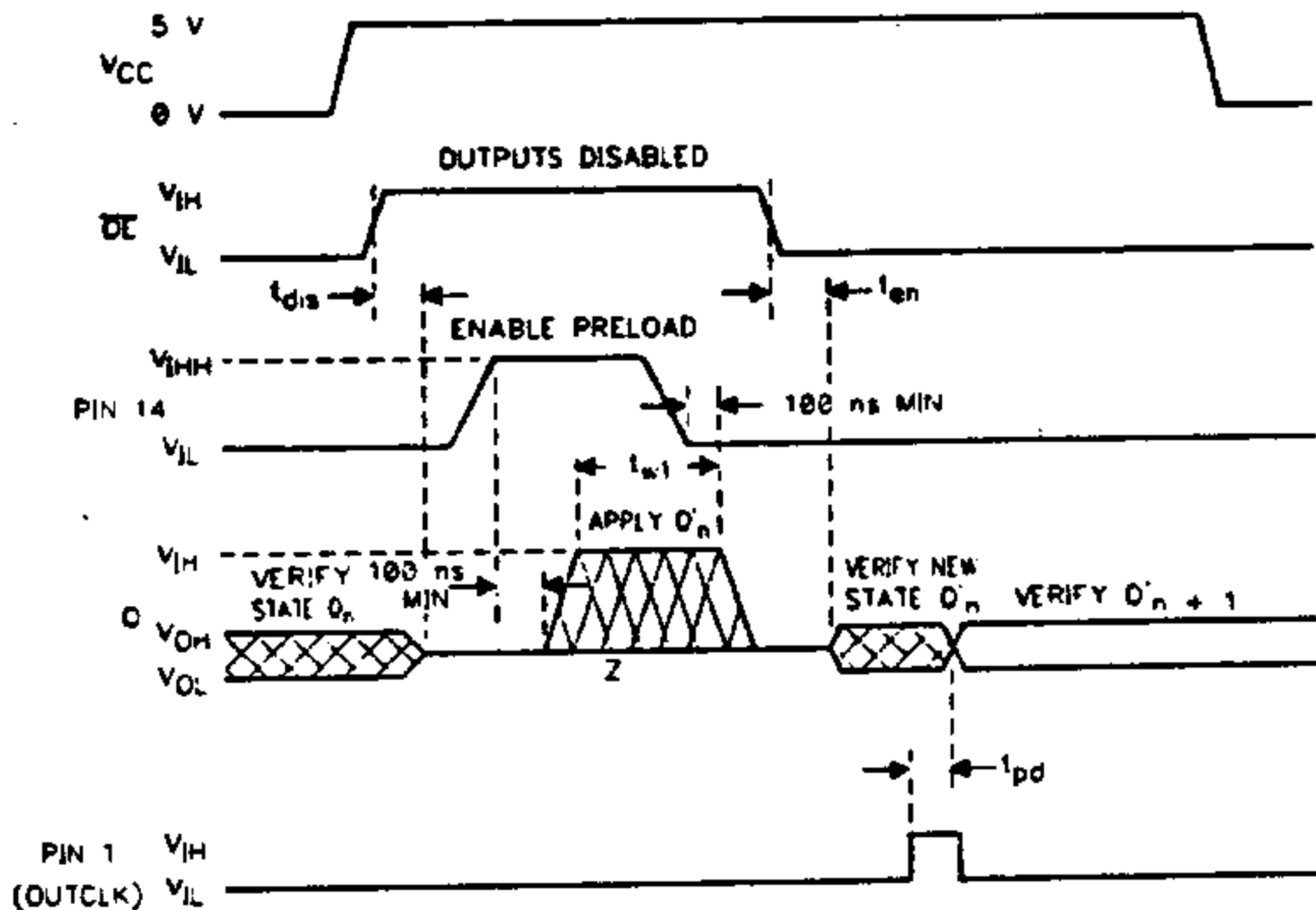
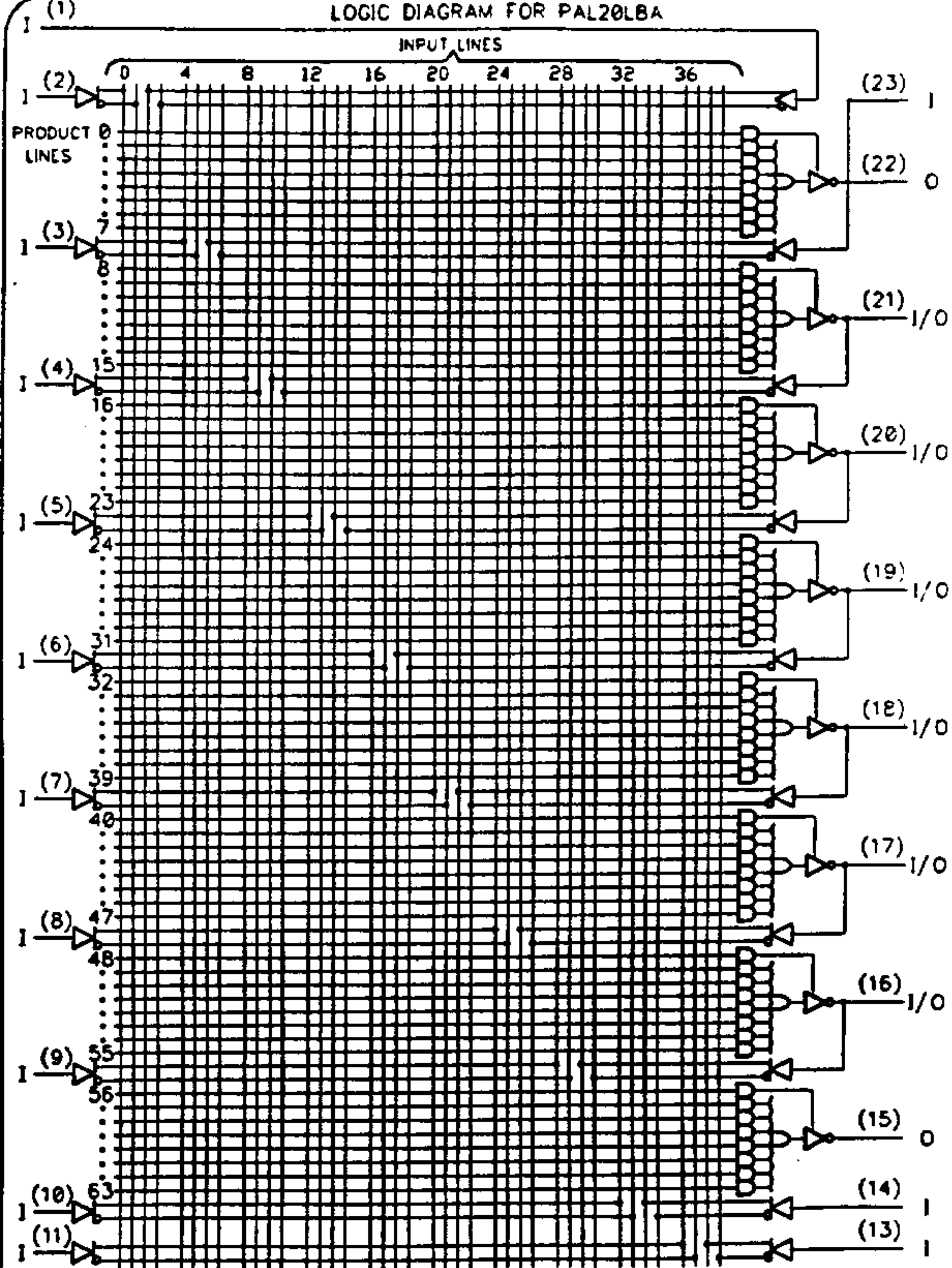


FIGURE 1. PRELOAD WAVEFORMS

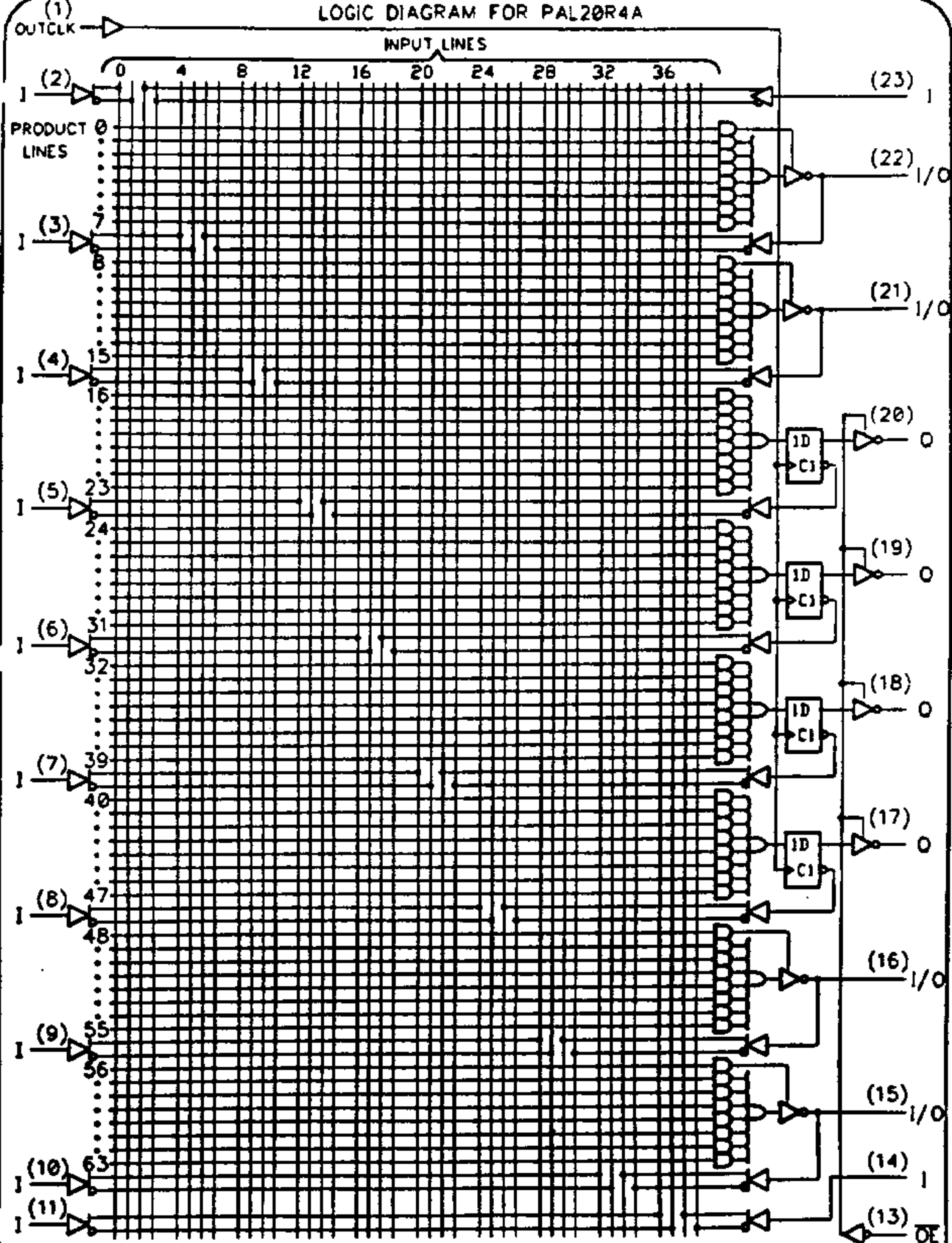
preload procedure for registered outputs

- Step 1: Pin 13 to V_{IH} , PIN 1 TO V_{IL} , AND V_{CC} to 5 volts.
- Step 2: Pin 14 to V_{IH} for 10 to 50 microseconds.
- Step 3: Apply V_{IL} for a low and V_{IH} for a high at the Q outputs.
- Step 4: Pin 14 to V_{IL} .
- Step 5: Remove the voltages applied to the outputs.
- Step 6: Pin 13 to V_{IL} .
- Step 7: Check the output states to verify preload.

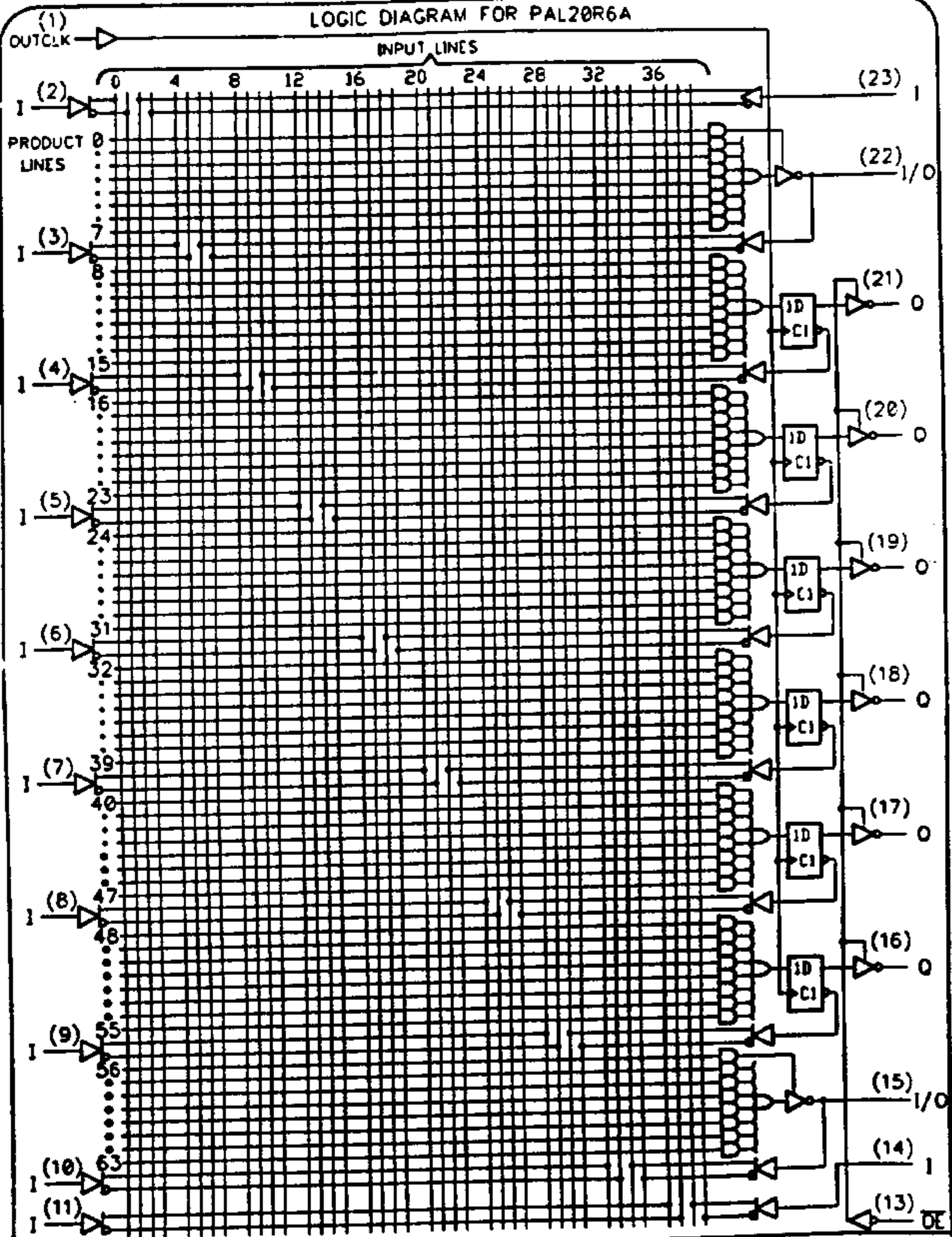
LOGIC DIAGRAM FOR PAL20LBA



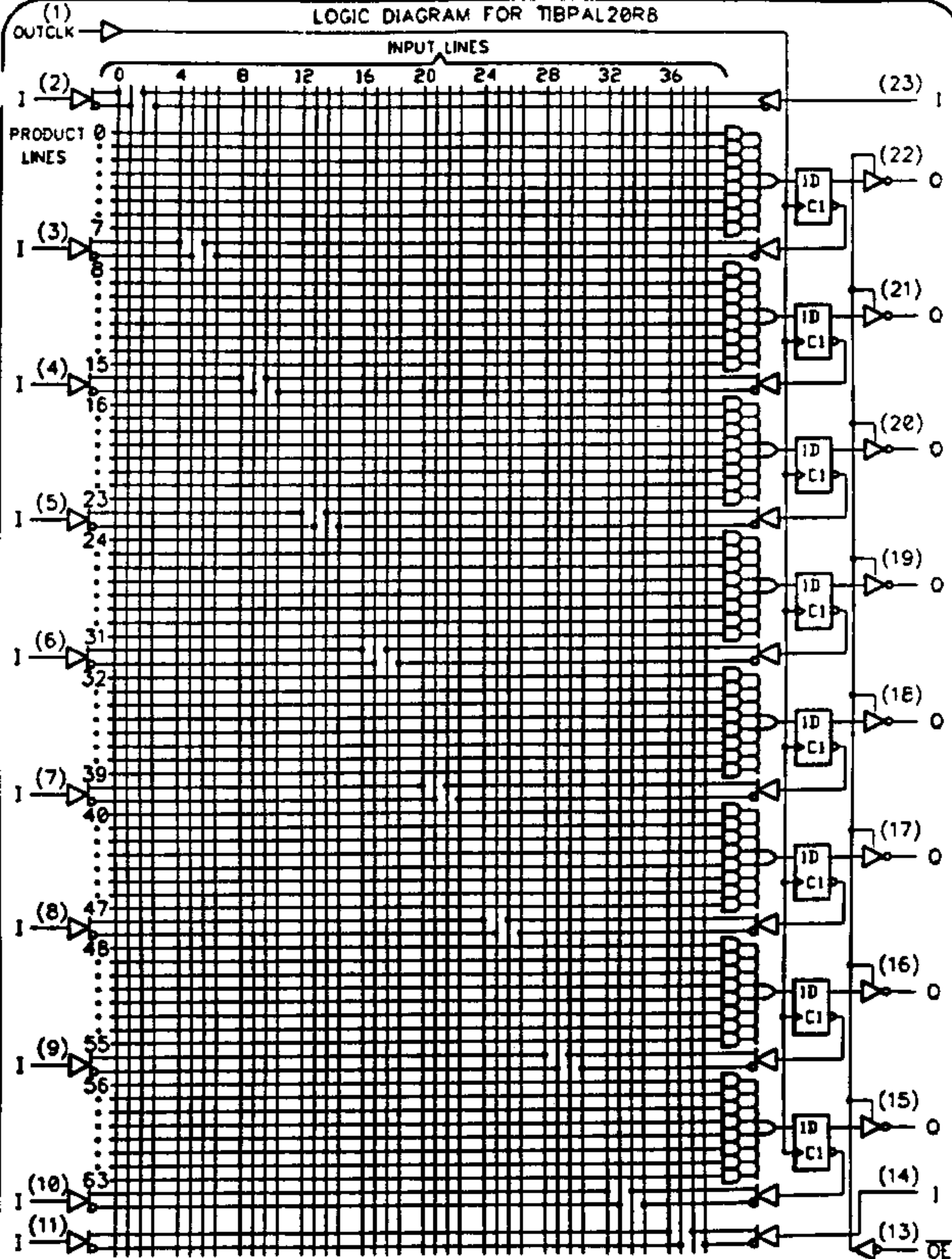
LOGIC DIAGRAM FOR PAL20R4A



LOGIC DIAGRAM FOR PAL20R6A



LOGIC DIAGRAM FOR TIBPAL20R8



REVISION HISTORY

REVISION LTR.	DATE	ENGINEER	DESCRIPTION OF CHANGES
A	11-86	Giddings	Security fuse statement added to programming procedure. Table 1-2; Z (high impedance) redefined Table 1-1; Corrected security fuse voltage. Figure 1-2; Pin 11 changed to pin 13. Figure 1-3; Preload waveforms added.
B	12-87	Thomas	Changed pin 11 to pin 13 in Figure 1-2.
C	4-88	Thomas	Sht. 2; Added PLCC Pinout. Sht. 3; Added $V_{CC} = 4.75$ Min. and $V_{CC} = 5.25$ Max.