

TEXAS INSTRUMENTS
FIELD PROGRAMMABLE LOGIC DEPARTMENT
PROGRAMMING ALGORITHM SPECIFICATION

DEVICE FAMILY T1BPAL20XX
DEVICES T1BPAL20L8-15, T1BPAL20R4-15, T1BPAL20R6-15, AND
INCLUDED T1BPAL20R8-15
 T1BPAL20L8-25, T1BPAL20R4-25, T1BPAL20R6-25, AND
 T1BPAL20R8-25

PROGRAMMING PROCEDURE:

Array fuses are programmed by executing the following programming sequence. The levels for selecting Input Lines and Product Lines are shown in Tables 1-2 and 1-3.

- Step 1: Raise PGM ENABLE to V_{IHH} .
- Step 2: Select an Input Line by applying appropriate logic levels to PI pins.
- Step 3: Select a Product Line group by applying appropriate logic levels to PA pins. The actual product line selected will be determined by the PO pin (described in step 5).
- Step 4: Raise /OE to V_{IH} .
- Step 5: Raise the selected PO pin to V_{IHH} .
- Step 6: Program the fuse by pulsing V_{CC} to V_{IHH} .
- Step 7: Remove the output voltage.
- Step 8: Lower /OE to V_{IL} to enable device.
- Step 9: Verify the blowing of fuse by checking for a V_{OL} at the selected PO pin.

If the fuse is still intact, steps 1 thru 9 may be repeated until the fuse is successfully blown, not to exceed 4 retries. Do not apply additional pulses to a fuse once it is correctly programmed. Verification is possible only with the Security fuse intact.

A single security fuse is provided on each device to discourage the unauthorized copying of fuse patterns. To program the security fuse, follow the steps above omitting steps 2, 5, and 9. Verification is achieved by verifying the entire fuse array. If the security fuse is blown, all other fuses will appear to be blown.

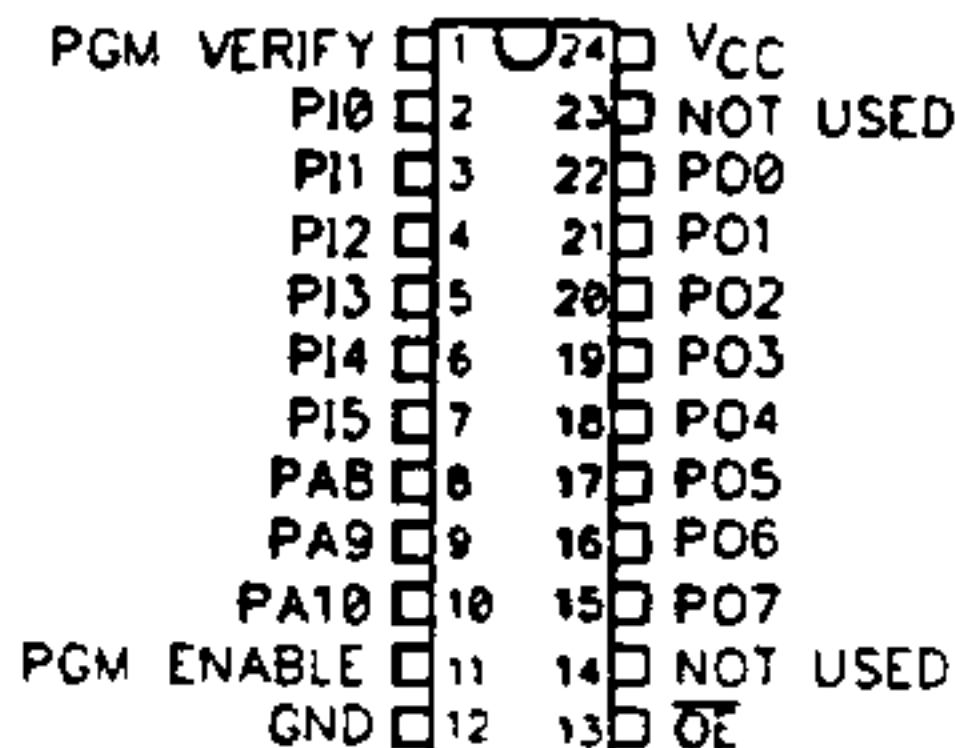
For Input and Product Line selection, see Tables 1-2 and 1-3.

For programming waveforms, see Figure 1-1.

PREPARED BY B. Cole TPAL20-1.DWG		DATE 10/24/86		TEXAS INSTRUMENTS	
CHECKED BY <i>Donald B. Roney</i>		DATE 02/12/88		TITLE: ALGORITHM SPECIFICATION T1BPAL20XX	
ENGINEER Doyce Roney		DATE 10/24/86			
APPROVED BY <i>Donald B. Roney</i>		DATE 02/12/88		REVISION E	SIZE A
RELEASED BY / /		DATE / /		PAL24003	
				SHEET 1 11	

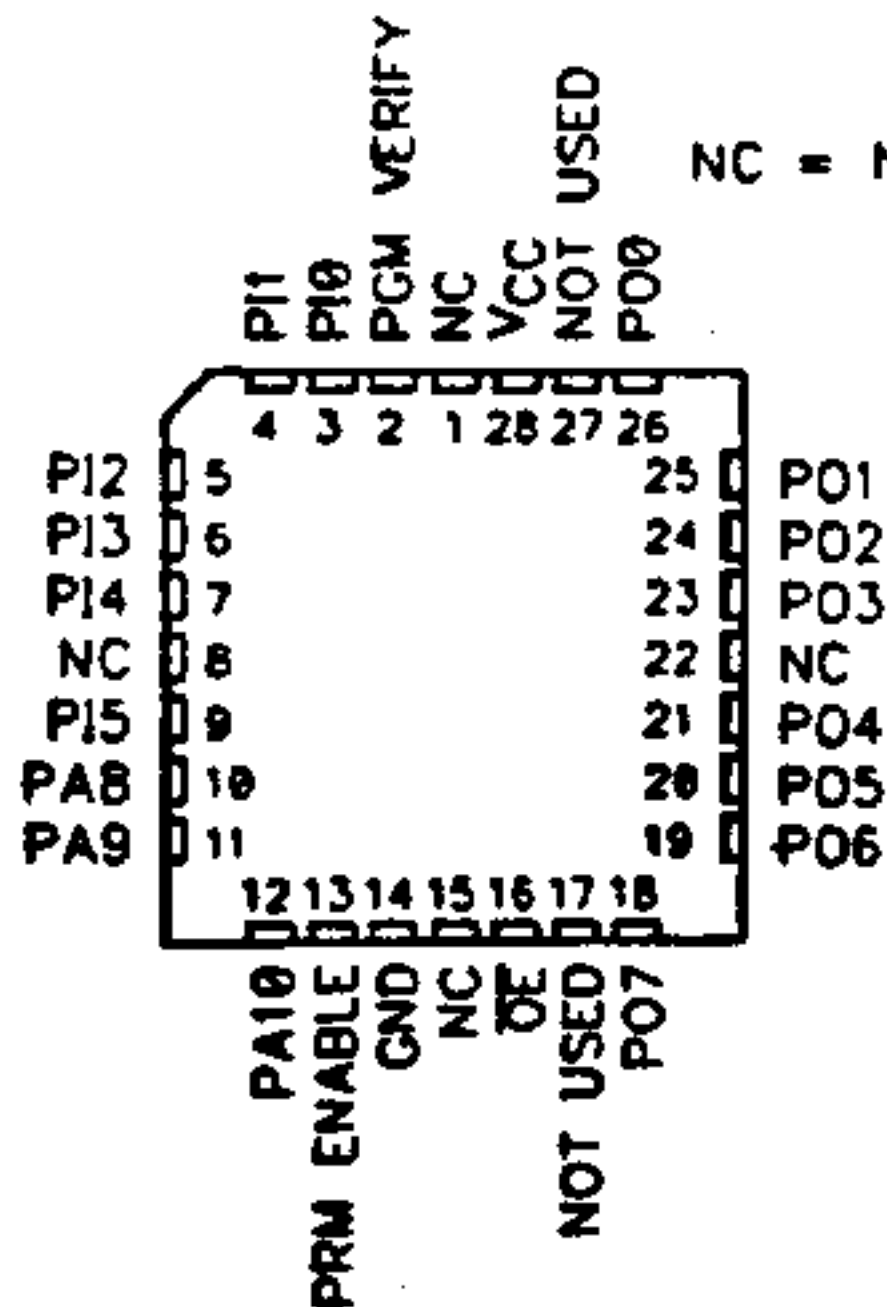
PIN ASSIGNMENTS IN PROGRAMMING MODE

JT OR NT PACKAGE
(TOP VIEW)



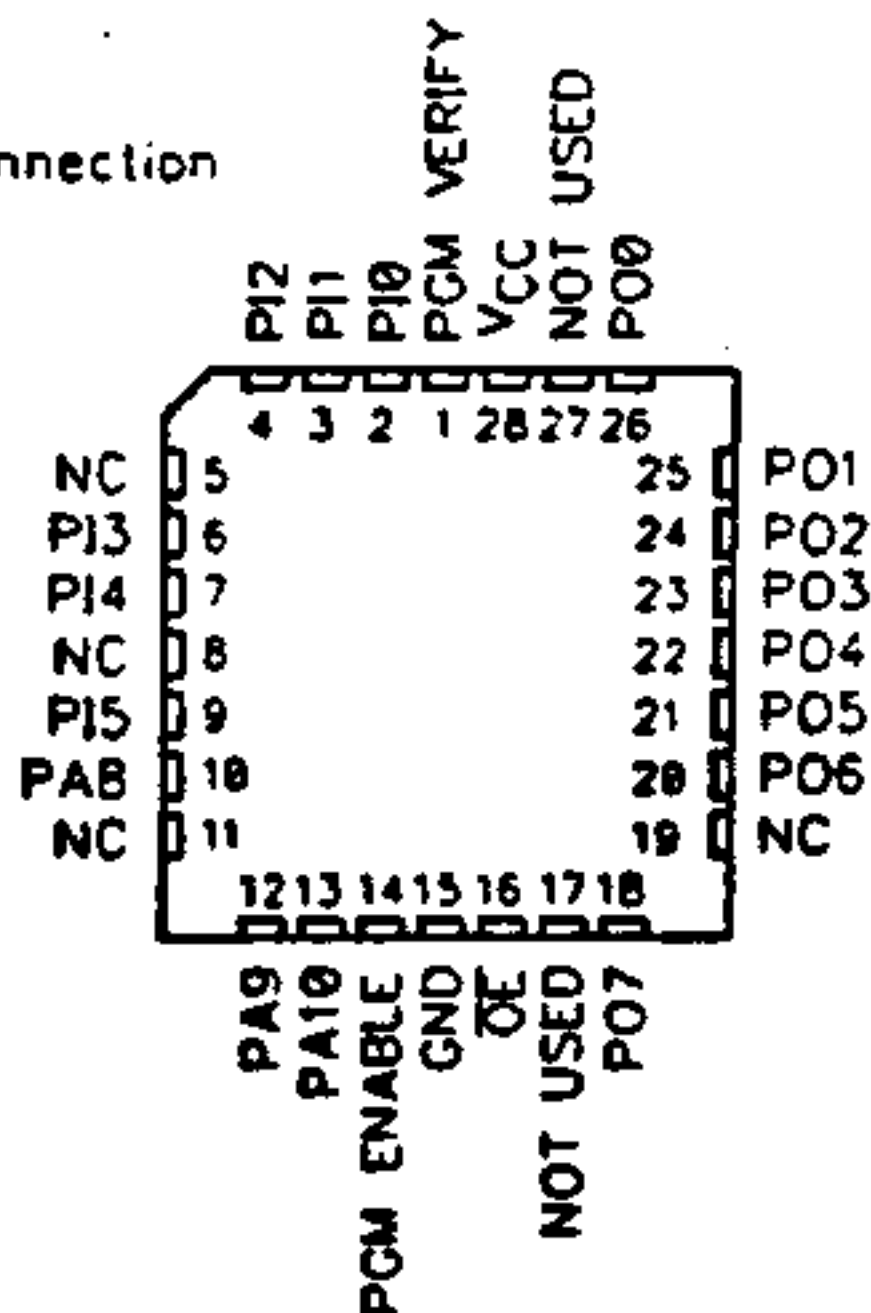
TBPA20XX-15CNT (JEDEC)

FK OR FN PACKAGE
(TOP VIEW)



TBPA20XX-15CFN (JEDEC)

FK OR FN PACKAGE
(TOP VIEW)



TBPA20XX-15CNL (NON-JEDEC)

TABLE 1-1, PROGRAMMING PARAMETERS, $T_A = 25^\circ\text{C}$

PARAM	DESCRIPTION	MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage	5.25	5.50	5.75	V
V_{IH}	High-Level input voltage	2.40		5.50	V
V_{IL}	Low-level input voltage			0.50	V
V_{IHH}	Program-pulse voltage	10.25	10.50	10.75	V
I_{IHH}	Program-pulse PO		20	50	ma
	current PGM ENA, OE		10	25	ma
	PI, PA		10	25	ma
	I_{CC}			500	ma
t_{w1}	Program-pulse duration at PO	10		50	us
t_{su}	Set-up time	100			ns
t_h	Hold time	100			ns
t_{d1}	Delay time from /OE low to to PGM verify 1.	100			ns
t_{d2}	Delay time from PGM verify 1 to valid output.	200			ns
t_{w2}	Pulse duration at PGM verify.	100			ns

TABLE 1-2. INPUT LINE SELECT

INPUT LINE NUMBER	Input Line Number-Address Pin Stoles						Hex
	P10	P11	P12	P13	P14	P15	
00	L	L	L	L	L	L	00
01	L	L	L	L	L	H	01
02	L	L	L	L	H	L	02
03	L	L	L	L	H	H	03
04	L	L	L	H	L	L	04
05	L	L	L	H	L	H	05
06	L	L	L	H	H	L	06
07	L	L	L	H	H	H	07
08	L	L	H	L	L	L	08
09	L	L	H	L	L	H	09
10	L	L	H	L	H	L	0A
11	L	L	H	L	H	H	0B
12	L	L	H	H	L	L	0C
13	L	L	H	H	L	H	0D
14	L	L	H	H	H	L	0E
15	L	L	H	H	H	H	0F
16	L	H	L	L	L	L	10
17	L	H	L	L	L	H	11
18	L	H	L	L	H	L	12
19	L	H	L	L	H	H	13
20	L	H	L	H	L	L	14
21	L	H	L	H	L	H	15
22	L	H	L	H	H	L	16
23	L	H	L	H	H	H	17
24	L	H	H	L	L	L	18
25	L	H	H	L	L	H	19
26	L	H	H	L	H	L	1A
27	L	H	H	L	H	H	1B
28	L	H	H	H	L	L	1C
29	L	H	H	H	L	H	1D
30	L	H	H	H	H	L	1E
31	L	H	H	H	H	H	1F
32	H	L	L	L	L	L	20
33	H	L	L	L	L	H	21
34	H	L	L	L	H	L	22
35	H	L	L	L	H	H	23
36	H	L	L	H	L	L	24
37	H	L	L	H	L	H	25
38	H	L	L	H	H	L	26
39	H	L	L	H	H	H	27
SF	H	H	H	H	H	H	3F

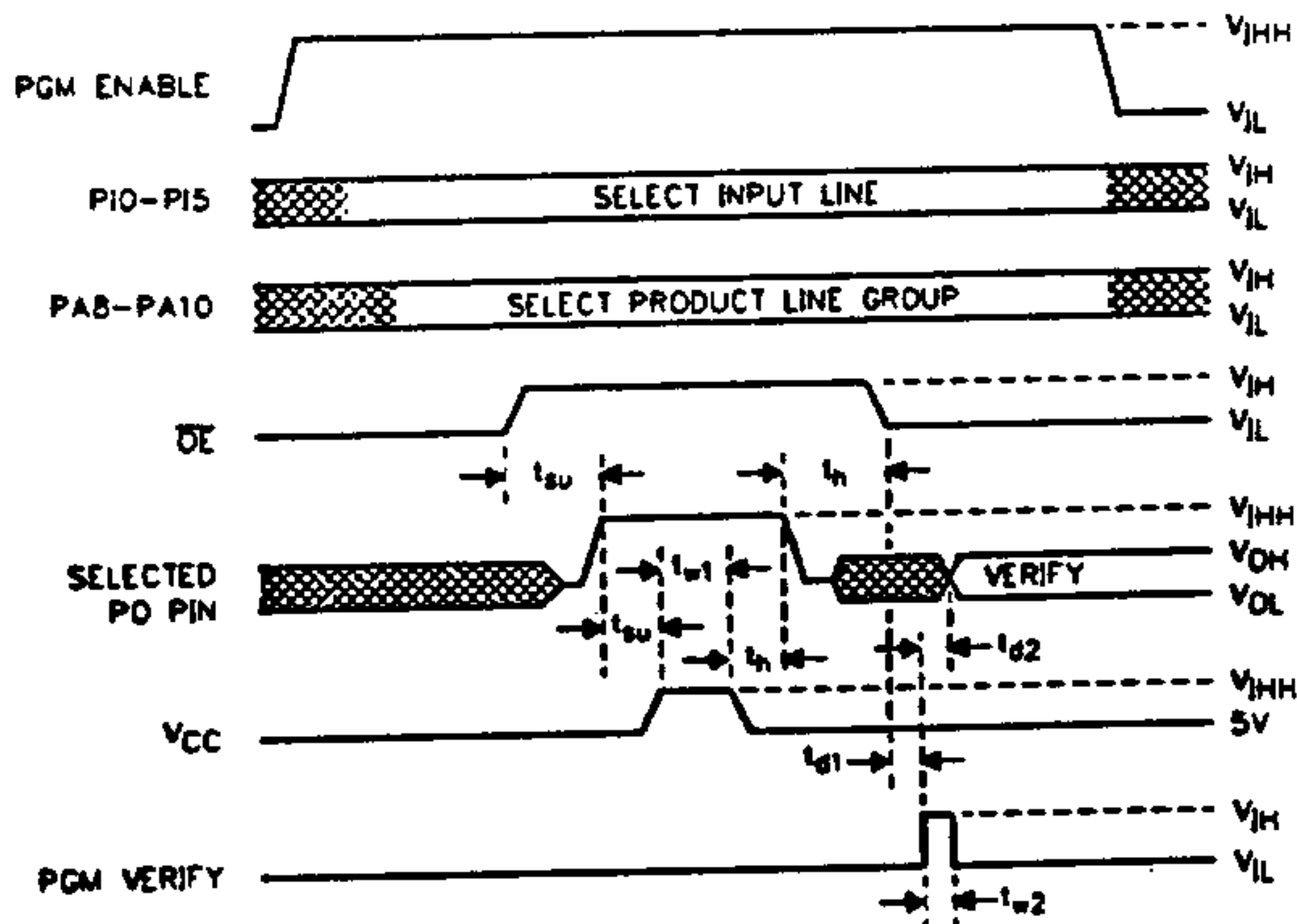
SF = SECURITY FUSE

TABLE 1-3. PRODUCT TERM ADDRESSING

PRODUCT TERMS								PRODUCT TERM ADDRESS PIN STATES		
P00	P01	P02	P03	P04	P05	P06	P07	PAB	PA9	PA10
00	08	16	24	32	40	48	56	L	L	L
01	09	17	25	33	41	49	57	L	L	H
02	10	18	26	34	42	50	58	L	H	L
03	11	19	27	35	43	51	59	L	H	H
04	12	20	28	36	44	52	60	H	L	L
05	13	21	29	37	45	53	61	H	L	H
06	14	22	30	38	46	54	62	H	H	L
07	15	23	31	39	47	55	63	H	H	H
SF-> --	--	--	--	--	--	--	--	X	X	HH <-SF

SF - SECURITY FUSE (DOES NOT REQUIRE VOLTAGE TO THE PO PIN)

FIGURE 1-1. PROGRAMMING WAVEFORMS

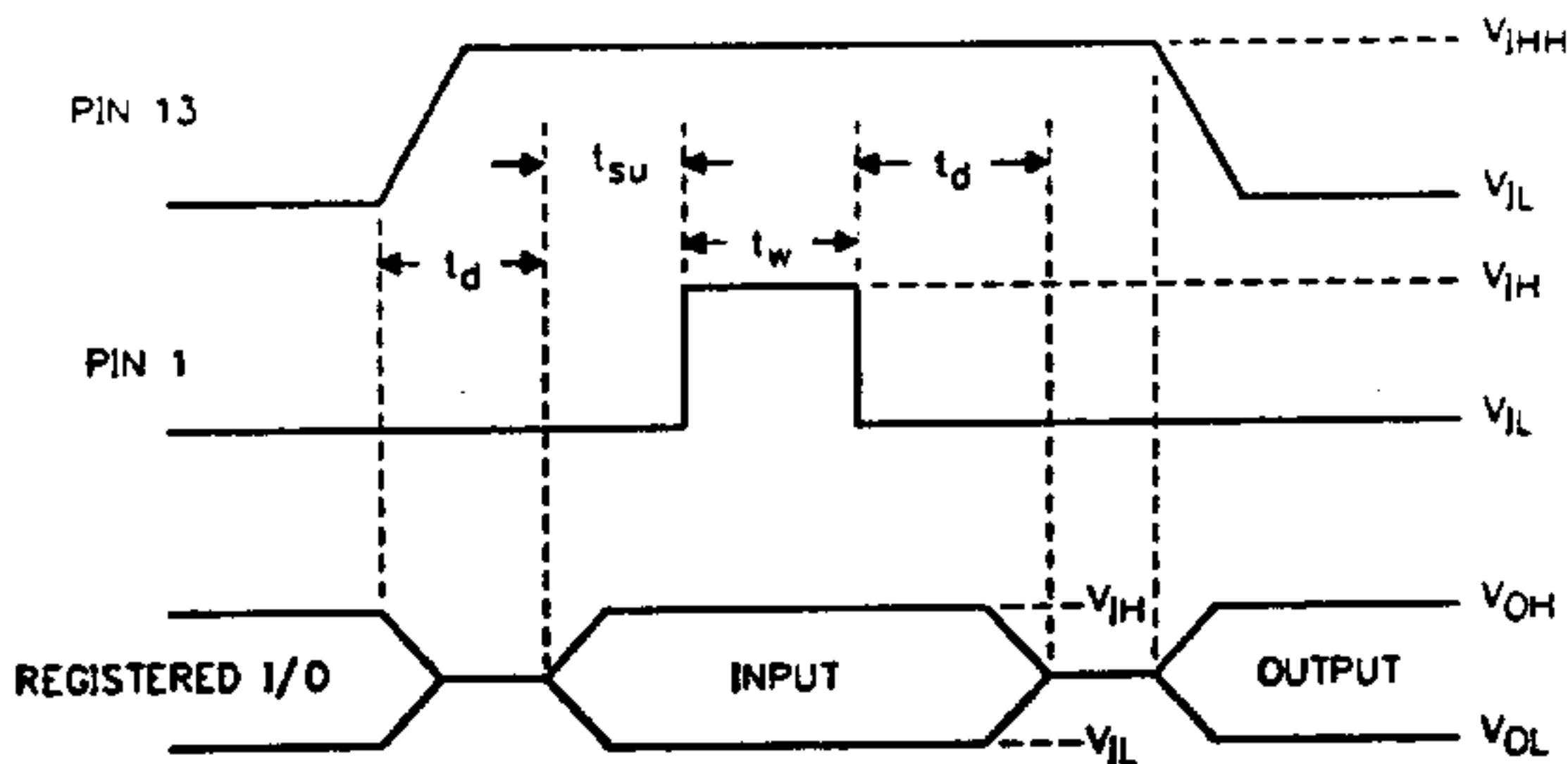


Preload procedure for registered outputs (See Note 2)

The output registers of the TBPAL20XX can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With V_{CC} at 5 volts and pin 1 at V_{IL} , raise pin 13 to V_{IHH} .
- Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
- Step 3. Pulse pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower pin 13 to V_{IL} .
Preload can be verified by observing the voltage level of the output pin.

Preload waveforms (See Notes 2 and 3)



Notes: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

3. $t_d = t_{su} = t_w = 100$ ns to 1000 ns.
 $V_{IHH} = 10.25$ V to 10.75 V.

PROGRAMMING ALGORITHM TEMPLATE

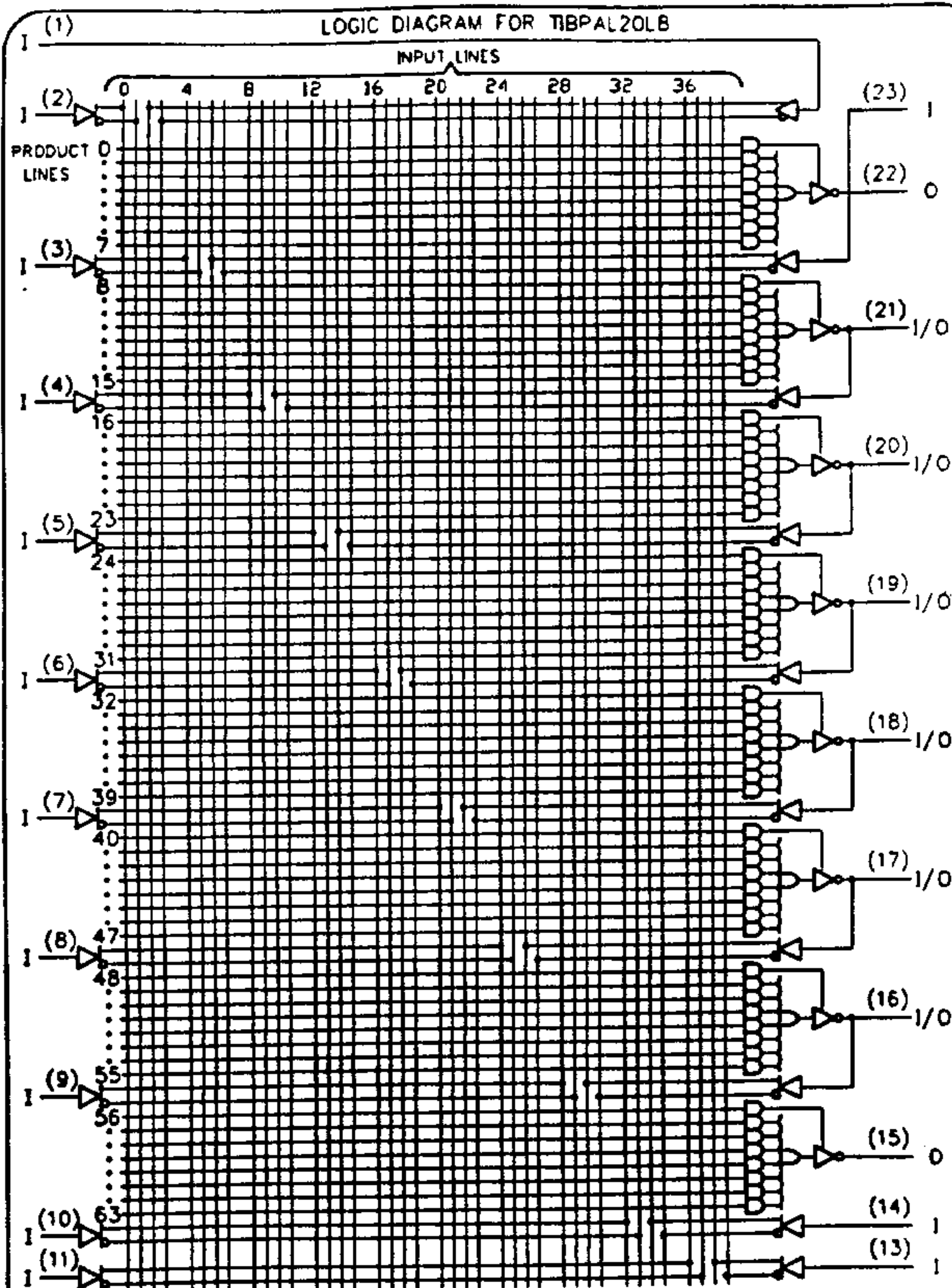
SPECIFICATION NUMBER PAL24003
 DEVICE FAMILY TIBPAL20XX
 INCLUDED DEVICES TIBPAL20L8,R4,R6,R8-15;25

PROGRAMMER INFO:

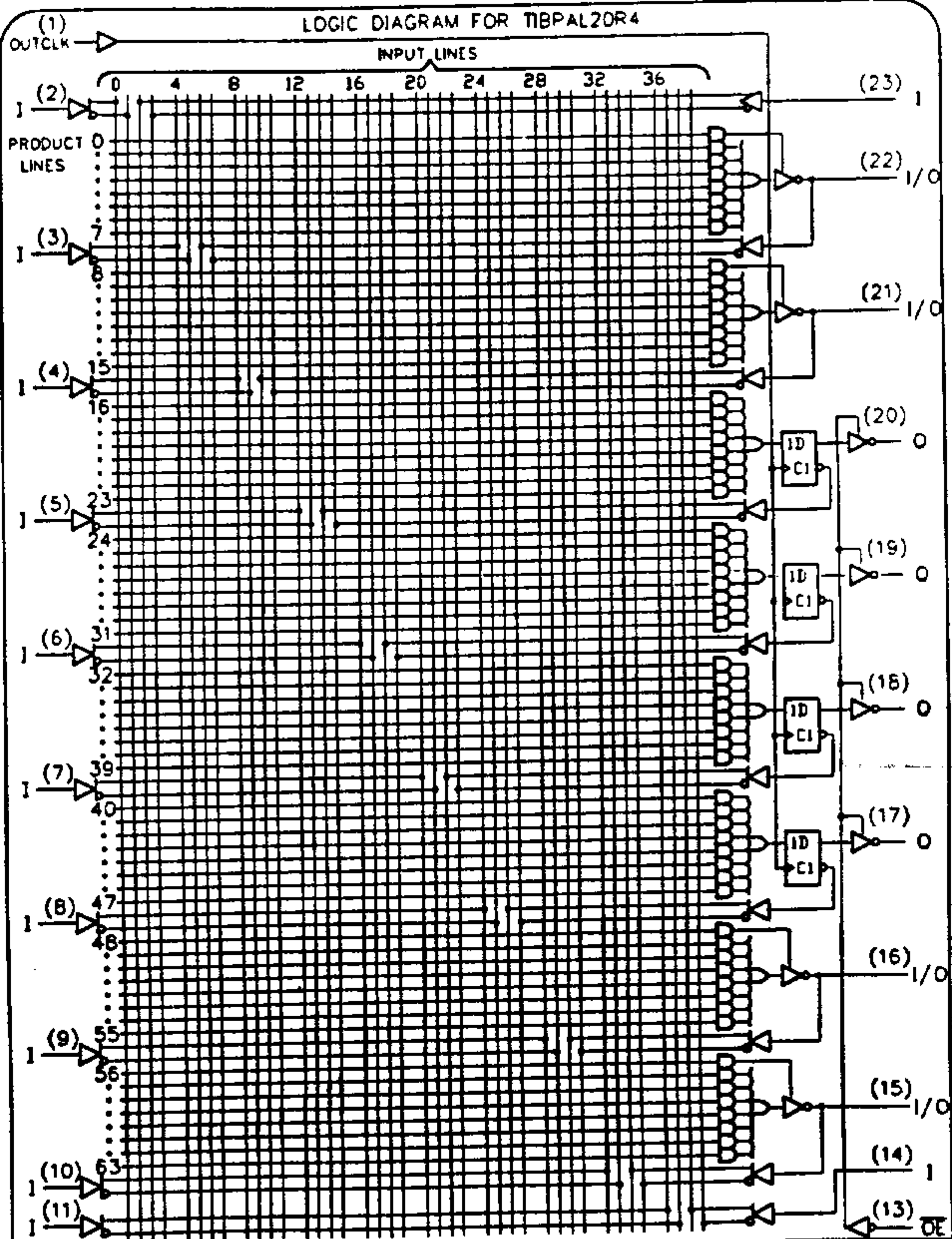
MANUFACTURER : _____ MODEL: _____ ADAPTER #: _____
 UPDATE VERSION : _____ FW/SW P/N: _____

PARAMETER	MIN	NOM	MAX	UNITS	ACTUAL
VCC - VERIFY LEVEL SUPPLY VOLTAGE	5.25	5.5	5.75	V	
VIH - HIGH LEVEL INPUT VOLTAGE	2.4		5.5	V	
VIL - LOW LEVEL INPUT VOLTAGE			0.5	V	
VIHH - PROGRAM-PULSE VOLTAGE (PG/EN)	10.25	10.5	10.75	V	
VIHH - PROGRAM-PULSE VOLTAGE (PO)	10.25	10.5	10.75	V	
VIHH - PROGRAM-PULSE VOLTAGE (VCC)	10.25	10.5	10.75	V	
tw1 - PROGRAM PULSE WIDTH AT VCC	10		50	us	
tw2 - PGM VERIFY PULSE WIDTH	100			ns	
tsu - SET UP TIME (/OE-PO)	100			ns	
tsu - SET UP TIME (PO-VCC)	100			ns	
th - HOLD TIME (/OE-PO)	100			ns	
th - HOLD TIME (PO-VCC)	100			ns	
td1 - DELAY TIME (SEE WAVEFORMS)	100			ns	

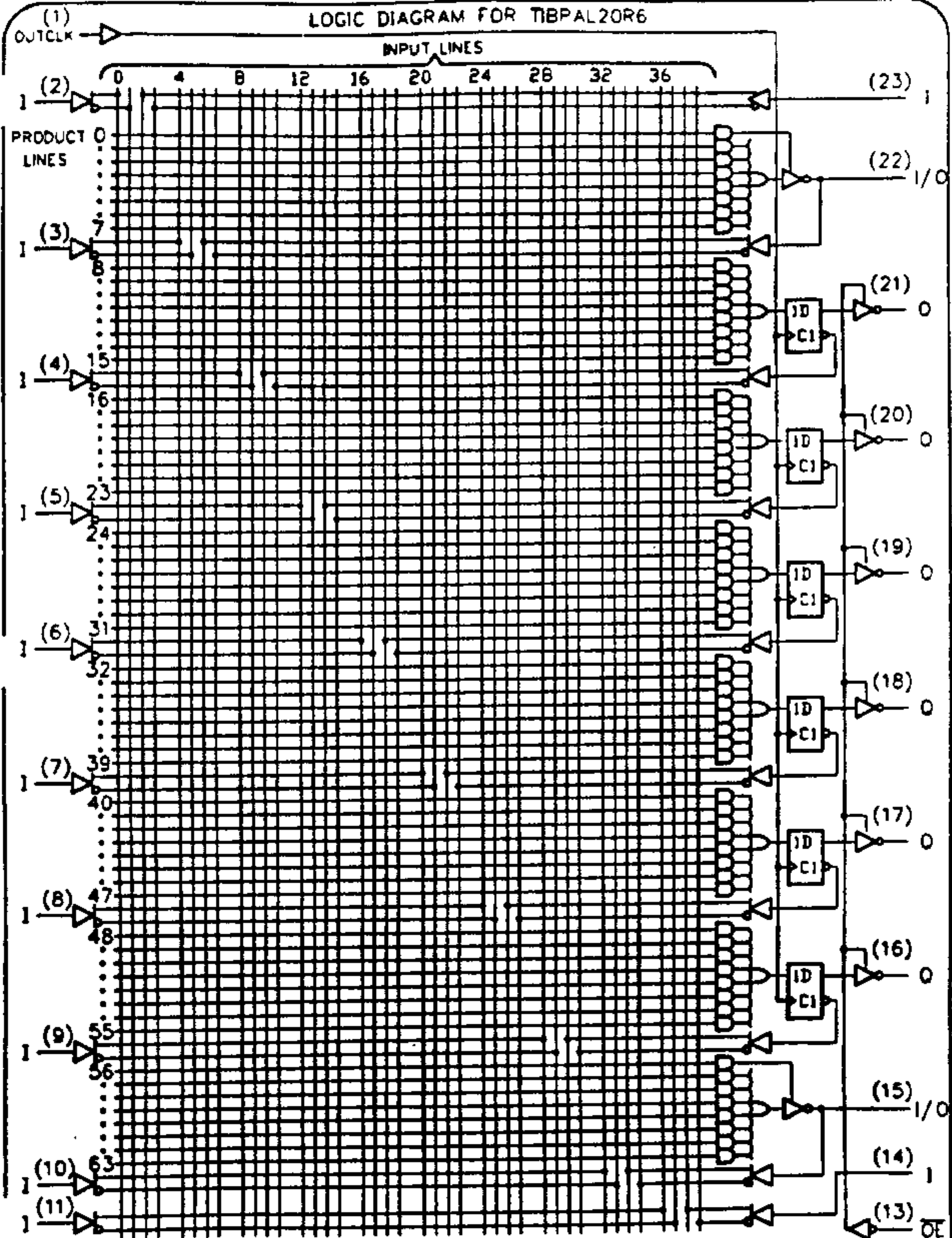
LOGIC DIAGRAM FOR TBPAL20LB



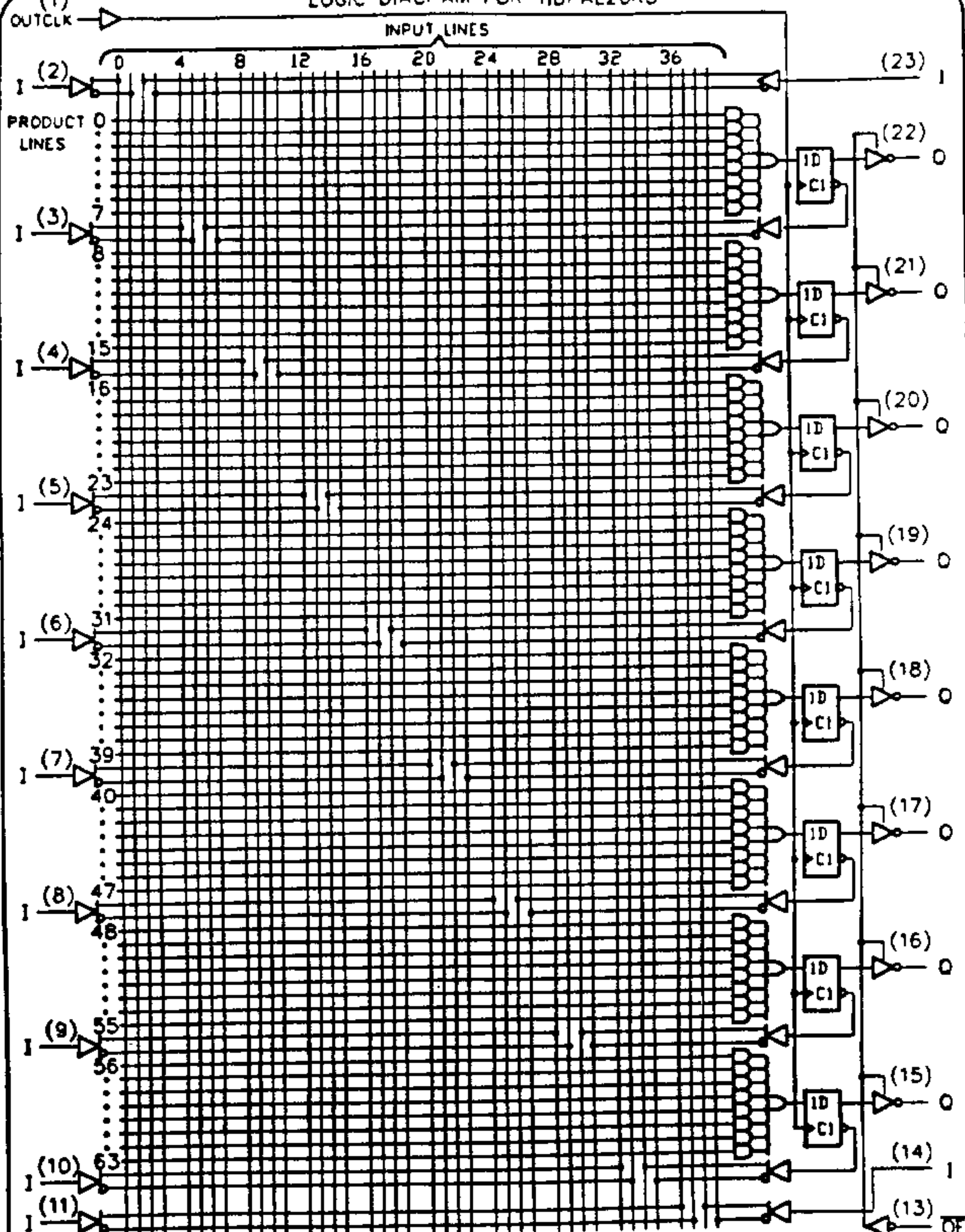
LOGIC DIAGRAM FOR TIBPAL20R4



LOGIC DIAGRAM FOR TBPAL20R6



LOGIC DIAGRAM FOR TIBPAL20R8



REVISION HISTORY

REVISION LTR.	DATE	ENGINEER	DESCRIPTION OF CHANGES
A	01-87	Giddings	Table 1-1, added parameters t_{d1} and t_{w2} . Table 1-2, removed extra input line addresses. Table 1-3, removed extra Product line addresses. Figure 1-1, PGM verify pulse added.
B	06-87	Thomas	Sheet 1 of 9. Changed Security fuse programming procedure
C	09-87	Thomas	Changed V_{CC} to 5.50 V.
D	01-88	Thomas	Combined specifications PAL24003 and PAL2400E
E	02-88	Thomas	Corrected non-Jedec PLCC pin assignments.