

TEXAS INSTRUMENTS  
FIELD PROGRAMMABLE LOGIC DEPARTMENT  
PROGRAMMING ALGORITHM SPECIFICATION

DEVICE FAMILY TIBPAL16XX-7  
DEVICES TIBPAL16R4H-15, TIBPAL16R6H-15, TIBPAL16R8H-15, and  
INCLUDED TIBPAL16L8H-15  
TIBPAL16R4-7, TIBPAL16R6-7, TIBPAL16R8-7, and  
TIBPAL16L8-7

**PROGRAMMING PROCEDURE:**

Array fuses are programmed by executing the following programming sequence. Each fuse can be opened by selecting the appropriate (1 of 32) Input Line and (1 of 8) Product Line. The levels for selecting Input Lines and Product Lines are shown in Tables 1-2 and 1-3

- Step 1: Raise PGM ENABLE to  $V_{IH}$ .
- Step 2: Select an Input Line by applying appropriate levels to PI pins
- Step 3: Select a Product Line group by applying appropriate logic levels to PA pins. The actual product line selected will be determined by the PO pin (described in step 5).
- Step 4: Raise /OE to  $V_{IH}$ .
- Step 5: Raise the selected PO pin to  $V_{IH}$ .
- Step 6: Program the fuse by pulsing  $V_{CC}$  to  $V_{IH}$ .
- Step 7: Remove the output voltage.
- Step 8: Lower /OE to  $V_{IL}$  to enable device.
- Step 9: Pulse PGM VER pin to  $V_{IH}$ .
- Step 10: Verify the blowing of fuse by checking for a  $V_{OL}$  at the selected PO pin.

If the fuse is still intact, steps 1 thru 10 may be repeated until the fuse is successfully blown, not to exceed 4 retries. Do not apply additional pulses to a fuse once it is correctly programmed. Verification is possible only with the Security fuse intact.

Security fuses are provided on each device to discourage the unauthorized copying of fuse patterns. To program the security fuse, follow the steps above omitting steps 2 and 10.

See Tables 1-2 and 1-3 for addressing information.

For programming waveforms, see Figure 1-1.

PREPARED BY B. Cole PAL202-1.DWG		DATE 06/29/88		<b>TEXAS INSTRUMENTS</b>	
CHECKED BY <i>[Signature]</i>		DATE 07/11/88		<b>TITLE:</b> ALGORITHM SPECIFICATION TIBPAL16XX-7	
ENGINEER Jim Morris		DATE 06/29/88			
APPROVED BY <i>[Signature]</i>		DATE 07/13/88		REVISION  <b>A</b>	SHEET 1
RELEASED BY / /		DATE / /		LETTER SIZE	PA-20067 10

# PIN ASSIGNMENTS IN PROGRAMMING MODE

(TOP VIEW)

PGM VERIFY	1	20	VCC
PI2	2	19	PO19
PI3	3	18	PO18
PI4	4	17	PO17
PI5	5	16	PO16
NOT USED	6	15	PO15
PA7	7	14	PO14
PAB	8	13	PO13
PGM ENABLE	9	12	PO12
GND	10	11	/OE

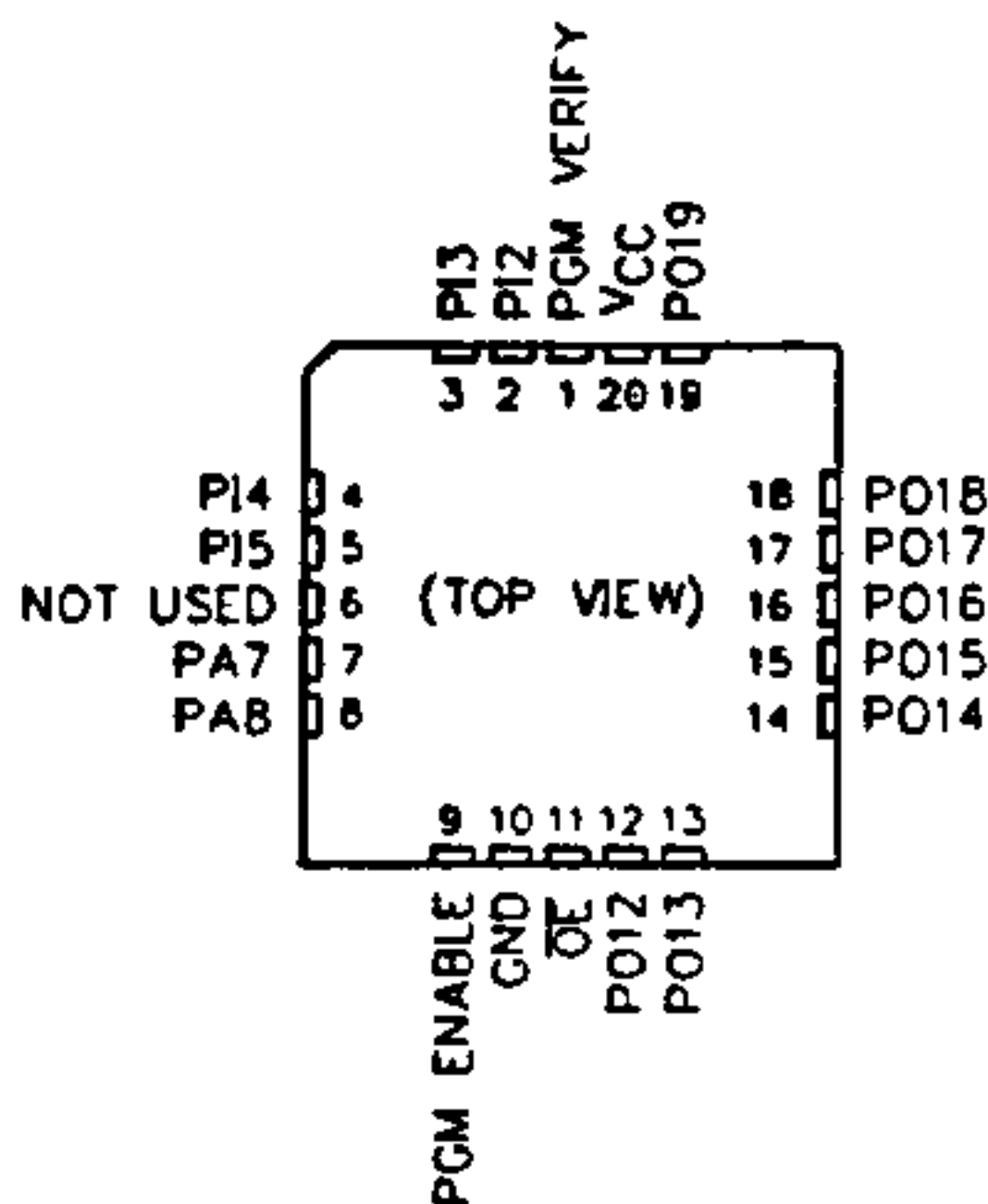


TABLE 1-1, PROGRAMMING PARAMETERS, TA = 25°C

PARAM	DESCRIPTION	MIN	NOM	MAX	UNIT
VCC	Verify-level supply voltage	4.75	5.00	5.25	V
V <sub>IH</sub>	High-Level input voltage	2.40		5.50	V
V <sub>IL</sub>	Low-level input voltage			0.50	V
V <sub>IHH</sub>	Program-pulse PO voltage	10.25	10.50	10.75	V
	PGM ENA	10.25	10.50	10.75	V
	PI, PA	10.25	10.50	10.75	V
	VCC	10.25	10.50	10.75	V
I <sub>IHH</sub>	Program-pulse PO current		20	40	ma
	PGM ENA		5	15	ma
	PI, PA		2	10	ma
	I <sub>CC</sub>			450	ma
t <sub>w1</sub>	Program-pulse duration at PO	10		50	us
t <sub>w2</sub>	Pulse duration at PGM VERIFY	100			us
t <sub>su</sub>	Set-up time	100			ns
t <sub>h</sub>	Hold time	100			ns
t <sub>d1</sub>	Delay time from /OE low to PGM VERIFY high.	100			ns
t <sub>d2</sub>	Delay time from PGM VERIFY high to valid output.	100			us

TABLE 1-2. INPUT LINE SELECT

Input Line Number	Input Line Number-Address Pin States			
	P12	P13	P14	P15
00	L	L	L	L
01	L	L	L	H
02	L	L	L	HH
03	L	L	H	L
04	L	L	H	HH
05	L	L	H	HH
06	L	L	HH	L
07	L	L	HH	H
08	L	L	HH	HH
09	L	H	L	L
10	L	H	L	HH
11	L	H	L	HH
12	L	H	H	L
13	L	H	H	H
14	L	H	H	HH
15	L	H	HH	L
16	L	H	HH	H
17	L	H	HH	HH
18	L	HH	L	L
19	L	HH	L	HH
20	L	HH	L	HH
21	L	HH	H	L
22	L	HH	H	HH
23	L	HH	H	HH
24	L	HH	HH	L
25	L	HH	HH	H
26	L	HH	HH	HH
27	H	L	L	L
28	H	L	L	HH
29	H	L	L	HH
30	H	L	H	L
31	H	L	H	HH
SF1/2	X	X	X	X

TABLE 1-3. PRODUCT TERM ADDRESSING

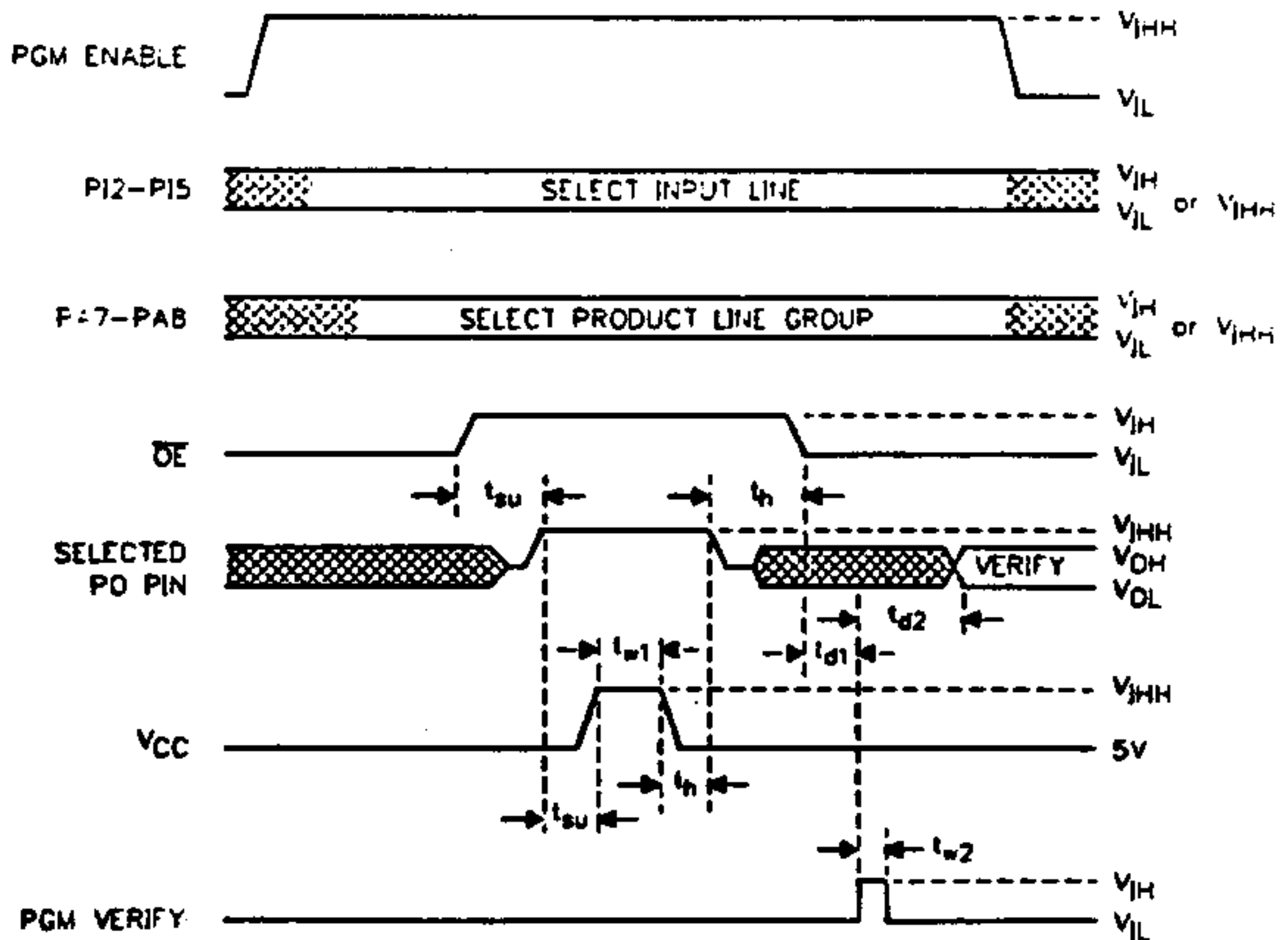
PRODUCT TERM								Address Pin States		
								PAB	PA7	
0	8	16	24	32	40	48	56	L	L	
1	9	17	25	33	41	49	57	H	L	
2	10	18	26	34	42	50	58	HH	L	
3	11	19	27	35	43	51	59	L	H	
4	12	20	28	36	44	52	60	H	H	
5	13	21	29	37	45	53	61	HH	H	
6	14	22	30	38	46	54	62	L	HH	
7	15	23	31	39	47	55	63	H	HH	
--	--	--	--	--	SF2	SF1	--	HH	HH	
PO19	PO18	PO17	PO16	PO15	PO14	PO13	PO12	L = V <sub>IL</sub> , HH = V <sub>IHH</sub> H = V <sub>IH</sub>		
Programing Access and Verify Pin										

SF1 - Security Fuse 1 - When programmed, array verifies as totally programmed

SF2 - Security Fuse 2 - When programmed, array verifies as totally blank.

Note SF1 over-rides SF2.

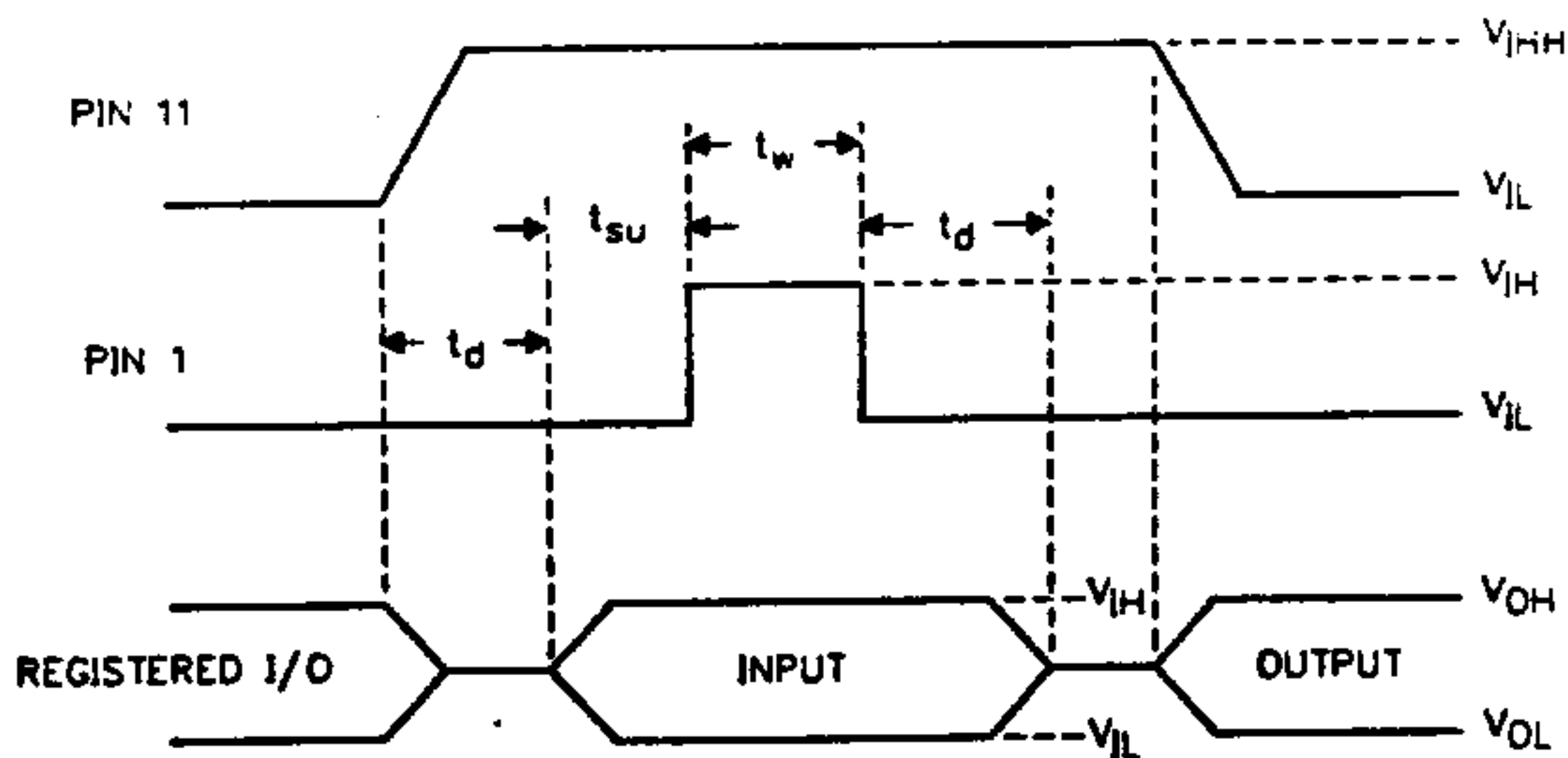
FIGURE 1-1. PROGRAMMING WAVEFORMS



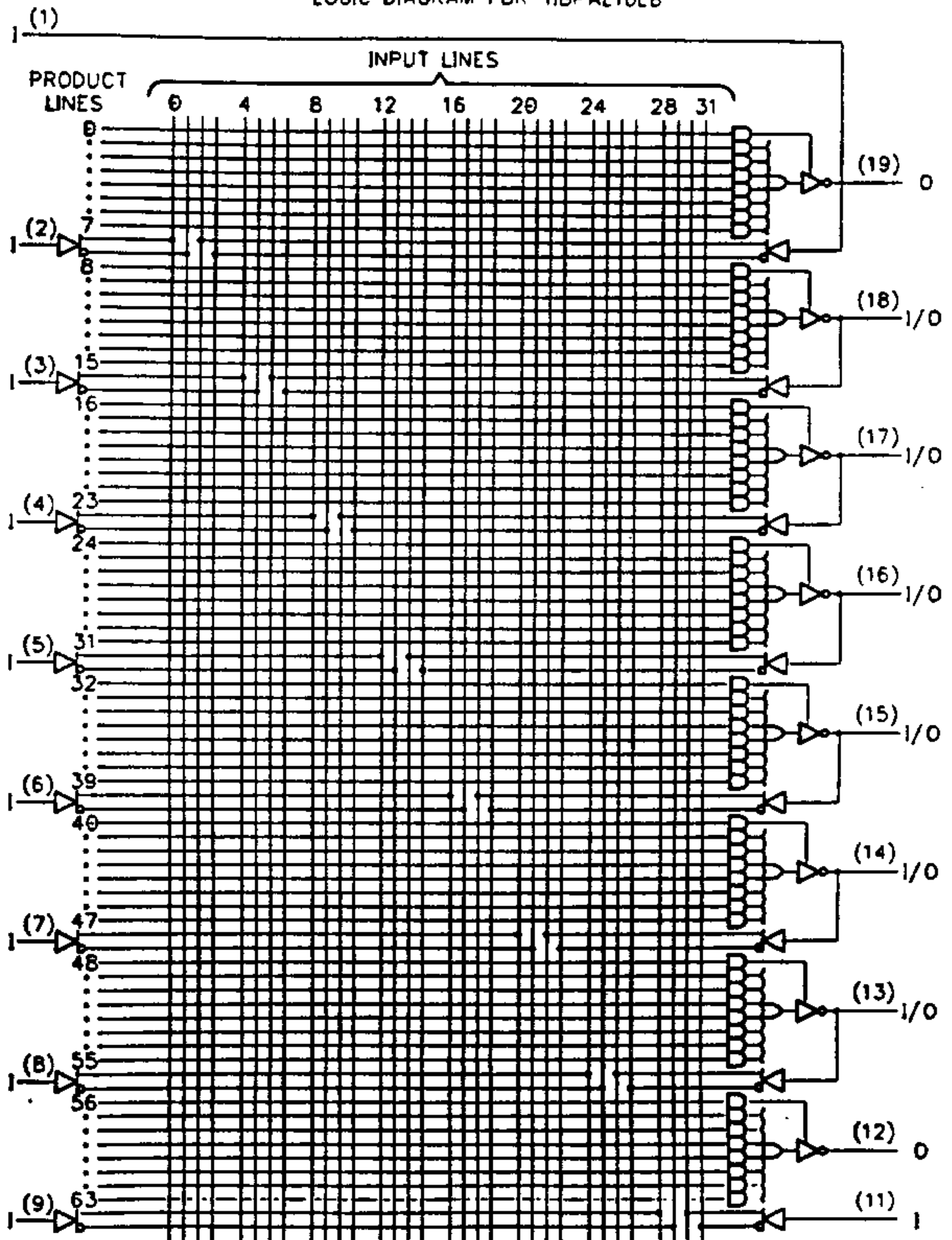
## Preload procedure for registered outputs (See Note 2)

The output registers of the TIBPAL16XX-7 can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

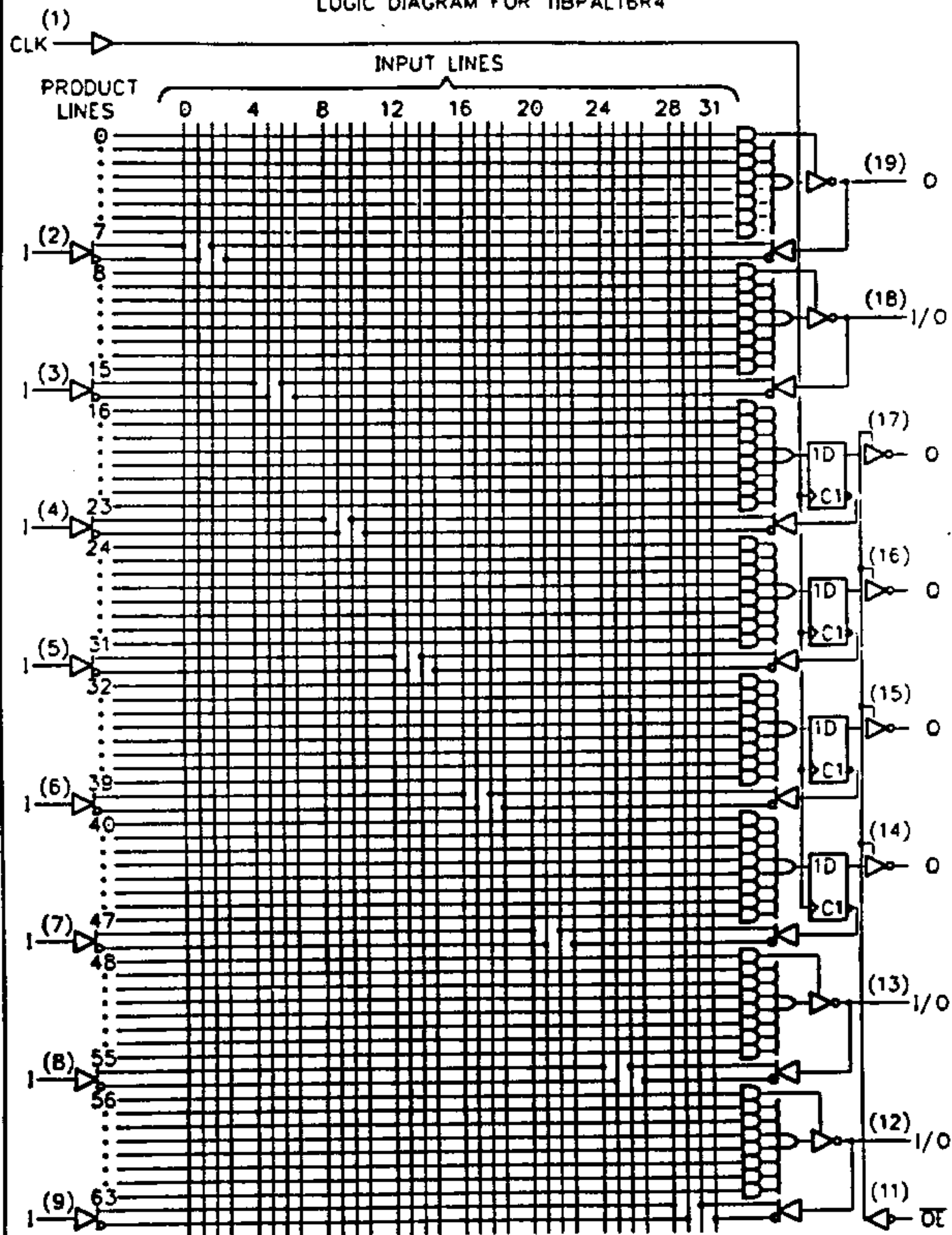
- Step 1: With  $V_{CC}$  at 5 volts and pin 1 at  $V_{IL}$ , raise pin 11 to  $V_{IHH}$ .
- Step 2: Apply either  $V_{IL}$  or  $V_{IH}$  to the output corresponding to the register to be preloaded.
- Step 3: Pulse pin 1, clocking in preload data.
- Step 4: Remove output voltage, then lower pin 11 to  $V_{IL}$ . Preload can be verified by observing the voltage level of the output pin.



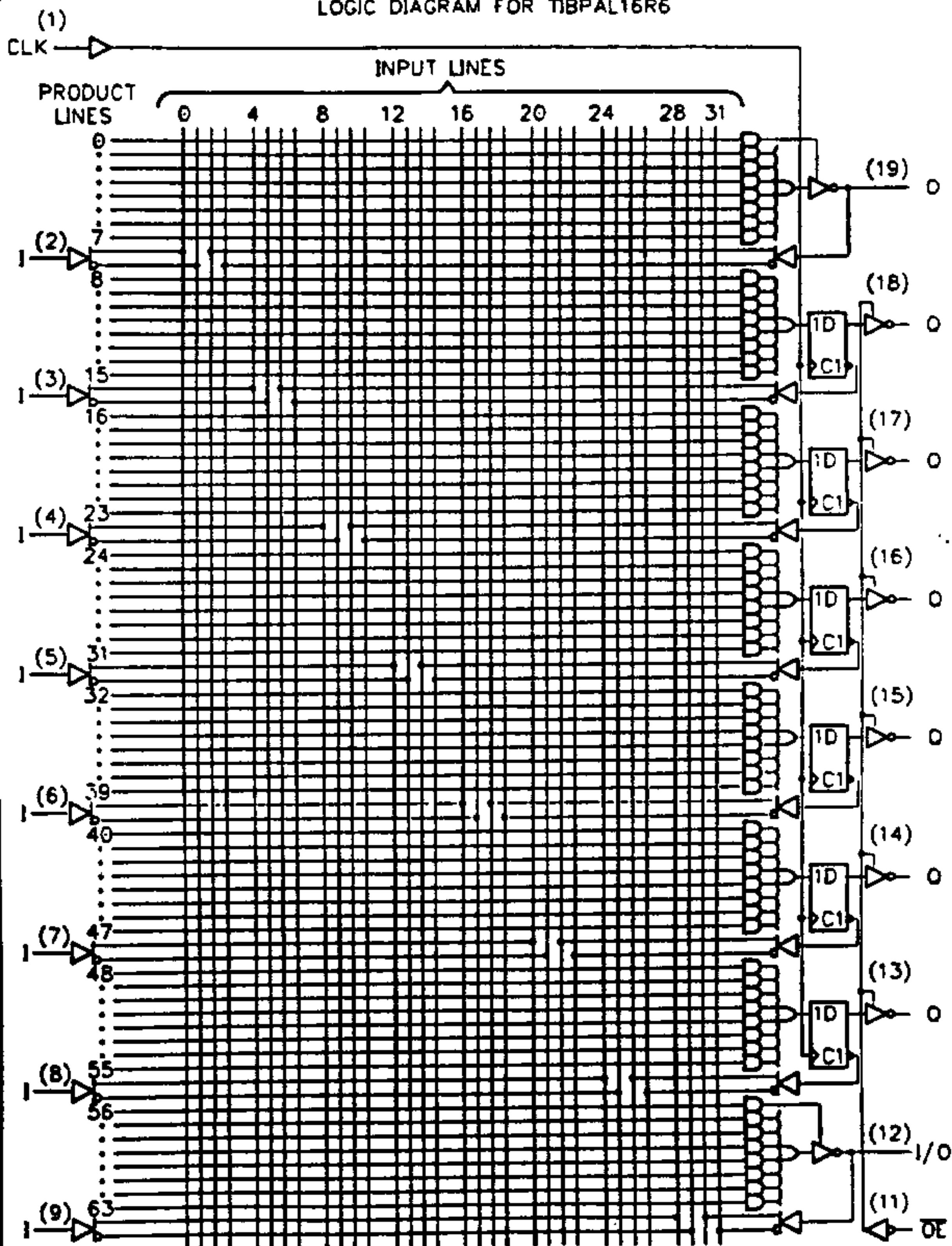
# LOGIC DIAGRAM FOR T1BPAL16LB



# LOGIC DIAGRAM FOR T1BPAL16R4

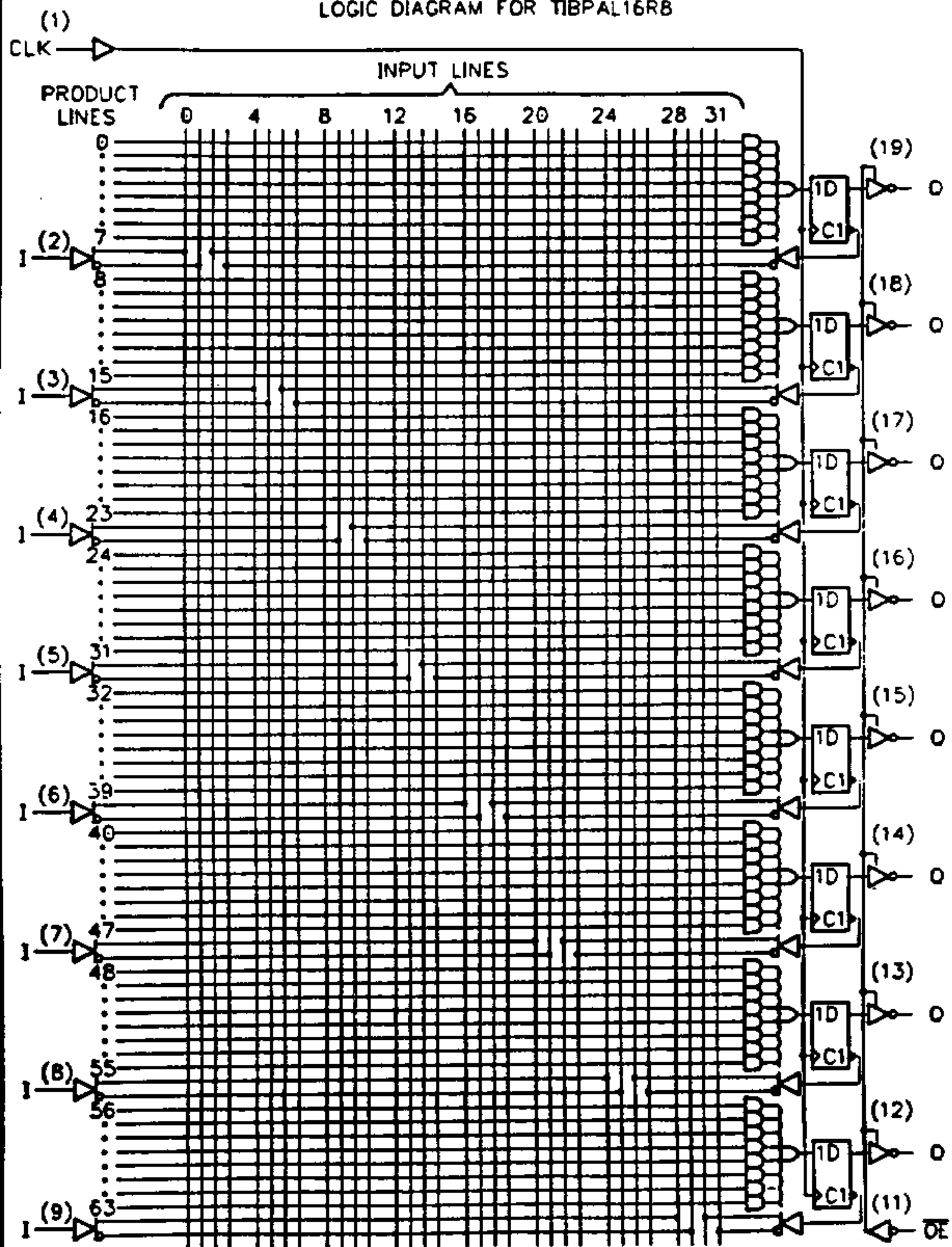


# LOGIC DIAGRAM FOR TIBPAL16R6





# LOGIC DIAGRAM FOR TIBPAL16R8



## REVISION HISTORY

REVISION LTR.	DATE	ENGINEER	DESCRIPTION OF CHANGES
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ALGORITHM SPECIFICATION TIBPAL16XX-7	PAL20Z10.DWG	SH 10 of 10	PAL20007
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