

TEXAS INSTRUMENTS  
FIELD PROGRAMMABLE LOGIC DEPARTMENT  
PROGRAMMING ALGORITHM SPECIFICATION

DEVICE FAMILY    TIBPAL22V10  
DEVICES            TIBPAL22V10, TIBPAL22V10A, TIBPAL22V10-15B  
INCLUDED          TIBPAL22V10-7/-10

**PROGRAMMING PROCEDURE:**

Array fuses are programmed by executing the following programming sequence. The levels for selecting Input Lines and Product Lines are shown in Tables 1-2 and 1-3.

- Step 1: Raise PGM ENABLE to  $V_{IH}$ .
- Step 2: Select an Input Line by applying appropriate levels to PI pins.
- Step 3: Select a Product Line group by applying appropriate logic levels to PA pins. The actual product line selected will be determined by the PO pin (described in step 5).
- Step 4: Raise  $\overline{OE}$  to  $V_{IH}$ .
- Step 5: Raise the selected PO pin to  $V_{IH}$ .
- Step 6: Program the fuse by pulsing  $V_{CC}$  to  $V_{IH}$ .
- Step 7: Remove the output voltage.
- Step 8: Lower  $\overline{OE}$  to  $V_{IL}$  to enable device.
- Step 9: Verify the blowing of fuse by checking for a  $V_{OL}$  on the selected PO pin.

If the fuse is still intact, steps 1 thru 9 may be repeated until the fuse is successfully blown, not to exceed 4 retries. Do not apply additional pulses to a fuse once it is correctly programmed. Verification is possible only with the Security fuse intact.

A single security fuse is provided on each device to discourage the unauthorized copying of fuse patterns. To program the security fuse, follow the steps above omitting steps 2 and 9. Verification is achieved by verifying the entire fuse array. If the security fuse is blown, all other fuses will appear to be blown.

For Input and Product Line selection, see Tables 1-2 and 1-3.

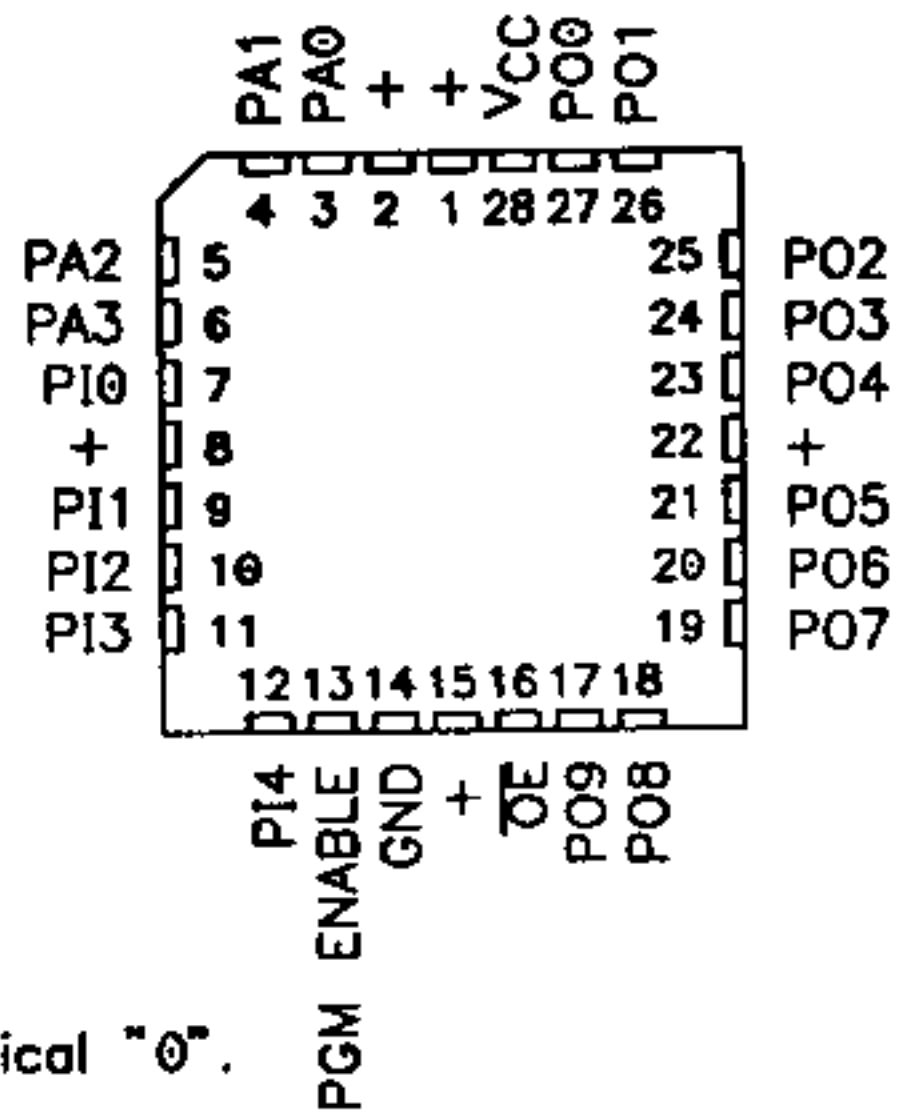
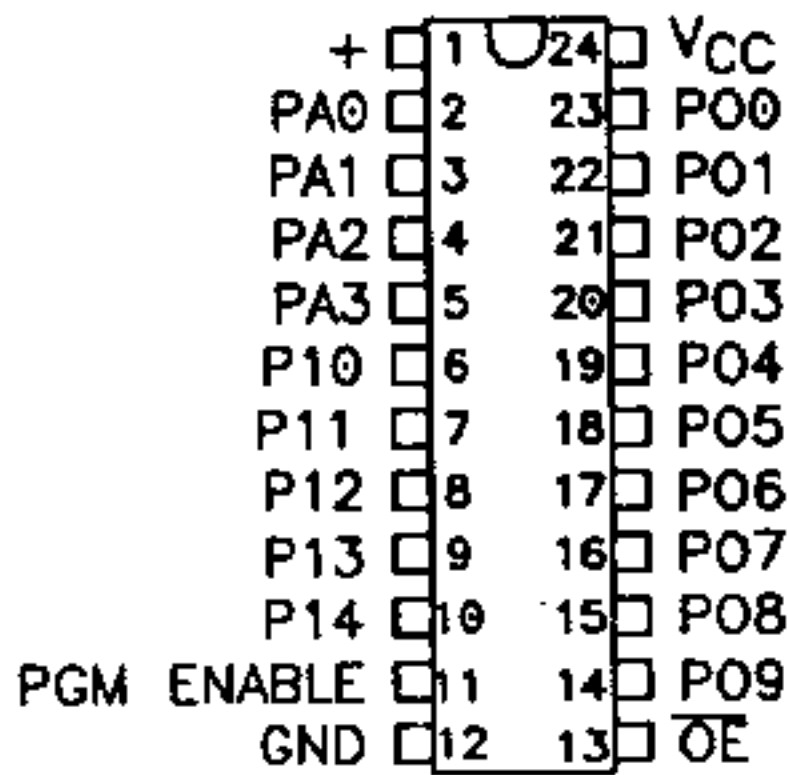
For programming waveforms, see Figure 1-1.

PREPARED BY B. Cole PAL22-1.DWG		DATE 10/02/86		<b>TEXAS INSTRUMENTS</b>		
CHECKED BY		DATE 1 / 1		<b>TITLE</b> ALGORITHM SPECIFICATION TIBPAL22V10		
ENGINEER <i>Charles B. Bentley</i>		DATE 8/25/92		PAL24001		
APPROVED BY <i>[Signature]</i>		DATE 9/15/92				
RELEASED BY <i>Bud Minner</i>		DATE 10/01/92				
REVISION F LETTER				<b>A</b> SIZE	SHEET 1 7	

## PIN ASSIGNMENTS IN PROGRAMMING MODE

(TOP VIEW)

(TOP VIEW)



**+ =** Set to ground or logical "0".

TABLE 1-1. PROGRAMMING PARAMETERS,  $T_A = 25^\circ\text{C}$

PARAM	DESCRIPTION	MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Verify—level supply voltage	4.75	5.00	5.25	V
V <sub>IH</sub>	High—Level input voltage	2.40		5.50	V
V <sub>IL</sub>	Low—level input voltage			0.50	V
V <sub>IHH</sub>	Program—pulse voltage	10.25	10.50	10.75	V
I <sub>IHH</sub>	Program—pulse PO		20	50	ma
	current PGM ENA, OE		10	25	ma
	PI, PA		10	25	ma
	I <sub>CC</sub>			500	ma
t <sub>w1</sub>	Program—pulse duration at V <sub>CC</sub>	10		50	us
t <sub>su</sub>	Set—up time	100			ns
t <sub>h</sub>	Hold time	100			ns
t <sub>d2</sub>	Delay time from /OE low to to valid output.	100			ns

TABLE 1-2, INPUT LINE SELECT

Input Line Number	Input Line Number-Address Pin States					Hex
	PI4	PI3	PI2	PI1	PI0	
00	L	L	L	L	L	00
01	L	L	L	L	H	01
02	L	L	L	H	L	02
03	L	L	L	H	H	03
04	L	L	H	L	L	04
05	L	L	H	L	H	05
06	L	L	H	H	L	06
07	L	L	H	H	H	07
08	L	H	L	L	L	08
09	L	H	L	L	H	09
10	L	H	L	H	L	0A
11	L	H	L	H	H	0B
12	L	H	H	L	L	0C
13	L	H	H	L	H	0D
14	L	H	H	H	L	0E
15	L	H	H	H	H	0F
16	H	L	L	L	L	10
17	H	L	L	L	H	11
18	H	L	L	H	L	12
19	H	L	L	H	H	13
20	H	L	H	L	L	14
21	H	L	H	L	H	15
22	H	L	H	H	L	16
23	H	L	H	H	H	17
24	H	H	L	L	L	18
25	H	H	L	L	H	19
26	H	H	L	H	L	1A
27	H	H	L	H	H	1B
28	H	H	H	L	L	1C
29	H	H	H	L	H	1D
30	H	H	H	H	L	1E
31	H	H	H	H	H	1F
32	HH	L	L	L	L	20
33	HH	L	L	L	H	21
34	HH	L	L	H	L	22
35	HH	L	L	H	H	23
36	HH	L	H	L	L	24
37	HH	L	H	L	H	25
38	HH	L	H	H	L	26
39	HH	L	H	H	H	27
40	HH	H	L	L	L	28
41	HH	H	L	L	H	29
42	HH	H	L	H	L	2A
43	HH	H	L	H	H	2B
#1 44	HH	H	H	L	L	2C
#2 45	HH	H	H	L	H	2D

#1=Output Polarity, #2=Register/Non-Register Output

TABLE 1-3, PRODUCT TERM ADDRESSING

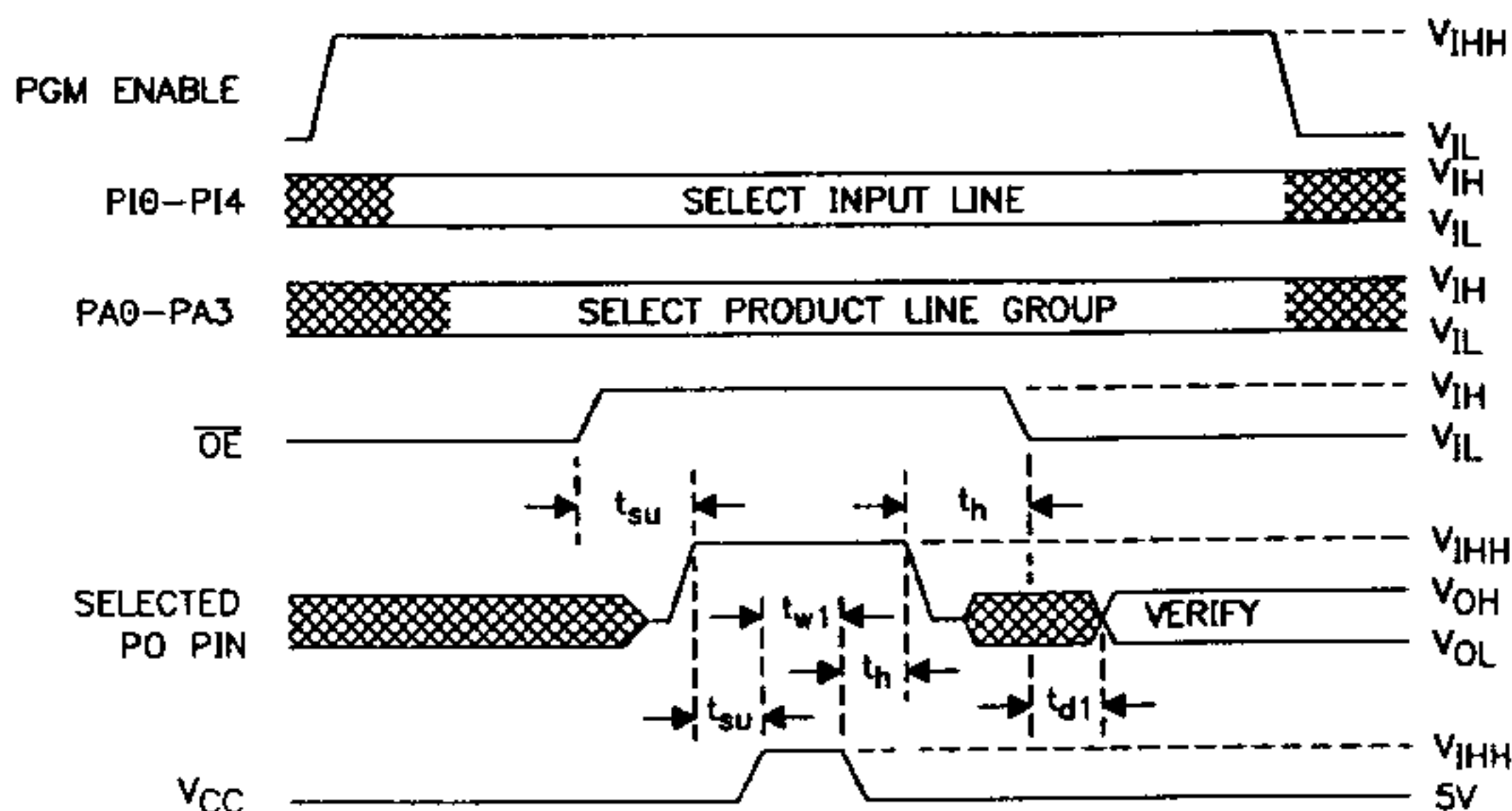
PRODUCT TERM										Product Term Select Address Pin States			
										PA3	PA2	PA1	PA0
0	0	0	0	0	0	0	0	0	0	L	L	L	L
1	1	1	1	1	1	1	1	1	1	L	L	L	H
2	2	2	2	2	2	2	2	2	2	L	L	H	L
3	3	3	3	3	3	3	3	3	3	L	L	H	H
4	4	4	4	4	4	4	4	4	4	L	H	L	L
5	5	5	5	5	5	5	5	5	5	L	H	L	H
6	6	6	6	6	6	6	6	6	6	L	H	H	L
7	7	7	7	7	7	7	7	7	7	L	H	H	H
--	8	8	8	8	8	8	8	8	--	H	L	L	L
--	9	9	9	9	9	9	9	9	--	H	L	L	H
--	--	10	10	10	10	10	10	--	--	H	L	H	L
--	--	11	11	11	11	11	11	--	--	H	L	H	H
--	--	--	12	12	12	12	--	--	--	H	H	L	L
--	--	--	13	13	13	13	--	--	--	H	H	L	H
--	--	--	--	14	14	--	--	--	--	H	H	H	L
--	--	--	--	15	15	--	--	--	--	H	H	H	H
OE	OE	OE	OE	OE	OE	OE	OE	OE	OE	HH	L	L	L
AP	AP	AP	AP	AP	AP	AP	AP	AP	AP	HH	L	L	L
--	AR*	--	--	--	--	--	--	SP**	--	HH	H	L	L
--	SF	--	--	--	--	--	--	--	--	HH	H	L	H
P00	P01	P02	P03	P04	P05	P06	P07	P08	P09	L = $V_{IL}$ , HH = $V_{IHH}$ H = $V_{IH}$			
Programming Access and Verify Pin													

**Logical PTs**

- #1 - Output Enable, #2 - Architecture Product  
 #3 - \*Asynchronous Reset, \*\* Synchronous Preset  
 #4 - Security Fuse ( Special verify required )

Note 1: Unused output, denoted by a --, are indeterminant and should be ignored during any verification operation.

FIGURE 1-1, PROGRAMMING WAVEFORMS

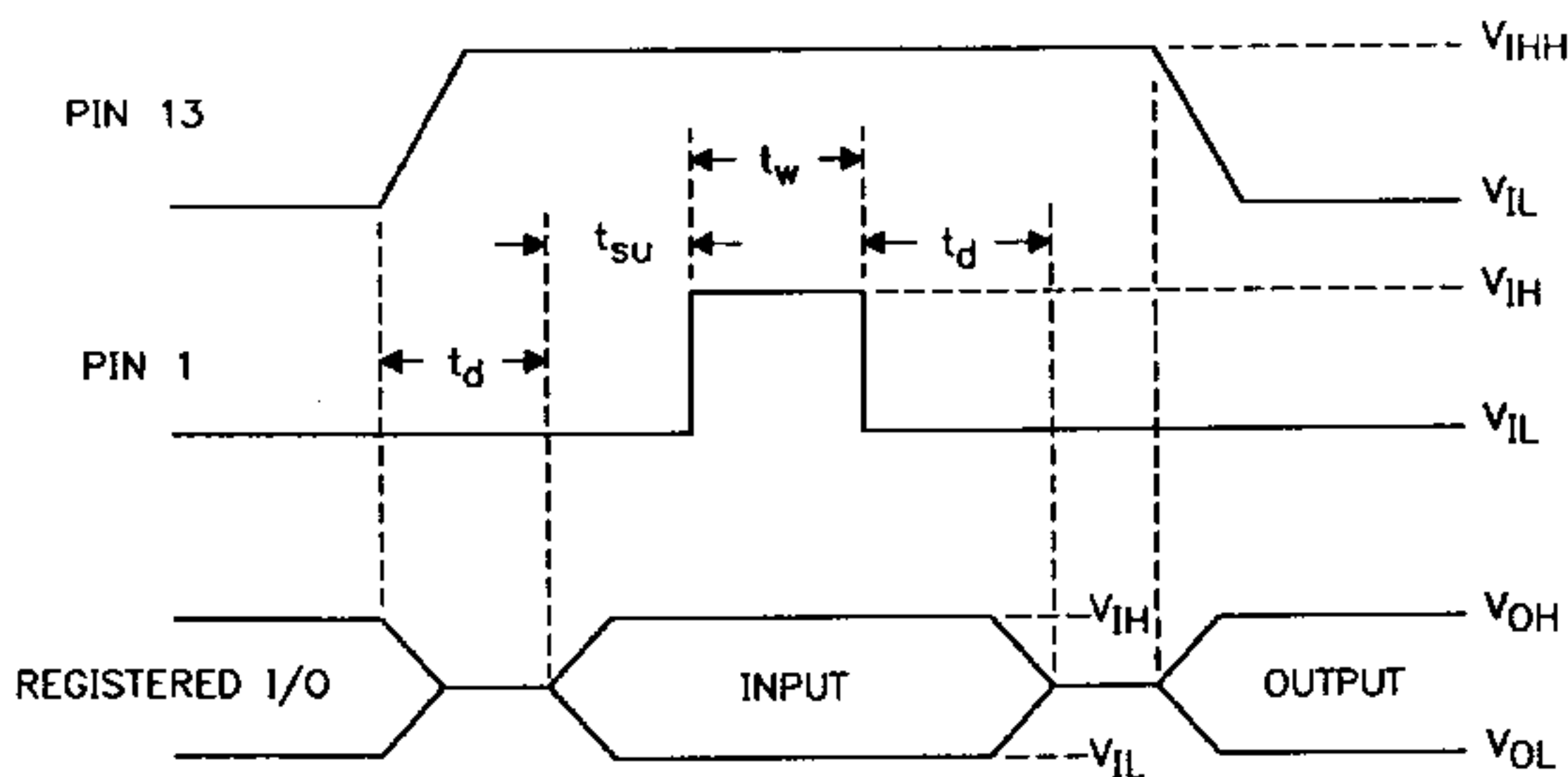


## Preload procedure for registered outputs (See Note 2)

The output registers of the TIBPAL22V10 can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1: With  $V_{CC}$  at 5 volts and pin 1 at  $V_{IL}$ , raise pin 13 to  $V_{IHH}$ .
- Step 2: Apply either  $V_{IL}$  or  $V_{IH}$  to the output corresponding to the register to be preloaded.
- Step 3: Pulse pin 1, clocking in preload data.
- Step 4: Remove output voltage, then lower pin 13 to  $V_{IL}$ .  
Preload can be verified by observing the voltage level at the output pin.

## Preload waveforms (See Notes 2 and 3)



Notes: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

3.  $t_d = t_{su} = t_w = 100$  ns to 1000 ns.  
 $V_{IHH} = 10.25$  V to 10.75 V.

# PROGRAMMING ALGORITHM TEMPLATE

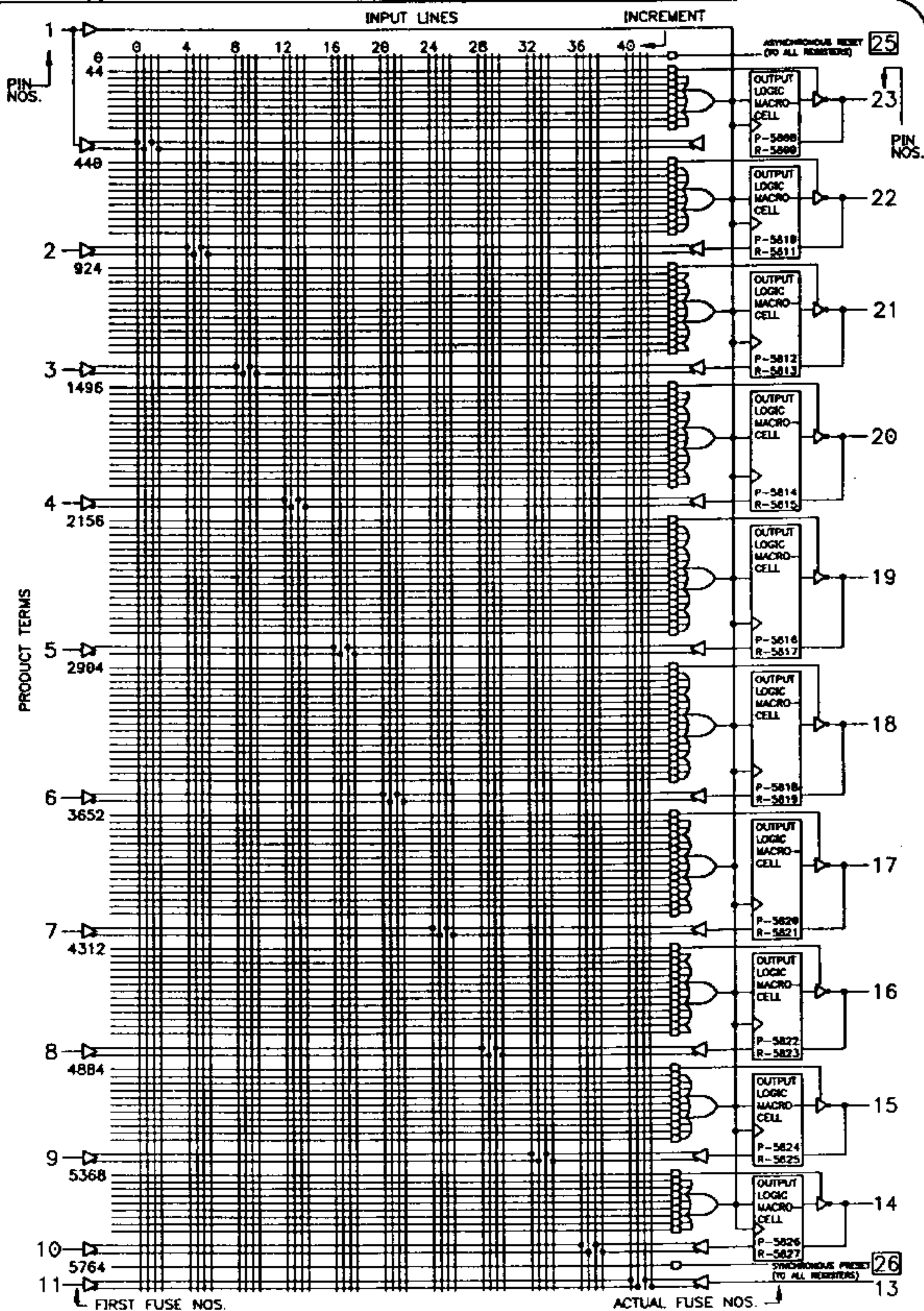
SPECIFICATION NUMBER PAL24001  
 DEVICE FAMILY TIBPAL22V10  
 INCLUDED DEVICES TIBPAL22V10, TIBPAL22V10A

## PROGRAMMER INFO:

MANUFACTURER : \_\_\_\_\_ MODEL: \_\_\_\_\_ ADAPTER #: \_\_\_\_\_  
 UPDATE VERSION : \_\_\_\_\_ FW/SW P/N: \_\_\_\_\_

PARAMETER	MIN	NOM	MAX	UNITS	ACTUAL
VCC - VERIFY LEVEL SUPPLY VOLTAGE	4.75	5	5.25	V	
VIH - HIGH LEVEL INPUT VOLTAGE	2.4		5.5	V	
VIL - LOW LEVEL INPUT VOLTAGE			0.5	V	
VIHH - PROGRAM-PULSE VOLTAGE (PGM/EN)	10.25	10.5	10.75	V	
VIHH - PROGRAM-PULSE VOLTAGE (PI,PA)	10.25	10.5	10.75	V	
VIHH - PROGRAM-PULSE VOLTAGE (PO)	10.25	10.5	10.75	V	
VIHH - PROGRAM-PULSE VOLTAGE (VCC)	10.25	10.5	10.75	V	
t <sub>w1</sub> - PROGRAM PULSE WIDTH AT VCC	10		50	us	
t <sub>su</sub> - SET UP TIME (/OE-PO)	100			ns	
t <sub>su</sub> - SET UP TIME (PO-VCC)	100			ns	
t <sub>h</sub> - HOLD TIME (/OE-PO)	100			ns	
t <sub>h</sub> - HOLD TIME (PO-VCC)	100			ns	

NOTE: Inside each Macrocell, the 'P' fuse No. is the polarity fuse, and the 'R' fuse No. is the register fuse.



# REVISION HISTORY

REVISION LTR.	DATE	ENGINEER	DESCRIPTION OF CHANGES
A	01-87	Ramey	Table 1-2, Removed Input Line 46 which only applies to TIBPAL22VP10.
B	03-88	Thomas	Added PLCC Pinout
C	12-88	Thomas	Sh. 1. Added TIBPAL22V10-15
D	02-90	Thomas	Sh. 1. Changed the TIBPAL22V10-15 to TIBPAL22V10-15B. Sh. 2. Changed the pins marked <u>NOT USED</u> to GND.
E	10-90	Lippens	Sh. 2. Changed $t_{w1}$ from: PO to: VCC
F	11-91	Lippens	Sh. 1. Added TIBPAL22V10-7/-10 Deleted 2nd sentence under PROGRAMMING PROCEDURE. Sh. 2. Chg. pin 2 from GND to +. Sh. 4. Added Note 1: Unused outputs, denoted on a --, are indeterminant and should be ignored during any verification operation.