

TEXAS INSTRUMENTS
FIELD PROGRAMMABLE LOGIC DEPARTMENT
PROGRAMMING ALGORITHM SPECIFICATION

DEVICE FAMILY PAL16XXA and PAL16XXA-2
DEVICES PAL16L8A, PAL16R4A, PAL16R6A, PAL16R8A
INCLUDED PAL16L8A-2, PAL16R4A-2, PAL16R6A-2, PAL16R8A-2

PROGRAMMING PROCEDURE:

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (1 of 32) Input Line and then pulsing the correct (1 of 64) Product Line. The levels for selecting Input Lines and Product Lines are shown in Table 1-2.

- Step 1: Raise PGM ENABLE to V_{IHH} .
- Step 2: Select an Input Line by applying appropriate levels to L/R and PI pins. Apply V_{IL} or V_{IH} to selected PI pin (See Table 1-2).
- Step 3: Select Product Line by applying appropriate levels to PA pins (See Table 1-2).
- Step 4: Raise V_{CC} to V_{IHH} .
- Step 5: Blow the fuse by pulsing the appropriate PO pin to V_{IHH} .
- Step 6: Return V_{CC} to 5 volts and pulse PGM VERIFY. The PO pin will exhibit a low output if the fuse is blown.

Four fuse locations can be verified simultaneously, however, fuses should be addressed and blown sequentially.

If the fuse is still intact, steps 4 thru 6 may be repeated until the fuse is successfully blown, not to exceed 4 retries. Do not apply additional pulses to a fuse once it is correctly programmed.

For Input and Product Line selection see Table 1-2.

For programming waveforms see Figure 1-1.

For Security Fuse programming see Figure 1-2.

PREPARED BY B. Cole PAL16-1.DWG		TEXAS INSTRUMENTS	
CHECKED BY <i>Donald B. Thomas</i>		TITLE: ALGORITHM SPECIFICATION	
ENGINEER Jim Giddings		PAL16XXA and PAL16XXA-2	
APPROVED BY <i>Donald B. Thomas</i>		REVISION B	A
RELEASED BY 		LETTER 	PAL20001
DATE 09/08/86		DATE 04/12/88	
DATE 09/08/85		DATE 04/29/88	
DATE / /		SHEET 1 / 10	

PIN ASSIGNMENTS IN PROGRAMMING MODE

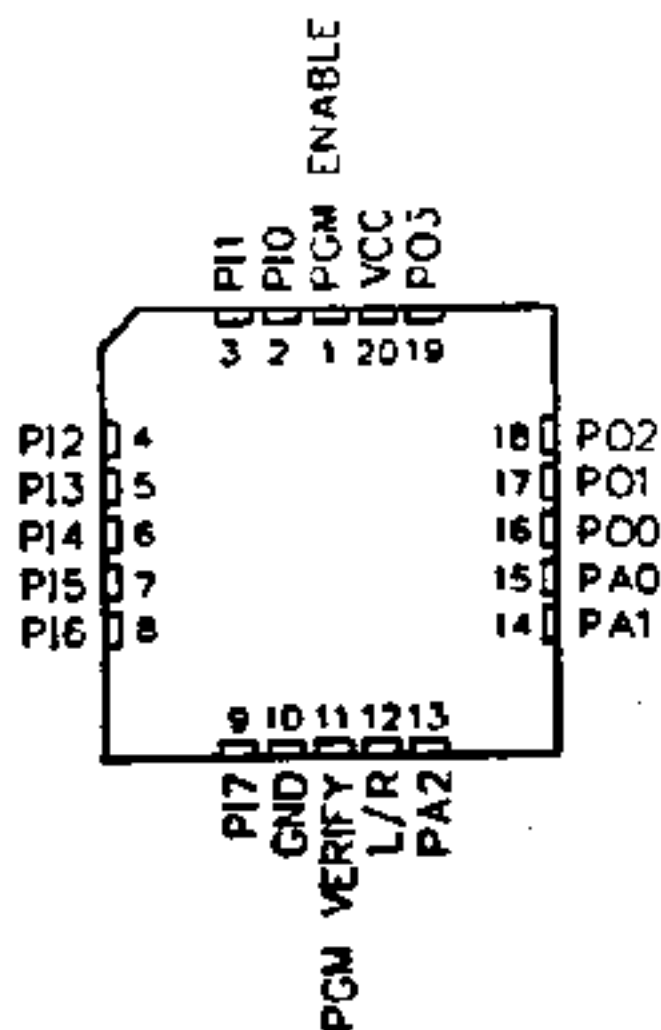
PRODUCT TERMS 0 THRU 31 (TOP VIEW)

PGM ENABLE	1	20	VCC
P10	2	19	P03
P11	3	18	P02
P12	4	17	P01
P13	5	16	P00
P14	6	15	PA0
P15	7	14	PA1
P16	8	13	PA2
P17	9	12	L/R
GND	10	11	PGM VERIFY

PRODUCT TERMS 32 THRU 63 (TOP VIEW)

PGM VERIFY	1	20	VCC
P10	2	19	L/R
P11	3	18	PA0
P12	4	17	PA1
P13	5	16	PA2
P14	6	15	P03
P15	7	14	P02
P16	8	13	P01
P17	9	12	P00
GND	10	11	PGM ENABLE

(TOP VIEW)



(TOP VIEW)

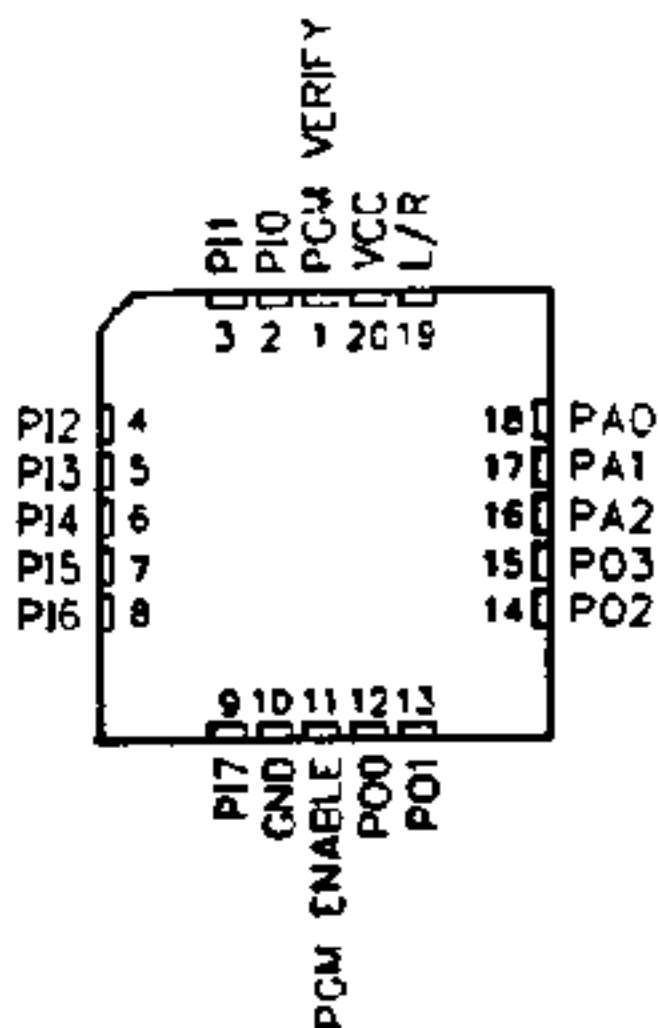


TABLE 1-1. PROGRAMMING PARAMETERS. TA = 25°C

PARAM	DESCRIPTION	MIN	NOM	MAX	UNIT
V _{CC}	Verify-level supply voltage	4.75	5.00	5.25	V
V _{IH}	High-level input voltage	2.40		5.50	V
V _{IL}	Low-level input voltage			0.50	V
V _{IHH}	Program-pulse voltage	10.25	10.50	10.75	V
I _{IHH}	Program-pulse PO		20	50	mA
	current PGM ENA, L/R		10	25	mA
	PI, PA		1.5	5	mA
	I _{CC}		250	400	mA
t _{w1}	Program-pulse duration at PO	10		50	μS
	Prog-pulse duty cycle, PO, V _{CC}			25	%
t _{w2}	Pulse duration at PGM VERIFY	100			nS
t _{su}	Set-up time	100			nS
t _h	Hold time	100			nS
t _{d1}	Delay time from V _{CC} to 5V to PGM VERIFY	100			μS
t _{d2}	Delay time from PGM VERIFY pulse to valid output	200			nS
	Voltage of pins 1 and 11 to open verify-protect (security) fuse	20	21	22	V
	current to open security fuse			400	mA
t _{w3}	Security fuse pulse duration	20		50	μS
	V _{CC} during security fusing		0	0.40	V

TABLE 1-2. INPUT/PRODUCT LINE SELECT

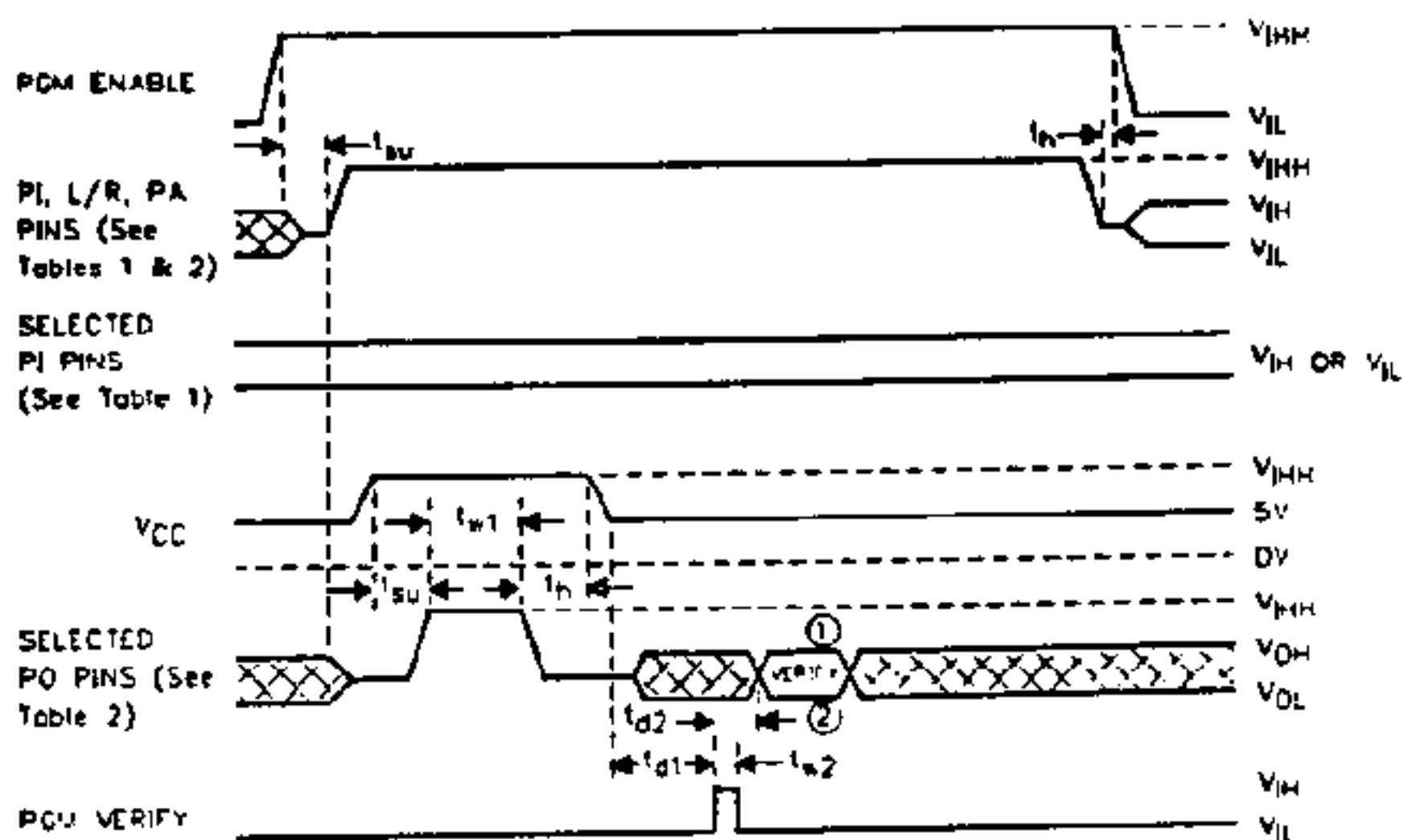
TABLE 1 - INPUT LINE SELECT

TABLE 2 - PRODUCT LINE SELECT

INPUT LINE NO.	PIN NAME									PRODUCT LINE NO.	PIN NAME						
	P17	P16	P15	P14	P13	P12	P11	P10	L/R		P00	P01	P02	P03	PA2	PA1	PA0
0	HH	HH	HH	HH	HH	HH	HH	L	Z	0,32	Z	Z	Z	HH	Z	Z	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z	1,33	Z	Z	Z	HH	Z	Z	HH
2	HH	HH	HH	HH	HH	HH	HH	L	HH	2,34	Z	Z	Z	HH	Z	HH	Z
3	HH	HH	HH	HH	HH	HH	HH	H	HH	3,35	Z	Z	Z	HH	Z	HH	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z	4,36	Z	Z	Z	HH	HH	Z	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z	5,37	Z	Z	Z	HH	HH	Z	HH
6	HH	HH	HH	HH	HH	HH	L	HH	HH	6,38	Z	Z	Z	HH	HH	HH	Z
7	HH	HH	HH	HH	HH	HH	H	HH	HH	7,39	Z	Z	Z	HH	HH	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z	8,40	Z	Z	HH	Z	Z	Z	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z	9,41	Z	Z	HH	Z	Z	Z	HH
10	HH	HH	HH	HH	HH	L	HH	HH	HH	10,42	Z	Z	HH	Z	Z	HH	Z
11	HH	HH	HH	HH	HH	H	HH	HH	HH	11,43	Z	Z	HH	Z	Z	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z	12,44	Z	Z	HH	Z	HH	Z	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z	13,45	Z	Z	HH	Z	HH	Z	HH
14	HH	HH	HH	HH	L	HH	HH	HH	HH	14,46	Z	Z	HH	Z	HH	HH	Z
15	HH	HH	HH	HH	H	HH	HH	HH	HH	15,47	Z	Z	HH	Z	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z	16,48	Z	HH	Z	Z	Z	Z	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z	17,49	Z	HH	Z	Z	Z	Z	HH
18	HH	HH	HH	L	HH	HH	HH	HH	HH	18,50	Z	HH	Z	Z	Z	HH	Z
19	HH	HH	HH	H	HH	HH	HH	HH	HH	19,51	Z	HH	Z	Z	Z	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z	20,52	Z	HH	Z	Z	HH	Z	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z	21,53	Z	HH	Z	Z	HH	Z	HH
22	HH	HH	L	HH	HH	HH	HH	HH	HH	22,54	Z	HH	Z	Z	HH	HH	Z
23	HH	HH	H	HH	HH	HH	HH	HH	HH	23,55	Z	HH	Z	Z	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z	24,56	HH	Z	Z	Z	Z	Z	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z	25,57	HH	Z	Z	Z	Z	Z	HH
26	HH	L	HH	HH	HH	HH	HH	HH	HH	26,58	HH	Z	Z	Z	Z	HH	Z
27	HH	H	HH	HH	HH	HH	HH	HH	HH	27,59	HH	Z	Z	Z	Z	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z	28,60	HH	Z	Z	Z	HH	Z	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z	29,61	HH	Z	Z	Z	HH	Z	HH
30	L	HH	HH	HH	HH	HH	HH	HH	HH	30,62	HH	Z	Z	Z	HH	HH	Z
31	H	HH	HH	HH	HH	HH	HH	HH	HH	31,63	HH	Z	Z	Z	HH	HH	HH

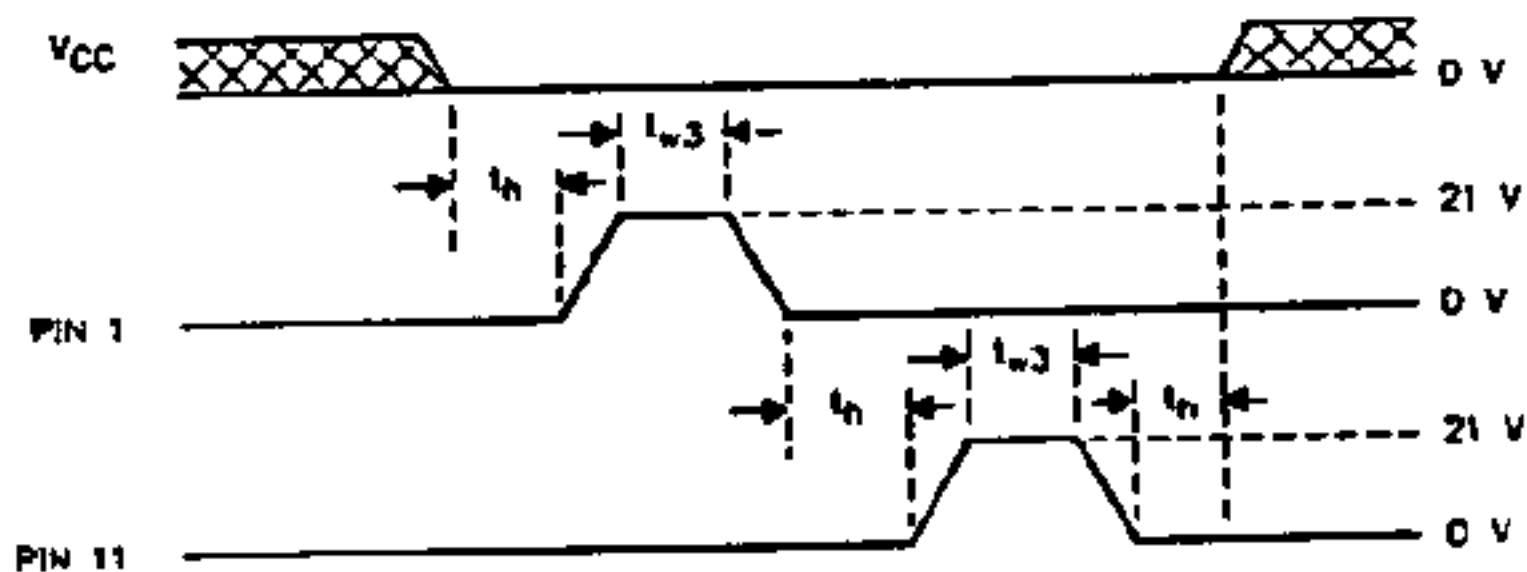
L = VL, H = VH, HH = VHH, Z = high impedance (e.g. 10 k Ω to 5 V)

FIGURE 1-1. PROGRAMMING WAVEFORMS



- ① A high level during the verify interval indicates that programming has not been successful
 ② a low level during the verify interval indicates that programming has been successful

FIGURE 1-2. SECURITY FUSE WAVEFORMS



PROGRAMMING ALGORITHM TEMPLATE

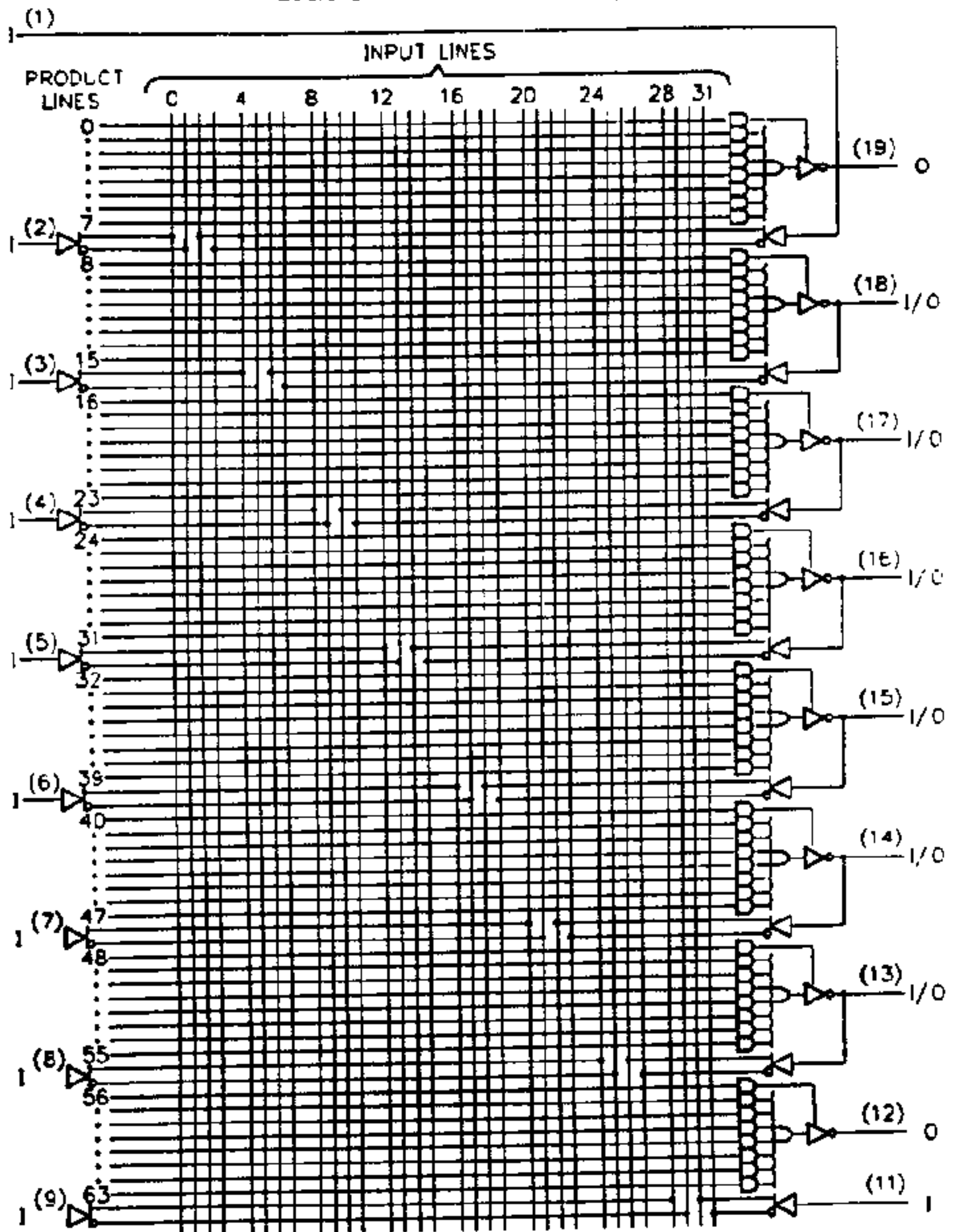
SPECIFICATION NUMBER PAL20001
 DEVICE FAMILY PAL16XXA
 INCLUDED DEVICES PAL16L8A, PAL16R4A, PAL16R6A, PAL16R8A
 PAL16L8A-2, PAL16R4A-2, PAL16R6A-2, PAL16R8A-2

PROGRAMMER INFO:

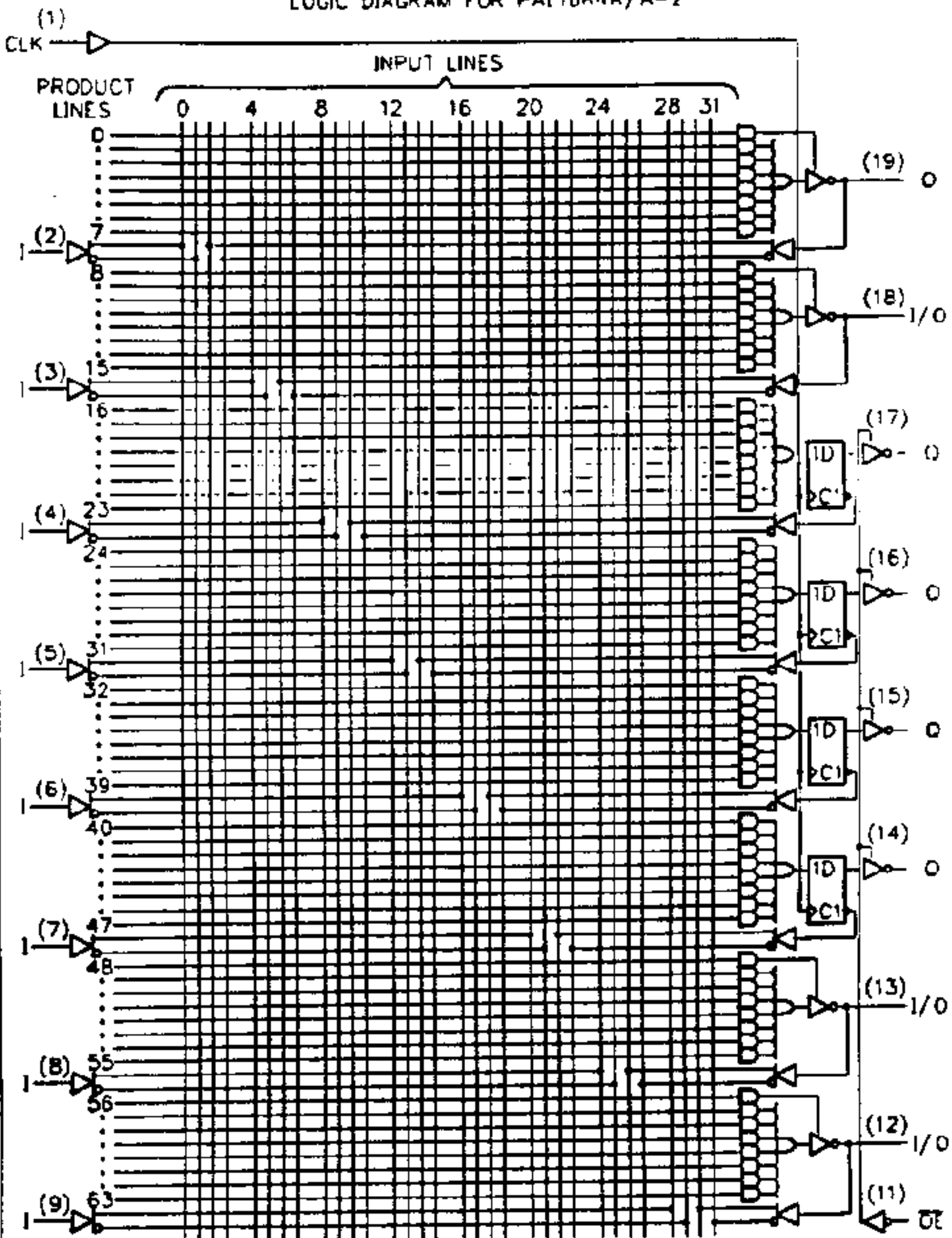
MANUFACTURER : _____ MODEL: _____ ADAPTER #: _____
 UPDATE VERSION : _____ FW/SW P/N: _____

PARAMETER	MIN	NOM	MAX	UNITS	ACTUAL
VCC - VERIFY LEVEL SUPPLY VOLTAGE	14.75	5	15.25	V	
VIH - HIGH LEVEL INPUT VOLTAGE	2.4		5.5	V	
VIL - LOW LEVEL INPUT VOLTAGE			0.5	V	
VIHH - PROGRAM INPUT VOLTAGE (PG/EN)	10.25	10.5	10.75	V	
VIHH - PROGRAM INPUT VOLTAGE (PI,L/R,PA)	10.25	10.5	10.75	V	
VIHH - PROGRAM INPUT VOLTAGE (VCC)	10.25	10.5	10.75	V	
VIHH - PROGRAM INPUT VOLTAGE (PO)	10.25	10.5	10.75	V	
t _{w1} - PROGRAM PULSE WIDTH AT PO	10		50	us	
t _{w2} - PGM VERIFY PULSE WIDTH	100			ns	
t _{su} - SET UP TIME (PG/EN-PI,L/R,PA)	100			ns	
t _{su} - SET UP TIME (VCC-PO)	100			ns	
t _{d1} - DELAY TIME (VCC (5V) TO PGM VERIFY)	100			us	
t _h - HOLD TIME (PG/EN-PI,L/R,PA)	100			ns	
t _h - HOLD TIME (VCC-PO)	100			ns	
t _h - HOLD TIME SECURITY (VCC-PIN1)	100			ns	
t _h - HOLD TIME SECURITY (PIN1-PIN11)	100			ns	
t _h - HOLD TIME SECURITY (PIN11-VCC)	100			ns	
t _{w3} - SECURITY FUSE PULSE (PIN 1)	20		50	us	
t _{w3} - SECURITY FUSE PULSE (PIN 11)	20		50	us	
- SECURITY FUSE VOLTAGE (PIN 1)	20	21	22	V	
- SECURITY FUSE VOLTAGE (PIN 11)	20	21	22	V	

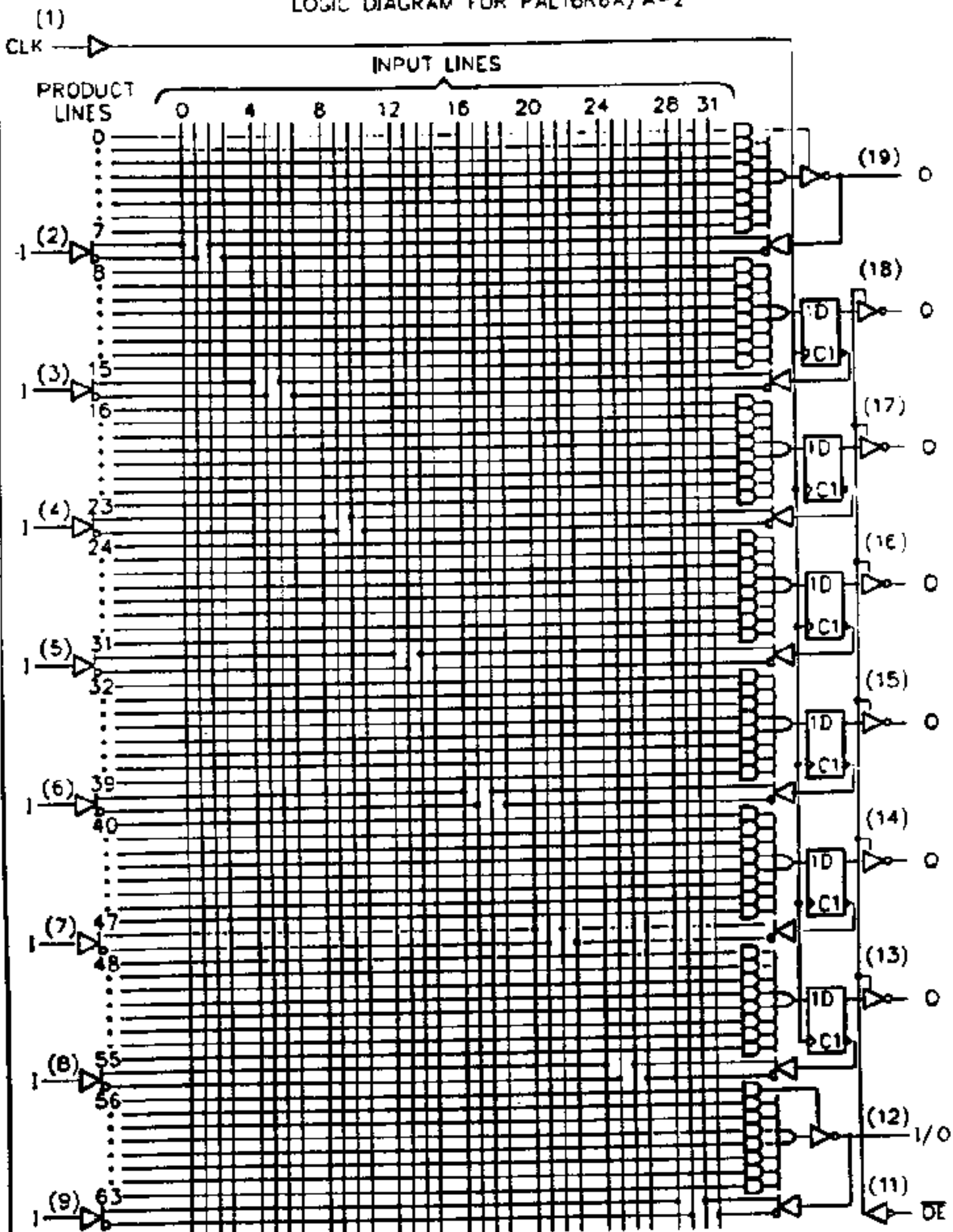
LOGIC DIAGRAM FOR PAL16LBA/A-2



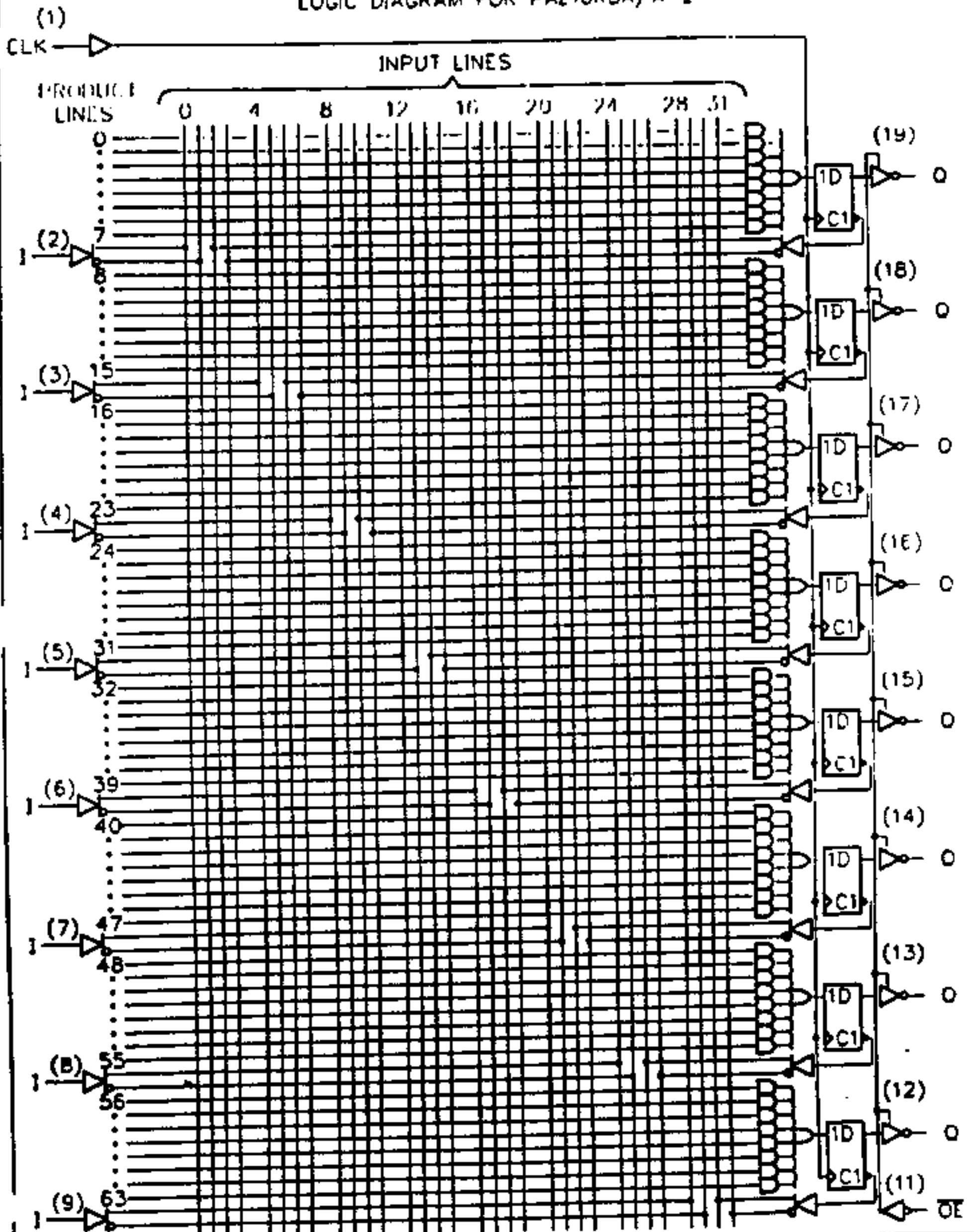
LOGIC DIAGRAM FOR PAL16R4A/A-2



LOGIC DIAGRAM FOR PAL16R6A/A-2



LOGIC DIAGRAM FOR PAL16RBA/A-2



REVISION HISTORY

REVISION LTR.	DATE	ENGINEER	DESCRIPTION OF CHANGES
A	09-86	Michal	VCC during verify to 5 V only V _{IH} min. to 2.4 V. V _{IL} max to .5 V. Return V _{IHH} to 10.5 V.
B	03-88	Thomas	Added PLCC pinouts, Page 2 Added V _{CC} = 4.75 volts, Min. Added V _{CC} = 5.25 volts, Max.