

## ***Test Considerations for PLDs***

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### **ABSTRACT**

Programmable Logic Device (PLD) architecture establishes some unique characteristics. Because PLDs do not have the functional needs for address pins as found in a PROM, the array must be addressed for programming through the use of super voltages (10.5 volts). Since the programming and verification circuitry are not the same as the functional circuitry, verification of the array fuses does not ensure total functionality. For this reason, there are two customer yield points to be considered for a PLD, 1) programmability yield, and 2) functionality after programming. Texas Instruments (TI) thoroughly tests PLDs in its factory; however, you may find the need to test after programming to achieve the highest quality levels.

This report describes the testing performed at Texas Instruments (TI™) prior to shipment of programmable logic devices, and discusses testing alternatives available after PLDs are programmed.

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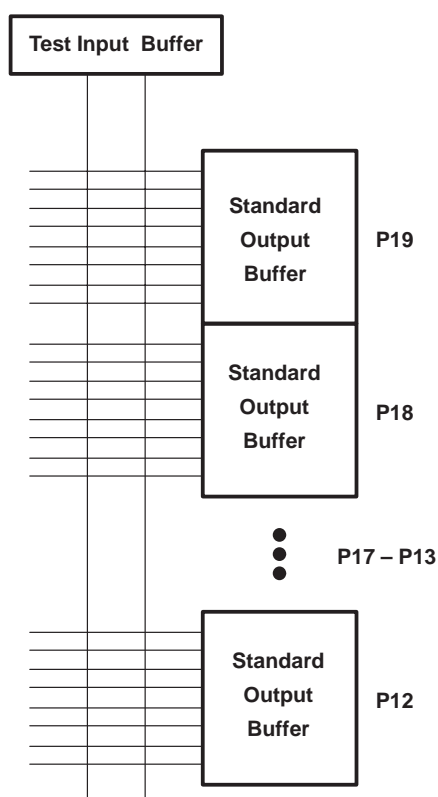
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NOTE: TI is a trademark of Texas Instruments.

## 1 Designed-In Factory Testability

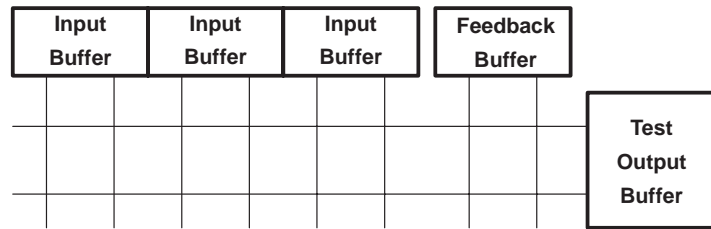
Texas Instruments has designed testability into its bipolar PLDs through the addition of test input and test product lines. Using the same circuitry as the main array fuses, a test pattern is programmed into the test array fuses that addresses and programs at least one fuse in each input and product line. In addition to verification of the main fuse array, the test lines provide additional programmability checkpoints for each device. These same test lines enable TI to perform functional, static (dc), and dynamic (ac) parametric testing on every packaged device.

Figure 1 and Figure 2 are simplified diagrams of the test circuitry for the TIBPAL16XX series devices. Note that the test lines allow testing of actual input and output circuitry; therefore, all ensured specifications can be tested. Dynamic testing through the test circuitry is closely correlated to worst-case paths and should eliminate the need for ac testing at the customer's incoming inspection.



**Figure 1. Additional Input Lines**

Using the test input lines, you can toggle all outputs and check the speed from one input to all outputs.



**Figure 2. Additional Product Lines**

Using the test product lines, TI can check every input and implement dynamic testing from every input to one output.

## **2 User Testability Features**

In addition to the designed-in testability features used in factory testing, features are also added to simplify user testability. Table 1 lists user testability features offered on TI programmable logic devices and associated software products available to assist you with testing PLDs.

### **2.1 Register Preload**

This feature allows you to preload the output registers to known states before you apply data or clocking at inputs and/or at I/Os.

Preload can be implemented by writing preload vectors in popular logic compilers following logic equations, or it can be automatically generated using automatic vector generation software. Most commercial programmers who perform functional tests support the use of preload vectors.

The advantage of register preload is that it allows you to fully test complex codes.

### **2.2 Power-Up Clear, Set, or Reset**

Power-up clear, set, or reset enables you to know the state of the register at power up. Again, this is a key feature for testability because it provides you or the automatic vector generation software with a starting point for register-intensive designs. Table 1 shows the power-up state of the register and resulting state at the output.

You can also contribute to the testability of the design by using other features of the PLD.

### **2.3 Unused Inputs/Product Lines**

Unused inputs and product lines can be used to implement set, reset, and clear functions to register-intensive designs which are often hard to test. Often register designs have unused input pins, as well as product lines available for implementing these functions.

### **2.4 Enable on Combinational Outputs**

Combinational outputs have one product line available for implementing the enable/disable function. The key advantage can be seen during board testing where devices must be isolated from each other. By disabling the output of the PLD, you can force input conditions from the external source to the devices being driven by the PLD.

**Table 1. User Testability Features**

DEVICE FAMILY	SPEED DESIGNATOR	REGISTERED PRELOAD	REGISTERED OUTPUTS	POWER-UP AT REGISTER	POWER-UP AT OUTPUT	VECTOR GENERATION SOFTWARE SUPPORT	
						AVIL ATG	DATA I/O PLDTEST+
TIBPAL16L8	-5/-7/-10	NA†	0	NA	NA	2.23	1.0
TIBPAL16R4	-5/-7/-10	YES	4	L	H	2.23	1.0
TIBPAL16R6	-5/-7/-10	YES	6	L	H	2.23	1.0
TIBPAL16R8	-5/-7/-10	YES	8	L	H	2.23	1.0
TIBPAL16L8	-15/-25	NA	0	NA	NA	2.23	1.0
TIBPAL16R4	-15/-25	–	4	H	L	2.23	1.0
TIBPAL16R6	-15/-25	–	6	H	L	2.23	1.0
TIBPAL16R8	-15/-25	–	8	H	L	2.23	1.0
TIBPAL20L8	-5/-7/-10	NA	0	NA	NA	2.23	1.0
TIBPAL20R4	-5/-7/-10	YES	4	L	H	2.23	1.0
TIBPAL20R6	-5/-7/-10	YES	6	L	H	2.23	1.0
TIBPAL20R8	-5/-7/-10	YES	8	L	H	2.23	1.0
TIBPAL20L8	-15/-25	NA	0	NA	NA	2.23	1.0
TIBPAL20R4	-15/-25	YES	4	L	H	2.23	1.0
TIBPAL20R6	-15/-25	YES	6	L	H	2.23	1.0
TIBPAL20R8	-15/-25	YES	8	L	H	2.23	1.0
TIBPAL22V10	/A	YES	10‡	L	H/L	2.23	1.0
TIBPAL22V10	-7/-10	YES	10‡	L	H/L	2.23	1.0
TIBPAL22V10	-15B	YES	10‡	L	H/L	2.23	1.0
TIBPAL22VP10	-20	YES	10‡	L	H/L	2.23	–
TICPAL22V10Z	-25/-30	YES	10§	–	–	2.23	1.0
TIB82S105B	–	–	8	H	H	2.23	–
TIB82S167B	–	–	6	H	H	2.23	–
TIBPLS506A	–	–	8‡	L	H	2.23	–
TIBPSG507A	–	–	8‡	L	H	2.23	–

† NA = Not applicable

‡ User-configured

§ The TIBPAL22V10Z is erasable for repeated programming

## 3 PLD Testing Options

After programming the PLD, you may want to consider the following testing options and their potential benefits.

### 3.1 Fuse Verification/Checksum

Checksum testing, or fuse verification, tests only the state of the array fuse (intact or blown) and only exercises programming circuitry. The functional circuitry is not tested. Each fuse location is assigned a value of 1, 2, 4, 8, 16, 32, 64, or 128. The checksum is the sum (in hexadecimal) of the values of positions with blown fuses.

### 3.2 Structured Vector Testing

Structured vector testing, using the software packages shown in Table 1 or generated manually at design conception, allows you to apply structured test vectors (see Figure 3) to the device either on device programmers or testers. Figure 4 shows how to implement preload into your vector test.

Fault coverage of structured vectors is graded and documented so you know how much coverage is used for the design. A fault is a potential for device failures. Faults graded are logic faults and fuse faults.

- Logic Faults—check affected gates
  - S-A-0 fault (stuck low)
  - S-A-1 fault (stuck high)

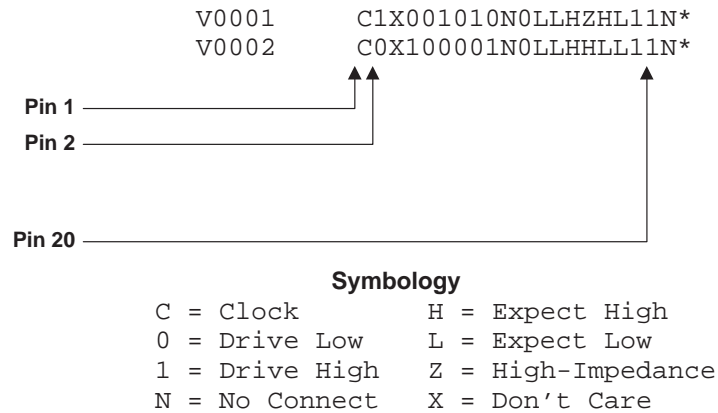
Figure 5 Illustrates these logic faults.

- Fuse Faults—check each fuse to see if intact or blown

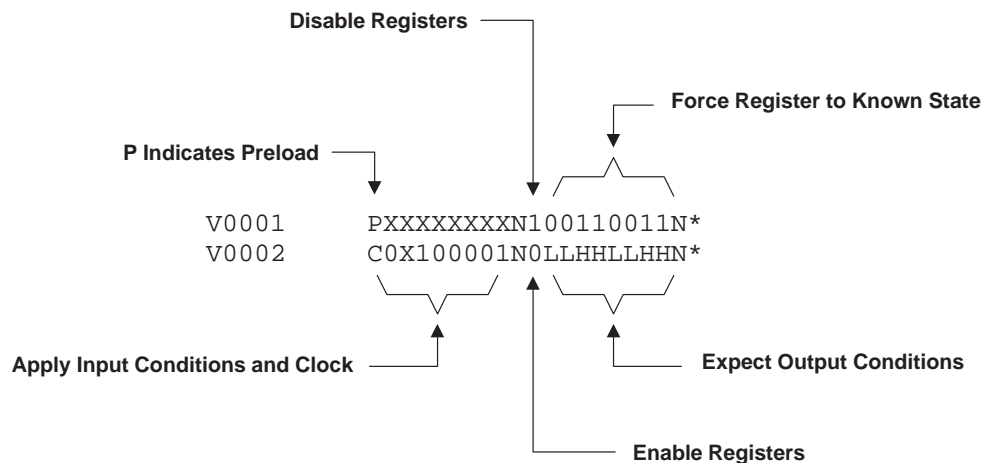
Structured vectors are generic so they can be applied to all manufactured PLDs of like function (for example, 16L8, 22V10). Structured vector testing ensures the functionality of the design, and can be performed on the device programmer. Structured vector testing should be considered the minimum amount of testing required prior to application.

### 3.3 Signature Analysis/Logic Fingerprint/Random Vector Testing

Signature analysis with Logic Fingerprint™ testing (also known as random vector testing) is sometimes seen as an alternative to structured vector testing. The test applies a predetermined or pseudorandom vector set to the inputs of a known good device and memorizes the output responses. Subsequent devices are tested against the master.



**Figure 3. Test Vectors (Standard JEDEC Form)**

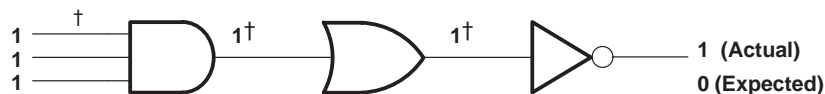


**Figure 4. Preload Implementation—TIBPAL16R8**

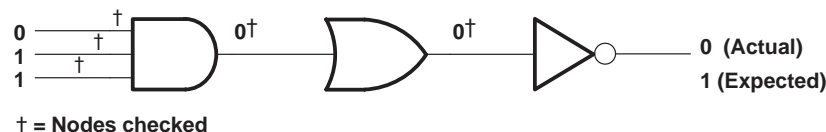
NOTE: Logic Fingerprint is a trademark of Data I/O Corporation.

### Structured Test Vectors Can Be Applied to Detect :

**S-A-1 Fault:** Circuit node ignores input stimuli and remains at a high or 1 state.



**S-A-0 Fault:** Circuit node ignores input stimuli and remains at a low or 0 state.



**Figure 5. Fault Grading**

## 3.4 Static (dc) Parametric Testing

Static parametric testing includes structured vector testing of functionality, as described previously, plus the testing of critical current/voltage parameters to ensure they meet the specifications prescribed in the TI *Programmable Logic Data Book*, literature number SRPD001B.

The testing of dc parametrics, such as input and I/O leakage currents, output high and low voltages under static loading, and power supply current, improves the quality of the PLD going into the application by ensuring that devices which are functional are not damaged due to ESD (electrostatic discharge) or EOS (electrical overstress) during the customization process.

Static parametric testing cannot presently be performed on device programmers and therefore requires the use of automated test equipment (ATE). Static parametric testing coupled with structured vector testing should provide you with an optimum test at a medium investment.

## 3.5 Dynamic (ac) Testing

Dynamic testing ensures that the PLD meets all the speed requirements of the design. A good ac test measures propagation delay time through all possible paths and, when coupled with functional and dc parametric testing, provides the optimum PLD test.

There are two types of ac testing to consider: functional ac and measurement ac testing. Functional ac testing is a popular test method for PLDs. This method applies structured test vectors and sets strobes to ensure transitions occur with proper timing. Functional ac testing performs a good job of simulating the actual design if structured vectors with good coverage are used.

In contrast, measurement ac testing tests and measures all speed parameters using all possible input and output combinations. This type of testing is typically only available from the factory because it requires another level of vector grading and dedicated engineering resources.

Dynamic testing usually requires a large investment not only in hardware, but also in engineering time developing extensive test programs, bench to tester correlation, load boards, and vector software, for example.

Texas Instruments performs extensive worst-case code characterizations prior to device release. Each device shipped from TI undergoes ac testing using the device's test rows and test columns; therefore, you may find that a post-programming ac test does not justify the payback in terms of a higher level of quality.



## 4 Why Test After Programming?

As previously discussed, verification of the fuse array following programming does not ensure total functionality; therefore, you must determine the amount of testing required after programming. The following concerns should be considered.

### 4.1 Programming

Programming exposes the device to super voltages (up to 10.75 volts) and currents high enough to overstress devices. TI PLDs are designed to withstand these conditions; however, all leakage current parameters should be tested to eliminate the risk of electrical overstress.

An uncalibrated programmer can expose devices to voltages/currents outside specified ranges.

### 4.2 Handling

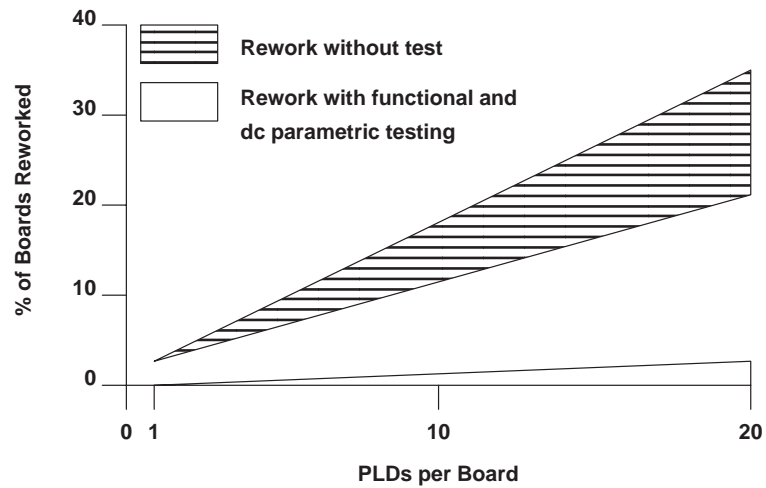
In addition to programming the PLD, most users identify the custom function programmed into the PLD by labeling or marking it. The added handling required to program and customize the PLD increases the chances for ESD (electrostatic discharge) damage unless strict adherence to ESD protection procedures is observed.

### 4.3 Custom Function

TI takes extraordinary measures to ensure device functionality and performance; however, each user design is a custom function and should be treated as such during final testing prior to application.

### 4.4 Test Versus Rework

Figure 6 compares the impact of testing on board rework and, consequently, manufacturing cost. This illustration compares no testing versus functional and dc parametric testing. Using conservative figures for rework cost, the data shows rework cost due to untested PLDs can exceed one dollar per PLD used. A similar analysis of your application may show a cost savings resulting from testing after programming.



Assume:

10 PLDs per board

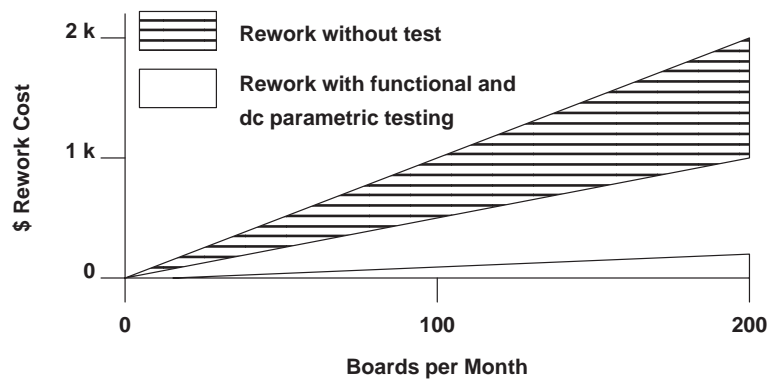
\$50 Rework cost per board

200 Boards per month

Rework cost due to untested PLDs:

$20\% \times 200 \times 50 = \$2000$

$10\% \times 200 \times 50 = \$1000$



**Figure 6. Test Versus Rework**

## **5 TI Programming and Test Services**

What services are offered by your PLD manufacturer? Texas Instruments provides its customers with a three-phase service program that provides for programmed and tested PLDs of the highest quality direct from the factory or through TI authorized distributors.

### **5.1 Factory Programmed and Tested PLDs**

TI can support run rates greater than 1000 parts per code per month with factory programmed and tested PLDs. TI generates structured test vectors and performs 100% functional, dc parametric, and ac testing on PLDs programmed to your custom logic function. Custom symbolization is also included in the factory programmed PLD flow, thereby delivering ship-to-stock and/or ship-to-WIP product.

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