Functional Safety Information

SN74HCS365-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for SN74HCS365-Q1 (D SOIC (16), PW TSSOP (16) and BQB WQFN (16)packages) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

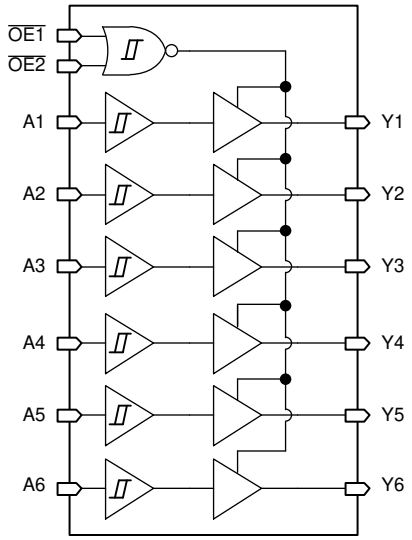

Figure 1-1. Functional Block Diagram

SN74HCS365-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 D SOIC (16) Package

This section provides functional safety failure in time (FIT) rates for the D SOIC (16) package of the SN74HCS365-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	20
Die FIT rate	2
Package FIT rate	18

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 14.3 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
3	CMOS Logic FCT, HC, LV, LVC, ALVC or VHC	5 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 PW TSSOP (16) Package

This section provides functional safety failure in time (FIT) rates for the PW TSSOP (16) package of the SN74HCS365-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	11
Die FIT rate	2
Package FIT rate	9

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 14.3 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
3	CMOS Logic FCT, HC, LV, LVC, ALVC or VHC	5 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 BQB WQFN (16) Package

This section provides functional safety failure in time (FIT) rates for the BQB WQFN (16) package of the SN74HCS365-Q1 based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	7
Die FIT rate	2
Package FIT rate	5

The failure rate and mission profile information in Table 2-5 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: TBD mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
3	CMOS Logic FCT, HC, LV, LVC, ALVC or VHC	5 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74HCS365-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output stuck-at fault	30%
Output Open (High Impedance)	25%
Output functional - out of specification timing or voltage	45%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the SN74HCS365-Q1 (D SOIC (16), PW TSSOP (16) and BQB WQFN (16) packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to V_{CC} (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 D SOIC (16) and PW TSSOP (16) Packages

Figure 4-1 shows the SN74HCS365-Q1 pin diagram for the D SOIC (16) and PW TSSOP (16) packages. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the SN74HCS365-Q1 data sheet.

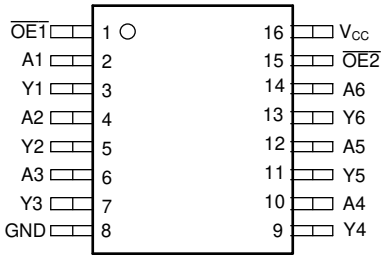

Figure 4-1. Pin Diagram (D SOIC (16) and PW TSSOP (16)) Packages

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A1-A6	2; 4; 6; 10; 12; 14	Input pin functionality is defined as LOW - see Device Function Table (for example, buffer input is GND, output is always driven LOW).	B
Y1-Y6	3; 5; 7; 9; 11; 13	Can cause excessive output current, output cannot switch (for example, if buffer output is shorted to ground and is attempting to drive to V_{CC}).	A
$\overline{OE1}$; $\overline{OE2}$	1; 15	Output is push-pull only. High impedance output functionality is lost.	B
GND	8	Normal operation	D
V_{CC}	16	The device is not be powered, because short is external to the device. System level damage can occur in this scenario.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A1-A6	2; 4; 6; 10; 12; 14	Pin is floating, which can change the output state and cause excessive current from V_{CC} to GND. See Implications of Slow or Floating CMOS Inputs.	A
Y1-Y6	3; 5; 7; 9; 11; 13	Normal operation	D
$\overline{OE1}$; $\overline{OE2}$	1; 15	Pin is floating, which can change the output state and cause excessive current from V_{CC} to GND. See Implications of Slow or Floating CMOS Inputs.	A
GND	8	The device is not be powered	B
V_{CC}	16	The device is not be powered	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
A1-A6	2; 4; 6; 10; 12; 14	Y1-Y6	Can cause excessive output current, output cannot switch (for example, if the buffer output is shorted to V_{CC} and is attempting to drive to GND).	A
A1-A6	2; 4; 6; 10; 12; 14	$\overline{OE1}$; $\overline{OE2}$	The output state depends on pin A condition. Functionality is be lost as outputs are LOW when A = LOW, and outputs are High-Impedance (HiZ) when A is HIGH.	B
Y1-Y6	3; 5; 7; 9; 11; 13	$\overline{OE1}$; $\overline{OE2}$	Can cause excessive output current, output cannot switch (for example, if the buffer output is shorted to V_{CC} and is attempting to drive to GND).	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{CC}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A1-A6	2; 4; 6; 10; 12; 14	Input pin functionality is defined as HIGH - see Device Function Table (for example, buffer input is GND, output is always driven LOW).	B
Y1-Y6	3; 5; 7; 9; 11; 13	Can cause excessive output current, output cannot switch (for example, if the buffer output is shorted to V_{CC} and is attempting to drive to GND).	A
$\overline{OE1}$; $\overline{OE2}$	1; 15	Output is High-Impedance only. push-pull output functionality is lost.	B
GND	8	The device is not powered	B
V_{CC}	16	Normal operation	D

4.2 BQB WQFN (16) Package

Figure 4-2 shows the SN74HCS365-Q1 pin diagram for the BQB WQFN (16) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the SN74HCS365-Q1 data sheet.

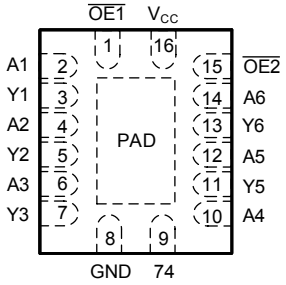

Figure 4-2. Pin Diagram (PW TSSOP (16) Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A1-A6	2; 4; 6; 10; 12; 14	Input pin functionality is defined as LOW - see Device Function Table (for example, buffer input is GND, output is always driven LOW).	B
Y1-Y6	3; 5; 7; 9; 11; 13	Can cause excessive output current, output cannot switch (for example, if buffer output is shorted to ground and is attempting to drive to V_{CC}).	A
$\overline{OE1}$; $\overline{OE2}$	1; 15	Output is push-pull only. High impedance output functionality is lost.	B
GND	8	Normal operation	D
V_{CC}	16	The device is not be powered, because short is external to the device. System level damage can occur in this scenario.	A

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A1-A6	2; 4; 6; 10; 12; 14	Pin is floating, which can change the output state and cause excessive current from V_{CC} to GND. See Implications of Slow or Floating CMOS Inputs.	A
Y1-Y6	3; 5; 7; 9; 11; 13	Normal operation	D
$\overline{OE1}$; $\overline{OE2}$	1; 15	Pin is floating, which can change the output state and cause excessive current from V_{CC} to GND. See Implications of Slow or Floating CMOS Inputs.	A
GND	8	The device is not be powered	B
V_{CC}	16	The device is not be powered	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
A1-A6	2; 4; 6; 10; 12; 14	Y1-Y6	Can cause excessive output current, output cannot switch (for example, if the buffer output is shorted to V_{CC} and is attempting to drive to GND).	A
A1-A6	2; 4; 6; 10; 12; 14	$\overline{OE1}$; $\overline{OE2}$	The output state depends on pin A condition. Functionality is be lost as outputs are LOW when A = LOW, and outputs are High-Impedance (HiZ) when A is HIGH.	B
Y1-Y6	3; 5; 7; 9; 11; 13	$\overline{OE1}$; $\overline{OE2}$	Can cause excessive output current, output cannot switch (for example, if the buffer output is shorted to V_{CC} and is attempting to drive to GND).	A

Table 4-9. Pin FMA for Device Pins Short-Circuited to V_{CC}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A1-A6	2; 4; 6; 10; 12; 14	Input pin functionality is defined as HIGH - see Device Function Table (for example, buffer input is GND, output is always driven LOW).	B
Y1-Y6	3; 5; 7; 9; 11; 13	Can cause excessive output current, output cannot switch (for example, if the buffer output is shorted to V_{CC} and is attempting to drive to GND).	A
$\overline{OE1}$; $\overline{OE2}$	1; 15	Output is High-Impedance only. push-pull output functionality is lost.	B
GND	8	The device is not powered	B
V_{CC}	16	Normal operation	D

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