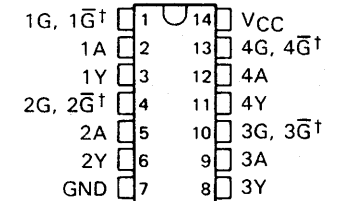


SN54BCT125, SN54BCT126
SN74BCT125, SN74BCT126
QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS
D3133, SEPTEMBER 1988—REVISED SEPTEMBER 1989

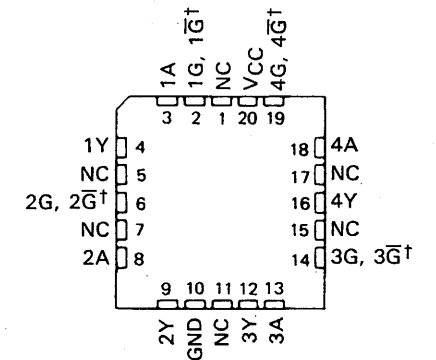
- State of the Art BiCMOS Design Significantly Reduces ICCZ
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015
- Package Options Include Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54BCT125, SN54BCT126 . . . J PACKAGE
 SN74BCT125, SN74BCT126 . . . N OR NS OR DB PACKAGE
 (TOP VIEW)



† \bar{G} on 'BCT125; G on 'BCT126

SN54BCT125, SN54BCT126 . . . FK PACKAGE
 (TOP VIEW)



† \bar{G} on 'BCT125; G on 'BCT126
 NC—No internal connection

description

These bus buffers feature independent line drivers with three-state outputs. Each 'BCT125 output is disabled when the associated \bar{G} is high, and each 'BCT126 output is disabled when the associated G is low.

The SN54BCT125 and SN54BCT126 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74BCT125 and SN74BCT126 are characterized for operation from 0°C to 70°C .

FUNCTION TABLES

'BCT125
(EACH BUFFER)

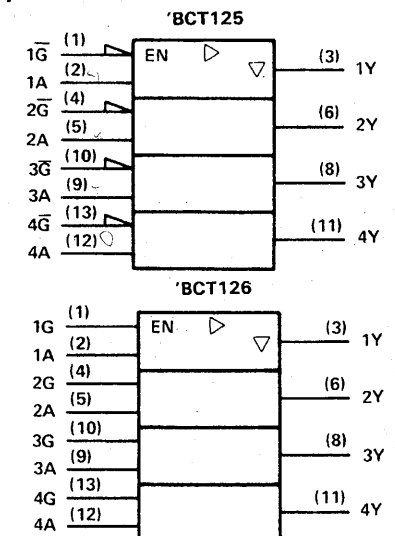
INPUTS		OUTPUT
\bar{G}	A	Y
L	H	H
L	L	L
H	X	Z

'BCT126
(EACH BUFFER)

INPUTS		OUTPUT
G	A	Y
H	H	H
H	L	L
L	X	Z

H = high level, L = low level, X = irrelevant

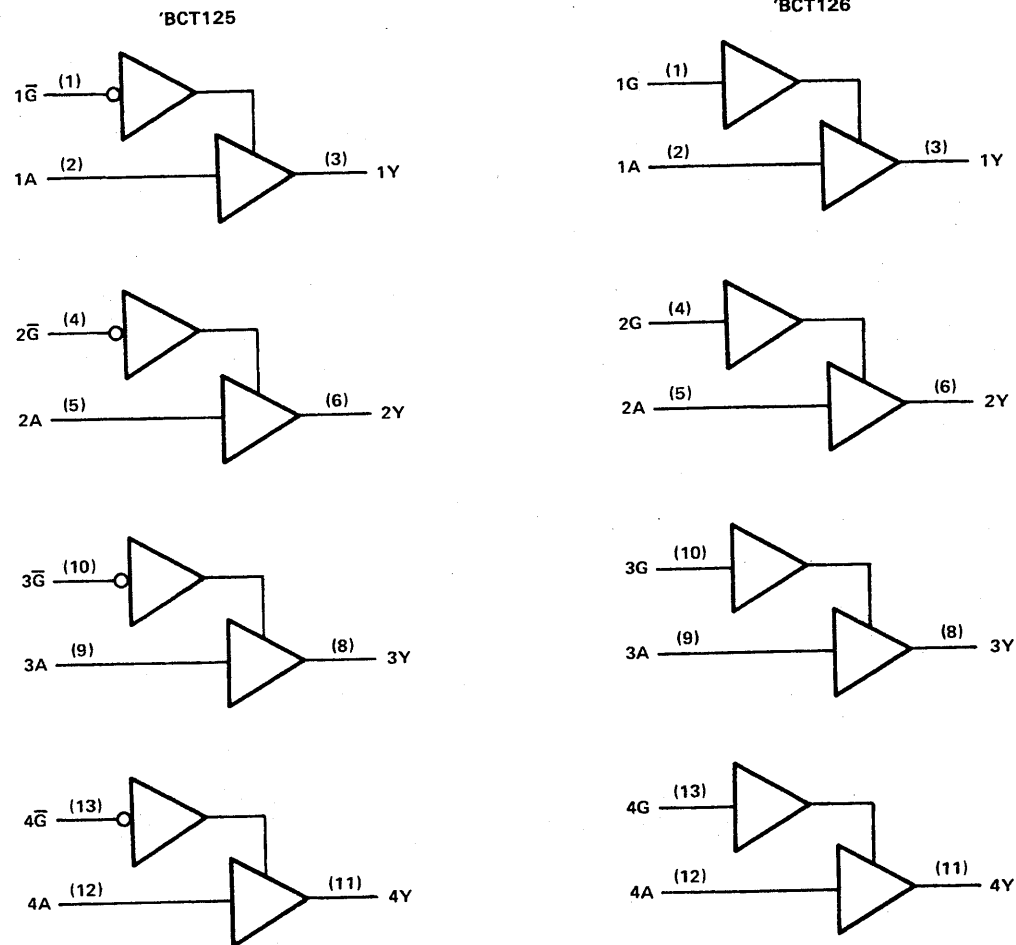
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**SN54BCT125, SN54BCT126
SN74BCT125, SN74BCT126
QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS**

logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage	-0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	-0.5 V to 5.5 V
Voltage applied to any output in the high state	-0.5 V to V_{CC}
Current into any output in the low state: SN54BCT125, SN54BCT126	96 mA
SN74BCT125, SN74BCT126	128 mA
Operating free-air temperature range: SN54BCT125, SN54BCT126	-55°C to 125°C
SN74BCT125, SN74BCT126	0°C to 70°C
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**SN54BCT125, SN54BCT126
SN74BCT125, SN74BCT126
QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS**

recommended operating conditions

	SN54BCT125			SN74BCT125			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{IK} Input clamp current			-18			-18	mA
I_{OH} High-level output current			-12			-15	mA
I_{OL} Low-level output current			48			64	mA
T_A Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT125			SN74BCT125			UNIT
	MIN	TYP†	MAX	MIN	TYP†	MAX			
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA		-1.2			-1.2			V
V_{OH}	$V_{CC} = 4.5$ V		$I_{OH} = -3$ mA		2.4	3.3	2.4	3.3	V
			$I_{OH} = -12$ mA		2	3.2			
			$I_{OH} = -15$ mA				2	3.1	
V_{OL}	$V_{CC} = 4.5$ V		$I_{OL} = 48$ mA		0.38	0.55			V
			$I_{OL} = 64$ mA				0.42	0.55	
I_I	$V_{CC} = 0$ V, $V_I = 7$ V		0.1			0.1			mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V		35			25			μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.5$ V		-20			-20			μA
I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 2.7$ V		50			50			μA
I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.5$ V		-50			-50			μA
I_{OS}^\ddagger	$V_{CC} = 5.5$ V, $V_O = 0$		-100			-100			mA
I_{CCH}	$V_{CC} = 5.5$ V, Outputs open		19		31	19		31	mA
I_{CCL}			46		49	46		49	
I_{CCZ}			6		12	6		12	
C_i	$V_{CC} = 5$ V, $V_I = 2.5$ V or 0.5 V		4			4			pF
C_o	$V_{CC} = 5$ V, $V_O = 2.5$ V or 0.5 V		9			9			

†All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

‡Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

SN54BCT126, SN74BCT126
QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54BCT126		SN74BCT126		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2	V	
V _{OH}	V _{CC} = 4.5 V	I _{OH} = -3 mA		2.4	3.3	2.4	3.3	V
		I _{OH} = -12 mA		2	3.2			
		I _{OH} = -15 mA				2	3.1	
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.38	0.55			V
		I _{OL} = 64 mA				0.42	0.55	
I _I	V _{CC} = 0 V, V _I = 7 V			0.1		0.1	mA	
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V			35		25	μA	
I _{IL}	V _{CC} = 5.5 V, V _I = 0.5 V			-20		-20	μA	
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			50		50	μA	
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V			-50		-50	μA	
I _{OS} †	V _{CC} = 5.5 V, V _O = 0	-100		-225	-100	-225	mA	
I _{CCH}	V _{CC} = 5.5 V, Outputs open		21	33		21	33	mA
I _{CCL}			35	51		35	51	
I _{CCZ}			5	8		5	8	
C _i	V _{CC} = 5 V, V _I = 2.5 V or 0.5 V			4		4	pF	
C _o	V _{CC} = 5 V, V _O = 2.5 V or 0.5 V			9		9		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

7

SN54BCT125, SN54BCT126
SN74BCT125, SN74BCT126
QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

'BCT125 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			'BCT125			SN54BCT125		SN74BCT125		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1.6	3.5	5.2	1.6	6	1.6	5.7	ns
t _{PHL}			2.7	5	6.9	2.7	8	2.7	7.7	
t _{PZH}	G	Y	3.4	6.7	9	3.4	11.1	3.4	10.3	ns
t _{PZL}			5	8.2	10.4	5	12.8	5	11.7	
t _{PHZ}	G	Y	3	5.8	7.4	3	9.4	3	8.9	ns
t _{PLZ}			2.8	5.5	7.3	2.8	9.9	2.8	8.6	

'BCT126 switching characteristics (see Figure 1)

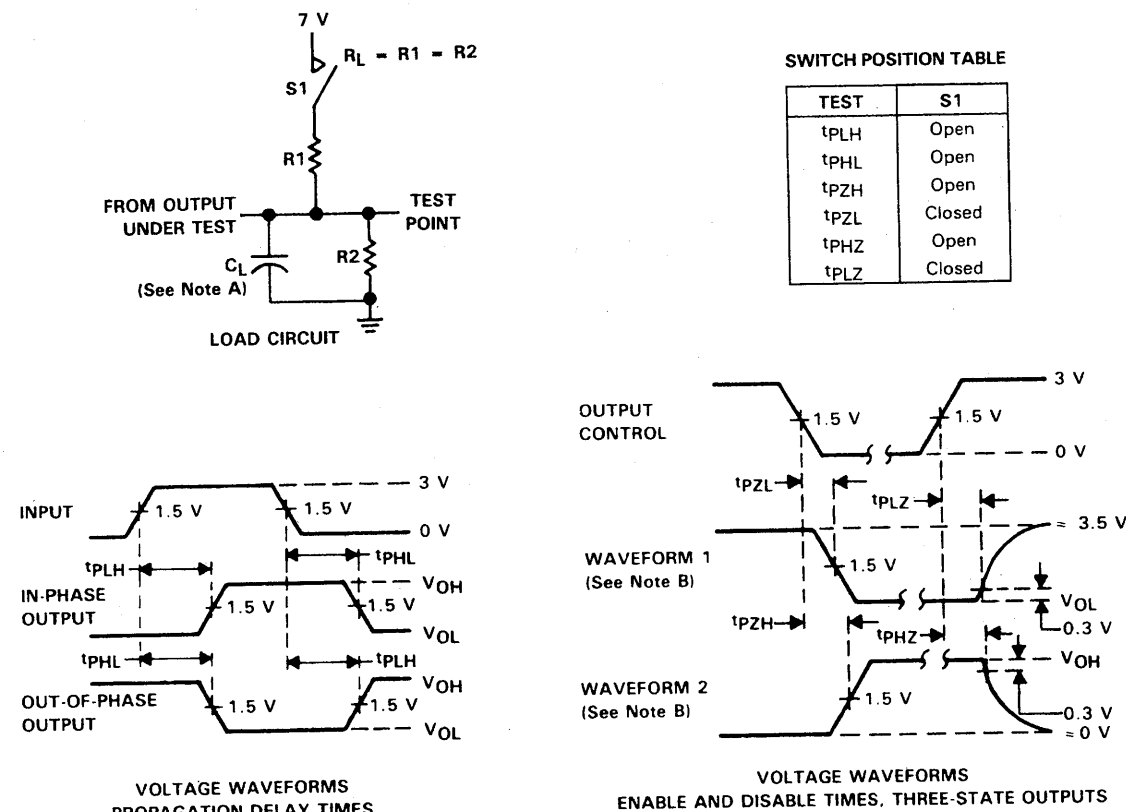
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			'BCT126			SN54BCT126		SN74BCT126		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	1.5	3.6	4.9	1.5	5.6	1.5	5.4	ns
t _{PHL}			2.7	5.3	6.9	2.7	7.7	2.7	7.4	
t _{PZH}	G	Y	2.6	4.8	6.4	2.6	7.2	2.6	7	ns
t _{PZL}			3.7	6.4	8.3	3.7	10.5	3.7	10	
t _{PHZ}	G	Y	3.2	6.6	8.2	3.2	9.6	3.2	9.1	ns
t _{PLZ}			3.4	6.5	8	3.4	12.3	3.4	10.7	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

7

SN54BCT125, SN54BCT126
SN74BCT125, SN74BCT126
QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



SWITCH POSITION TABLE

TEST	S1
t _{PLH}	Open
t _{PHL}	Open
t _{PZH}	Open
t _{PZL}	Closed
t _{PHZ}	Open
t _{PLZ}	Closed

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

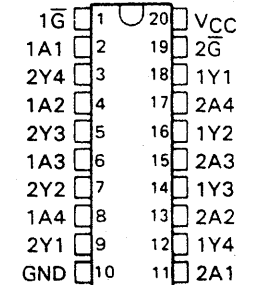
- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR \geq 10 MHz, $Z_o = 50 \Omega$, $t_r = 2.5$ ns, $t_f = 2.5$ ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

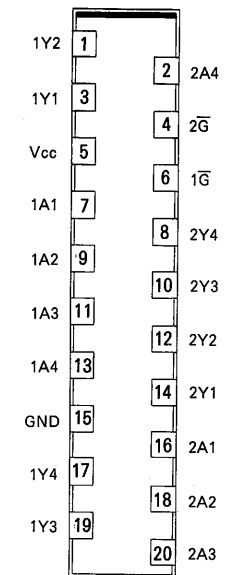
SN54BCT240, SN74BCT240
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D3057, OCTOBER 1987—REVISED AUGUST 1989

SN54BCT240 ... J PACKAGE
SN74BCT240 ... N OR NS OR DB PACKAGE
(TOP VIEW)



SN74BCT240 ... SD PACKAGE
(TOP VIEW)



- State of the Art BiCMOS Design Significantly Reduces ICCZ
- Comparable Speed and Improved Power Performance Relative to 54F/74F240
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

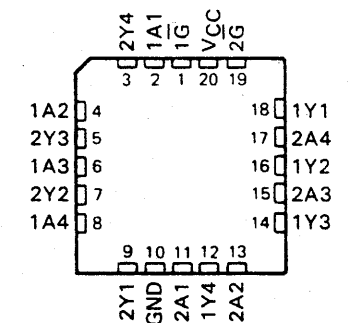
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT241 and 'BCT244, these devices provide a choice of selected combinations of inverting and non-inverting outputs, symmetrical \bar{G} (active-low output control) inputs, and complementary G and \bar{G} inputs. These devices feature high fan-out and improved fan-in.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

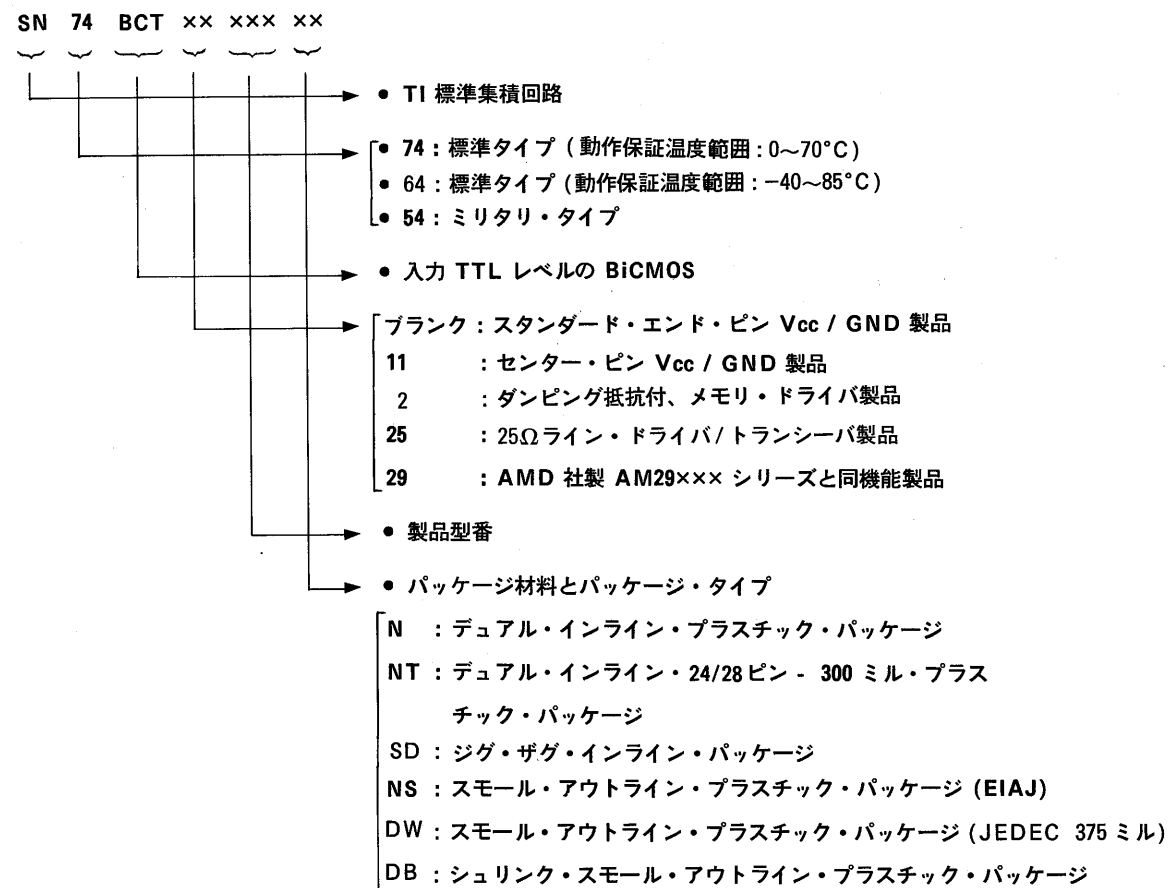
FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\bar{G}	A	Y
L	H	L
L	L	H
H	X	Z

SN54BCT240 ... FK PACKAGE
(TOP VIEW)

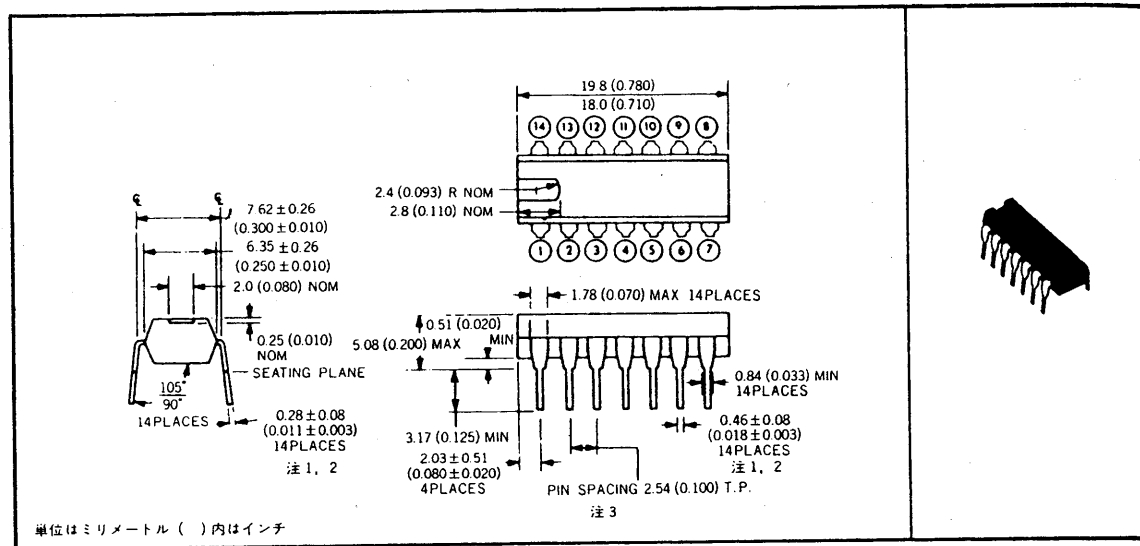


製品の型名は、

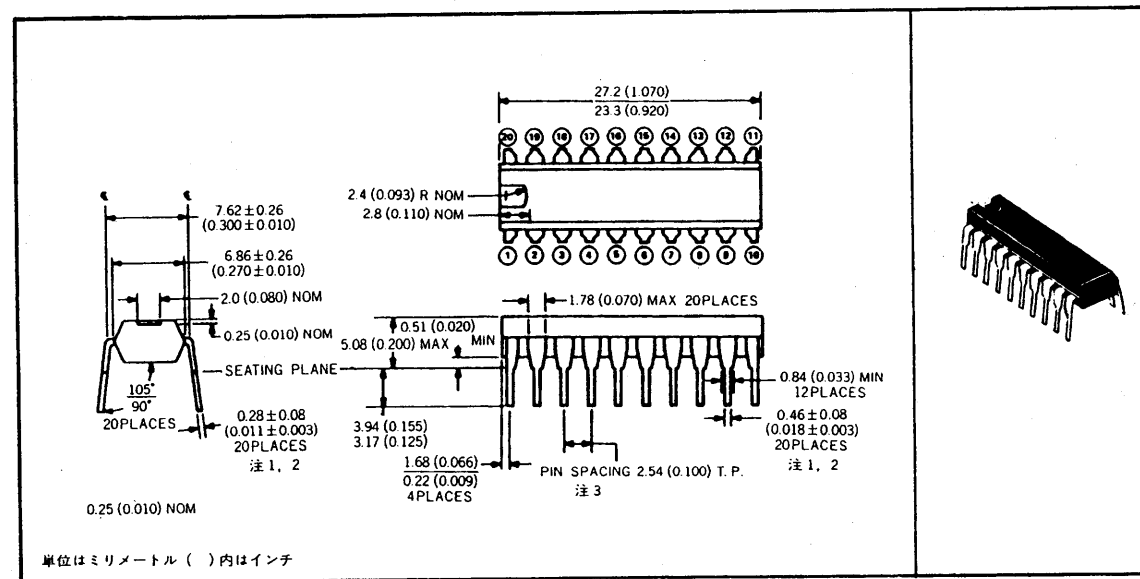


BiCMOSバス・インターフェイスロジック パッケージの外形図
プラスチック・デュアル・インライン・パッケージ

■14ピンN プラスチック・パッケージ (*DIP014-P-0300)



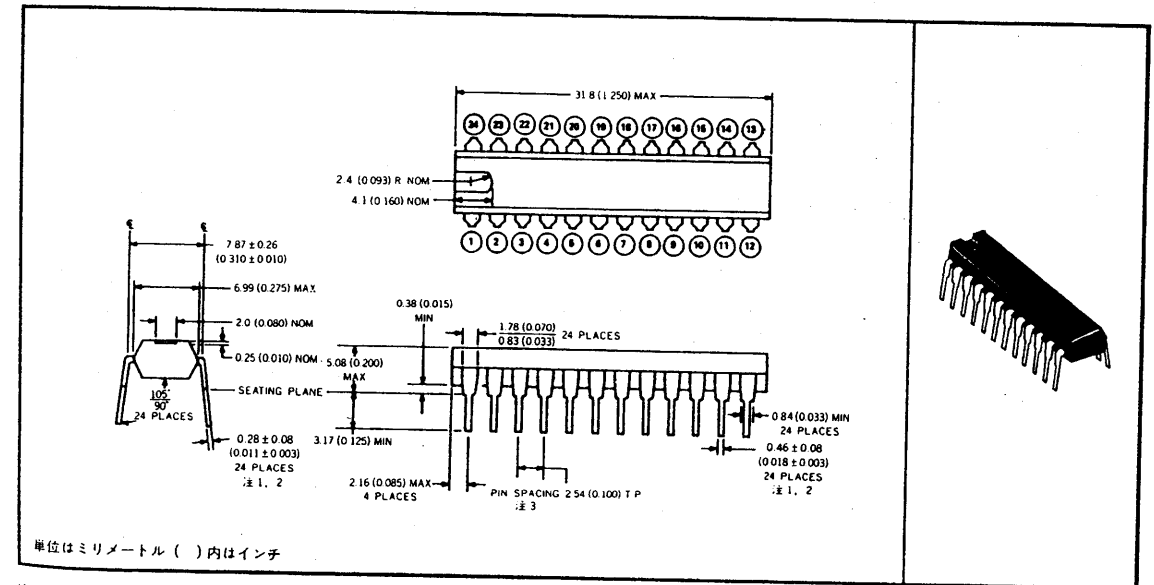
■20ピンN プラスチック・パッケージ (*DIP020-P-0300)



- 注1) この値は、ソルダ・ディップ処理品には適用されません。
 2) ソルダ・ディップ処理品において、ディップ処理長はリード先端から SEATING PLANE の上0.51ミリ (0.020インチ) 以上です。
 3) 各ピンの中心線誤差0.26ミリ (0.010インチ) 以内です。

BiCMOSバス・インターフェイスロジック パッケージの外形図
プラスチック・デュアル・インライン・パッケージ

■24ピンNT プラスチック・パッケージ (*DIP024-P-0300)



- 注1) この値は、ソルダ・ディップ処理品には適用されません。
 2) ソルダ・ディップ処理品において、ディップ処理長はリード先端から SEATING PLANE の上0.51ミリ (0.020インチ) 以上です。
 3) 各ピンの中心線誤差0.26ミリ (0.010インチ) 以内です。