TI Information - Selective Disclosure

Application Report

SN74HCS00-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

1 Overview....2
2 Functional Safety Failure In Time (FIT) Rates....3
2.1 SOIC Package....3
2.2 TSSOP Package....4
2.3 SOIC and TSSOP Package....5
3 Failure Mode Distribution (FMD)....6
4 Pin Failure Mode Analysis (Pin FMA)....7
4.1 SOIC and TSSOP Package....7
5 Revision History....9

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1 Overview

This document contains information for SN74HCS00-Q1 (SOIC and TSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

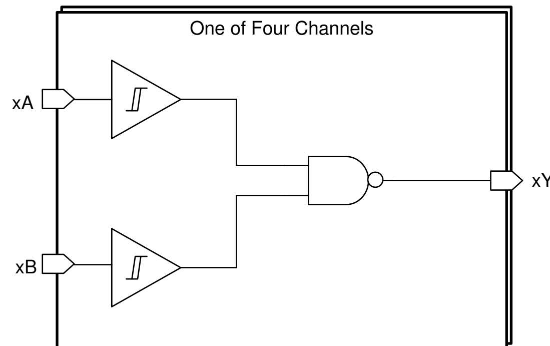

Figure 1-1. Functional Block Diagram

SN74HCS00-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

2.1 SOIC Package

This section provides Functional Safety Failure In Time (FIT) rates for SOIC package of SN74HCS00-Q1:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	20
Die FIT Rate	4
Package FIT Rate	16

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 210 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

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2.2 TSSOP Package

This section provides Functional Safety Failure In Time (FIT) rates for the TSSOP package of SN74HCS00-Q1:

- Table 2-2 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

Table 2-2. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	13
Die FIT Rate	4
Package FIT Rate	9

The failure rate and mission profile information in Table 2-2 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 210 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

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2.3 SOIC and TSSOP Package

This section provides Functional Safety Failure In Time (FIT) rates for the SOIC and TSSOP package of SN74HCS00-Q1:

- Table 2-3 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS Logic FCT, HC, LV, LVC, ALVC, VHC, etc.	5 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-3 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74HCS00-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output stuck-at fault	30%
Output open (HIZ)	25%
Output functional – out of specification timing or voltage	45%

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the SN74HCS00-Q1 (SOIC and TSSOP package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

4.1 SOIC and TSSOP Package

Figure 4-1 shows the SN74HCS00-Q1 pin diagram for the SOIC and TSSOP package. The following pin FMA tables may be provided as a reference based on each pin type (input, output, GND, VCC, etc.) instead of pin name (A, Y, GND, VCC, etc.). For a detailed description of the device pins and their corresponding pin type, please refer to the *Pin Configuration and Functions* section in the SN74HCS00-Q1 data sheet.

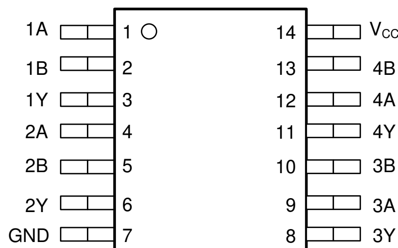

Figure 4-1. Pin Diagram (SOIC and TSSOP) Package

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Description of Potential Failure Effect(s)	Failure Effect Class
Input	Input pin functionality is defined such as input is LOW - see Device Function Table (for example, if buffer input is GND, output will always be driven LOW).	B
Output	Can cause excessive output current, output will not switch (for example, if buffer output is shorted to ground and is attempting to drive to VCC).	A
Vcc	Device will not be powered, because short is external to device. System level damage may occur in this scenario.	B
GND	Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Description of Potential Failure Effect(s)	Failure Effect Class
Input	Pin is floating, can change output state and cause excessive current from VCC to GND - see Implications of Slow or Floating CMOS Inputs - ti.com/lit/scba004.	A
Output	Normal operation.	D
Vcc	Device will not be powered.	B
GND	Device will not be powered.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
Input	Input	Two inputs shorted together will not cause damage unless there is external bus contention that drives the input such that VIL < Input Voltage < VIH in which case excessive supply current to gnd may cause damage. System level damage may occur in this scenario.	A
Input	Output	Can cause excessive output current, output will not switch (for example, if inverter input is shorted to output).	A
Input	GND	See Input response in "Short to GND" table.	A
Input	Vcc	See Input response in "Short to VCC" table.	A
Output	Output	Can cause excessive output current, output will not switch (for example, if one output is driving to VCC and another output is driving to GND).	A
Output	GND	See Output response in "Short to GND" table	A
Output	Vcc	See Output response in "Short to VCC" table	A
GND	Vcc	Device will not be powered, because short is external to device. System level damage may occur in this scenario.	B
NC	Any Pin	A No Connect connected to any pin will not cause damage to the device, as No Connect pins have no internal connection.	D
DNU	Any Pin	A Do Not Use connected to any pin may cause damage to the device.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

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Pin Name	Description of Potential Failure Effect(s)	Failure Effect Class
Input	Input pin functionality is defined such as input is HIGH - see Device Function Table (for example, if buffer input is VCC, output will always be driven HIGH).	B
Output	Can cause excessive output current, output will not switch (for example, if buffer output is shorted to VCC and is attempting to drive to GND).	A
Vcc	Normal operation.	D
GND	Device will not be powered, because short is external to device. System level damage may occur in this scenario.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2020	*	Initial Release

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