Functional Safety Information

SN74LVC1G125-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for SN74LVC1G125-Q1 (SOT-23, SC-70 or SON package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

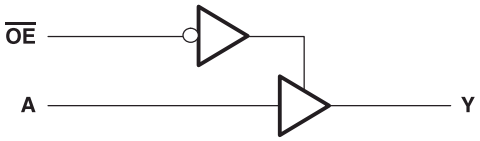

Figure 1-1. Functional Block Diagram

SN74LVC1G125-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for SN74LVC1G125-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	5-pin SOT-23 (DBV) FIT (Failures Per 10^9 Hours)	6-pin SON (DRY) FIT (Failures Per 10^9 Hours)	5-pin SC-70 (DCK) FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6	6	6
Die FIT Rate	4	5	5
Package FIT Rate	2	1	1

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 125mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
3	CMOS Logic FCT, HC, LV, LVC, ALVC, VHC, and so forth	3 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74LVC1G125-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output Stuck-at fault	20%
Output Open (HiZ)	20%
Output functional - out of specification timing or voltage	40%
Short circuit any two pins	20%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the SN74LVC1G125-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to V_{CC} (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 SOT-23 and SC-70 Packages

Figure 4-1 shows the SN74LVC1G125-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the SN74LVC1G125-Q1 data sheet.

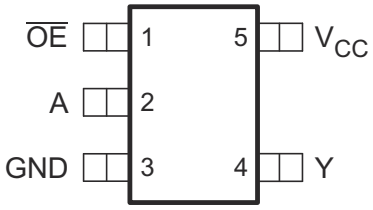

Figure 4-1. Pin Diagram (SOT-23, SC-70)

Table 4-2. Pin FMA for Device Pins Short-Circuited to GND

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
$\overline{OE}$	1	Input pin functionality is defined such as input is high – see the Device Function table (for example, if the buffer input is V_{CC}, output will always be driven high).	B
A	2	Input pin functionality is defined such as input is low – see *Device Function Table* (for example, if the buffer input is GND, output will always be driven low).	B
GND	3	Normal operation	D
Y	4	Can cause excessive output current. Output will not switch (for example, if the buffer output is shorted to GND and is attempting to drive to V_{CC}).	A
V_{CC}	5	The device will not be powered, because short is external to the device. System level damage may occur in this scenario.	B
N.C.	—	If N.C. is tied to GND, normal operation	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
$\overline{OE}$	1	Output may be high Impedance or active, unknown input state.	B
A	2	Pin is floating, which can change the output state and cause excessive current from V_{CC} to GND. See Implications of Slow or Floating CMOS Inputs.	A
GND	3	The device will not be powered.	B
Y	4	Normal operation	D
V_{CC}	5	The device will not be powered.	B
N.C.	—	Normal operation	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
$\overline{OE}$	1	A	The output state will depend on pin A condition. Functionality will be lost as outputs will be low when A = low, and outputs will be high Impedance (HiZ) when A is high.	B
A	2	Y	Can cause excessive output current, output will not switch (for example, if inverter input is shorted to output).	A
A	2	N.C.	If N.C. is tied to GND, Input pin functionality is defined such as input is high – see the Device Function table (for example, if the buffer input is V_{CC}, output will always be driven high).	B
N.C.	—	Y	If N.C. is tied to GND, can cause excessive output current. Output will not switch (for example, if the buffer output is shorted to GND and is attempting to drive to V_{CC}).	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{CC}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
$\overline{OE}$	1	The output will remain in high Impedance (HiZ).	B
A	2	Input pin functionality is defined such as input is high – see the Device Function table (for example, if the buffer input is V_{CC}, output will always be driven high).	B
GND	3	Device will not be powered, because short is external to the device. System level damage may occur in this scenario.	B
Y	4	Can cause excessive output current, output will not switch (for example, if the buffer output is shorted to V_{CC} and is attempting to drive to GND).	A
V_{CC}	5	Normal operation	D
N.C.	—	Normal operation	D

4.2 SON Package

Figure 4-2 shows the SN74LVC1G125-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the SN74LVC1G125-Q1 data sheet.

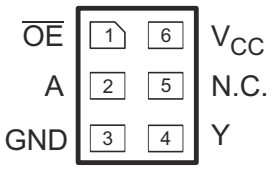

Figure 4-2. Pin Diagram (SON)

Table 4-6. Pin FMA for Device Pins Short-Circuited to GND

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
$\overline{OE}$	1	Input pin functionality is defined such as input is high – see the Device Function table (for example, if the buffer input is V_{CC}, output will always be driven high).	B
A	2	Input pin functionality is defined such as input is low – see *Device Function Table* (for example, if the buffer input is GND, output will always be driven low).	B
GND	3	Normal operation	D
Y	4	Can cause excessive output current. Output will not switch (for example, if the buffer output is shorted to GND and is attempting to drive to V_{CC}).	A
N.C.	5	If N.C. is tied to GND, normal operation	D
V_{CC}	6	The device will not be powered, because short is external to the device. System level damage may occur in this scenario.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
$\overline{OE}$	1	Output may be high Impedance or active, unknown input state.	B
A	2	Pin is floating, which can change the output state and cause excessive current from V_{CC} to GND. See Implications of Slow or Floating CMOS Inputs.	A
GND	3	The device will not be powered.	B
Y	4	Normal operation	D
N.C.	5	Normal operation	D
V_{CC}	6	The device will not be powered.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
$\overline{OE}$	1	A	The output state will depend on pin A condition. Functionality will be lost as outputs will be low when A = low, and outputs will be high Impedance (HiZ) when A is high.	B
A	2	Y	Can cause excessive output current, output will not switch (for example, if inverter input is shorted to output).	A
A	2	N.C.	If N.C. is tied to GND, Input pin functionality is defined such as input is high – see the Device Function table (for example, if the buffer input is V_{CC}, output will always be driven high).	B
N.C.	5	Y	If N.C. is tied to GND, can cause excessive output current. Output will not switch (for example, if the buffer output is shorted to GND and is attempting to drive to V_{CC}).	A

Table 4-9. Pin FMA for Device Pins Short-Circuited to V_{CC}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
$\overline{OE}$	1	The output will remain in high Impedance (HiZ).	B
A	2	Input pin functionality is defined such as input is high – see the Device Function table (for example, if the buffer input is V_{CC}, output will always be driven high).	B
GND	3	Device will not be powered, because short is external to the device. System level damage may occur in this scenario.	B
Y	4	Can cause excessive output current, output will not switch (for example, if the buffer output is shorted to V_{CC} and is attempting to drive to GND).	A
N.C.	5	Normal operation	D
V_{CC}	6	Normal operation	D

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