1、schematic



B1~B4, OE is connected to FPGA IOs(bank2.5V); A1~A4 is connected to AFE5818.

Signal direction:

A1—>B1; SDO

B2—>A2; Tsclk=160ns

B3—>A3; SEN

B4—>A4; SDIN

AFE5818 Pin Functions:





2、wave

|  |  |
| --- | --- |
| B2 wave | A2 wave |
|  |  |

|  |  |
| --- | --- |
| B3 wave | A3 wave |
|  |  |

|  |  |
| --- | --- |
| B4 wave | A4 wave |
|  |  |

3、Please advise what would be the problem root cuase and how to solve this problem. Thanks.