TXS0206 – PCB Layout recommendations

1. Short PCB trace lengths to avoid excessive capacitive loading.
2. Ensure that proper O.S. triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver.
3. The O.S. circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration.
4. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance to the SDIO output, so it is recommended that this lumped-load capacitance be considered and kept below 50 pF to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

5) For the WCSP package in particular, we need to pay attention to the following aspects:

- Reference Planes
- Routing
- Trace lengths
- Trace widths
- High speed signal trace routing
- All of the above are detailed in ths application note below.

  - **http://www.ti.com/lit/an/scea042/scea042.pdf**